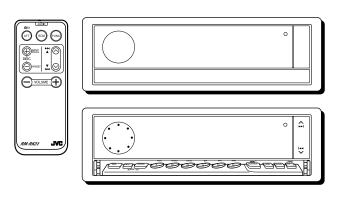
# **JVC**

# **SERVICE MANUAL**

# **CD RECEIVER**

# KD-LX300/KD-LX100







Difference piont	LINE IN	SUBWOOFER OUT
KD-LX300	0	0
KD-LX100	Х	X

### **Contents**

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# **Safety precaution**

A CAUTION Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.

A CAUTION Please use enough caution not to see the beam directly or touch it in case of an adjustment or operation check.

# **Preventing static electricity**

## 1. Grounding to prevent damage by static electricity

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

2. About the earth processing for the destruction prevention by static electricity

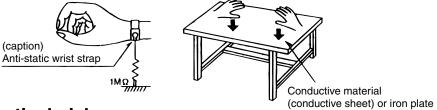
Static electricity in the work area can destroy the optical pickup (laser diode) in devices such as CD players. Be careful to use proper grounding in the area where repairs are being performed.

### 2-1 Ground the workbench

Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

### 2-2 Ground yourself

Use an anti-static wrist strap to release any static electricity built up in your body.



### 3. Handling the optical pickup

- 1. In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the text.)
- 2. Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

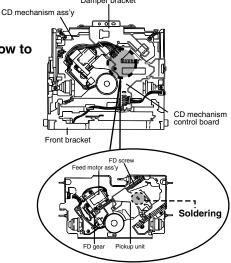
# 4. Handling the traverse unit (optical pickup)

- 1. Do not subject the traverse unit (optical pickup) to strong shocks, as it is a sensitive, complex unit.
- 2. Cut off the shorted part of the flexible cable using nippers, etc. after replacing the optical pickup. For specific details, refer to the replacement procedure in the text. Remove the anti-static pin when replacing the traverse unit. Be careful not to take too long a time when attaching it to the connector.
- 3. Handle the flexible cable carefully as it may break when subjected to strong force.
- 4. It is not possible to adjust the semi-fixed resistor that adjusts the laser power. Do not turn it

# Attention when traverse unit is decomposed

\*Please refer to "Disassembly method" in the text for pick-up and how to detach the substrate.

- 1.Solder is put up before the card wire is removed from connector on the CD substrate as shown in Figure.
  (When the wire is removed without putting up colder the CD pick with the colder.)
  - (When the wire is removed without putting up solder, the CD pick-up assembly might destroy.)
- 2.Please remove solder after connecting the card wire with when you install picking up in the substrate.



# **Disassembly method**

# <Main body>

# ■ Removing the top chassis

(See Fig.1 to 5)

- 1. Remove the two screws **A** attaching the bottom cover to the top chassis on the bottom of the body.
- 2. Remove the two screws **B** attaching the top chassis on both sides of the body.
- 3. Remove the two screws **C** and the two screw **D** attaching the heat sink on the left side of the body.
- 4. Remove the two screws **E** and the screw **F** on the back of the body.
- 5. Remove the two screws **G** on the upper side of the body.
- Move the top chassis upward and disconnect the CD mechanism connector from the main board connector by pulling it. Remove the top chassis from the body.

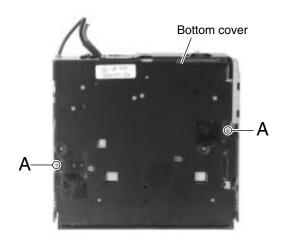
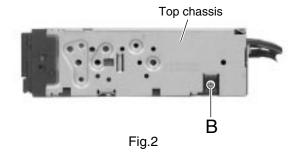


Fig.1



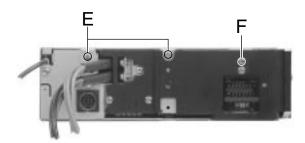
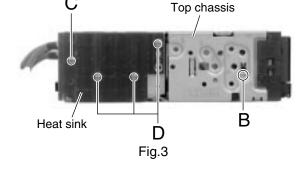


Fig.4-1 (KD-LX300)



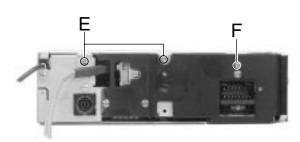


Fig.4-2 (KD-LX100)

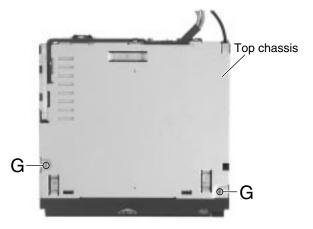
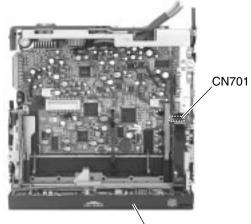


Fig.5

# ■ Removing the front panel assembly (See Fig.6 to 8)

- Prior to performing the following procedure, remove the top chassis assembly.
- 1. Disconnect the flexible harness from connector CN701 on the main board assembly.
- 2. Remove the four screws **H** attaching the front panel assembly on both sides of the body. Remove the front panel toward the front.



Front panel assembly Fig.6-1 (KD-LX300)

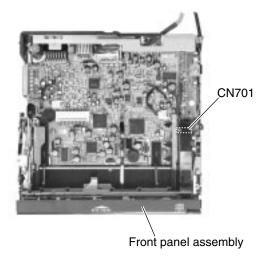


Fig.6-2 (KD-LX100)

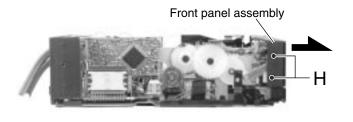
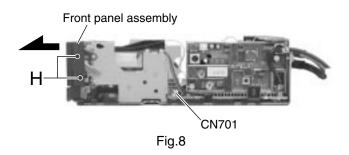
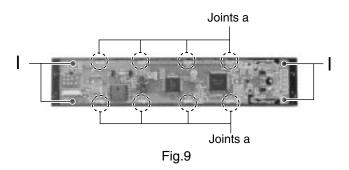


Fig.7



# ■ Removing the Front Board (See Fig.9)

- Prior to performing the following procedure, remove the top chassis assembly and the front panel assembly.
- 1. Remove the four screws I attaching the front board on the back of the front panel assembly and release the eight joints **a**.



### ■ Removing the lifter unit (See Fig.10)

- Prior to performing the following procedure, remove the top chassis assembly and the front panel assembly.
- 1. Disconnect the harness from connector CN503and CN504 on the main board.
- 2. Remove the four screws **J** and detach the lifter unit from the bottom cover.

### ■ Removing the feed motor (L) (See Fig.11)

- · Prior to performing the following procedure, remove the lifter unit.
- 1. Remove the washer attaching the clutch assembly and detach the clutch assembly from the shaft of the lifter unit.
- 2. Remove the two screws  ${\bf K}$  attaching the feed motor (L).

## ■ Removing the feed motor (R) (See Fig.12)

- · Prior to performing the following procedure, remove the lifter unit.
- 1. Remove the washer attaching the clutch assembly and detach the clutch assembly from the shaft of the lifter unit
- 2. Remove the two screws **L** attaching the feed motor (R).

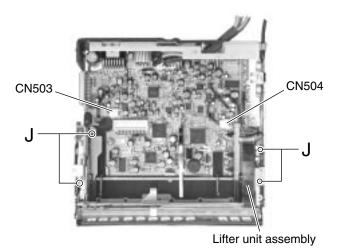


Fig.10-1 (KD-LX300)

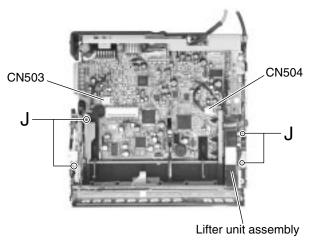
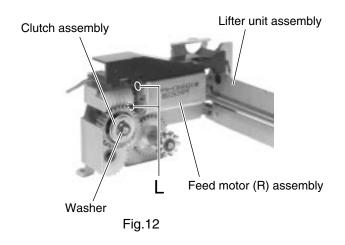
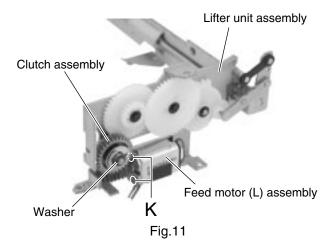


Fig.10-2 (KD-LX100)

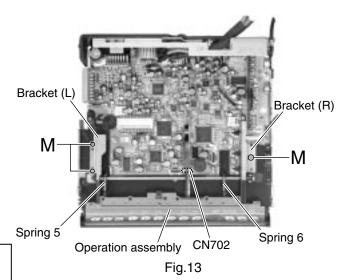


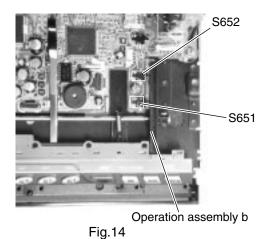


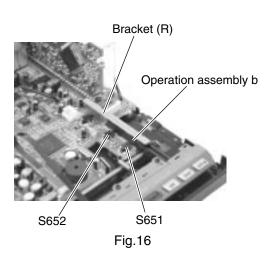
# ■ Removing the operation assembly (See Fig.13 to 17)

- Prior to performing the following procedure, remove the top chassis assembly, the front panel assembly and the lifer unit.
- 1. Disconnect the card wire from connector CN702 on the main board and remove the operation assembly.
- 2. Remove the three screws **M** attaching the right and left brackets which fix gears on both sides of the operation assembly.
- 3. Remove the springs 5 and 6 from the operation assembly.

ATTENTION: When reassembling, correctly engage the switch S651 and S652 on the main board and the right gear with the part **b** of the operation assembly.







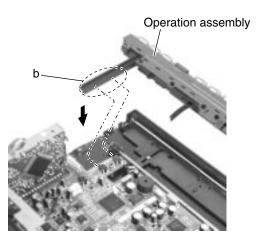


Fig.15

# ■ Removing the operation switch board (See Fig.17 and 18)

- · Prior to performing the following procedure, remove the operation assembly.
- 1. Remove the six screws **N** attaching the button panel on the operation assembly.
- 2. Pull out the operation switch board from inside of the button panel.

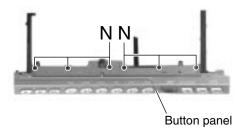


Fig.17

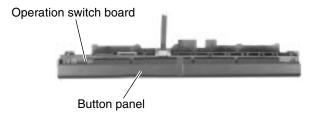


Fig.18

# ■ Removing the CD mechanism assembly (See Fig.19)

- · Prior to performing the following procedure, remove the top chassis.
- 1. Remove the three screws **O** and the CD mechanism assembly from the top chassis.

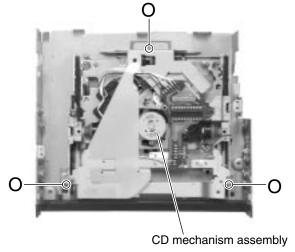
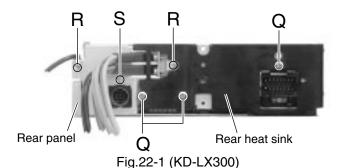


Fig.19

# ■ Removing the main board assembly (See Fig.20 to 22)

- Prior to performing the following procedure, remove the top chassis.
- Disconnect the flexible harness from connector CN701, the card wire from CN702 on the main board and the harness from CN503 and CN504 respectively.
- 2. Remove the three screws **P** attaching the main board assembly to the bottom cover on the upper side of the body.
- 3. Move the main board in the direction of the arrow and release the three joints **c**. (At this point, the main board can be removed with the rear panel and the rear heat sink.)
- 4. Remove the three screws **Q** attaching the rear heat sink on the back of the body.
- 5. Remove the two screws **R** and the screw **S** attaching the rear panel. Now, the main board assembly will be removed.

ATTENTION: When reassembling, correctly engage the switch S651 and S652 on the main board and the right gear with the part **b** of the operation assembly (Refer to Fig.21).



Rear panel Q Rear heat sink

Fig.22-2 (KD-LX100)

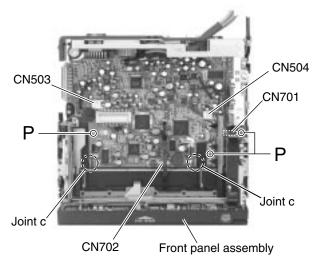


Fig.20-1 (KD-LX300)

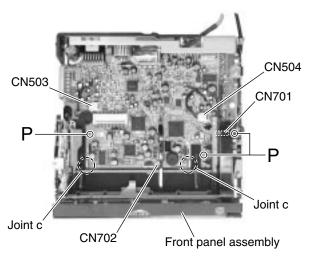
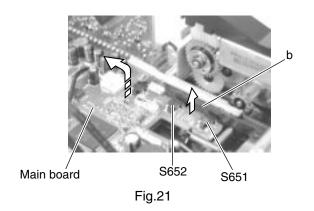


Fig.20-2 (KD-LX100)

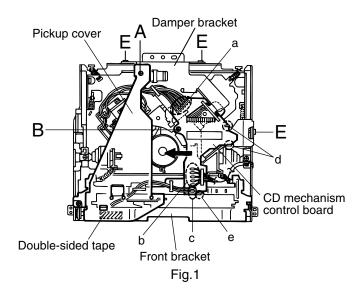


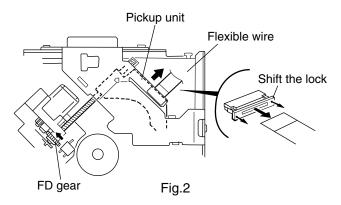
### <CD mechanism section>

# ■ Removing the CD mechanism control board (See Fig.1 and 2)

- 1. Remove the screw **A** and the pickup cover attached to the front bracket with the double-sided tapes.
- 2. Unsolder the three parts **a**, **b** and **c** on the CD mechanism control board.
- 3. Remove the stator fixing the CD mechanism control board and the damper bracket (To remove the stator smoothly, pick up the center part).
- Remove the screw B attaching the CD mechanism control board.
- 5. Remove the CD mechanism control board in the direction of the arrow while releasing it from the two damper bracket slots **d** and the front bracket slot **e**.
- 6. Disconnect the flexible wire from connector on the pickup unit.

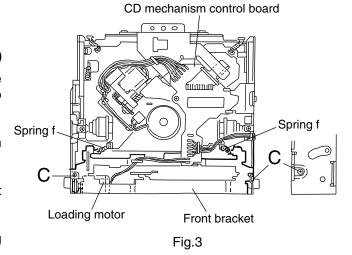
ATTENTION: Turn the FD gear in the direction of the arrow to move the entire pickup unit to the appropriate position where the flexible wire of the CD mechanism unit can be disconnected easily (Refer to Fig.2).

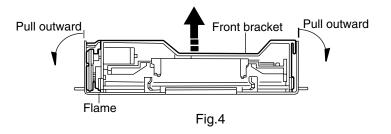




# ■ Removing the loading motor (See Fig.3 to 5)

- Prior to performing the following procedure, remove the CD mechanism control board and the pickup cover.
- 1. Remove the two springs **f** attaching the CD mechanism assembly and the front bracket.
- 2. Remove the two screws **C** and the front bracket while pulling the flame outward.
- 3. Remove the belt and the screw **D** from the loading motor.





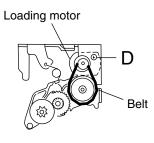
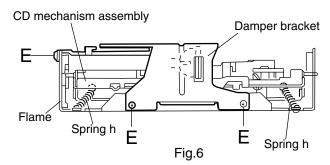


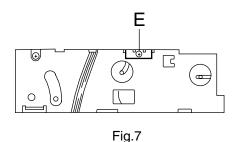
Fig.5

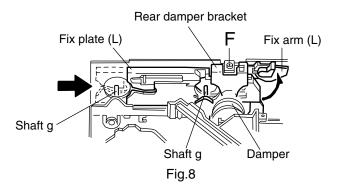
# ■ Removing the CD mechanism assembly (See Fig.1, 6 to 9)

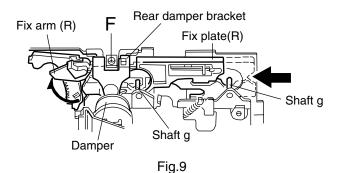
- Prior to performing the following procedure, remove the CD mechanism control board and the front bracket (loading motor).
- Remove the three screws E and the damper bracket.
- 2. Raise the both sides fix arms and move the fix plates in the direction of the arrow to place the four shafts **g** as shown in Fig.8 and 9.
- 3. Remove the CD mechanism assembly and the two springs **h** attaching the flame.
- Remove the two screws F and both sides rear damper brackets from the dampers. Detach the CD mechanism assembly from the left side to the right side.

ATTENTION: The CD mechanism assembly can be removed if only the rear damper bracket on the left side is removed.



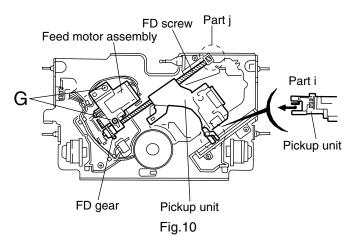






# ■ Removing the feed motor assmbly (See Fig.10)

- Prior to performing the following procedure, remove the CD mechanism control board, the front bracket (loading motor) and the CD mechanism assembly.
- Remove the two screws G and the feed motor assembly.



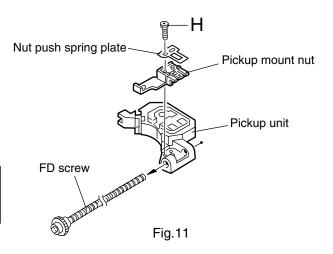
# ■ Removing the pickup unit

### (See Fig.10 and 11)

- Prior to performing the following procedure, remove the CD mechanism control board, the front bracket (loading motor), the CD mechanism assembly and the feed motor assembly.
- 1. Detach the FD gear part of the pickup unit upward. Then remove the pickup unit while pulling out the part j of the FD screw.

ATTENTION: When reattaching the pickup unit, reattach the part i of the pickup unit, then the part j of the FD screw.

2. Remove the screw **H** attaching the nut push spring plate and the pickup mount nut from the pickup unit. Pull out the FD screw.



# ■ Removing the spindle motor (See Fig.12 and 13)

- Prior to performing the following procedure, remove the CD mechanism control board, the front bracket (loading motor), the CD mechanism assembly and the feed motor assembly.
- 1. Turn up the CD mechanism assembly and remove the two springs **k** on both sides of the clamper arms. Open the clamper arm upward.
- 2. Turn the turn table and remove the two screws I and the spindle motor.

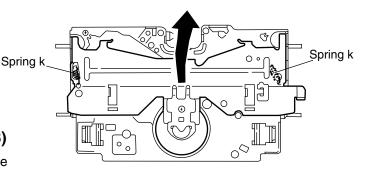
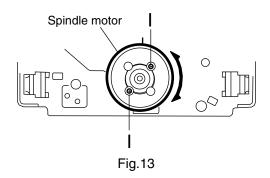


Fig.12



# **Adjustment method**

- Test instruments required for adjustment
  - 1. Digital oscilloscope (100MHz)
  - 2. AM Standard signal generator
  - 3. FM Standard signal generator
  - 4. Stereo modulator
  - 5. Electric voltmeter
  - 6. Digital tester
  - 7. Tracking offset meter
  - 8. Test Disc JVC :CTS-1000
  - 9. Extension cable for check EXTGS004-26P × 1
- Standard measuring conditions

Power supply voltage DC14.4V(10.5~16V)

Load impedance 20Kohm(2 Speakers connection)
Output Level Line out 2.0V (Vol. MAX)

■ How to connect the extension cable for adjusting

■ Standard volume position

Balance and Bass &Treble volume: Indication"0"

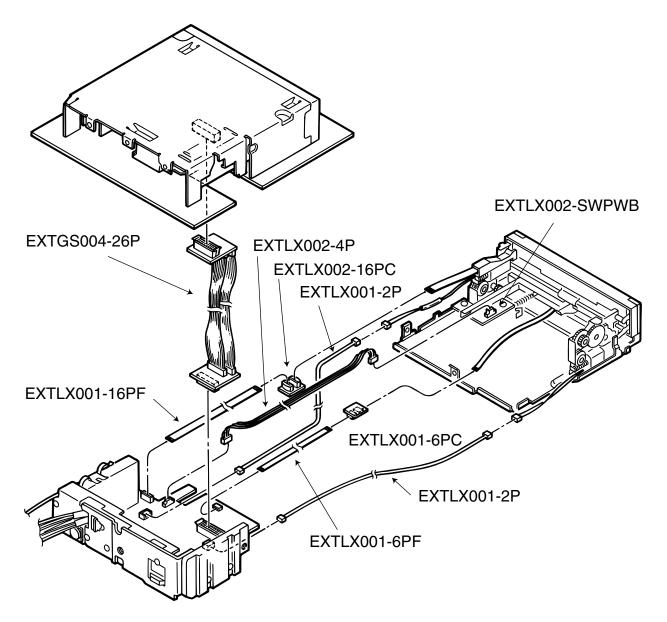
Loudness : OFF BBE : OFF

Frequency Band

■ FM 87.5MHz ~ 108.0MHz MW 520kHz ~ 1620 kHz

■ Dummy load

Exclusive dummy load should be used for AM,and FM. For FM dummy load,there is a loss of 6dB between SSG output and antenna input. The loss of 6dB need not be considered since direct reading of figures are applied in this working standard.

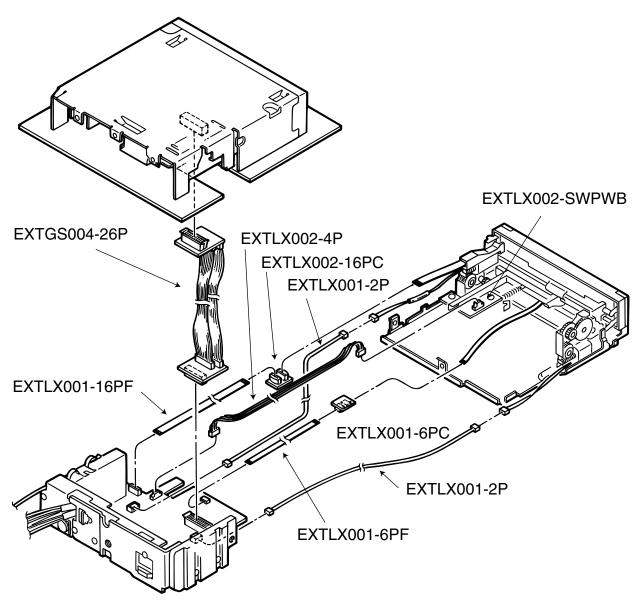


# **Extension cord connecting method**

### Using the extention cords to connect the front panel with the main board

Remove the main board follwing the disassembly methode. Then reattachi the heat sink to main board.

- 1. Using the 2pin extention cord (EXTLX001-2p), connect the harness of the feed motor (L) assembly with the connector CN503 on the main board.
- 2. Using the 2pin extention cord (EXTLX001-2p), connect the harness of the feed motor (R) assembly with the connector CN504 on the main board.
- Using the jig board (EXTLX002-SWPWB), its installing to the chassis, then using 4pin extention cord (EXTLX002-4P) connect the harness of the lifter detecting board with the connector CN704 on the board.
- 4. Connect the connector (EXTLX001-6PC) and extension wire (EXTLX001-6PF), connect the 6pin connector CN702 on the main board.
- 5. Connect the connector (EXTLX002-16PC) and extension wire (EXTLX002-16PF), connect the 16pin connector CN701 on the main board.

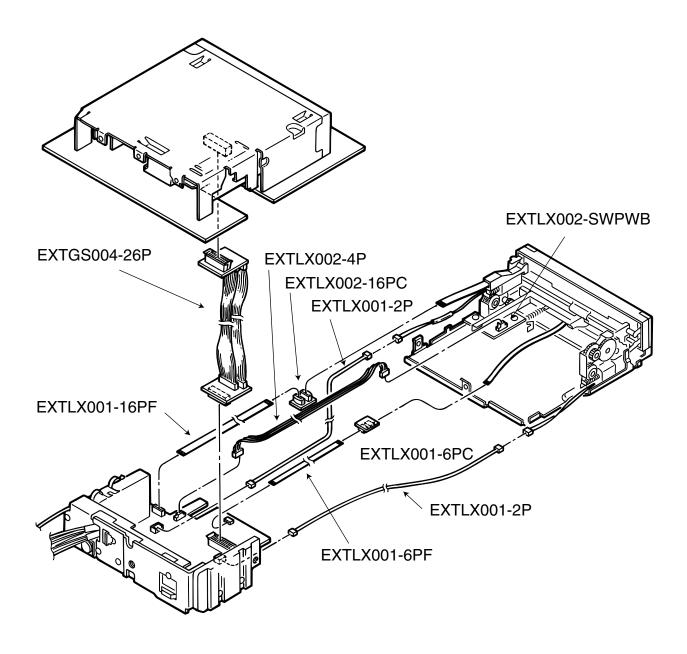


### **■** Extension cord list

EXTLX002-JIG: Kit including the following 8 extension parts.

No.	Parts number	Quantity	Description
1	EXTLX001-2P	2	2Pin, 30cm extension cord
2	EXTLX001-6PF	1	6Pin, 30cm flat wire
3	EXTLX001-6PC	1	6Pin x 2, interlocking connector
4	EXTLX002-16PF	1	16Pin flat wire
5	EXTLX002-16PC	1	16Pin, interlocking connector
6	EXTLX002-SWPWB	1	3 switch PWB
7	EXTLX002-4P	1	4Pin, 30cm extension cord

Besides the above kit, we offer the conventional extension cord for CD mechanism which are not essential to operation check or service. The mechanism should be directly connected to the board using the extension wire. EXTGS004-26P

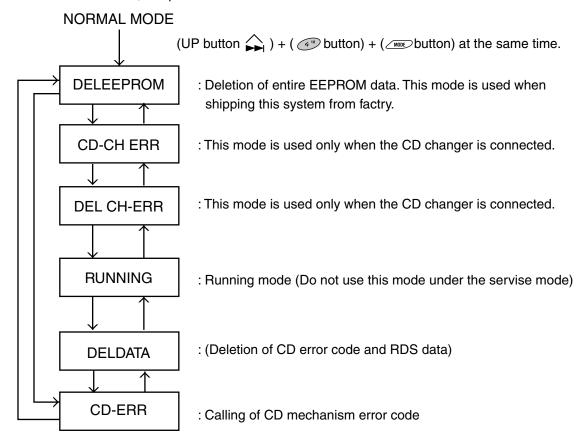


# Functions of the mechanism under the service mode

With the three error modes stored in maximum in the internal memory of the mechanism in the body of this system, it is posible under the service mode to call the contents of error according to the following steps when any error has occurred.

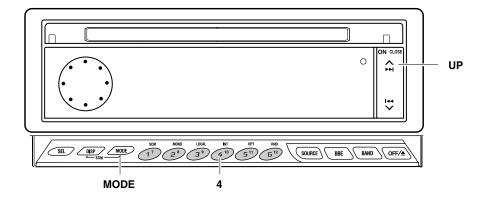
Press the three buttons (UP button )+( button)+(Func button ). Then it is possible to select the following service modes. After changing over to the service mode, press the UP button ) and DOWN button ) to change the mode. For executing the respective service modes, press the SEL button.

With the service mode 2, it is possible to call the error codes of the mechanism.



Data stored in EEPROM

- 1. RDS data
- 2. CD mechanism error cord
- 3. Station name (to be input by user)
- 4. DISC name (to be input by user)
- 5. AUX input name
- \*Any data 3 to 5 above should not be deleted.



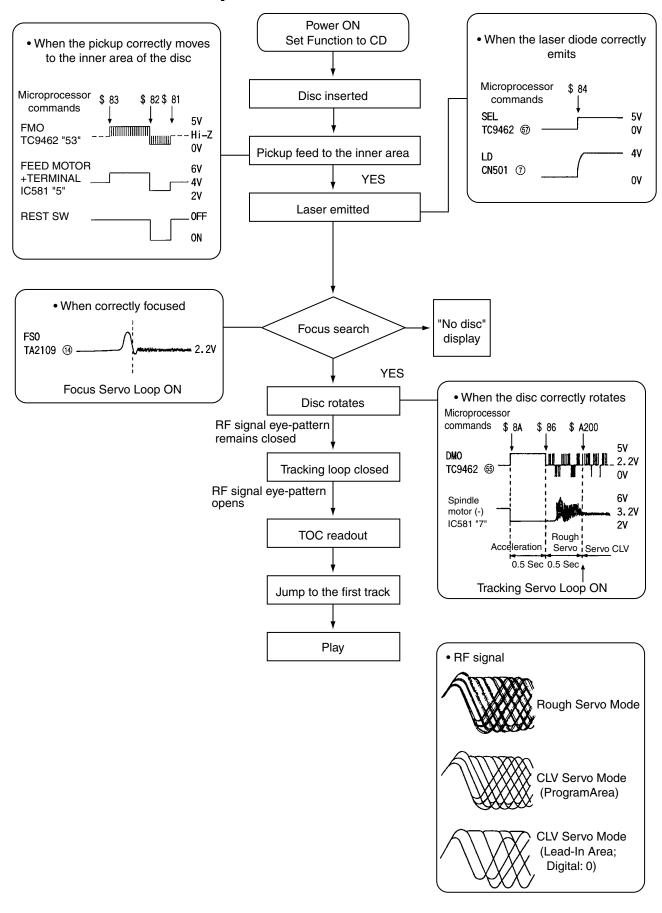
# 1. Display of mechanism error

Occurrence condition	Description	Error codes
Disc loading error	SW4 is not turned off.     SW3 is not turned on.	09 0011 09 0013
Eject error	1. SW# is not turned off.	01 0021
Error during standby for loading	In case SW2 has been positioned to "L" before starting loading during waiting for 15sec.	80 0031

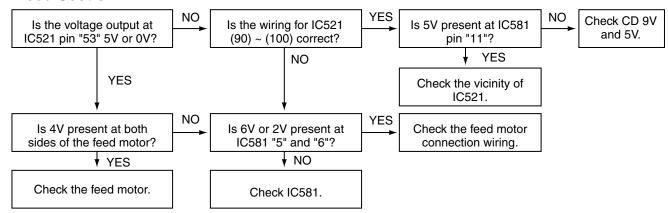
# 2. Display of CD error

Occurrence condition	Description	Error codes
Pickup feeding error		
Inner peripheral feeding error (10sec.)	The pickup cannot returned to the inner peripheral, and the REST switch is not turned off.	04 0051
2. Outer peripheral feeding error (10sec.)	The pickup cannot be returned to the outer peripheral, and the REST switch is not turned off.	04 0052
Focus search error	In case the focus cannot be searched by one set	
In the case of focusing error after 3-way focus searching	of focus searching (3-way focus searching) after disc change and focus shock, judge that the focus searching system is in error.	81 0053
Tracking balance adjusting error In the case of time-over (1sec.) of timer	In case tracking balance cannot be adjusted even after elapse of 1sec. following execution of the adjusting command (TBA).	82 0054
TOC area searching error	,	
In the case of time-over (10sec.) of timer	In case TOC area searching is not ended even after elapse of 10sec.	82 0055
Reading error IN the case of time-over (30sec.) of timer	In case reading is not ended even after elapse of 30 sec. during TOC reading action.	84 0059
1st tracking access error In the case of time-over (10sec.) of timer	In case the first tracking access is not ended even after elapse of 10sec. following completion of TOC reading.	80 0060
Last tracking access error In the case of time-over (10sec.) of timer	In case the last tracking access is not ended even after elapse of 10sec. following completion of first tracking under the RUNNING mode.	80 0061
Q code reading error In the case of time-over (0.6sec.) of timer	In case the Q code cannot be read for 0.6sec. during playing TOC program area.	80 0062
TEXT data reading error	In case all TEXT data cannot be read.	80 0063

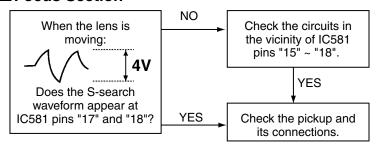
# Flow of functional operation until TOC read



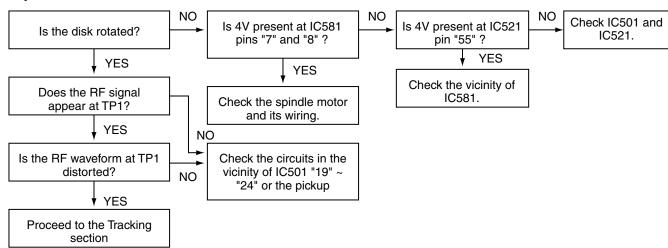
### **■**Feed Section



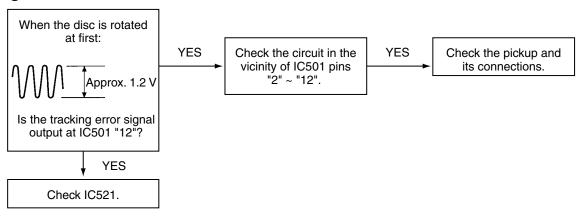
### **■** Focus Section



### **■**Spindle Section

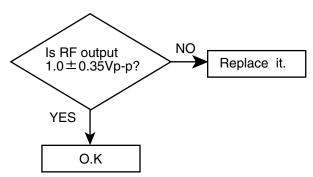


### ■ Tracking Section



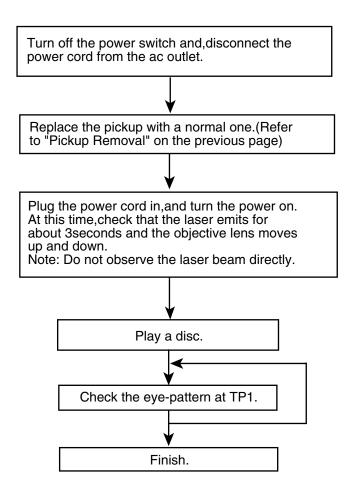
# Maintenance of laser pickup

- (1) Cleaning the pick up lens Before you replace the pick up, please try to clean the lens with a alcohol soaked cotton swab.
- (2) Life of the laser diode When the life of the laser diode has expired. the following symptoms will appear.
  (1) The level of RF output (EFM output:ampli
  - tude of eye pattern) will be low.



(3) Semi-fixed resistor on the APC PC board The semi-fixed resistor on the APC printed circuit board which is attached to the pickup is used to adjust the laser power. Since this adjustment should be performed to match the characteristics of the whole optical block, do not touch the semi-fixed resistor. If the laser power is lower than the specified value, the laser diode is almost worn out, and the laser pickup should be replaced. If the semi-fixed resistor is adjusted while the pickup is functioning normally, the laser pickup may be damaged due to excessive current.

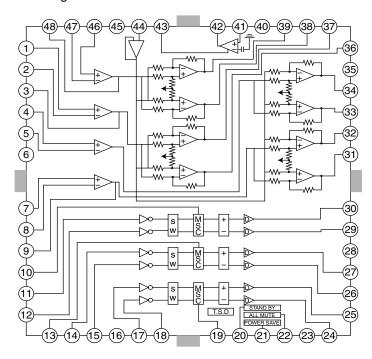
# Replacement of laser pickup



# **Description of major ICs**

# ■ FAN8037 (IC661) : CD driver

1. Pin layout & Block diagram



### 2. Pin function

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	IN2+	I	CH2 op-amp input(+)	25	DO7+	0	CH7 drive output(+)
2	IN2-	ı	CH2 op-amp input(-)	26	DO6-	0	CH6 drive output(-)
3	OUT2	0	CH2 op-amp output	27	DO6+	0	CH6 drive output(+)
4	IN3+	ı	CH3 op-amp input(+)	28	PGND2	-	Power ground2
5	IN3-	ı	Ch3 op-amp input(-)	29	DO5-	0	CH5 drive output(-)
6	OUT3	0	CH3 op-amp output	30	DO5+	0	CH5 drive output(+)
7	IN4+	ı	CH4 op-amp input(+)	31	DO4-	0	CH4 drive output(-)
8	IN4-	ı	CH4 op-amp input(-)	32	DO4+	0	CH4 drive output(+)
9	OUT4	0	CH4 op-amp output(+)	33	DO3-	0	CH3 drive output(-)
10	CTL1	ı	CH5 motor speed control	34	DO3+	0	CH3 drive output(+)
11	FWD1	ı	CH5 forward input	35	PGND1	•	Power ground1
12	REV1	ı	CH5 reverse input	36	DO2-	0	CH2 drive output(-)
13	CTL2	ı	CH6 motor speed control	37	DO2+	0	CH2 drive output(+)
14	FWD2	ı	CH6 forward input	38	DO1-	0	CH1 drive output(-)
15	REV2	ı	CH6 reverse input	39	DO1+	0	CH1 drive output(+)
16	SGND	-	Signal ground	40	PVCC1	-	Power supply voltage
17	FWD3	ı	CH7 forward input	41	REGOX	ı	Regulator feedback input
18	REV3	ı	CH7 reverse input	42	REGX	0	Regulator output
19	CTL3	ı	CH7 motor speed control	43	RESX	ı	Regulator reset input
20	SB	ı	Stand by	44	VREF	ı	Bias voltage input
21	PS	ı	Power save	45	SVCC	-	Signal supply voltage
22	MUTE	ı	All mute	46	IN1+	I	CH1 op-amp input(+)
23	PVCC2	-	Power supply voltage	47	IN1-	ı	CH1 op-amp input(-)
24	DO7-	0	CH7 drive output(-)	48	OUT1	0	CH1 op-amp output

# ■ UPD784215AGC-128 (IC701) : UNIT CPU 1.Terminal Layout

75	~	51
76		50
1		1
100		26
\ 1	~	25

# 2.Pin Function (1/2)

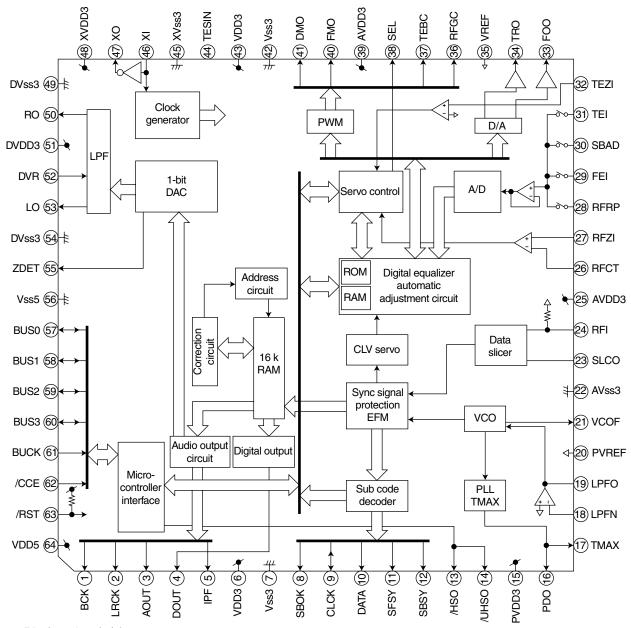
Pin No.	Symbol	I/O	Function
1	SW2	ı	Detection switch of CD mechanism
2	SW3	I	Detection switch of CD mechanism
3	SW4	ı	Detection switch of CD mechanism
4	REST-SW	ı	Reset signal input from CD mechanism
5	LM0	0	Loading motor control signal output
6	LM1	0	Loading motor control signal output
7	DIMMER-OUT	0	Dimmer signal output
8	LCD-PWR	0	LCD driver power supply control output H:ON
9	VDD	-	Power supply terminal
10	X2	-	Connecting the crystal oscillator for system main clock
11	X1	-	Connecting the crystal oscillator for system main clock
12	VSS	-	Power supply terminal
13	XT2	-	Connecting the crystal oscillator for system sub clock
14	XT1	-	Connecting the crystal oscillator for system sub clock
15	RESET	Ι	System reset signal input
16	SW1	ı	Detection switch of CD mechanism
17	BUS-INT	Ι	Cut-in input for J-BUS signal
18	PS2	ı	Power save 2, Working together back up by H input, to stop mode
19	CRUISE	ı	Pulse signal input port for Cruise control
20	NC	-	Clock signal input for RDS
21	NC	-	RDS data input
22	REMOCON	ı	Remote control signal input
23	AVDD	-	Power supply terminal
24	AVREF0	-	Power supply terminal
25	VOL1	Ι	Input for rotation volume detection pulse judgment to relation V1
26	VOL2	I	Input for rotation volume detection pulse judgment to relation V2
27	KEY0	I	Key control signal input 0
28	KEY1	I	Key control signal input 1
29	KEY2	I	Key control signal input 2
30	LEVEL		Signal input port of level meter
31	NC		Non connect
32	S.METER	Ι	S.Meter level input
33	AVSS		Connect to GND
34	W-VOL	0	Subwoofer volume control analogue output
35	DOT-CONT	0	Dot contrast signal output
36	AVREF	-	Power supply terminal
37	BUS-SI	I	J-BUS data input
38	BUS-SO	0	J-BUS data output
39	BUS-SCK	I/O	J-BUS Clock signal I/O
40	STAGE2	I	Initial setting
41	LCD-DA	0	Data output to LCD driver
42	LCDCL	0	Clock output to LCD driver

## Pin Function (2/2)

D: N	0	1.0	Fination
Pin No.	Symbol	I/O	Function
43	LCD-CE1	0	Chip enable output to LCD driver
44	BUZZER	0	BUZZER control signal output
45	E2PR-DA-I	I	Data input terminal from EEPROM
46	E2PR-DA-O	0	Data output terminal for EEPROM
47	E2PR-CLK	0	Clock signal I/O terminal with EEPROM
48	BUS-I/O	I/O	J-BUS I/O signal terminal
49	TM0	0	Tray motor negative signal output terminal
50	TM1	0	Tray motor positive signal output terminal
51	DM0	0	Door motor negative signal output terminal
52	DM1	0	Door motor positive signal output terminal
53	SD/ST	I	Station detector, Stereo signal input, H:Find Station L:Stereo
54	LOCAL	0	Local ON/OFF select signal output terminal
55	MONO	0	Monaural ON/OFF selecting output, H:MONO ON
56~60	CA-SW1~5	I	DOOR/TRAY open close detect switch signal input terminal
61,62	NC	-	Non connect
63	SEEK/STOP	0	Auto seek/stop selecting output, H:Seek L:Stop
64	NC	-	Non connect
65	FM/AM	0	Selecting output for FM/AM, L:FM H:AM
66	PLL-CE	0	CE output for IC control for PLL
67	PLL-DA	0	Data output for IC control for PLL
68	PLL-CK	0	Clock output for IC control for PLL
69	BAND IN	ī	AM detect signal input
70	NC	-	Non connect
71	AMP KILL	_	Non connect
72	VSS	<b>-</b>	Connect to GND
73	DIMMER-IN	ı	DIMMER signal input terminal
74	PS1	i	Power supply terminal
75	POWER	Ö	Selecting output for power ON/OFF, H:power ON
76	CD-ON	0	Power supply control signal for CD H:CD
77	MUTE	0	MUTE output, L:MUTE ON
78	W-LPF1	0	Subwoofer cut off frequency output 1
79	W-LPF2	0	Subwoofer cut off frequency output 2
80	W-MUTE	0	MUTE output for Subwoofer
81	VDD	-	Power supply terminal
82	VO-DA	0	Data output terminal
83	VOL-CLK	0	Clock signal output terminal
84	NC		Non connect
85	GVSW	-	AGC/FE/TE amp gain change terminal
	LCDRST	0	· • •
86		0	LCD reset signal output terminal
87	LCD-CE2 DMK	0	Chip enable 2 output terminal for LCD driver
88		0	Motor speed control signal output terminal
89	TMK	0	Tray motor control signal output terminal
90	NC	-	Non connect
91	BUCK	0	Micon interface clock output terminal
92	CCE	0	Command and data sending/receiving chip enable signal output
93	RST	0	Reset signal output terminal reset at "L" level
94	TEST	-	Connect to GND
95~98	BUS0~3	I/O	Micon interface data input/output terminal
99	DISC SEL	I	Initial setting
100	NC	-	Non connect

## ■TC9490FA (IC521): DSP

### 1. Pin layout & Block diagram



### 2. Pin function (1/2)

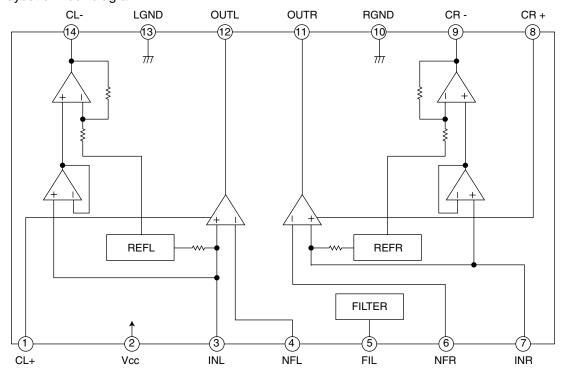
Pin No.	Symbol	I/O	Function
1	BCK	0	Bit clock output terminal
2	LRCK	0	L/R channel clock output terminal
3	AOUT	0	Audio data output terminal
4	DOUT	0	Digital data output terminal
5	IPF	0	Correction flag output terminal
6	VDD3	-	Digital 3.3V power supply voltage terminal
7	Vss3	-	Digital GND terminal
8	SBOK	0	Subcode Q data CRCC result output terminal
9	CLCK	0	Subcode P-W data read clock I/O terminal
10	DATA	0	Subcode P-W data output terminal
11	SFSY	0	Playback frame sync signal output terminal
12	SBSY	0	Subcode block sync signal output terminal
13	/HSO	0	Playback speed mode output terminal

## 2. Pin function (2/2)

Pin No.   Symbol   Vo		011011 (2/2)	1/0	F P
16    PVDD3	Pin No.	Symbol	I/O	Function
16 PDO O EFM and PLCK phase difference signal output terminal 17 TMAX O TMAX detection result output terminal 18 LPFN I Inverted input terminal for PLL LPF amp 19 LPFO O Outpuit terminal for PLL LPF amp 20 PYREF - PLL-only VRDEF terminal 21 VCOF O VCO filter terminal 22 AVss3 - Analog GND terminal 23 SLCO O DAC output terminal for data slice level generation 24 RFI I RF signal input terminal 25 AVDD3 - Analog 3.3V power supply voltage terminal 26 RFCT I RFRP signal zero-cross input terminal 27 RFZI I RFRP signal zero-cross input terminal 28 RFRP I RFR ripple signal input terminal 29 FEI I Focus error signal input terminal 30 SBAD I Sub-beam adder signal input terminal 31 TEI I Tracking error ripput terminal 32 TEZI I Tracking error signal zero-cross input terminal 33 FOO O Focus equalizer output terminal 34 TRO O Tracking equalizer output terminal 35 VREF - Analog reference power supply vpltage terminal 36 RFGC O RF amplitude adjustment control signal output terminal 37 TEBC O Tracking balance control signal output terminal 40 FMO O Feed equalizer output terminal 41 DMO O Disc equalizer output terminal 42 Vss3 - Digital 3.3V power supply voltage terminal 44 TESIN I Test In Ser in terminal 45 XVss3 - System clock oscillator GND terminal 46 XI I System clock oscillator GND terminal 47 XVs0 O System clock oscillator GND terminal 48 XVDD3 - Analog 3.3V power supply voltage terminal 49 DVss3 - Digital 3.3V power supply voltage terminal 50 RO O R-channel data forward output terminal 51 DVDD3 - DA converter 3.3V power supply voltage terminal 52 DVR - Reference voltage terminal 53 CVEF - DIGITAL SYSTEM CONTROL TERMINAL 54 DVSS3 - Digital GND terminal 55 DVR - Reference voltage terminal 56 VSS5 - Microcontroller interface data I/O terminal 57 DVDD3 - DA converter GND terminal 58 DUS I/O Microcontroller interface clock input terminal 59 BUS2 I/O Microcontroller interface clock input terminal 60 BUSS I/O Microcontroller interface clock input terminal 61 BUCK I Microcontroller interface clock input terminal				•
17 TMAX O TMAX detection result output terminal 18 LPFN I Inverted input terminal for PLL LPF amp 19 LPFO O Output terminal for PLL LPF amp 20 PVREF - PLL-only VREF terminal 21 VCOF O VCO filter terminal 22 AVss3 - Analog GND terminal 23 SLCO O DAC output terminal for data slice level generation 24 RFI I RF signal input terminal 25 AVDD3 - Analog 3.3V power supply voltage terminal 26 RFCT I RFRP signal zero-cross input terminal 27 RFZI I RFRP signal zero-cross input terminal 28 RFRP I RFP signal zero-cross input terminal 29 FEI I Focus error signal input terminal 30 SBAD I Sub-beam adder signal input terminal 31 TEI I Tracking error input terminal 32 TEZI I Tracking error input terminal 33 FOO O Focus equalizer output terminal 34 TRO O Tracking equalizer output terminal 35 VREF - Analog reference power supply voltage terminal 36 RFGC O RF amplitude adjustment control signal output terminal 37 TEBC O Tracking balance control signal output terminal 38 SEL O APC circuit ON/OFF signal output terminal 40 FMO O Disc equalizer output terminal 41 DMO O Disc equalizer output terminal 42 Vss3 - Digital GND terminal 43 VDD3 - Digital SJV power supply voltage terminal 44 TESIN I Test input terminal 45 XVss3 - System clock oscillator input terminal 46 XI System clock oscillator input terminal 57 DA Concrete Control signal output terminal 58 VSS3 - Digital GND terminal 59 RFG O R- Analog reference power supply voltage terminal 50 RFG O DA Concrete Control signal output terminal 51 DMO O Disc equalizer output terminal 52 DA Concrete Control Signal output terminal 53 VSS3 - Digital GND terminal 54 XVss3 - System clock oscillator input terminal 55 DWD3 - Digital SJ Vpower supply voltage terminal 56 NS System clock oscillator input terminal 57 DA Concrete GND terminal 58 DA Concrete GND terminal 59 DWS - DA converter GND terminal 50 DWD3 - DA converter GND terminal 51 DVD3 - DA converter GND terminal 53 LO O L-channel data forward output terminal 56 Vss5 - Microcontroller interface clock input terminal 57 BUSO I/O Microcontrolle				
18	16			·
19 LPFO O Outpuit terminal for PLL LPF amp 20 PVREF - PLL-only VREF terminal 21 VCOF O VCO filter terminal 22 AVSS3 - Analog GND terminal 23 SLCO O DAC output terminal for data slice level generation 24 RFI I RF signal input terminal 25 AVDD3 - Analog 3.3V power supply voltage terminal 26 RFCT I RFRP signal center level input terminal 27 RFZI I RFRP signal zero-cross input terminal 28 RFRP I RFR signal zero-cross input terminal 29 FEI I Focus error signal input terminal 30 SBAD I Sub-beam adder signal input terminal 31 TEI I Tracking error input terminal 32 TEZI I Tracking error signal input terminal 33 FOO O Focus equalizer output terminal 34 TRO O Tracking equalizer output terminal 35 VREF - Analog reference power supply voltage terminal 36 RFGC O RF amplitude adjustment control signal output terminal 37 TEBC O Tracking balance control signal output terminal 38 SEL O APC circuit ON/OFF signal output terminal 40 FMO O Feed equalizer output terminal 41 DMO O Disc equalizer output terminal 41 DMO O Disc equalizer output terminal 42 Vss3 - Digital GND terminal 44 TESIN I Test input terminal 45 XVSS3 - System clock oscillator output terminal 46 XI System clock oscillator frout terminal 57 CA O System clock oscillator output terminal 58 DVR - Reference observed by terminal 59 DVR - Reference observed by over supply voltage terminal 50 RO O Disc equalizer output terminal 51 DVDD3 - Digital 3/3 y power supply voltage terminal 52 DVR - Reference observed by over supply voltage terminal 55 DVR - Reference observed output terminal 56 Vss5 - DA converter GND terminal 57 DVD3 - DA converter GND terminal 58 LO O L-channel data forward output terminal 59 DVR - Reference voltage terminal 50 DVR - Reference voltage terminal 51 DVDD3 - DA converter GND terminal 52 DVR - Reference voltage terminal 53 LO O L-channel data forward output terminal 54 DVSs3 - DA converter GND terminal 55 ZDET O 1 bit DA converter GND terminal 56 Vss5 - Microcontroller interface data I/O terminal 57 BUSU I/O Microcontroller interface data I/O termina	17	TMAX	0	•
20	18	LPFN	ı	Inverted input terminal for PLL LPF amp
21 VCOF O VCO filter terminal 22 AVss3 - Analog GND terminal 23 SLCO DAC output terminal for data slice level generation 24 RFI I RF signal input terminal 25 AVDD3 - Analog 3.3V power supply voltage terminal 26 RFCT I RFRP signal center level input terminal 27 RFZI I RFRP signal center level input terminal 28 RFRP I RFRP signal zero-cross input terminal 29 FEI I Focus error signal input terminal 30 SBAD I Sub-beam adder signal input terminal 31 TEI I Tracking error input terminal 32 TEZI I Tracking error signal input terminal 33 FOO O Focus equalizer output terminal 34 TRO O Tracking equalizer output terminal 35 VREF - Analog reference power supply vpltage terminal 36 RFGC O RF amplitude adjustment control signal output terminal 37 TEBC O Tracking balance control signal output terminal 38 SEL O APC circuit ON/OFF signal output terminal 39 AVDD3 - Analog 3.3V power supply voltage terminal 40 FMO O Feed equalizer output terminal 41 DMO O Disc equalizer output terminal 42 Vss3 - Digital GND terminal 44 TESIN I Test input terminal 45 XVSs3 - System clock oscillator GND terminal 46 XI System clock oscillator GND terminal 47 XO O System clock oscillator GND terminal 48 XVDD3 - Da Converter 3.3V power supply voltage terminal 49 DVss3 - DA converter GND terminal 50 RO O R-channel data forward output terminal 51 DVDD3 - DA converter GND terminal 52 DVR - Reference voltage terminal 53 CD - Channel data forward output terminal 54 DVss3 - DA converter GND terminal 55 DVR - Reference voltage terminal 56 Vss5 - Microcontroller interface data I/O terminal 57 BUSO I/O Microcontroller interface data I/O terminal 58 BUS1 I/O Microcontroller interface data I/O terminal 59 BUS2 I/O Microcontroller interface clock input terminal 60 BUS3 I/O Microcontroller interface clock input terminal 61 BUCK I Microcontroller interface clock input terminal 62 I/CCE I Microcontroller interface clock input terminal	19	LPFO	0	Outpuit terminal for PLL LPF amp
22 AVss3 - Analog GND terminal 23 SLCO O DAC output terminal for data slice level generation 24 RFI I RF signal input terminal 25 AVDD3 - Analog 3.3V power supply voltage terminal 26 RFCT I RFRP signal center level input terminal 27 RFZI I RFRP signal zero-cross input terminal 28 RFRP I RF ripple signal input terminal 29 FEI I Focus error signal input terminal 30 SBAD I Sub-beam adder signal input terminal 31 TEI I Tracking error input terminal 31 TEI I Tracking error signal zero-cross input terminal 32 TEZI I Tracking error signal zero-cross input terminal 33 FOO O Focus equalizer output terminal 34 TRO O Tracking equalizer output terminal 35 VREF - Analog reference power supply voltage terminal 36 RFGC O RF amplitude adjustment control signal output terminal 37 TEBC O Tracking balance control signal output terminal 38 SEL O APC circuit ON/OFF signal output terminal 40 FMO O Feed equalizer output terminal 41 DMO O Disc equalizer output terminal 42 Vss3 - Digital GND terminal 43 VDD3 - Analog 3.3V power supply voltage terminal 44 TESIN I Test input terminal 45 XVss3 - Digital 3.0V power supply voltage terminal 46 XI I System clock oscillator GND terminal 47 XO O System clock oscillator input terminal 48 XVDD3 - System clock oscillator input terminal 49 DVss3 - Digital GND terminal 50 RO O R-channel data forward output terminal 51 DVDD3 - DA converter GND terminal 52 DVR - Reference voltage terminal 53 LO O L-channel data forward output terminal 54 DVss3 - DA converter GND terminal 55 DVss5 - Microcontroller interface data I/O terminal 56 Vss5 - Microcontroller interface data I/O terminal 57 BUSO I/O Microcontroller interface data I/O terminal 58 BUS1 I/O Microcontroller interface data I/O terminal 59 BUSC I/O Microcontroller interface clock input terminal 60 BUS3 I/O Microcontroller interface clock input terminal 61 BUCK I Microcontroller interface clock input terminal	20	PVREF	-	PLL-only VREF terminal
23 SLCO O DAC output terminal for data slice level generation 24 RFI I RF signal input terminal 25 AVDD3 - Analog 3,3V power supply voltage terminal 26 RFCT I RFRP signal center level input terminal 27 RFZI I RFRP signal zero-cross input terminal 28 RFRP I RF ripple signal input terminal 29 FEI I Focus error signal input terminal 30 SBAD I Tracking error signal input terminal 31 TEI I Tracking error signal input terminal 32 TEZI I Tracking error signal zero-cross input terminal 33 FOO O Focus equalizer output terminal 34 TRO O Tracking equalizer output terminal 35 VREF - Analog reference power supply vpltage terminal 36 RFGC O RF amplitude adjustment control signal output terminal 37 TEBC O Tracking balance control signal output terminal 38 SEL O APC circuit ON/OFF signal output terminal 40 FMO Feed equalizer output terminal 41 DMO O Disc equalizer output terminal 42 Vss3 - Digital GND terminal 43 VDD3 - Digital GND terminal 44 TESIN I Test input terminal 45 XVss3 - Digital GND terminal 46 XI I System clock oscillator input terminal 47 XO O System clock oscillator input terminal 48 XVDD3 - System clock oscillator input terminal 49 DVss3 - DA converter GND terminal 50 RFG O R-channel data forward output terminal 51 DVDD3 - DA converter GND terminal 52 DVR - Reference voltage terminal 53 DVSS3 - DA converter GND terminal 54 DVss3 - DA converter GND terminal 55 DVSS3 - DA converter GND terminal 56 DVSS3 - DA converter GND terminal 57 BUSO I/O Microcontroller interface data I/O terminal 58 BUS1 I/O Microcontroller interface data I/O terminal 59 BUSS I/O Microcontroller interface data I/O terminal 60 BUS3 I/O Microcontroller interface data I/O terminal 61 BUCK I Microcontroller interface choic input terminal 62 I/CCE I Microcontroller interface choic penale signal input terminal 63 I/RST I Reset signal input terminal	21	VCOF	0	VCO filter terminal
24         RFI         I         RF signal input terminal           25         AVDD3         -         Analog 3.3V power supply voltage terminal           26         RFCT         I         RFRP signal zero-cross input terminal           27         RFZI         I         RFRP signal zero-cross input terminal           28         RFRP         I         F ripple signal input terminal           30         SBAD         I         Sub-beam adder signal input terminal           31         TEI         I         Tracking error signal input terminal           31         TEI         I         Tracking error signal zero-cross input terminal           32         TEZI         I         Tracking error signal zero-cross input terminal           34         TRO         O         Focus equalizer output terminal           35         VREF         -         Analog reference power supply voltage terminal           36         RFGC         O         Tracking balance control signal output terminal           37         TEBC         O         Tracking balance control signal output terminal           38         SEL         O         APC circuit ON/OFF signal output terminal           40         FMO         Analog 3.3V power supply voltage terminal	22	AVss3	-	Analog GND terminal
24         RFI         I         RF signal input terminal           25         AVDD3         -         Analog 3.3V power supply voltage terminal           26         RFCT         I         RFRP signal zero-cross input terminal           27         RFZI         I         RFRP signal zero-cross input terminal           28         RFRP         I         F ripple signal input terminal           30         SBAD         I         Sub-beam adder signal input terminal           31         TEI         I         Tracking error signal input terminal           31         TEI         I         Tracking error signal zero-cross input terminal           32         TEZI         I         Tracking error signal zero-cross input terminal           34         TRO         O         Focus equalizer output terminal           35         VREF         -         Analog reference power supply voltage terminal           36         RFGC         O         Tracking balance control signal output terminal           37         TEBC         O         Tracking balance control signal output terminal           38         SEL         O         APC circuit ON/OFF signal output terminal           40         FMO         Analog 3.3V power supply voltage terminal	23	SLCO	0	DAC output terminal for data slice level generation
25 AVDD3 - Analog 3.3V power supply voltage terminal 26 RFCT I RFRP signal center level input terminal 27 RFZI I RFRP signal zero-cross input terminal 28 RFRP I RFR pignal zero-cross input terminal 30 SBAD I Sub-beam adder signal input terminal 31 TEI I Tracking error signal input terminal 32 TEZI I Tracking error signal zero-cross input terminal 33 FOO O Focus equalizer output terminal 34 TRO O Tracking error signal zero-cross input terminal 35 VREF - Analog reference power supply vpltage terminal 36 RFGC O RF amplitude adjustment control signal output terminal 37 TEBC O Tracking balance control signal output terminal 38 SEL O APC circuit ON/OFF signal output terminal 39 AVDD3 - Analog 3.3V power supply voltage terminal 40 FMO O Feed equalizer output terminal 41 DMO O Disc equalizer output terminal 42 Vss3 - Digital GND terminal 44 TESIN I Test input terminal 45 XYss3 - System clock oscillator input terminal 46 XI I System clock oscillator input terminal 47 XO O System clock oscillator input terminal 48 XVDD3 - DA converter GND terminal 49 DVss3 - DA converter GND terminal 50 RO O R-channel data forward output terminal 51 DVDD3 - DA converter GND terminal 52 DVR - Reference voltage terminal 53 LO O L-channel data forward output terminal 54 DVss3 - DA converter GND terminal 55 ZDET O I bit DA converter zero data detection flag output terminal 56 Wss5 - Microcontroller interface data I/O terminal 57 BUSO I/O Microcontroller interface data I/O terminal 58 BUS1 I/O Microcontroller interface data I/O terminal 69 BUS3 I/O Microcontroller interface data I/O terminal 60 BUS3 I/O Microcontroller interface choic penale signal input terminal 61 BUCK I Microcontroller interface choic penale signal input terminal 63 I/RST I Reset signal input terminal	24	RFI	ı	
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# ■ BA3220FV-X (IC301,IC401) : Driver

1. Pin layout & Block diagram

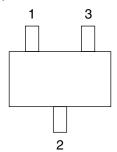


### 2. Pin function

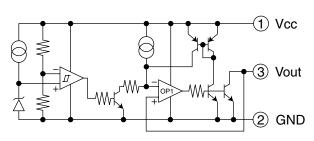
Pin No.	Symbol	Function
1	CL+	Powe supply terminal for amp.
2	Vcc	power supply terminal.
3	INL	input terminal.
4	NFL	Negative feedback terminal.
5	FIL	Filter terminal.
6	NFR	Negative feedback terminal.
7	INR	Input terminal
8	CR+	Power supply terminal for amp.
9	CR-	Output terminal of internal amp.
10	RGND	Rch GND terminal.
11	OUTR	Rch output terminal.
12	OUTL	Lch output terminal.
13	LGND	Lch GND terminal.
14	CL-	Output terminal of internal amp.

# ■ 000874360-T (IC702) : System reset



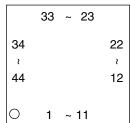


### 2. Block diagram

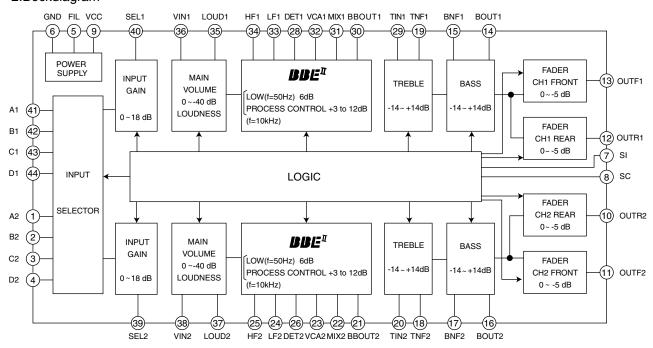


## ■ BD3860K (IC911): E. volume

### 1.Terminal layout



### 2.Bockdiagram

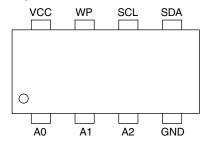


### 3.Pin function

•		••			
Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	A2	CH2 Input Pin A	23	VCA2	CH2 High Pass VCA Output Pin
2	B2	CH2 Input Pin B	24	LF2	CH2 Low Pass Filter Setting Pin
3	C2	CH2 Input Pin C	25	HF2	CH2 High Pass Filter Setting Pin
4	D2	CH2 Input Pin D	26	DET2	CH2 High Pass Attack/Release Time Setting Pin
5	FIL	1/2 VCC Pin	27	NC	Non connect
6	GND	Ground Pin	28	DET1	CH1 High Pass Attack/Release Time Setting Pin
7	SI	Serial Data Receiving Pin	29	TIN1	CH1 treble Input Pin
8	SC	Serial Clock Receiving Pin	30	BBOUT1	CH1 BBE II Signal Output Pin
9	VCC	Power Supply Pin	31	MIX1	CH1 Output MIX Amplifier Inverse Input Pin
10	OUTR2	CH2 Rear Output Pin	32	VCA1	CH1 High Pass VCA Output Pin
11	OUTF2	CH2 Front Output Pin	33	LF1	CH1 Low Pass Filter Setting Pin
12	OUTR1	CH1 Rear Output Pin	34	HF1	CH1 High Pass Filter Setting Pin
13	OUTF1	CH1 Front Output Pin	35	LOUD1	CH1 Loudness Filter Setting Pin
14	BOUT1	CH1 Bass Filter Setting Pin	36	VIN1	CH1 Main Volume Input Pin
15	BNF1	CH1 Bass Filter Setting Pin	37	LOUD2	VCH2 Loudness Filter setting Pin
16	BOUT2	CH2 Bass Filter Setting Pin	38	VIN2	CH2 Main Volume Input Pin
17	BNF2	CH2 Bass Filter Setting Pin	39	SEL2	CH2 Input Gain Output Pin
18	TNF2	CH2 treble Filter Setting Pin	40	SEL1	CH1 Input Gain output Pin
19	TNF1	CH1 treble Filter Setting Pin	41	A1	CH1 Input Pin A
20	TIN2	CH2 treble Input Pin	42	B1	CH1 Input Pin B
21	BBOUT2	CH2 BBE II Signal Output Pin	43	C1	CH1 Input Pin C
22	MIX2	CH2 Output MIX Amplifier	44	D1	CH1 Input Pin D
		Inverse Input Pin			

# **■** BR24C16F-X (IC703) : EEPROM

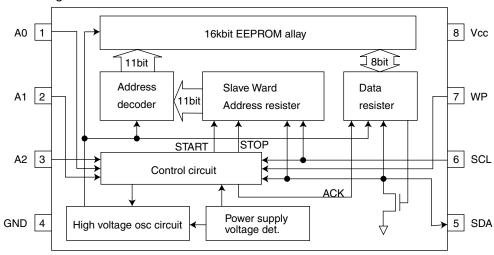
### 1. Pin layout



### 2. Pin function

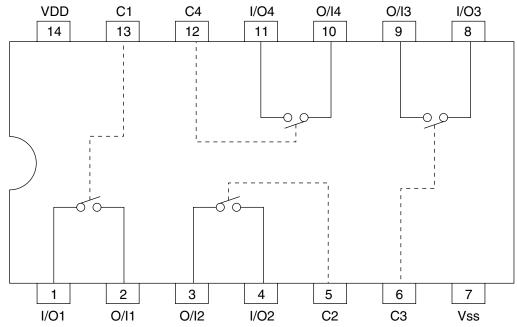
Symbol	I/O	Function
VCC -		Power supply.
GND	•	GND
A0,A1,A2 I		No use connect to GND.
SCL I		Serial clock input.
SDA	I/O	Serial data I/O of slave and ward address.
WP I Write p		Write protect terminal.

### 3. Block diagram

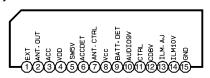


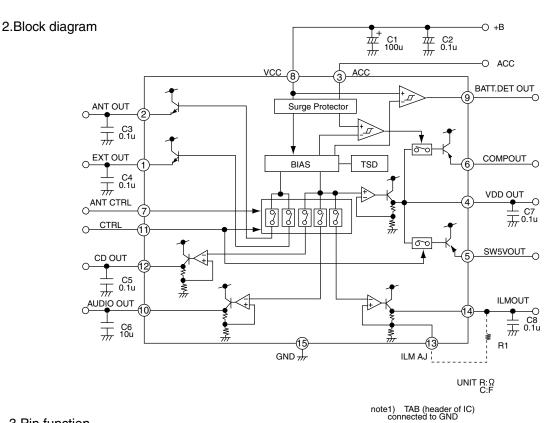
# ■BU4066BCFV-X (IC322) : Quad analog switch

### 1. Pin layout & Block diagram



# ■ HA13164 (IC961) : Regulator 1.Terminal layout

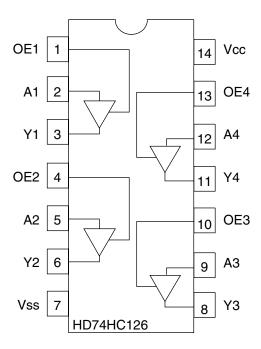




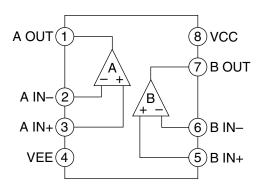
3.Pin function

Pin No.	Symbol	Function		
1	EXTOUT	Output voltage is VCC-1 V when M or H level applied to CTRL pin.		
2	ANTOUT	Output voltage is VCC-1 V when M or H level to CTRL pin and H level		
		to ANT-CTRL.		
3	ACCIN	Connected to ACC.		
4	VDDOUT	Regular 5.7V.		
5	SW5VOUT	Output voltage is 5V when M or H level applies to CTRL pin.		
6	COMPOUT	Output for ACC detector.		
7	ANT CTRL	L:ANT output OFF , H:ANT output ON		
8	VCC	Connected to VCC.		
9	BATT DET	Low battery detect.		
10	AUDIO OUT	Output voltage is 9V when M or H level applied to CTRL pin.		
11	CTRL	L:BIAS OFF, M:BIAS ON, H:CD ON		
12	CD OUT	Output voltage is 8V when H level applied to CTRL pin.		
13	ILM AJ	Adjustment pin for ILM output voltage.		
14	ILM OUT	Output voltage is 10V when M or H level applies to CTRL pin.		
15	GND	Connected to GND.		

# ■ HD74HC126FP (IC771) : Changer control

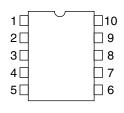


# ■ NJM2100M (IC821) : Operation amp

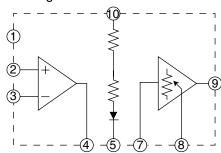


# ■ M5282FP-XE (IC321) : E. volume



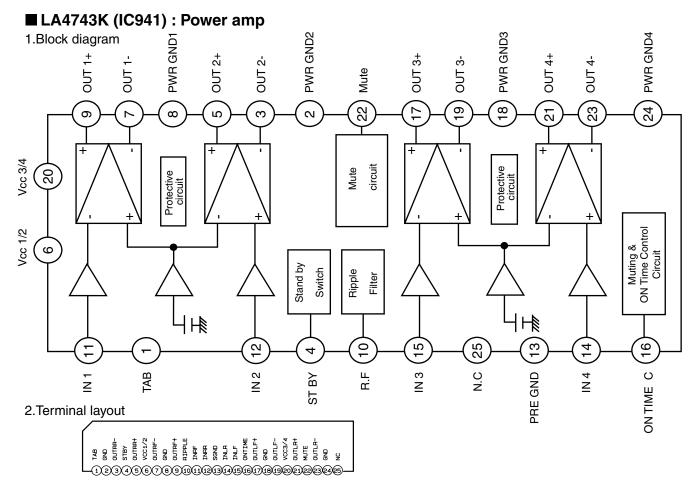


2. Block diagram



### 3. Pin function

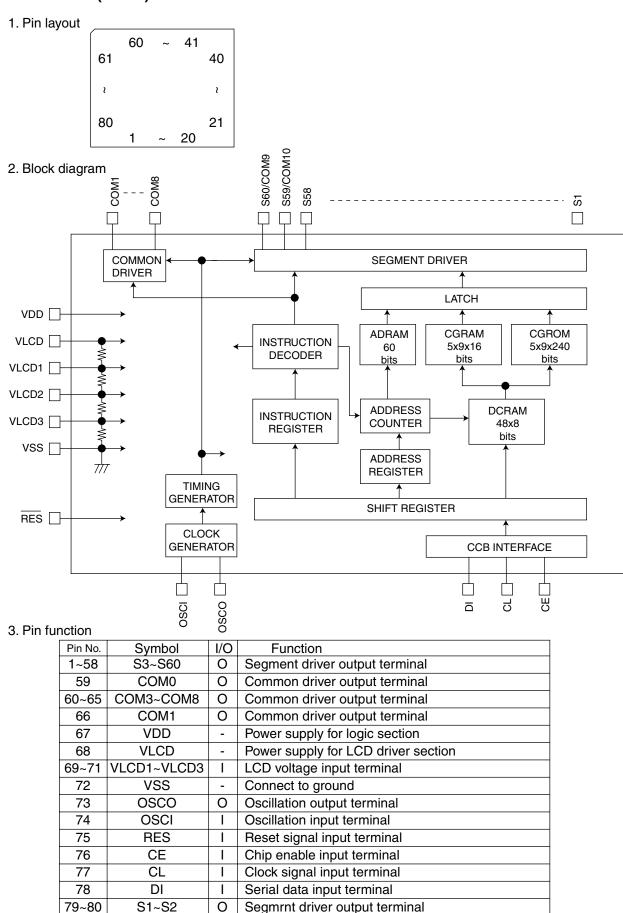
Pin No.	Symbol	Function		
1	Vcc/2	Vcc/2 output for microphone amp.		
2	Amp+IN	Microphone amp. positive input terminal.		
3	Amp-IN	Microphone amp. negative input terminal.		
4	Amp OUT	Microphone amp. output terminal.		
5	GND	Ground.		
6	NC	Non connection.		
7	VCA IN	VCA input terminal.		
8	Vc	VCA control terminal.		
9	VCA OUT	VCA output terminal.		
10	Vcc	Power supply.		



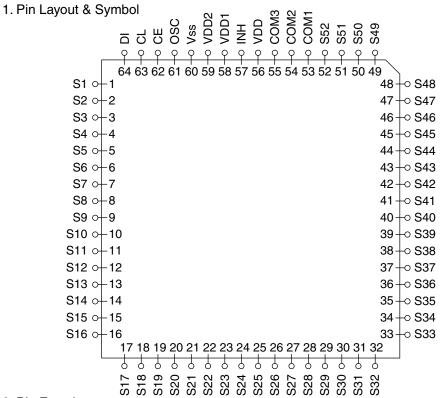
### 3.Pin function

1 function					
Pin No.	Symbol	Function			
1	TAB	Header of IC			
2	GND	Power GND			
3	OUTRR-	Outpur(-) for front Rch			
4	STBY	Stand by input			
5	OUTRR+	Output (+) for front Rch			
6	VCC1/2	Power input			
7	OUTRF-	Output (-) for rear Rch			
8	GND	Power GND			
9	OUTRF+	Output (+) for rear Rch			
10	RIPPLE	Ripple filter			
11	INRF	Rear Rch input			
12	INRR	Front Rch input			
13	SGND	Signal GND			
14	INLR	Front Lch input			
15	INLF	Rear Lch input			
16	ONTIME	Power on time control			
17	OUTLF+	Output (+) for rear Lch			
18	GND	Power GND			
19	OUTLF-	Output (-) for rear Lch			
20	VCC3/4	Power input			
21	OUTLR+	Output (+) for front			
22	MUTE	Muting control input			
23	OUTLR-	Output (-) for front			
24	GND	Power GND			
25	NC	Non connection			

## ■ LC75811W (IC602) : LCD driver



## ■ LC75823W (IC602) : LCD driver

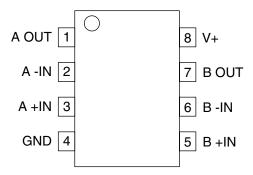


### 2. Pin Function

Pin No.	Symbol	I/O	Function					
1 to 52	S1 to S52	0	Segment output pins used to display data transferred					
			by serial data input.					
53 to 55	COM1 to COM3	0	Common driver output pins. The frame frequency is given					
			by: t0=(fosc/384)Hz.					
56	VDD		Power supply connection. Provide a voltage of between					
			4.5 and 6.0V.					
57	ĪNH	I	Display turning off input pin.					
			<u>INT</u> ="L" (Vss) off (S1 to S52, COM1 to COM3="L"					
			INT="H" (VDD) on					
		_	Serial data can be transferred in display off mode.					
58	VDD1	I	Used for applying the LCD drive 2/3 bias voltage					
			externally.					
			Must be connected to VDD2 when a 1/2 bias drive scheme					
			is used.					
59	VDD2	ı	Used for applying the LCD drive 1/3 bias voltage					
			externally.					
		Must be connected to VDD1 when a 1/2 bias drive scheme						
- 00	V	is used.						
60	Vss		Power supply connection. Connect to GND.					
61	OSC	I/O						
			An oscillator circuit is formed by connecting an external					
60	CE	resistor and capacitor at this pin.  Serial data  CE : Chip enable						
62	CE		Serial data CE : Chip enable interface connection					
63	CL		to the controller. CL : Sync clock					
03	CL	'	to the controller. OL . Synic clock					
64	DI		DI : Transfer data					
	Di		Di . Italioloi data					

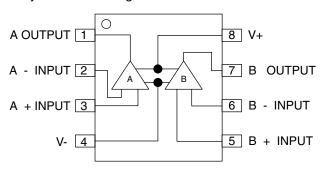
## ■ NJM2904M (IC951) : Dual ope amp

### 1. Pin layout



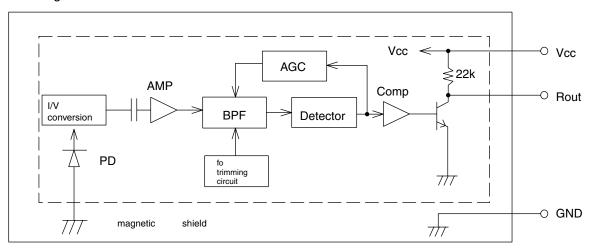
# ■ NJM4565MD (IC323,IC960) : Ope amp

1. Pin layout & Block diagram

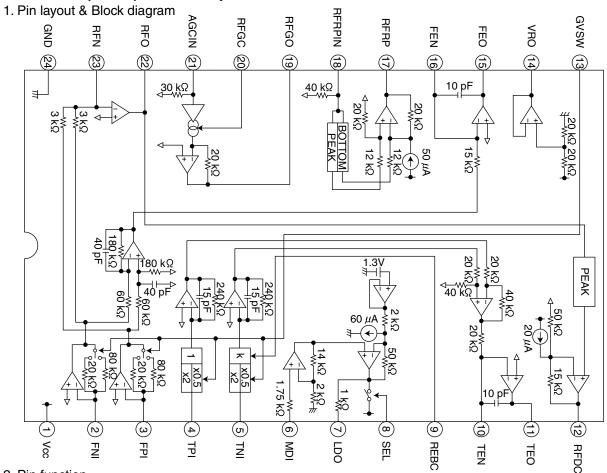


# ■ RPM6938-SV4 (IC603) : Remote censor

# 1.Block diagram



# ■ TA2147F-X (IC601) : Head amp

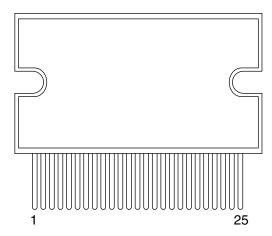


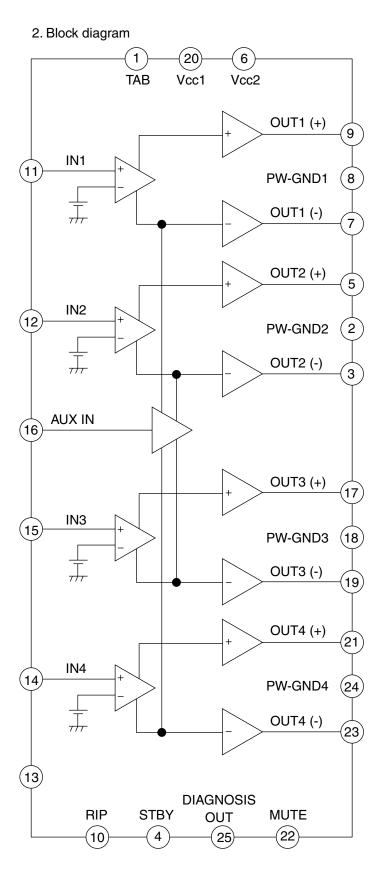
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	anction		
Pin No.	Symbol	I/O	Function
1	Vcc	-	3.3V power supply terminal
2	FIN	I	Main-beam amp input terminal
3	FPI	I	Main-beam amp input terminal
4	TPI	I	Sub-beam amp input terminal
5	TNI	ı	Sub-beam amp input terminal
6	MDI	I	Monitor photo diode amp input terminal
7	LDO	0	Laser diode amp output terminal
8	SEL	I	APC circuit ON/OFF control signmal, laser diode (LDO) control signal input or
			bottom/peak detection frequency change terminal
9	TEBC	I	Tracking error balance adjustment signal input terminal
10	TEN	l	Tracking error signal generation amp negative-phase input terminal
11	TEO	0	Tracking error signal generation amp output terminal
12	RFDC	0	RF signal peak detection output terminal
13	GVSW	I	AGC/FE/TE amp gain change terminal
14	VRO	0	Reference voltage (VRO) output terminal
15	FEO	0	Focus error signal generation amp output terminal
16	FEN	I	Focus error signal generation amp negative-phase input terminal
17	RFRP	0	Signal amp output pin for track count
18	RFRPIN	I	Signal generation amp input terminal for track count
19	RFGO	0	RF signal amplitude adjustment amp output terminal
20	RFGC	I	RF amplitude adjustment control signal input terminal
21	AGCIN	I	RF signal amplitude adjustment amp input terminal
22	RFO	0	RF signal generation amp output terminal
23	RFN	ı	RF signal generation amp input terminal
24	GND	-	GND terminal

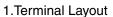
# ■TA8273H (IC941): 4ch amp

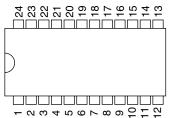
1. Pin layout



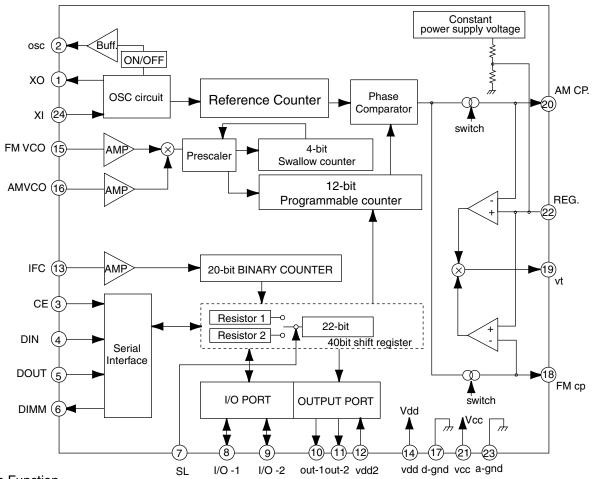


# ■TB2118F-X (IC21): PLL





### 2.Block diagram



### 3.Pin Function

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	XOUT	0	Crystal oscillator pin	13	IFC	I	IF signal input
2	OSC	-	Non connect	14	VDD	-	Power pins for digital block
3	CE	- 1	Chip enable input	15	FMIN	Ι	FM band local signal input
4	DI	ı	Serial data input	16	AMIN	ı	AM band local signal input
5	CK	Ι	Clock input	17	DGND		Connect to GND (for digital circuit)
6	DOUT	0	Serial data output	18	FMCP	0	Charge pump output for FM
7	SR	0	Register control pin	19	VT	-	Tuning voltage biased to 2.5V.
8	I/01	I/O	I/O ports	20	AMCP	0	Charge pump output for AM
9	1/02	I/O	I/O ports	21	VCC	-	Power pins for analog block
10	OUT1	-	Non connect	22	RF	ı	Ripple filter connecting pin
11	OUT2	-	Non connect	23	AGND		Connect to GND (for analog circuit)
12	VDD2	-	Single power supply for REF. frequency block	24	XIN	I	Crystal oscillator pin



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