CompactPCI®

ICP-PIII

High-Performance CPU Boards

USER'S MANUAL

Publication Number: **PD00581013.004 AB**
MAN-ICP-PIII

inova® Computers

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CompactPCI®

Preface

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Unpacking and Special Handling Instructions

This product has been designed for a long and fault-free life; nonetheless, its life expectancy can be severely reduced by improper treatment during unpacking and installation.

Observe standard antistatic precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces as these can cause short circuits, damage the batteries or disrupt the conductive tracks on the board.

Do not exceed the specified operational temperature ranges of the board version ordered. If batteries are present, their temperature restrictions must be taken into account.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, re-pack it as it was originally packed.

Before returning this product for repair, please ask for an RMA (Returned Material Authorization) number and supply the following information:

- Company name, contact person, shipping address and invoice address
- Product name and serial number
- Failure or fault description
- Clearly write the RMA number on the outside of the transportation carton.

Revision History

Revision History			
Manual	MAN-ICP-PIII		
Publication Number	PD00581013.XXX		
Issue	**Brief Description of Changes**	**Author**	**Date of Issue**
PD00581013.001	Preliminary, First Release; All pages revised	AB	31/11/2000
PD00581013.002	Updated to include Radeon VE and Rear I/O options	AB	15/08/2001
PD00581013.003	Final Version - Included Appendix A-D I/O Modules	AB	21/09/2001
PD00581013.004	Specs. Updated & Rear I/O Table Corrected	AB	15/02/2002

Three Year Limited Warranty

Inova Computers ('**Inova**') grant the original purchaser of Inova products the following hardware warranty. No other warranties that may be granted or implied by anyone on behalf of **Inova** are valid unless the consumer has the expressed written consent of **Inova**.

Inova warrants their own products (excluding software) to be free from defects in workmanship and materials for a period of 36 consecutive months from the date of purchase. This warranty is not transferable nor extendible to cover any other consumers or long term storage of the product.

This warranty does not cover products which have been modified, altered, or repaired by any other party than **Inova** or their authorized agents. Furthermore, any product which has been, or is suspected of being damaged as a result of negligence, misuse, incorrect handling, servicing or maintenance; or has been damaged as a result of excessive current/voltage or temperature; or has had its serial number(s), any other markings, or parts thereof altered, defaced, or removed will also be excluded from this warranty.

A customer who has not excluded his eligibility for this warranty may, in the event of any claim, return the product at the earliest possible convenience, together with a copy of the original proof of purchase, a full description of the application it is used on, and a description of the defect; to the original place of purchase.

Pack the product in such a way as to ensure safe transportation (we recommend the original packing materials), whereby **Inova** undertakes to repair or replace any part, assembly or sub-assembly at our discretion; or, to refund the original cost of purchase, if appropriate.

In the event of repair, refund, or replacement of any part, the ownership of the removed or replaced parts reverts to **Inova**, and the remaining part of the original guarantee, or any new guarantee to cover the repaired or replaced items, will be transferred to cover the new or repaired items. Any extensions to the original guarantee are considered gestures of goodwill, and will be defined in the "Repair Report" returned from **Inova** with the repaired or replaced item.

Other than the repair, replacement, or refund specified above, **Inova** will not accept any liability for any further claims which result directly or indirectly from any warranty claim. We specifically exclude any claim for damage to any system or process in which the product was employed, or any loss incurred as a result of the product not functioning at any given time. The extent of **Inova's** liability to the customer shall not be greater than the original purchase price of the item for which any claim exists.

Inova makes no warranty or representation, either expressed or implied, with respect to its products, reliability, fitness, quality, marketability or ability to fulfil any particular application or purpose. As a result, the products are sold "as is," and the responsibility to ensure their suitability for any given task remains the purchaser's. In no event will **Inova** be liable for direct, indirect, or consequential damages resulting from the use of our hardware or software products, or documentation; even if we were advised of the possibility of such claims prior to the purchase of, or during any period since the purchase of the product. Please remember that no **Inova** employee, dealer, or agent are authorized to make any modification or addition to the above terms, either verbally or in any other form written or electronically transmitted, without consent.

CompactPCI®

Product Overview

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Overview Contents

1.0 ICP-PIII CPU

The ICP-PIII is a high-performance 3U CompactPCI single-board Socket 370 based universal CPU that satisfies the needs of a wide range of industrial automation, military, medical, aerospace, imaging, telecommunications, process control and embedded/OEM applications. The powerhouse in any application, Inova's Socket 370 based high-performance 3U CompactPCI CPU is packed with a feature set unheard of on such a small scale. With 128MByte on-board SDRAM with BIOS controlled ECC, the ICP-PIII suits the demands placed by modern operating systems. In addition, performance scalability is assured through the broad selection of Intel Pentium III and Celeron BGA2 (mobile) and FC-PGA devices.

Conforming to the latest PICMG CompactPCI specification the ICP-PIII has a colourful feature set of rear I/O options and supports basic hot-swap. Being of a universal design, both 5.0 and 3.3V I/O signalling voltages are possible without modification.

Although the CPU measures just 160mm by 100mm it is fabricated using the latest 12-layer PCB technology and with over 4800 PCB links and 6550 solder points the ICP-PIII is truly a miracle of engineering achievement.

Inova's high-performance, high-density 3U PIII board provides support on all three major serial networking levels that include Fast Ethernet, FireWire and USB. To enable so much functionality to exist in such a small footprint, the ICP-PIII is able to host the I/O on either the front-panel or in the form of rear I/O or even both. Implementing the latest Intel chipsets and processors available for the embedded market the ICP-PIII is adequately equipped to provide support for all major operating systems and off-the-shelf application software.

The built-in graphic solution not only saves space within a rack that would otherwise be taken-up by an additional graphics board, but due to its extremely efficient use of hardware real-estate, costs can be cut too. Modularity is further assured through the use of dedicated plug-in SDRAM modules.

On-board peripheral connectors allow the CPU to be enhanced to include mouse, keyboard, COM and LPT functions. Slim-line 1.44MByte floppy disk and EIDE interfaces provide the mass-storage possibilities and due to the rear I/O possibilities, one of the EIDE channels (2 devices) can be used for remote connection of hard disks or CD-ROM drive etc.

1.01 Interfacing

For maximum communication flexibility, multiple interfaces satisfying different industrial standards are implemented. LAN applications can take advantage of Inova's 10BaseT/100BaseTx (dual) Ethernet implementation or, if high-speed system-level serial interfacing is required, the built-in 400/100 Mbit/s FireWire port is available. Peripherals may be connected to the standard USB or, as an option, the on-board PCI bus allows support of custom I/O piggybacks conforming to Inova's open specification.

The Intel 21554 non-transparent PCI/PCI bridge is utilised for multiprocessing applications equipped with a Master and Slave CPU in the same system.

1.02 Peripherals

The ICP-PIII supports standard PC peripherals like floppy disk, hard disk and CD ROM. Notebook style hard disks may be connected directly to the base-board (2-slot) and possess their own front-panel offering COM ports and PS-2 style connectors for mouse and keyboard.

1.03 Software

The following operating systems have been verified with Inova's PIII, 3U CompactPCI CPU:

- Linux
- Windows® NT® & VenturCom RTX® (Real-Time Extension)
- Windows® 2000
- Windows ® CE
- Windows ® 9x
- Windriver VxWorks®
- QNX®
- Esmeralda Technology Jbed® (under development)
- Solaris x86

All readily available application software designed for operation on the standard x86 architecture will execute without modification.

1.04 Graphics

The Lynx3DM graphic controller is a highly integrated 128-bit GUI (Graphical User Interface) engine supporting dual independent graphic displays. Screen resolutions up to 1600 x 1200 pixels with 24-bit (True Colour) are supported.

The introduction of the ATI Radeon VE, with its 16MByte video RAM and superior 3D acceleration & hardware MPEG-2 support, enables screen resolutions up to 2048 x 1536 pixels to be driven.

Dual video and TFT dual-scan/single-scan colour panels are supported with configurable colour depths. In addition, Inova's ICP-PIII caters for the needs of the GigaST★R, PanelLink™ and LVDS user.

1.1 Specifications

Processor	Socket 370 BGA (mobile) or FC-PGA based Intel Pentium III or Celeron
Pentium III	Up to 1000MHz (100MHz PSB, 256kByte L2 cache)
Mobile PIII	Up to 700MHz BGA2 package with interposer (100MHz PSB, 256kByte L2 cache)
Mobile Celeron	BGA2 package with interposer (100Mz PSB, 128kByte L2 cache)
L2 Cache	128/256kByte L2 cache depending on processor
Memory	128MByte soldered synchronous DRAM with optional BIOS activated ECC feature. Additional Piggyback provides additional 128MByte, or 384MByte
FLASH-Disk	Available as an option (Disk-on-Chip™) providing up to 500MByte FLASH
Battery	Lithium cell for RTC (NV-RAM) with a lifetime > 8 years
North Bridge	440BX North Bridge 82443BX supporting: ▸ 100MHz system bus DRAM controller with 64bit, 100MHz SDRAM interface ▸ ECC support ▸ AGP 2X interface (66/133MHz) ▸ Power management
South Bridge	M1543C: ▸ PCI/ISA Bridge ▸ Super I/O: 1 Floppy Disk Controller, 1 Parallel Port, 2 Serial Ports ▸ Fast IR ▸ IDE Controller (4 devices) ▸ Ultra 66 DMA support ▸ 12Mbit/s USB controller ▸ Interrupt controller ▸ Power Management Unit ▸ Full support for ACPI and OS directed power management ▸ Mouse & keyboard controller
Graphics	Lynx3DM or Radeon VE graphic accelerator ▸ 8/16Mbyte SGRAM/SDRAM ▸ 3D graphics, DVD & MPEG-2 support ▸ Multi-Display ▸ Dual View support under Microsoft Windows® 9x, Windows® NT® & Windows® 2000 ▸ CRT / TFT resolutions up to 2048x1536 ▸ GigaST★R / PanelLink™ or TFT Piggyback Dual display option or TFT will require dedicated front-panel.
Recovery BIOS	FLASH Recovery BIOS
Watchdog	Programmable up to 10 minutes; issues NMI or Reset

PCI/PCI	Intel 21150 transparent bridge (Master) or Intel 21554 non-transparent PCI/PCI bridge for multiprocessing (Slave) operation with Basic Hot-Swap support (PICMG 2.1 R1.0), Serialized interrupts and universal (3.3/5.0V) V I/O support
On-Board I/O	▸ 10/100 MBit/s Ethernet (Intel 82559) ▸ optional 2nd independent Fast Ethernet ▸ Up to 2x 12Mbit/s USB ▸ Up to 2x 400Mbit/s FireWire interfaces
Rear I/O	Standard to all CPU variants is option 'C' which provides 2nd FireWire channel, 2nd USB channel, LPT1 (Floppy), EIDE and loudspeaker. Other I/O configurations including customized are possible.
Mass Storage	1.44MByte 3.5" floppy drive and EIDE (flex cable/rear I/O) supporting 2 pairs (Master/Slave) hard-disks or CD ROMs
Front-Panels	Optional 4TE front-panel extension provides: COM1, COM2, keyboard, PS-2 mouse Extended front-panel (4TE) provides: COM2, LPT1
Connectors	USB (USB), RJ45 (Ethernet), 6-pin FireWire (FireWire), 15-pin D-Sub (PanelLink), 15-pin high-density D-Sub (VGA), 9-pin D-Sub (GigaST★R)
CompactPCI	PICMG 2.0 R3.0, 32-bit, 33MHz system slot interface with 7 Master (DMA) support. Dual-slot operation
Mechanics	3U (100 x 160 x 21mm) 4 TE 3U (100 x 160 x 42mm) 8 TE 3U (100 x 160 x 63mm) 12 TE
Power Cons.	25W typ. PIII @ 850MHz (Lynx) 21W typ. PIII @ 700MHz (Lynx) 12W typ. Mobile PIII @ 500MHz (Lynx)
Software Support	Windows® NT®, Windows® 2000, Windows® 9x, Linux, VxWorks®, QNX®
Mass	220g (4TE)
Oper. Temp. **Storage Temp.** **Extended Temp.** **Humidity**	0°C to +60°C (Ambient)* -40°C to +85°C (400MHz Mobile [Lynx] only) -40 to +85°C (Seleted CPUs only) 5% to 95% (non-condensing)
Warranty	Three-year limited warranty
Conformance	PICMG 2.0 R3.0 CE

*Note: Any CPU fitted with HD, FD or CD-ROM etc. has a max. operational temperature of 50 °C
CPUs without HD or PC inter faces ar e single-slot (4TE) for 'pr ocessor speeds ≤ 700MHz.
Mobile processors are passively cooled - installation **MUST** have >0.3m/s air flow!

1.2 Configuration

Inova's high-performance, high-density 3U PIII board supports functionality and connectivity on all three major serial networking levels like Fast Ethernet, FireWire and USB as well as most state-of-the-art fieldbus standards such as PROFIBUS, CAN, Interbus, and LON.

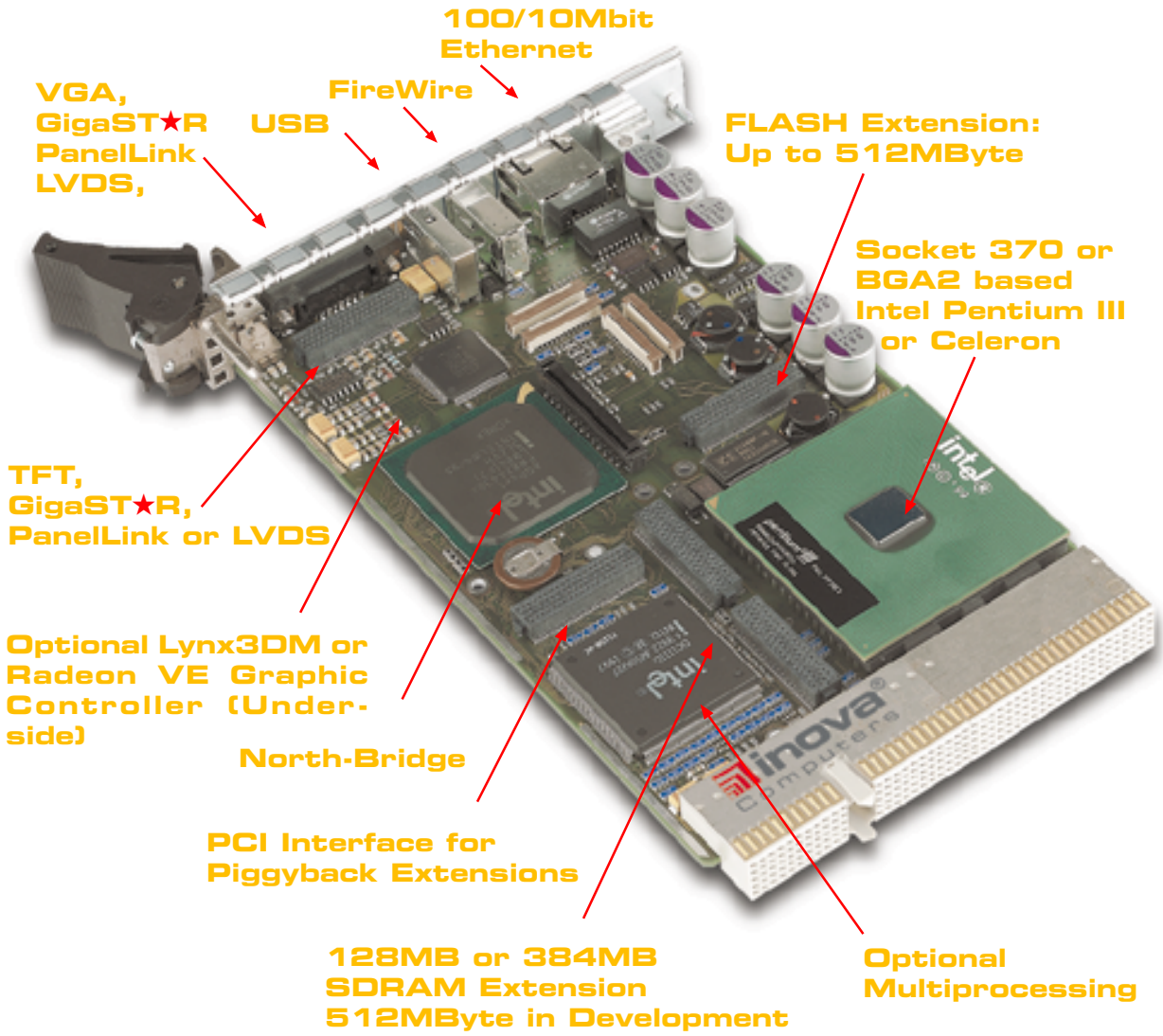
Three CPU groups exist to cater for the needs of all aspects of CompactPCI integration: The high-end typically supports 128MBytes on-board soldered SDRAM, Lynx3DM graphic controller with 8MByte SGRAM and all I/O. For standard applications, the same base layout is utilized however, the soldered SDRAM, graphic controller and many of the peripheral connections are absent for use in typical embedded applications. Finally, for multiprocessing applications, the PCI/PCI transparent bridge is replaced by the 21554 non-transparent version.

Table 1.20 'Processor Overview

CPU Family	Processor	CPU Speed(s)	Multi-Processing	Package
ICP-PIII-fegsm	Intel PIII	400 to 850MHz	No	FC-PGA
ICP-SPIII-fegsm	Intel PIII	400 to 850MHz	Yes	FC-PGA
ICP-xxPIII-fegsm	Mobile PIII/Celeron	400 to 700MHz	Yes / No	BGA2 (Interposer)

All CPU family members can possess up to 512MByte SDRAM with BIOS controlled ECC through a combination of soldered memory units and plug-in modules. FLASH up to 512MByte may be realised in a similar manner. All CPUs are equipped with a shielded front-panel with typically VGA, USB, FireWire and Fast Ethernet interfaces installed. Other front-panels are available with mouse, keyboard, COM, LPT, TFT, PanelLink or dual Ethernet interfaces. The choice of Lynx 3DM or ATI Radeon VE graphic controller complete with 8/16MByte video RAM is available as an option as is multiprocessing.

Figure 1.20 ICP-PIII Overview



Inova's CPUs have been prepared for rear I/O operation. Currently (RIO-C), EIDE, FireWire2, USB2, LPT1 and the loudspeaker signals are present on the backplane (if requested at time of order.) Other options may also be available (including customer specific) but are not referred to in this user's handbook. In order to take full advantage of the rear I/O features, the CompactPCI backplane needs to support them. Inova provides two standard versions; one has the J2 connector at the CPU location extended to the rear of the backplane while the other version has all slots fitted with the J2 connector on both the front and rear.

1.3 Software

1.31 Linux

Being a modern operating system, Linux executes a 32-bit architecture, uses pre-emptive multitasking, has protected memory, supports multiple users, and has rich support for networking, including TCP/IP. Linux was originally written for Intel's 386 architecture, but now runs on a wide variety of hardware platforms including the full x86 family of processors as well as Alpha, SPARC, and PowerPC.

Linux's architecture also creates a more reliable and inherently stable system through the use of protected memory and pre-emptive multitasking. Protected memory prevents an error in one application from bringing down the entire system, and genuine multitasking means that a bottleneck in one application does not hold up the entire system. Linux also maintains a very clean separation between user processes and kernel processes. While other server class operating systems use protected memory this feature is prone to failure if faulty applications are allowed to invade kernel space with their processes.

1.32 VentureCom

Hard, real-time scalability and embedded operation extensions are required for Windows NT by HAL modification for deterministic interrupt handling at multiple priority levels. This approach achieves response times in the µs range and reduces hardware resource requirements while maintaining full compatibility with the enormous range of standard software and device drivers written for the Windows NT operating system.

1.33 Windows 2000

Windows 2000 is highly reliable and available 32-bit OS.

Support for USB devices allows connection of peripherals without the need to reboot the system and unlike Windows NT 4.0 support is also provided for the IEE1394a (FireWire) devices. Finally, secure, wireless communication between two Windows 2000-based computers is possible using the popular IrDA infrared protocol.

Removable storage devices such as DVD and Device Bay are supported as are new display devices such as Accelerated Graphics Port (AGP), multiple video cards and monitors, OpenGL 1.2, DirectX® 7.0 API, and Video Port Extensions.

With Plug and Play automatic installation of new hardware is possible with only minimal configuration. More than 12,000 devices now support this functionality.

1.34 Windows CE

Microsoft® Windows CE is an operating system designed for a wide variety of embedded systems and products, from hand-held PCs and consumer electronic devices to specialized industrial controllers and embedded communications devices. The Windows CE operating system has proved itself capable of handling the most demanding 32-bit embedded applications by bringing the full power of the Microsoft's 32-bit programming and operating systems technology to the embedded systems designer. Windows CE is actually a collection of operating system modules and components that can be selected and configured to meet the needs of a specific embedded application or product.

1.35 VxWorks

WindRiver's run-time system solution is a high-performance RTOS with a scalable microkernel and sophisticated networking facilities - like TCP/IP networking across various media.

The open architecture provides efficient support of PC-based architectures. Flexible, intertask communication, µs interrupt handling, POSIX 1003.1b real-time extensions, fast and flexible I/O system etc. are some of the many key features.

1.36 OS-9 x86

Microware's real-time operating system has a track record that has been proved in the industrial/embedded market and has continued to provide reliable intelligence to sophisticated applications. OS-9 x86's flexibility, modularity and reliability in conjunction with a rich driver structure allow its use in I/O intensive applications.

1.37 QNX

This solution ports the Win32 API to a QNX kernel. The Win32 API aims to define a standard for developing open systems applications that are optimized to run on 'Wintel' platforms. This operating system evolves around a small microkernel RTOS that produces a protected-mode, POSIX-certified API. Being fully modular and scalable, this technology creates the smallest footprint that is beneficial to high-end server applications.

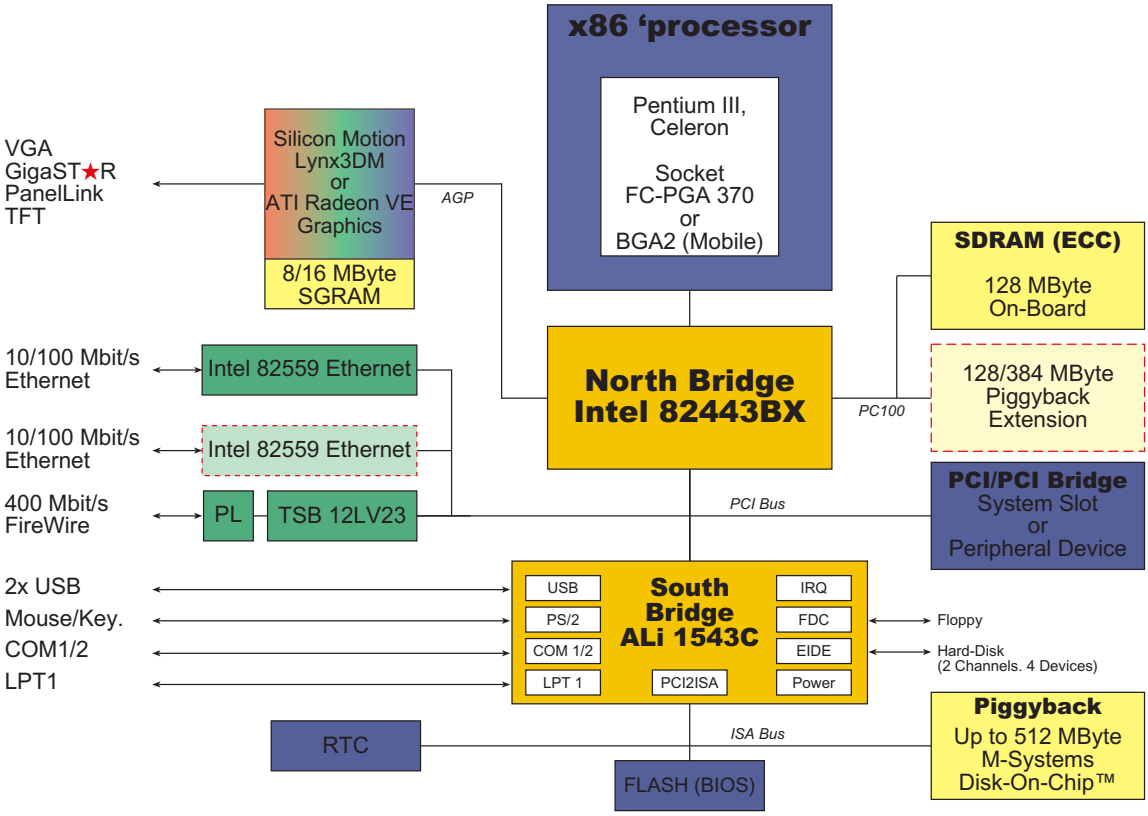
1.38 Jbed

Esmertec's Jbed is a new generation of real-time operating system. Java-based innovation provides unprecedented safety and ease of use without compromising resource efficiency (native processor speed) or hard real-time performance. In addition, advanced features are implemented such as modularity, hot updates, deadline-driven scheduling admission testing as well as a fast and productive cross-development.

1.4 Hardware

1.41 Block Diagram

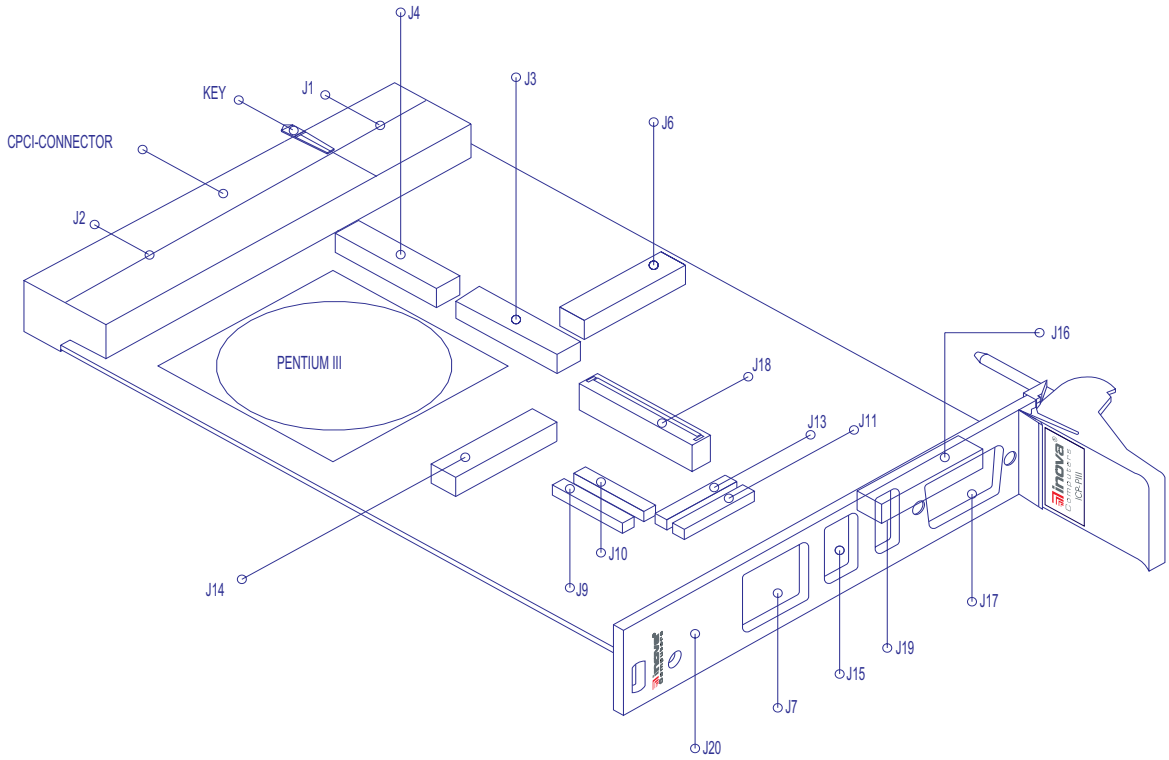
Figure 1.41 Block Diagram



This block diagram is applicable to all Inova's PIII-based CPUs. Components and/or functionality may change without notice. An extra PCI load can be attached to the on-board 80-pin header. An open specification is available allowing developers to manufacture their own PCI device.

1.42 Connector Location

Figure 1.42 Connector Locations



1.43 Connector Description

Table 1.43 Connector Description

Connector	Description
J1, J2	CompactPCI Interface Connector
J3, J4	SDRAM Piggyback Expansion Interface Connector for up 384MBytes
J6	PCI Expansion Slot
J7	10BaseT/100BaseTx Fast Ethernet Interface
J12	Optional Independent 10BaseT/100BaseTx Fast Ethernet Interface

Table 1.43 Continued

Connector	Description
J9, J10	Hard Disk Interface
J11	COM1, Keyboard and Mouse Interfaces
J13	COM2 and LPT1 Interfaces
J14[1)]	FLASH Extension Piggyback Connector for up to 288MBytes
J15	FireWire Interface
J16	TFT Flat-Panel, PanelLink™ or GigaSTAR Interface
J17	15-Pin High Density D-Sub VGA Graphics Interface
J18	1.4 MByte Slim-Line Floppy Drive Interface
J19	USB Interface
J20	iRDA, Reset

[1)] DOC FLASH greater than 288MByte may be available

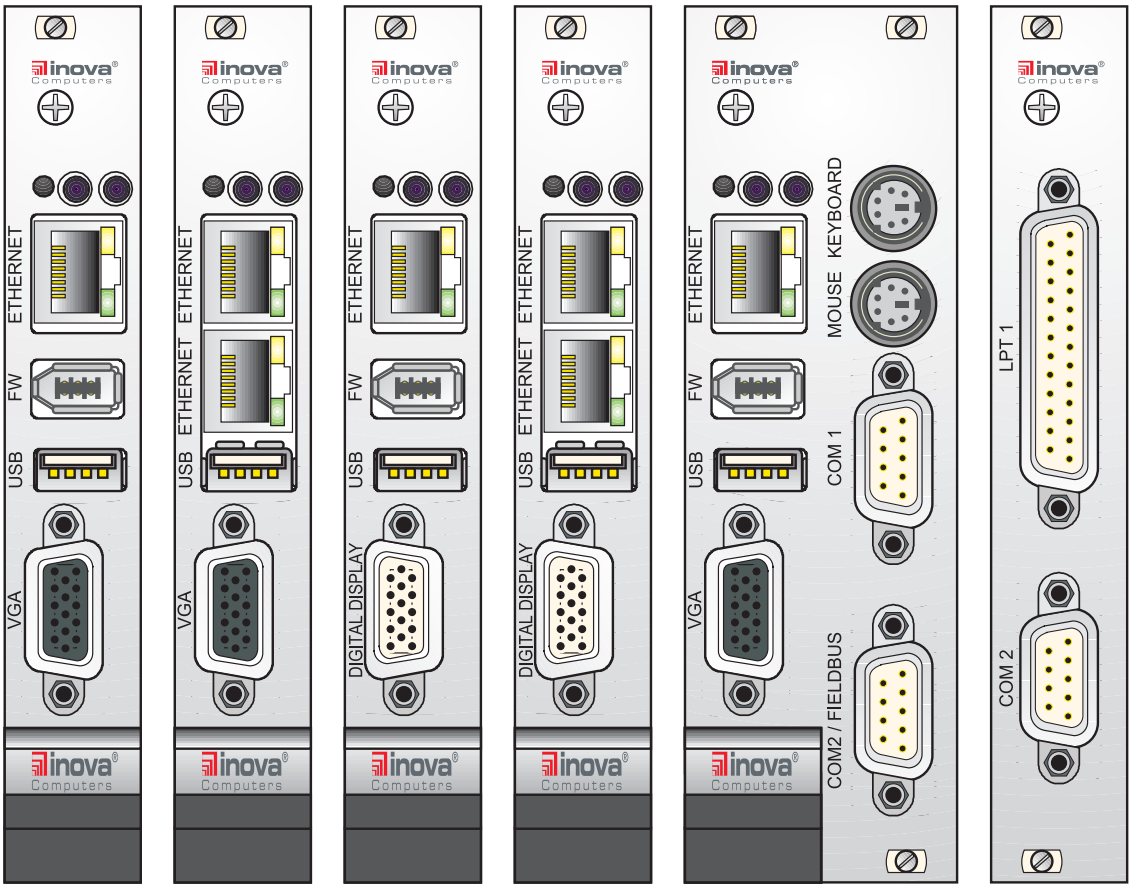
1.44 Front-Panel Features

Table 1.44 Front Panels

Interface	Description & Location
Ethernet	RJ45 Connector Common to all 4TE CPU Front-Panels
FireWire	Firewire Connector on 4TE CPU Front-Panel
USB	USB Connector on 4TE CPU Front-Panel
VGA	15-Pin High-Density D-Sub Connector on 4TE CPU Front-Panel
Keyboard	PS-2 Style on 8TE CPU Front-Panel
Mouse	PS-2 Style on 8TE CPU Front-Panel
COM1	9-Pin D-Sub on 8TE CPU Front-Panel
COM2[1)]	9-Pin D-Sub on 8TE CPU Front-Panel or 4/12TE CPU Extension
LPT1	25-Pin D-Sub on 4/12TE CPU Extension
PanelLink[2)]	15-Pin D-Sub on 4TE CPU Front-Panel or 8TE CPU Front-Panel
GigaSTAR[2)]	9-Pin D-Sub on 4TE CPU Front-Panel or 8TE CPU Front-Panel

[1)] The physical COM2 interface is missing on Inova's IPB-FPE8 piggyback allowing a PCI piggyback device to be installed.
[2)] If this piggyback is installed the hard-disk (IDE FLASH) must be installed as stand-alone

Figure 1.44 Front-Panel Options



The front-panels shown in Figure 1.44 show the tremendous flexibility built into Inova's CPU concept. From left, the standard CPU is 4TE with Ethernet, FireWire, USB and VGA graphic connections. If, instead of VGA graphics, PanelLink is required then the piggyback is installed on J14 for this purpose. TFT graphics are realised in a similar way except an extra 4TE front-panel is required (not shown) to carry the flat-band ribbon cables.

If the application requires the mouse, keyboard and COM ports or if the CPU is equipped with a hard disk or FLASH that is greater than 144MByte[1)] then an 8TE front-panel is selected. Both COM ports are installed on Inova's HD or IDE FLASH carrier board. A piggyback with COM1, mouse and keyboard is also available allowing the lower 9-pin D-Sub connector position to be used for a PCI-based piggyback.

LPT and COM2 interfaces are available on a dedicated panel shown to the right of Figure 1.44.

If a high-profile DOC FLASH is installed and a hard disk is required, the HD is mounted separately

1.45 Interface Positions

Figure 1.45 Interfaces

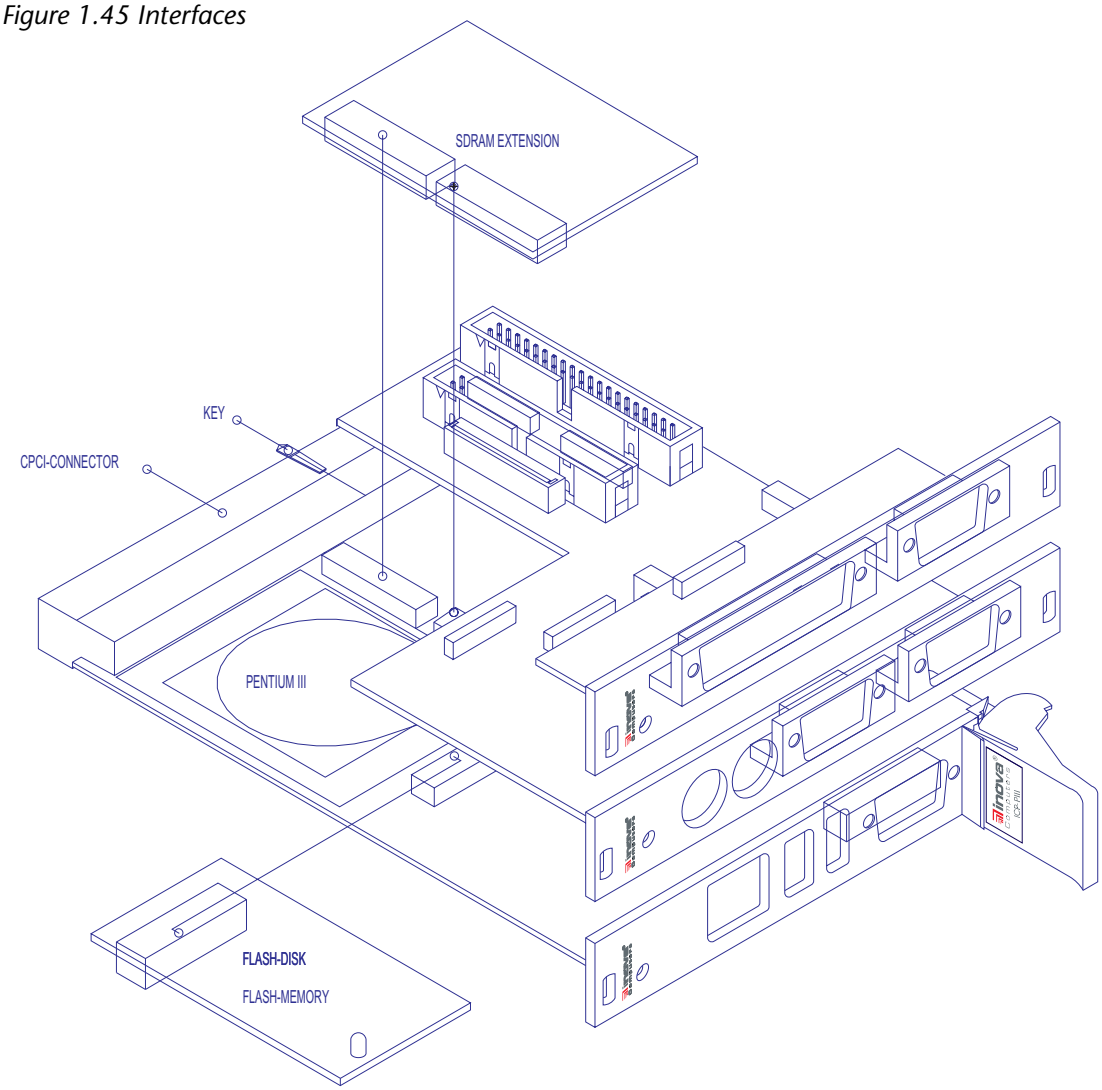


Figure 1.45 shows the typical positioning of the front panel extension modules for mouse, keyboard, COM1, COM2, LPT1 and COM2/Fieldbus interfaces.

> ***Note***
>
> ***A hard disk, if installed, will generally be fitted to the piggyback containing the mouse, keyboard, COM1 and COM2 interfaces.***

CompactPCI®

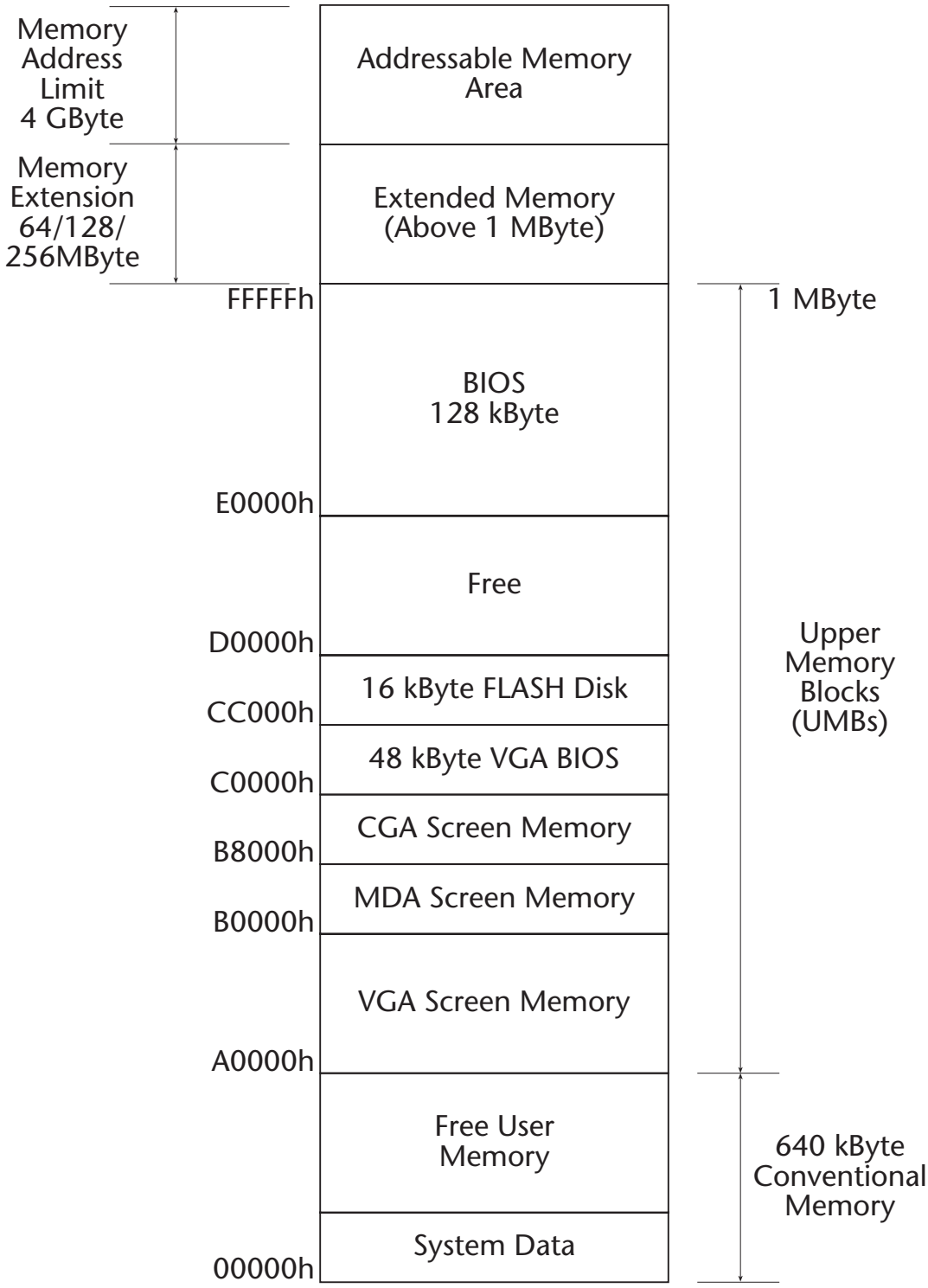
Configuration

2

Configuration Contents

2.0 Memory Map

Figure 2.00 System Architecture



The UMB reservation may be set up with the BIOS

Table 2.00 UMB Reservations for ISA

UMB Reservations for ISA	
Start Address	**Finish Address**
0CC00h	0CFFFh
0D000h	0D3FFh
0D400h	0D7FFh
0D800h	0DBFFh
0DC00h	0DFFFh

Table 2.01 Port Addressing

Port Addressing	
Port	**Address**
COM1	3F8h
COM2	2F8h
LPT1	378h

2.1 I/O Mapped Peripherals

The original PC-XT and PC-AT desktop computer (ISA bus) specification allows for 10-bit I/O addressed peripherals. This permits peripheral boards to be I/O mapped from 0h to 3FFh. CompactPCI systems permit the full 16-bit addressing capability of the Intel 80x86 'processors, from 0h to 0FFFFh.

All Inova CPU boards include peripheral devices requiring I/O address space on board and hence the BIOS automatically assigns the I/O address required by peripheral boards and PCI devices at boot time based on the requirements of each device. The assigned addresses can be determined by reading the configuration address space registers using special software tools.

Table 2.10 Legacy I/O Map (ISA Compatible)

I/O Address	Description
$000 - $00F	8237 DMA controller #1
$020 - $021	8259 Master Interrupt Controller
$040 - $043	8254 Programmable Interrupt Timer
$060 - $06F	8042 Keyboard Controller
$070 – $071	CMOS RAM, NMI Mask Reg., RTC
$080 - $08B	DMA page registers
$0A0 - $0BF	8259 Slave Interrupt Controller
$0C0 – $0DF	8237 DMA Controller #2
$0F0	Coprocessor Error Ignored Register
$170 - $177 *)	Secondary Hard Disk Controller
$1F0 - $1F8 *)	Primary Hard Disk Controller
$200 - $207	Reserved (Game Port)
$238 - $23B	Bus Mouse
$2E0 - $2E7	Reserved (GPIB)
$2E8 - $2EF	Reserved (Serial Port)
$2F8 - $2FF *)	Serial Port (COM2)
$CF8	PCI Configuration Address
$CFC	PCI Configuration Data

> *Note:*
>
> **) Denotes Plug 'n' Play devices that are configured during the BSP POST. Values shown are ISA compatible I/O addresses for reference only.*

2.2 Memory Mapped Peripherals

PC-AT desktop computers (ISA bus) allow 24-bit memory addressed peripherals. This decoding permits peripheral boards to be mapped in the Intel 80x86 memory map from 0h to 0FFFFFFh.

Inova's CompactPCI systems allow the full 32-bit addressing capability of the Intel Pentium/Celeron range of 'processors so that memory mapped peripheral devices may be mapped locally to the 'processor board at any location in the memory map not being used by other devices (e.g. system RAM.)

The BIOS automatically assigns memory addresses required by peripheral boards and PCI devices at boot time based on the requirements of each device. The assigned addresses can be determined by reading the configuration address space registers using PCI software tools.

> *Note:*
>
> *Devices not located on the CPU side of the PCI/PCI bridge are not normally accessible by DOS.*

2.3 Interrupt Routing

The IBM-compatible architecture includes one (PC-XT) or two (PC-AT) programmable interrupt controllers (Intel 8259A-compatible 'PICs') configured to set the priority of interrupt requests to the CPU.

In the PC-AT architecture, one PIC is programmed as the 'master' with one input (IRQ2) being the 'cascaded' interrupt from the second 'slave' PIC.

This configuration allows for a total of 15 interrupt sources to the CPU. Table 2.3 shows the interrupts with their corresponding vectors and sources as defined for AT PCs.

Table 2.30 PC-AT Interrupt Definitions

Interrupt Request	Interrupt Vector	Function/Assignment
IRQ0	08h	Timer
IRQ1	09h	Keyboard
IRQ2	0Ah	Slave 8259
IRQ3[1)]	0Bh	COM 2/4
IRQ4[1)]	0Ch	COM 1/3
IRQ5[1)]	0Dh	LPT2
IRQ6	0Eh	Floppy
IRQ7[1)]	0Fh	LPT1
IRQ8	70h	Real-Time Clock
IRQ9[1)]	71h	Redirected IRQ2
IRQ10	72h	USB
IRQ11[1)]	73h	Ethernet/FireWire
IRQ12	74h	Reserved
IRQ13	75h	Co-processor
IRQ14[1)]	76h	Hard Disk (IDE 0)
IRQ15[1)]	77h	IDE 1

[1)] Entries may be reserved for ISA devices with the BIOS

2.4 Inova PIII Device List

Table 2.40 shows the available PCI devices both on-board and off-board (CompactPCI backplane). It should be noted that the interrupt routing assumes a standard Inova backplane configuration with a right-hand system slot.

Table 2.40 Legacy I/O Map (ISA Compatible)

PCI Bus Number	Device Number	Description	PCI Interrupt Routing
0 (On-board PCI)	0x00	Host-PCI Bridge (82443BX)	N/A
0	0x01	PCI-PCI Bridge (82443BX)	N/A
0	0x07	PCI-ISA Bridge (Ali 1543C B1)	N/A
0	0x08	PCI-PCI Bridge (Intel 21150 or 21154)	INTD#
0	0x09	IEEE1394 (TI TSB12LV26) FireWire	INTB#
0	0x0A	Ethernet (Intel 82559)	INTA#
0	0x0B	Optional 2nd Ethernet (Intel 82559)	INTD#
0	0x0C	PCI Extension, Device 0	INTC#
0	0x0D	PCI Extension, Device 1	INTB#
0	0x10	IDE (Ali 1543C B1)	N/A
0	0x11	PMU (Ali 1543C B1)	N/A
0	0x14	USB (Ali 1543C B1)	N/A
1 (On-board AGP)	0x00	Graphics (ATI Radeon or SMI Lynx3DM)	INTC#
2 (cPCI Backplane)	0x09	CompactPCI Slot 1 [1)]	INTD#
2	0x0A	CompactPCI Slot 2	INTC#
2	0x0B	CompactPCI Slot 3	INTB#
2	0x0C	CompactPCI Slot 4	INTA#
2	0x0D	CompactPCI Slot 5	INTD#
2	0x0E	CompactPCI Slot 6	INTC#
2	0x0F	CompactPCI Slot 7 [next to Master]	INTB#

[1)] CompactPCI backplane numeration is based on a 7-slot backplane

2.5 Interrupt Configuration

The CompactPCI specification defines a total of six interrupt signals on the backplane. INTA# through INTD# are used to route interrupts from the CompactPCI boards to the PIC on the 'processor board. The interrupt request level generated by the device depends on the backplane slot number which the board is plugged into, and the interrupt signal which is driven by the particular PCI device.

> ***Note:***
>
> ***CompactPCI interrupts may be shared by multiple sources***

Table 2.50 CompactPCI Bus Interrupts

CompactPCI Bus Interrupts	
INTA#	
INTB#	
INTC#	
INTD#	
INTP	(IRQ14)
INTS	Serialized Interrupt Refer to BIOS Documentation
ENUM#	(IRQ5)

2.6 Timer / Counter

The IBM-compatible architecture configures the programmable timer / counter (Intel 8254-compatible) devices for system-specific functions as shown in Table 2.50.

The BIOS programs Timer 0 to generate an interrupt approximately every 55ms (18.2 times per second.) This interrupt, known as the system timer tick, updates the BIOS clock and turns off the floppy disk motor drive after a few seconds of inactivity for example.

The BIOS featured in Inova's CPUs programs the system timer tick for PC compatibility. The interrupt generated by the timer creates an interrupt request on IRQ0 of the programmable interrupt controller (PIC) which is serviced by the CPU as interrupt vector 08h.

In addition, Timer 1 and Timer 2 are also initialised by the BIOS as necessary for the specific 'processor board functions.

Table 2.50 Timer and Counter Functions

Timer	Function/Assignment
Timer 0	System Timer, Periodic Interrupt (55 ms)
Timer 1	SDRAM Refresh
Timer 2	Speaker Frequency Generator

2.7 Watchdog

A three tier watchdog function with configurable timer is implemented in the ICP-PIII. Once the timer has been set (between 64ms and 64x5min) the interrupt mode may be set. Either a Reset, INIT, NMI or SMI interrupt is issued upon timeout.

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CompactPCI®

Interfaces

Interfaces Contents

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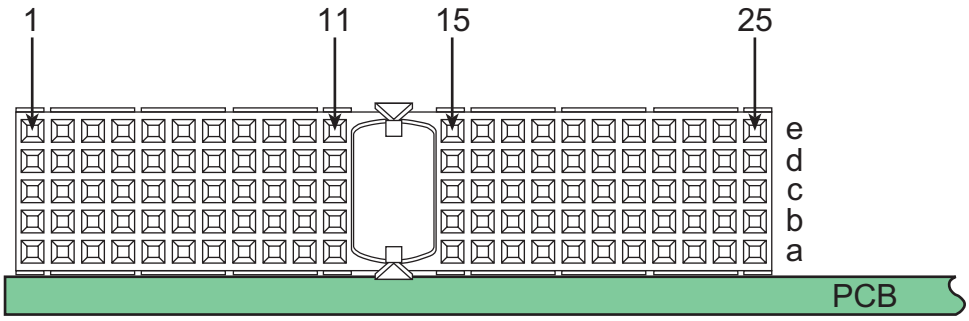
CompactPCI®

3.0 CompactPCI J1/J2 Connector

The CompactPCI standard is electrically identical to the PCI local bus standard but has been enhanced to support rugged industrial environments and up to 8 slots. The standard is based upon a 3U board size and uses a rugged pin-in-socket hard 2mm connector (IEC-1076-4-101.)

3.01 CompactPCI Connector

Figure 3.01 The 32-Bit CompactPCI Bus Interface Connector



3.02 ICP-PIII Connector J1 and J2

Inova's ICP-PIII CPU board has been designed as a 32-bit system slot device able to operate in either +5V or +3.3V (I/O) systems. The CompactPCI backplane connector is keyed accordingly (yellow for +3.3V and blue for +5V.)

> ***Note:***
>
> ***Do not remove the keys. An I/O board operating at 5.0V and keyed accordingly will cause a 3.3V configured system to fail if the keys are removed.***

Table 3.02 Inova's ICP-PIII 32-Bit CompactPCI J1 Pin Assignment

Pin Nr	Row A	Row B	Row C	Row D	Row E
J1-25	+5V	REQ64# Pull-Up V(I / O)	ENUM#	+3.3V	+5V
J1-24	AD[1]	+5V	V(I / O)	AD[0]	ACK64# Pull-Up V(I / O)
J1-23	+3.3V	AD[4]	AD[3]	+5V	AD[2]
J1-22	AD[7]	GND	+3.3V	AD[6]	AD[5]
J1-21	+3.3V	AD[9]	AD[8]	M66EN – Gnd	C / BE[0]#
J1-20	AD[12]	GND	V(I / O)	AD[11]	AD[10]
J1-19	+3.3V	AD[15]	AD[14]	GND	AD[13]
J1-18	SERR#	GND	+3.3V	PAR	C / BE[1]#
J1-17	+3.3V	IPMB-SCL	IPMB-SDA	GND	PERR#
J1-16	DEVSEL#	GND	V(I / O)	STOP#	LOCK#
J1-15	+3.3V	FRAME#	IRDY#	BD-SEL#	TRDY#
J1-14	KEY AREA				
J1-13					
J1-12					
J1-11	AD[18]	AD[17]	AD[16]	GND	C / BE[2]#
J1-10	AD[21]	GND	+3.3V	AD[20]	AD[19]
J1-09	C / BE[3]	-	AD[23]	GND	AD[22]
J1-08	AD[26]	GND	V(I / O)	AD[25]	AD[24]
J1-07	AD[30]	AD[29]	AD[28]	GND	AD[27]
J1-06	REQ#	GND	+3.3V	CLK	AD[31]
J1-05	-	-	RST#	GND	GNT#
J1-04	UPS[1)]	HEALTHY#	V(I / O)	INTP	INTS
J1-03	INTA#	INTB#	INTC	+5V	INTD#
J1-02	-	+5V	-	-	-
J1-01	+5V	-12V	-	+12V	+5V

[1)] Reserved for use for Inova's Uninterruptible Power Supply (UPS)

Table 3.03 Inova's ICP-PIII 32-Bit CompactPCI J2 Pin Assignment (Standard)

Pin Nr	Row A	Row B	Row C	Row D	Row E
J2-22	-	-	-	-	-
J2-21	CLK6	GND	-	-	-
J2-20	CLK5	GND	-	GND	-
J2-19	GND	GND	-	-	-
J2-18	-	-	-	GND	-
J2-17	-	GND	PRST#	REQ6#	GNT6#
J2-16	-	-	-	GND	(UBAT)[5)]
J2-15	-	GND	-	REQ5#	GNT5#
J2-14	-	-	-	GND	-
J2-13	-	GND	V(I/O)	-	-
J2-12	-	-	-	GND	-
J2-11	-	GND	V(I/O)	-	-
J2-10	-	-	-	GND	-
J2-09	-	GND	V(I/O)	-	-
J2-08	-	-	-	GND	-
J2-07	-	GND	V(I/O)	-	-
J2-06	-	-	-	GND	-
J2-05	-	GND	V(I/O)	-	-
J2-04	V(I/O)	SPEAKER[4)]	-	GND	-
J2-03	CLK4	GND	GNT3#	REQ4#	GNT4#
J2-02	CLK2	CLK3	SYSEN#	GNT2#	GNT3#
J2-01	CLK1	GND	REQ1#	GNT1#	REQ2#

4) : 5V open collector signal (5V/100mA)

5) : Option "External Battery" **(Note: battery must be removed from CPU board)** U_{bat} = +3.4V to +3.6V

Table 3.04 Inova's ICP-PIII 32-Bit CompactPCI J2 Pin Assignment for Rear I/O (A)

Pin Nr	Row A	Row B	Row C	Row D	Row E
J2-22	-	-	-	-	-
J2-21	CLK6	GND	ETH_TxF+	ETH_TxF-	ETH_R45
J2-20	CLK5	GND	COM 2-[6)]	GND	ETH_R78
J2-19	GND	GND	COM 2+[6)]	ETH_RxF+	ETH_RxF-
J2-18	-	-	COM 1-[6)]	GND	COM 1+[6)]
J2-17	-	GND	PRST#	REQ6#	GNT6#
J2-16	-	-	-	GND	(UBAT)[5)]
J2-15	-	GND	-	REQ5#	GNT5#
J2-14	-	-	-	GND	-
J2-13	-	GND	V(I/O)	-	-
J2-12	-	-	-	GND	-
J2-11	-	GND	V(I/O)	-	-
J2-10	-	-	-	GND	-
J2-09	-	GND	V(I/O)	-	-
J2-08	-	-	-	GND	-
J2-07	-	GND	V(I/O)	-	-
J2-06	-	-	-	GND	-
J2-05	-	GND	V(I/O)	-	-
J2-04	V(I/O)	SPEAKER[4)]	-	GND	-
J2-03	CLK4	GND	GNT3#	REQ4#	GNT4#
J2-02	CLK2	CLK3	SYSEN#	GNT2#	GNT3#
J2-01	CLK1	GND	REQ1#	GNT1#	REQ2#

4) : 5V open collector signal (5V/100mA)
5) : Option "External Battery" **(Note: battery must be removed from CPU board)** U_{bat} = +3.4V to +3.6V
6) : RS485 signals

Table 3.05 Inova's ICP-PIII 32-Bit CompactPCI J2 Pin Assignment for Rear I/O (B)

Pin Nr	Row A	Row B	Row C	Row D	Row E
J2-22	-	-	-	-	-
J2-21	CLK6	GND	ETH_TxF+	ETH_TxF-	ETH_R45
J2-20	CLK5	GND	-	GND	ETH_R78
J2-19	GND	GND	-	ETH_RxF+	ETH_RxF-
J2-18	LPT-STP[3)]	LPT-PE[3)]	-	GND	-
J2-17	LPT-AFD[3)]	GND	PRST#	REQ6#	GNT6#
J2-16	LPT-D0[3)]	LPT-ACK[3)]	USB1-DATA+[2)]	GND	(UBAT)[5)]
J2-15	LPT-ERR[3)]	GND	USB1-DATA-[2)]	REQ5#	GNT5#
J2-14	LPT-D1[3)]	LPT-SLCT[3)]	H5V(1A)	GND	RI1[1)]
J2-13	LPT-INIT[3)]	GND	V(I/O)	DTR1[1)]	CTS1[1)]
J2-12	LPT-D2[3)]	-	USB2-DATA+[2)]	GND	TxD1[1)]
J2-11	LPT-SLIN[3)]	GND	V(I/O)	RTS1[1)]	RxD1[1)]
J2-10	LPT-D3[3)]	-	USB2-DATA-[2)]	GND	DSR1[1)]
J2-09	LPT-D4[3)]	GND	V(I/O)	DCD1[1)]	RI2[1)]
J2-08	LPT-D5[3)]	-	-	GND	DTR2[1)]
J2-07	LPT-BUSY[3)]	GND	V(I/O)	CTS2[1)]	TxD2[1)]
J2-06	LPT-D6[3)]	-	-	GND	RTS2[1)]
J2-05	LPT-D7[3)]	GND	V(I/O)	RxD2[1)]	DSR2[1)]
J2-04	V(I/O)	SPEAKER[4)]	-	GND	DCD2[1)]
J2-03	CLK4	GND	GNT3#	REQ4#	GNT4#
J2-02	CLK2	CLK3	SYSEN#	GNT2#	GNT3#
J2-01	CLK1	GND	REQ1#	GNT1#	REQ2#

1) : 5V TTL signals from serial I/O controller
2) : Termination of USB lines on CPU. The +5V and GND signals need fuses and inductors for decoupling (USB specification).
3) : The 5V LPT signals need decoupling and pull-up resistors near the backplane LPT 1 connector.
4) : 5V open collector signal (5V/100mA)
5) : Option "External Battery" **(Note: battery must be removed from CPU board)** U_{bat} = +3.4V to +3.6V
6) : RS485 signals

Table 3.06 Inova's ICP-PIII 32-Bit CompactPCI J2 Pin Assignment for Rear I/O (C)

Pin Nr	Row A	Row B	Row C	Row D	Row E
J2-22	-	-	-	-	-
J2-21	CLK6	GND	FW_TPA+	FW_TPA-	HCS0#
J2-20	CLK5	GND	HADR0	GND	HRST#
J2-19	GND	GND	HADR1	FW_TPB+	FW_TPB-
J2-18	LPT-STP[3)]	LPT-PE[3)]	HADR2	GND	HCS1#
J2-17	LPT-AFD[3)]	GND	PRST#	REQ6#	GNT6#
J2-16	LPT-D0[3)]	LPT-ACK[3)]	[DEG# = LPT-D0]	GND	(UBAT)[5)]
J2-15	LPT-ERR[3)]	GND	[FAL# = LPT-D1]	REQ5#	GNT5#
J2-14	LPT-D1[3)]	LPT-SLCT[3)]	H5V(1A)	GND	HD0
J2-13	LPT-INIT[3)]	GND	V(I/O)	HD1	HD2
J2-12	LPT-D2[3)]	HIOW#	USB2-DATA+[2)]	GND	HD3
J2-11	LPT-SLIN[3)]	GND	V(I/O)	HD4	HD5
J2-10	LPT-D3[3)]	HIOR#	USB2-DATA-[2)]	GND	HD6
J2-09	LPT-D4[3)]	GND	V(I/O)	HD7	HD8
J2-08	LPT-D5[3)]	HIRQ15	HDMARQ	GND	HD9
J2-07	LPT-BUSY[3)]	GND	V(I/O)	HD10	HD11
J2-06	LPT-D6[3)]	-	HDMACK	GND	HD12
J2-05	LPT-D7[3)]	GND	V(I/O)	HD13	HD14
J2-04	V(I/O)	SPEAKER[4)]	HIORDY#	GND	HD15
J2-03	CLK4	GND	GNT3#	REQ4#	GNT4#
J2-02	CLK2	CLK3	SYSEN#	GNT2#	GNT3#
J2-01	CLK1	GND	REQ1#	GNT1#	REQ2#

1) : 5V TTL signals from serial I/O controller
2) : Termination of USB lines on CPU. The +5V and GND signals need fuses and inductors for decoupling (USB specification).
3) : The 5V LPT signals need decoupling and pull-up resistors near the backplane LPT 1 connector.
4) : 5V open collector signal (5V/100mA)
5) : Option "External Battery" **(Note: battery must be removed from CPU board)** U_{bat} = +3.4V to +3.6V
6) : RS485 signals

Table 3.07 Inova's ICP-PIII Rear I/O J2 (CPU) Integration

REAR I/O OPTION	Rear I/O			
	STANDARD	A	B	C
ETHERNET	No	Yes	Yes	No
COM 1/2	No	Both (RS485)	Both (TTL)	No
USB 1/2	No	No	Both	USB 2
FireWire 2	No	No	No	Yes
LPT 1	No	No	Yes	Yes
SPEAKER	Yes	Yes	Yes	Yes
BATTERY	No	No	No	No
EIDE	No	No	No	Yes

Currently three forms of rear I/O are available and, depending on the version currently in use, decides which (if any) of the J2 signals are available to the rear J2 connector.

The rear I/O options described here do not detract from the latest PICMG 2.0 R3.0 specification.

3.1 CompactPCI Backplane

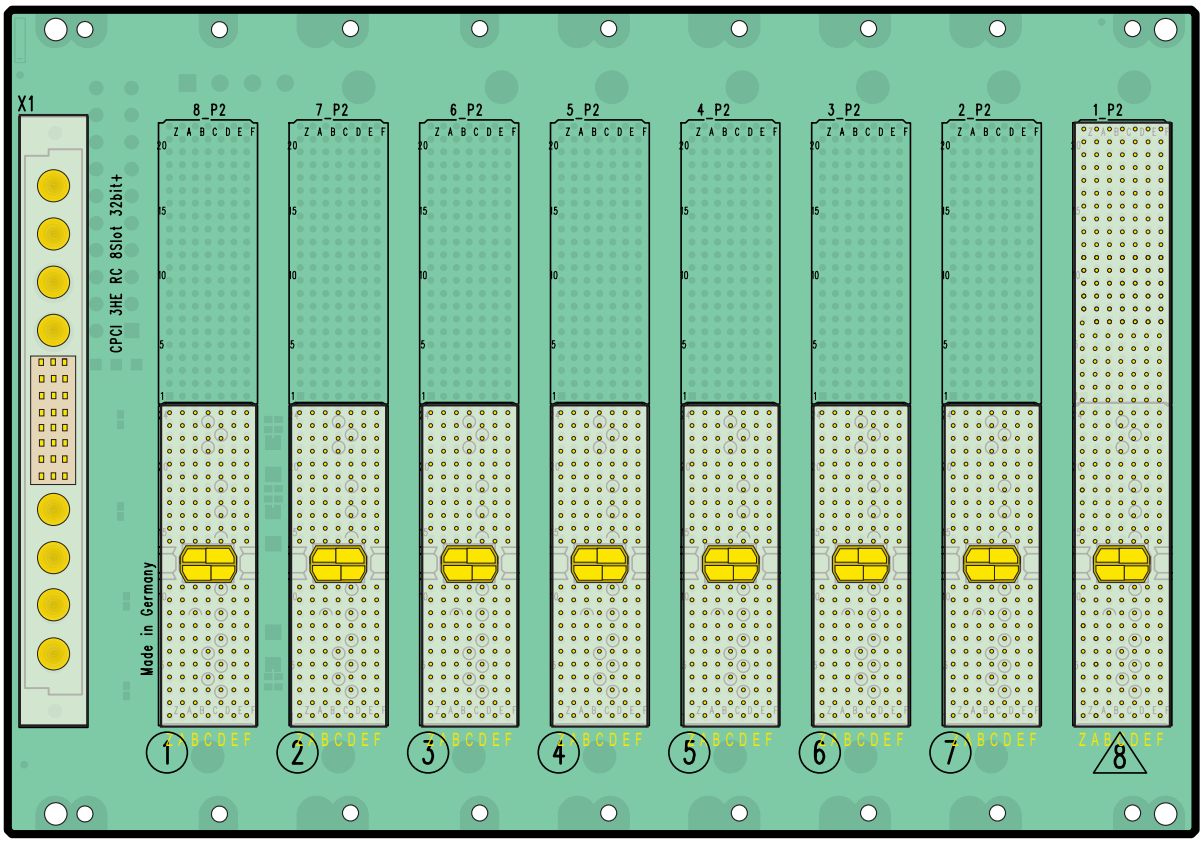
The form factor defined for CompactPCI boards is based upon the Euro-card industry standard. Both 3U (100 mm by 160 mm) and 6U (233 mm by 100 mm) board sizes are defined. A CompactPCI system is composed of up to eight CompactPCI cards. The CompactPCI backplane consists of one System Slot, and up to seven Peripheral Slots.

The System Slot provides arbitration, clock distribution, and reset functions for all boards on the bus. The System Slot is responsible for performing system initialization by managing each local board's IDSEL signal.

Physically, the System Slot may be located at either end of the backplane but Inova have placed theirs on the right to cater for physical expansion due to heat-sink, hard disk, extended functionality etc. The Peripheral Slots may contain simple boards, intelligent slaves, or PCI bus masters.

> ***Note:***
>
> ***Inova's 3U CompactPCI CPU boards can be used as either master or slave boards i.e. occupying either the system slot or the peripheral slot. The choice of PCI/PCI bridge (multiprocessing or standard) decides which of the slots is used.***

Figure 3.10 Inova's 32-Bit CompactPCI 8-Slot Backplane - RH System Slot



> ***Note:***
>
> ***The logical slots are different to the physical slots. The slot marked with the '△' is the System Slot and always assigned logical '0'. The neighbouring slot is logical '0xF'!***

3.2 Interfaces

3.21 J7 & J12 Fast Ethernet

J7 is available as standard on the CPU front-panel and, as an option, J12 may also be available but at the expense of the FireWire interface. The RJ45 interface supports both the 10BaseT and 100BaseTX twisted pair standard.

Figure 3.21 RJ45 Pinout

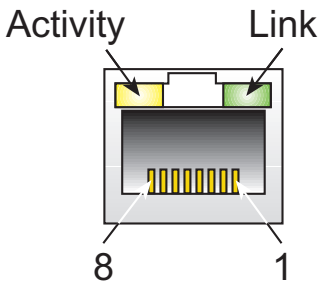


Table 3.21 Ethernet Connector Signals

Pin No.	Signal
1	TXF+
2	TXF-
3	RXF+
4,5	R45
6	RXF-
7, 8	R78
9, 10	Link LED; not accessible on pins
11, 12	Active LED; not accessible on pins
13, 14	PE; not accessible on pins

Note:

Users taking advantage of the CPU's rear I/O options are advised not to use the front-panel interface if the rear interface is being used. Possible damage to the board could occur and data integrity cannot be assured.

3.22 J17 VGA Interface

J17 is available on the CPU front-panel if this option is required and if this position is not already occupied by a PCI, PanelLink or GigaST★R piggyback. The 15-pin high-density D-Sub connector forms the physical interface for the video on the ICP-PIII which is based on either the Silicon Motion Lynx3DM graphic accelerator equipped with 8MByte RAM or the Radeon VE controller with 16MByte RAM. In both cases, the controller is a highly integrated 128-bit GUI (Grahpical User Interface) engine that has been optimized for handling graphic-intensive environments like those found in Windows NT.

The controller uses a 64-bit data path to the RAM video memory, a 24-bit high-performance 135 MHz RAMDAC and a flat-panel interface capable of controlling the latest STN and TFT panels.

All ICP-PIII CPUs, if prepared for graphics, are equipped with 8/16MByte high-speed RAM supporting resolutions up to 1600 x 1200 pixels with 24-bit (True Colour) depth or 2048 x 1536 pixels with 16-bit (Hi-Colour) depth. VGA, SVGA, XGA, XSGA Composite video and TFT dual-scan/single-scan colour panels are supported with configurable colour depths.

Figure 3.22 High-Density D-Sub VGA Interface Pinout

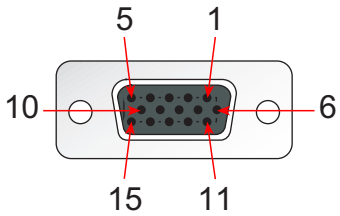


Table 3.22 Video Output Connector Signals

Pin No.	Signal
1	Analog RED
2	Analog GREEN
3	Analog BLUE
4	N/C
5, 6, 7, 8	CRT Ground
9, 11	N/C
10	CRT Ground
12	DDC-SDA
13	HSYNC
14	VSYNC
15	DDC-SCL

Table 3.22b Video Resolutions

Lynx3DM Controller

VGA Resolution	Colour Depth			Refresh Rates (Hz)
	256	65, 000	16.7M	
640x480	60/72/75/85	60/72/75/85	60/72/75/85	
800x600	60/72/75/85	60/72/75/85	60/72/75/85	
1024x768	43I/60/70/ 75/85	43I/60/70/ 75/85	43I/60/70/ 75/85	
1280x1024	43I/60/75	43I/60/75	N/A	
1600x1200	43I	43I (not 65k)	N/A	

Note: 32k colours are not selectable in Microsoft's Windows 98
'I' in the above table refers to interlaced monitors.

ATI Radeon VE Controller

VGA Resolution	Colour Depth			Refresh Rates (Hz)
	256	65, 000	16.7M	
640x480	60 to 200	60 to 200	60 to 200	
800x600	60 to 200	60 to 200	60 to 200	
1024x768	60 to 200	60 to 200	60 to 200	
1152x864	43 to 160	43 to 160	43 to 160	
1280x1024	60 to 120	60 to 120	60 to 120	
1600x1200	52 to 100	52 to 100	52 to 100	
1920x1080	60 to 80	60 to 80	60 to 80	
1920x1200	60 to 85	60 to 85	60 to 85	
1920x1440	60/75	60/75	60/75	
2048x1536	60	60	60	

TFT Resolution	Colour Depth			Refresh Rates (Hz)
	256	65, 000	16.7M	
640x480	60	60	60	
800x600	60	60	60	
1024x768	60	60	60	
1280x1024	60	60	60	

Note: Screen resolutions and refresh rates are subject to change without notice.

3.23 J16 PanelLink Interface

J16 is available if requested at time of order and replaces the standard VGA connector on the front-panel.

Figure 3.23 PanelLink Interface Connector

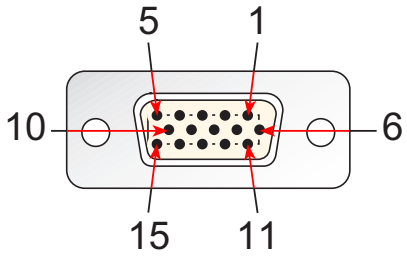


Table 2.12 PanelLink Interface

Pin No.	Signal
1	Tx2-
2	Tx1-
3	Tx0-
4	TxC-
5	DDC Data
6, 7, 8, 9	GND
10	+5V (<100mA)
11	Tx2+
12	Tx1+
13	Tx0+
14	TxC+
15	DDC Clock

2.24 J16 GigaSTAR Interface

The standard 9-pin D-Sub connector is used for GigaSTAR video transmission.

Figure 2.24 GigaSTAR D-Sub Interface Pinout

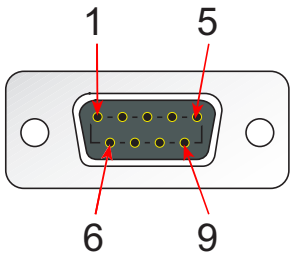


Table 2.11 GigaSTAR Interface

Pin No.	Signal
1	GigaSTAR Tx+
2	N/C
3	N/C
4	N/C
5	N/C
6	GigaSTAR Tx-
7	N/C
8	N/C
9	N/C

3.25 J19 USB Interface

J19 is located as standard on the front panel

Figure 3.25 USB Interface Pinout

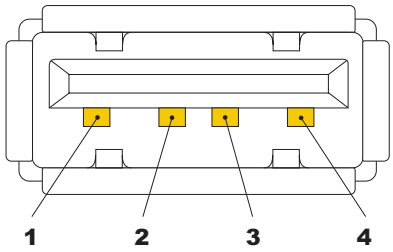


Table 3.25 USB Connector Signals

Pin No.	Signal
1	+5V
2	USB P0-
3	USB P0+
4	GND
Housing	PE

3.26 J15 FireWire Interface

J15 is located on the front panel (if this option is available)

Figure 3.26 FireWire Interface Pinout

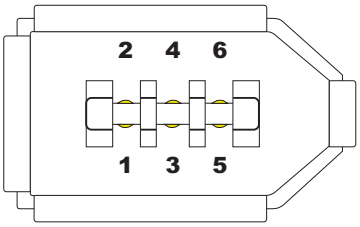


Table 3.26 FireWire Connector Signals

Pin No.	Signal
1	IEEE 1394 S +12V (1A Fuse)
2	IEEE 1394 S GND
3	IEEE 1294 S TPB-
4	IEEE 1394 S TPB+
5	IEEE 1394 S TPA-
6	IEEE 1394 S TPA+
Housing	PE

3.27 J20 Infrared (iRdA) Interface

This option is proprietary and not documented here.

3.28 J20 Reset Button

The reset button allows the CPU to be rest in the event that it 'hangs' Performing a reset in this manner is known as a 'warm' start as power is not removed from the peripherals (IDE etc.) This reset button is also used when recovering a corrupt BIOS image - refer to the PIII BIOS user's manual for details.

3.29 J14 FLASH Interface

J14 is proprietary and not documented here

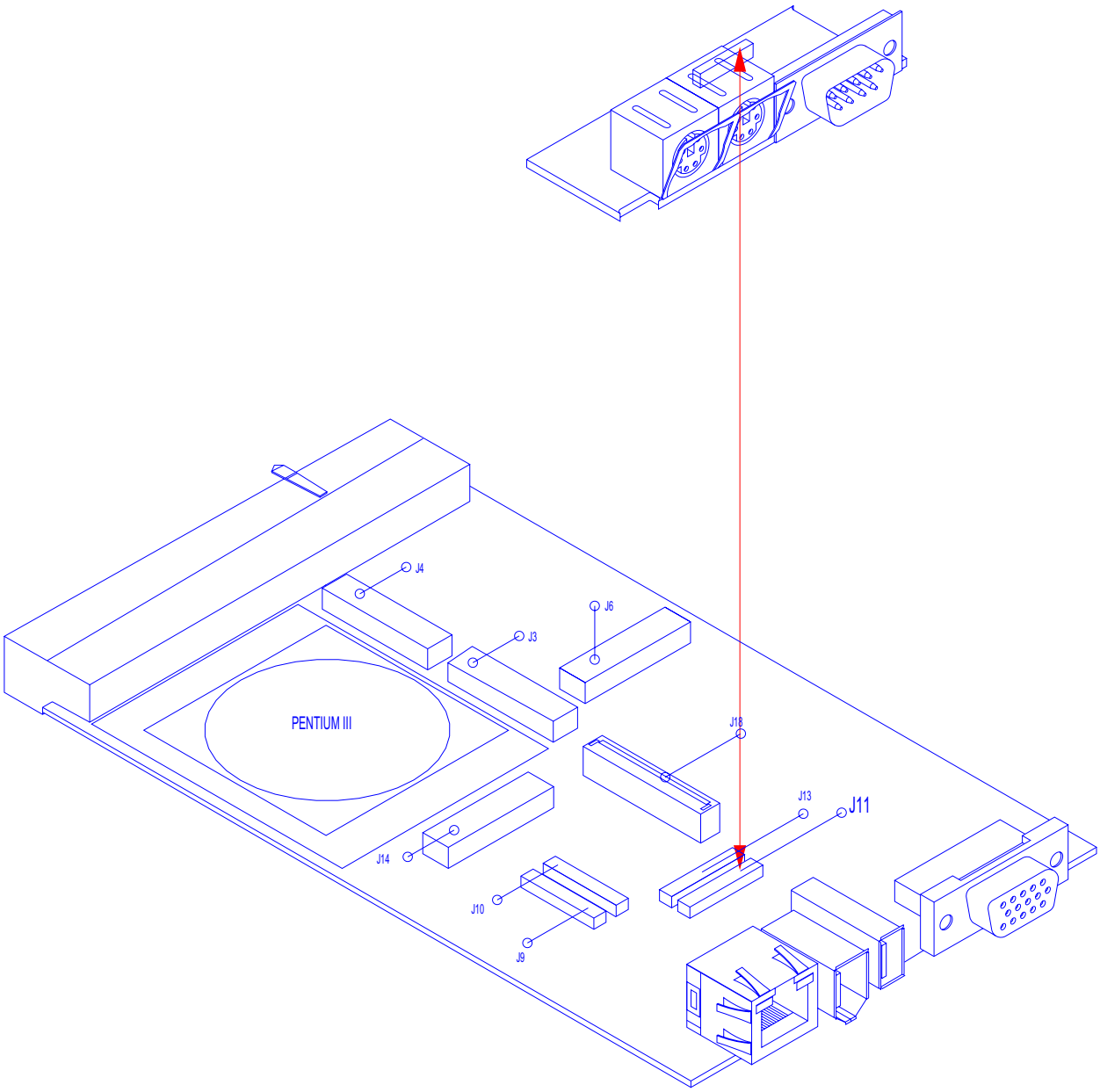
3.30 J18 Floppy Disk Interface

J18 is proprietary and not documented here but observes the standard slim-line floppy pin-out.

3.31 Connecting the PIII to the Inova IPB-FPE8

Appendix A provides more information on the IPB-FPE8 and its derivatives. Figure 3.31 shows how the CPU connects to the piggyback by a length of flex-cable.

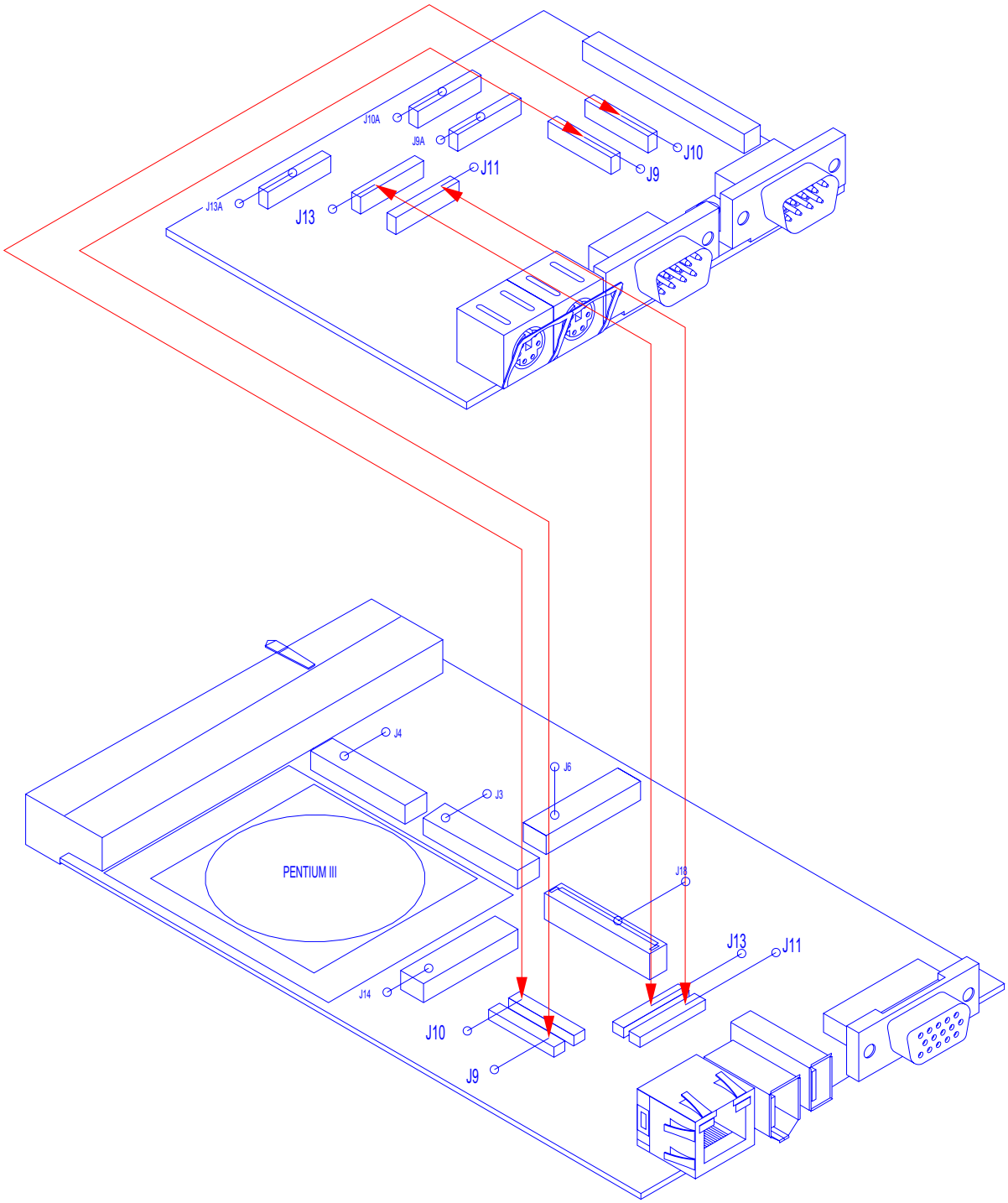
Figure 3.31 CPU to IPB-FPE8 Connection



3.32 Connecting the PIII to the Inova ICP-HD-1

Appendix B provides more information on the ICP-HD-1 and its derivatives. Figure 3.32 shows how the CPU connects to the piggyback by lengths of flex-cable.

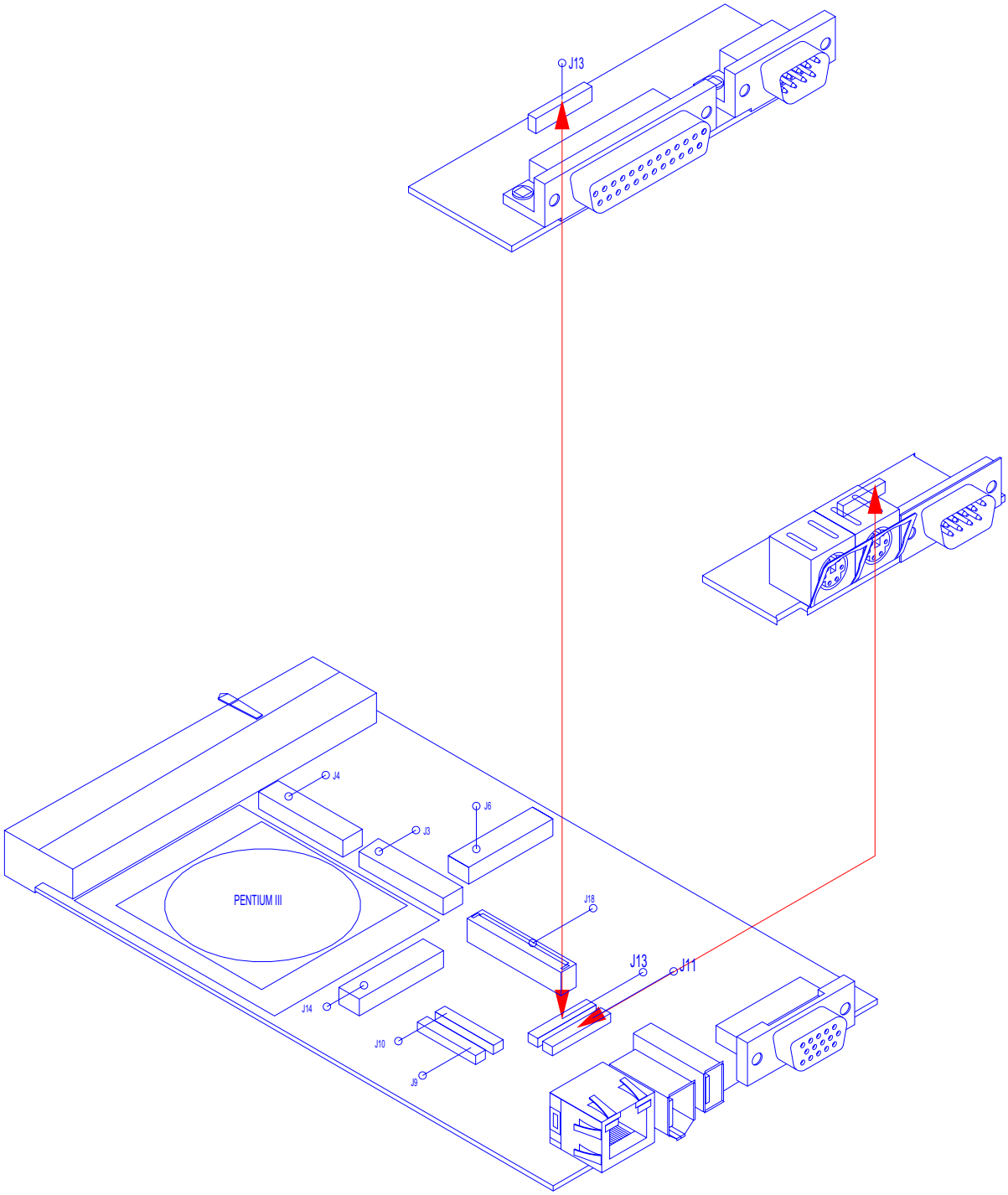
Figure 3.32 CPU to ICP-HD-1 Connection



3.33 Connecting the PIII to the Inova IPB-FPE12

Appendix C provides more information on the IPB-FPE12 and its derivatives. Figure 3.33 shows how the CPU connects to the piggyback by a length of flex-cable. The illustration also shows the IPB-FPE8 connection (Appendix A)

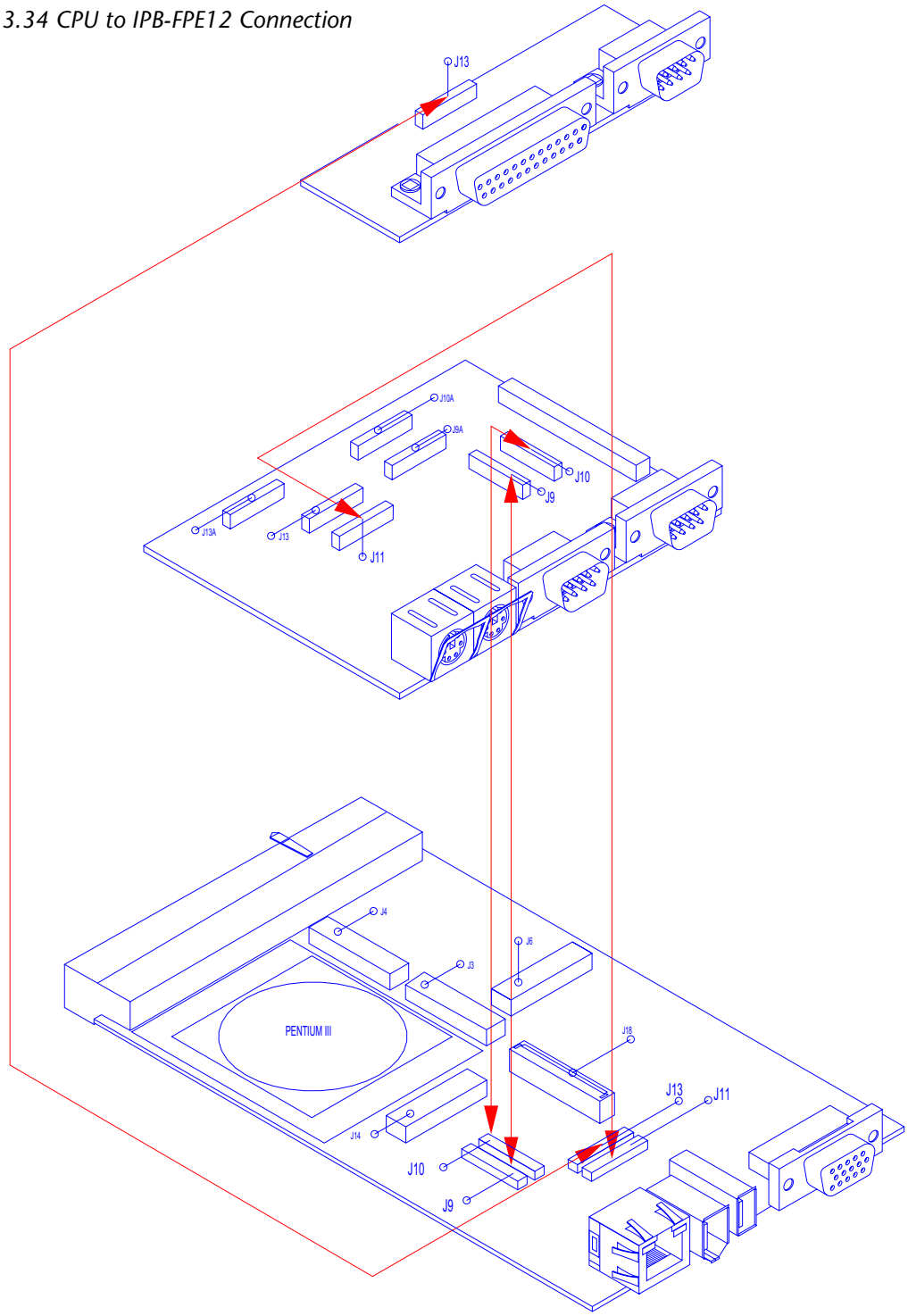
Figure 3.33 CPU to IPB-FPE12 Connection



3.34 Connecting the PIII to the Inova IPB-FPE12

Appendix C provides more information on the IPB-FPE12 and its derivatives. Figure 3.34 shows how the CPU connects to the piggyback by a length of flex-cable. The illustration also shows the ICP-HD-1 connection (Appendix B)

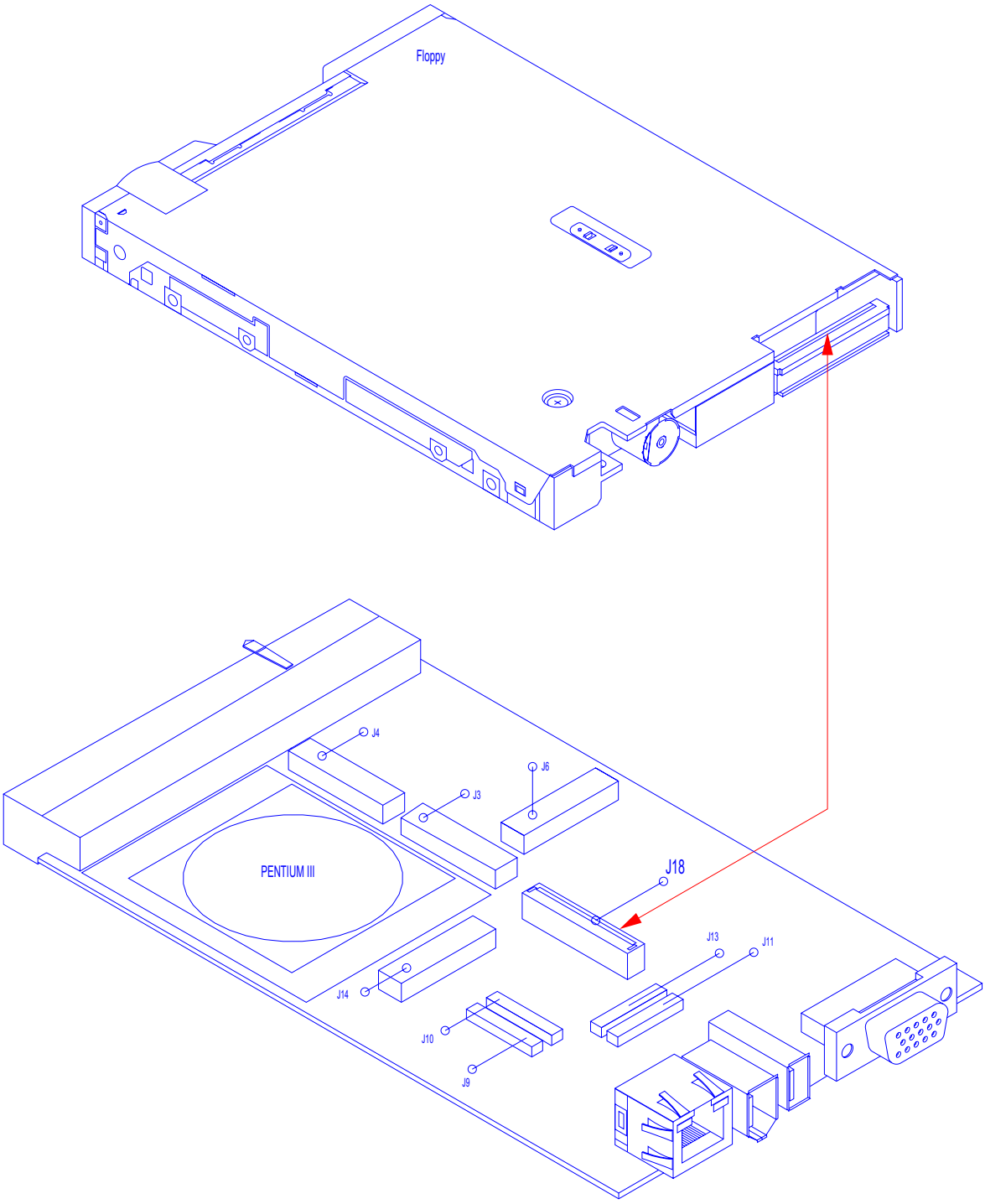
Figure 3.34 CPU to IPB-FPE12 Connection



3.35 Connecting the PIII to the ICP-FD-1

Figure 3.35 shows how the CPU connects to the slim-line floppy disk unit.

Figure 3.35 CPU to Slim-Line Floppy Disk Connection



CompactPCI®

IPB-FPE8

IPB-FPE8 Contents

A

A1 IPB-FPE8 CPU Extension

The IPBFPE8 provides additional CPU functionality in the form of PS-2 style mouse and keyboard connectors and a serial COM1 port.

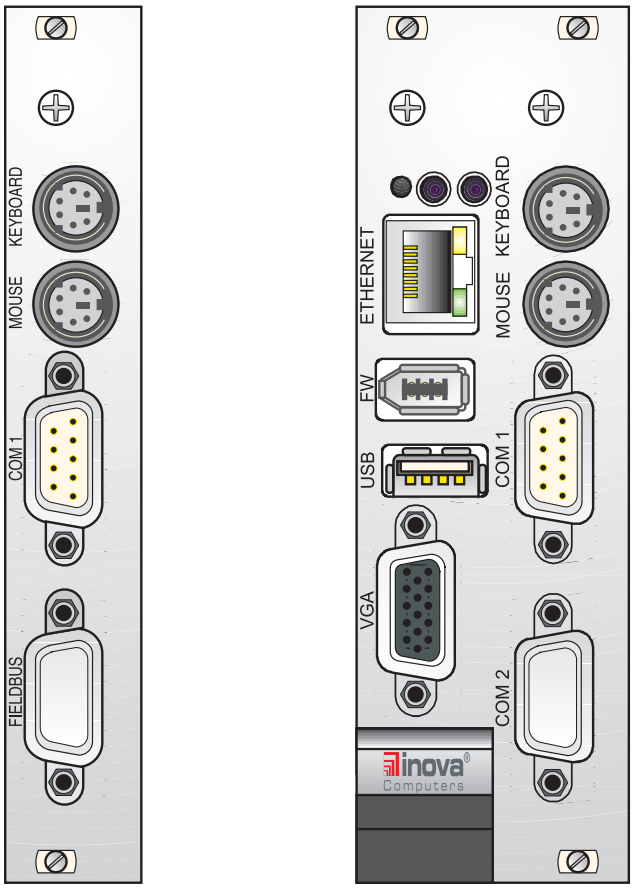
A1.1 J11 Interface for COM1, Mouse & Keyboard

The control of the mouse, keyboard and COM1 interfaces is performed through the J11 connector on the CPU base board. The location of this connector may be determined by referring to Section 1 - Product Overview of the CPU User's Manual. A flex cable from J11 connects to a number of interface boards - all of which are discussed in this section.

A1.2 IPB-FPE8 & Front-panel (4HP or 8HP)

The Inova IPB-FPE8 interface is a small piggyback either as stand-alone with its own 4HP front-panel or integrated with the CPU as in figure A1.2.

Figure A1.2 IPB-FPE8 Stand-Alone or Integrated with CPU

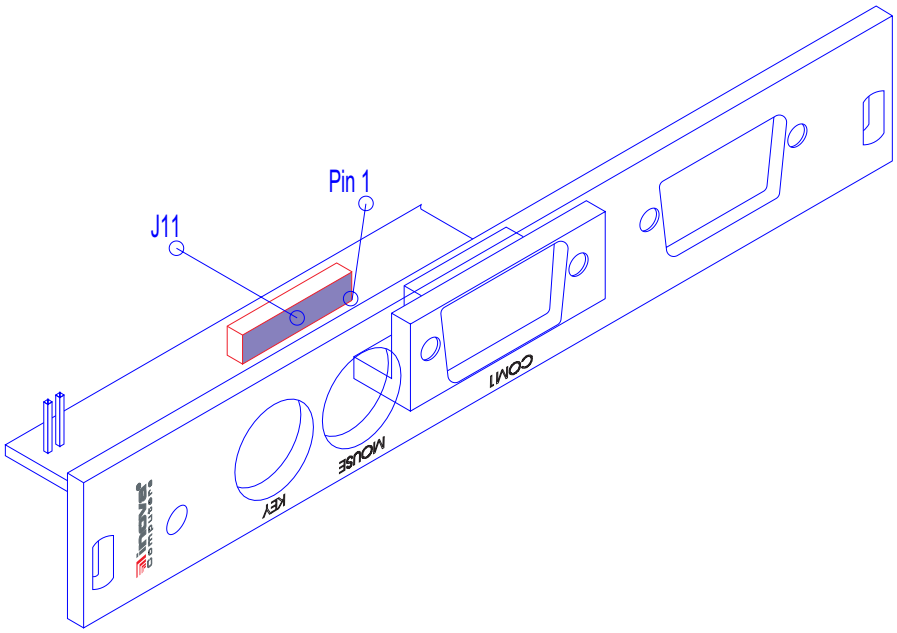


A1.3 Stand-Alone IPB-FPE8

Figure A1.3 illustrates the construction of the stand-alone IPB-FPE8 piggyback and the underside location of the J11 connector. Care should be taken to ensure that pin 1 of J11 on the CPU base board is linked by an appropriate length of flex cable to pin 1 on the piggyback. To help with the orientation, the connector flanks that are blue indicate the blue face of the flex-cable. Unmarked flanks indicate the metallic connection of the flex-cable. Also, pin 1 has been highlighted by a red triangle.

> ***Note:***
> ***Damage to the CPU board or the piggyback may result if the flex cable is positioned incorrectly. Inova will not accept responsibility for negligent actions!***

Figure A1.3 Stand-Alone Piggyback Interface IPB-FPE8



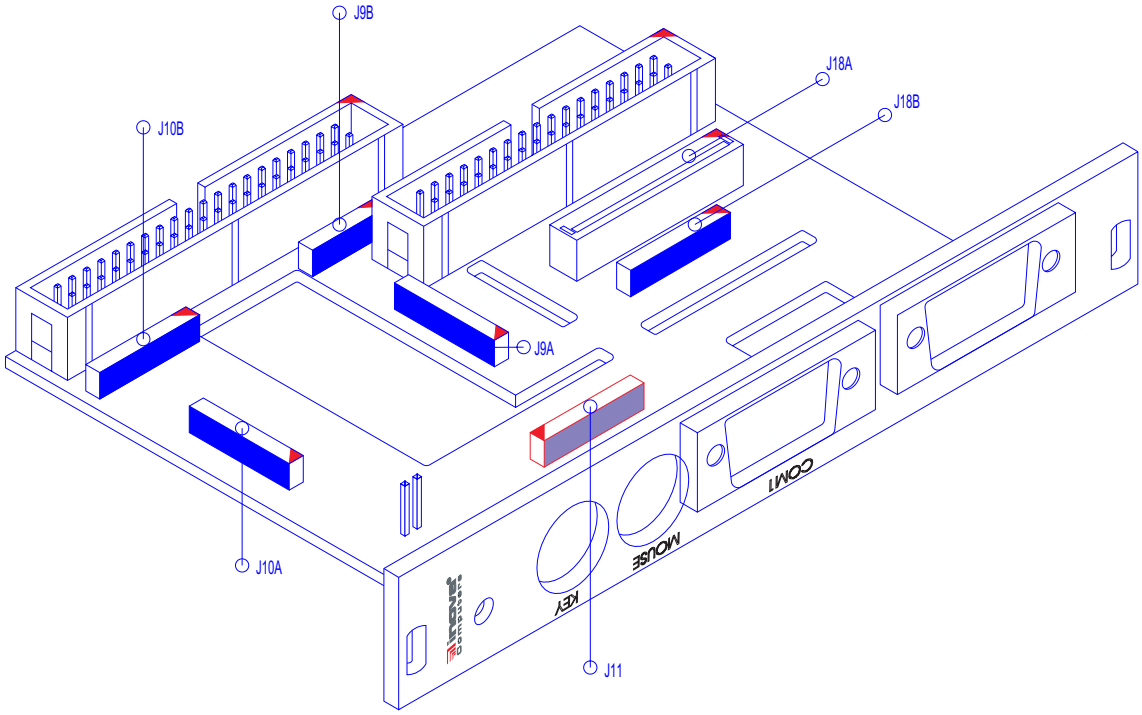
> ***Note:***
> ***The physical connection of the IPB-FPE8 is electrically identical regardless of the nature of connection (stand-alone or integrated!)***

A

A1.4 IPB-FPE8MS (Theme Variation)

Figure A1.4 illustrates the construction of the IPB-FPE8MS - a variation of the IPB-FPE8 but with a number of extra features. The electrical connection to the CPU base board is still via the underside connector J11 and again, the precautions mentioned for the IPB-FPE8 are valid here.

Figure A1.4 Piggyback Interface IPB-FPE8MS



Note that the IPB-FPE8 module does not allow a HD to be connected behind it and the lower 9-pin D-Sub slot may be used for remote connection of PanelLink for example. The IPB-FPE8MS shown in figure A1.4 enables connection of floppy, a CD-ROM and other peripherals. The connector names and descriptions are declared in table A1.4.

Table A1.4 IPB-FPE8MS Connector Description

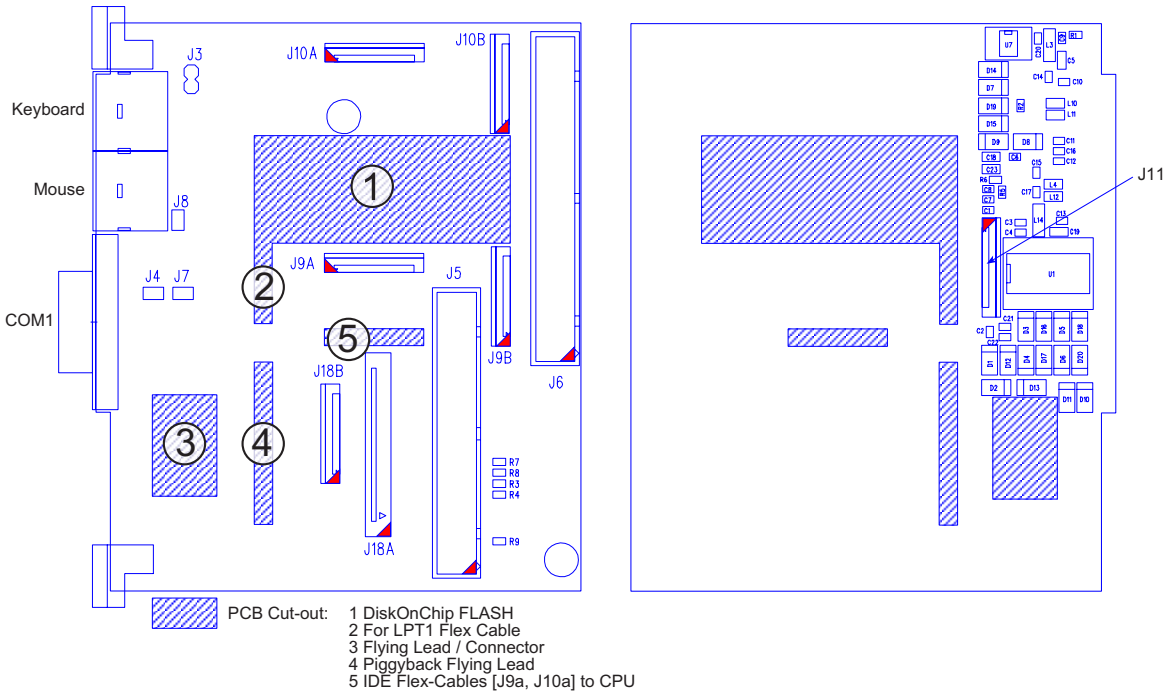
Connector	Description
J9A, J10A	IDE Primary (Master or Slave)
J9B, J10B	IDE Primary (Master or Slave)*
J11	Mouse, Keyboard and COM1
J18A, J18B	Floppy Disk (either a standard slim-line floppy connector or flex cable)

* If connectors 9a and 10a are configured as Master then 9b and 10b must be Slave.

A1.5 IPB-FPE8MS Description

As mentioned previously, the IPB-FPE8MS has a number of additional features compared to the standard IPB-FPE8 module. These extra features include HD and FD connection with both standard connectors and the Inova flex cables. This provides the user with system flexibility.

Figure A1.5 Top & Bottom Views of the IPB-FPE8MS



> ***Note:***
> ***Damage to the CPU board or the piggyback may result if the cables are incorrectly positioned. Inova will not accept responsibility for negligent actions!***

Figure A1.5 makes reference to two standard PC-style connectors (J5 and J6). The function of these connectors is given in table A1.5.

Table A1.5 Standard Hard-Disk & Floppy Disk Connectors

Connector	Description
J5	PC-Style Floppy Disk Connector
J6	Standard Primary IDE Connector (Master or Slave)

A1.6 Keyboard Interface

A front-panel with COM1, COM2 mouse and keyboard interfaces is either integrated into an 8HP standard CPU front-panel or available as a separate 4HP unit. The piggyback located behind these interfaces connects to the CPU-mounted J11 connector.

Figure A1.6 Keyboard Interface Pinout

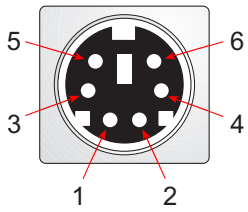


Table A1.6 Keyboard Connector Signals

Pin No.	Signal	Pin No.	Signal
1	Data	2	N/C
3	GND	4	+5V
5	CLK	6	N/C

A1.7 Mouse Interface

A front-panel with COM1, COM2 mouse and keyboard interfaces is either integrated into an 8HP standard CPU front-panel or available as a separate 4HP unit. The piggyback located behind these interfaces connects to the CPU-mounted J11 connector.

Figure A1.7 Mouse Interface Pinout

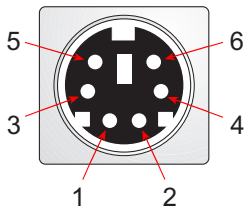


Table A1.7 Mouse Connector Signals

Pin No.	Signal	Pin No.	Signal
1	Data	2	N/C
3	GND	4	+5V
5	CLK	6	N/C

A1.8 COM1 Interface

The COM1 port features a complete set of handshaking and modem control signals, maskable interrupt generation and high-speed data transfer rates. A front-panel with COM1, mouse and keyboard interfaces is either integrated into an 8HP standard CPU front-panel or available as a separate 4HP unit. The piggyback located behind these interfaces connects to the CPU-mounted J11 connector.

Figure A1.8 COM1 Interface Pinout

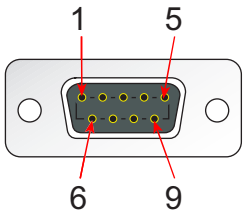


Table A1.8 COM1 Connector Signals

Pin No.	Signal	
	RS232	RS485
1	DCD	
2	RxD	RxD, TxD +
3	TxD	RxD, TxD -
4	DTR	
5	GND	
6	DSR	
7	RTS	
8	CTS	
9	RI	

Note:

The standard CPU configuration has COM1 set for RS232 communication.

However, this device can be configured to observe a two-wire, non galvanically separated, RS485 protocol. The data direction is governed by controlling the UART's RTS signal. Writing a hex value of 0B to this register allows data to be transmitted. Writing 1B to this register configures the device to receive data.

A

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CompactPCI®

ICP-HD

ICP-HD Contents

B

B1 ICP-HD CPU Extension

Several hard-disk connection possibilities exist of which two are documented here. Both of these provide additional CPU functionality in the form of PS-2 style mouse and keyboard connectors and serial COM1 and COM2 ports.

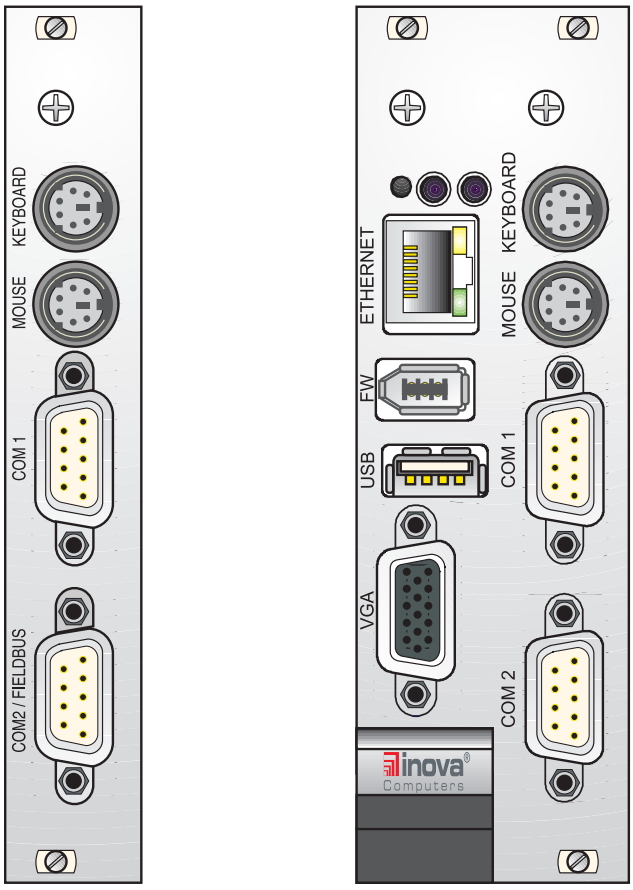
B1.1 J11, J13 Interfaces

The control of the mouse, keyboard, COM1 & COM2 interfaces is performed through the J11 and J13 connectors respectively on the CPU base board. The location of these connectors may be determined by referring to Section 1 - Product Overview of the CPU User's Manual. A flex cable from J11 and J13 connects to the interface boards discussed in this section.

B1.2 ICP-HD-1 & Front-panel (4HP or 8HP)

The Inova ICP-HD-1 interface is an IDE device carrier board available as a stand-alone device with its own 4HP front-panel or integrated with the CPU as in figure B1.2.

Figure B1.2 ICP-HDE8 Stand-Alone or Integrated with CPU

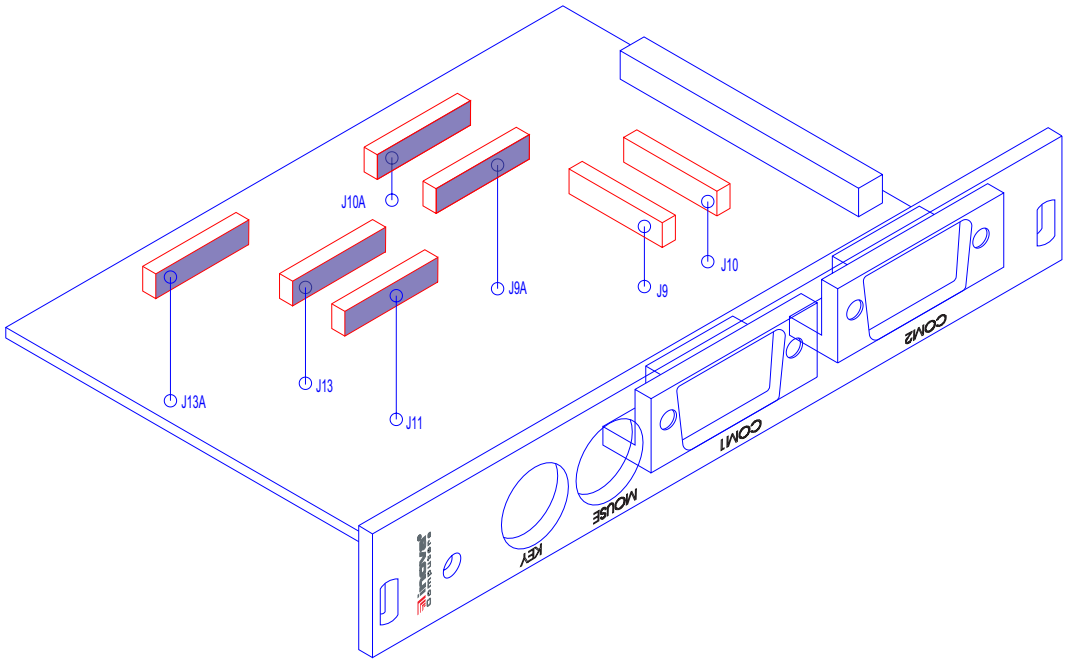


B1.3 IDE Carrier Board ICP-HD-1

Figure B1.3 illustrates the construction of the stand-alone ICP-HD1 carrier and the underside location of the J11 & J13 connectors. The same mechanical construction applies to the integrated version. Care should be taken to ensure that pin 1 of J11/J13 on the CPU base board is linked by an appropriate length of flex cable to pin 1 on the carrier. To help with the orientation, the connector flanks that are blue indicate the blue face of the flex-cable. Unmarked flanks indicate the metallic connection of the flex-cable. Also, pin 1 has been highlighted by a red triangle.

> ***Note:***
> ***Damage to the CPU board or the piggyback may result if the flex cable is positioned incorrectly. Inova will not accept responsibility for negligent actions!***

Figure B1.3 IDE Carrier Board ICP-HD1



> ***Note:***
> ***The physical connection of the ICP-HD-1 is electrically identical regardless of the nature of connection (stand-alone or integrated!)***

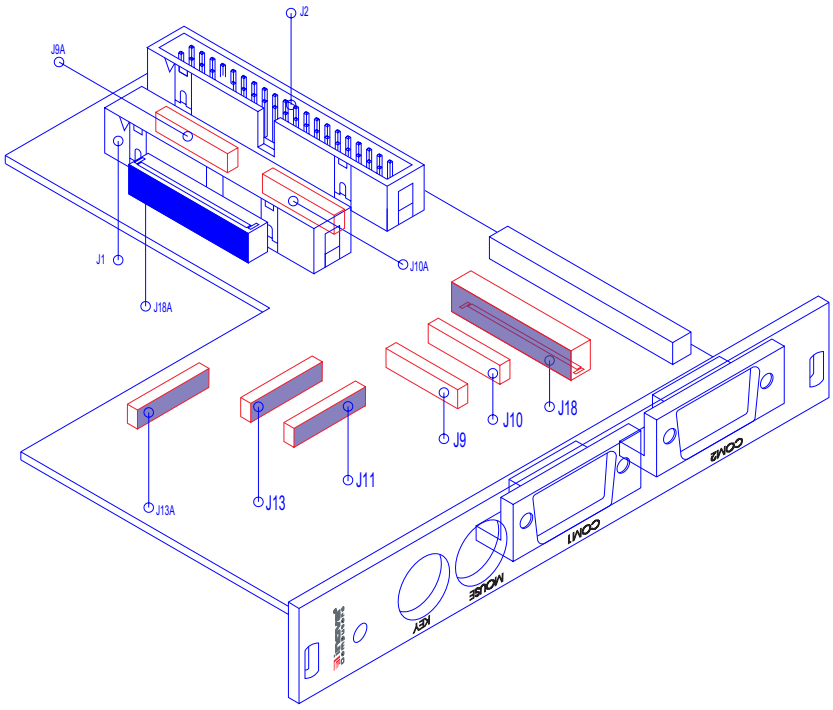
Table B1.3 ICP-HD-1 Connector Description

Connector	Description
J9, J10	Primary IDE (Master / Slave)
J9a, J10a	Primary IDE (Master / Slave)
J11	COM1, Mouse & Keyboard
J13	LPT1 & COM2
J13a	LPT1 & COM2*

B1.4 ICP-HDE8MS (Theme Variation)

Figure B1.4 illustrates the construction of the ICP-HDE8MS - a variation of the ICP-HD-1 but with a number of extra features. The electrical connection to the CPU base board is still via the underside connectors J11 and J13 and again, the precautions mentioned for the ICP-HD-1 are valid here.

Figure B1.4 IDE Carrier ICP-HDE8MS



The ICP-HDE8MS shown in figure B1.4 enables connection of floppy, a CD-ROM and other peripherals. The connector names and descriptions are declared in table B1.4.

Table B1.4 IPB-HDE8MS Connector Description

Connector	Description
J1	Standard Floppy Disk Connector - To Floppy Disk
J2	Standard IDE Connector - To Hard Disk / FLASH
J9, J10	Primary HD (Master / Slave)
J9a, J10A	Primary HD (Master / Slave)
J11	COM1, Mouse & Keyboard
J13	LPT1 & COM2
J13A	LPT1 & COM2*
J18	Slim-Line Floppy Disk Connector - To CPU Base Board
J18A	Slim-Line Floppy Disk Connector - To Floppy Disk

* If connectors 9 and 10 are connected to a Master device then 9a and 10a must be connected to a Slave.

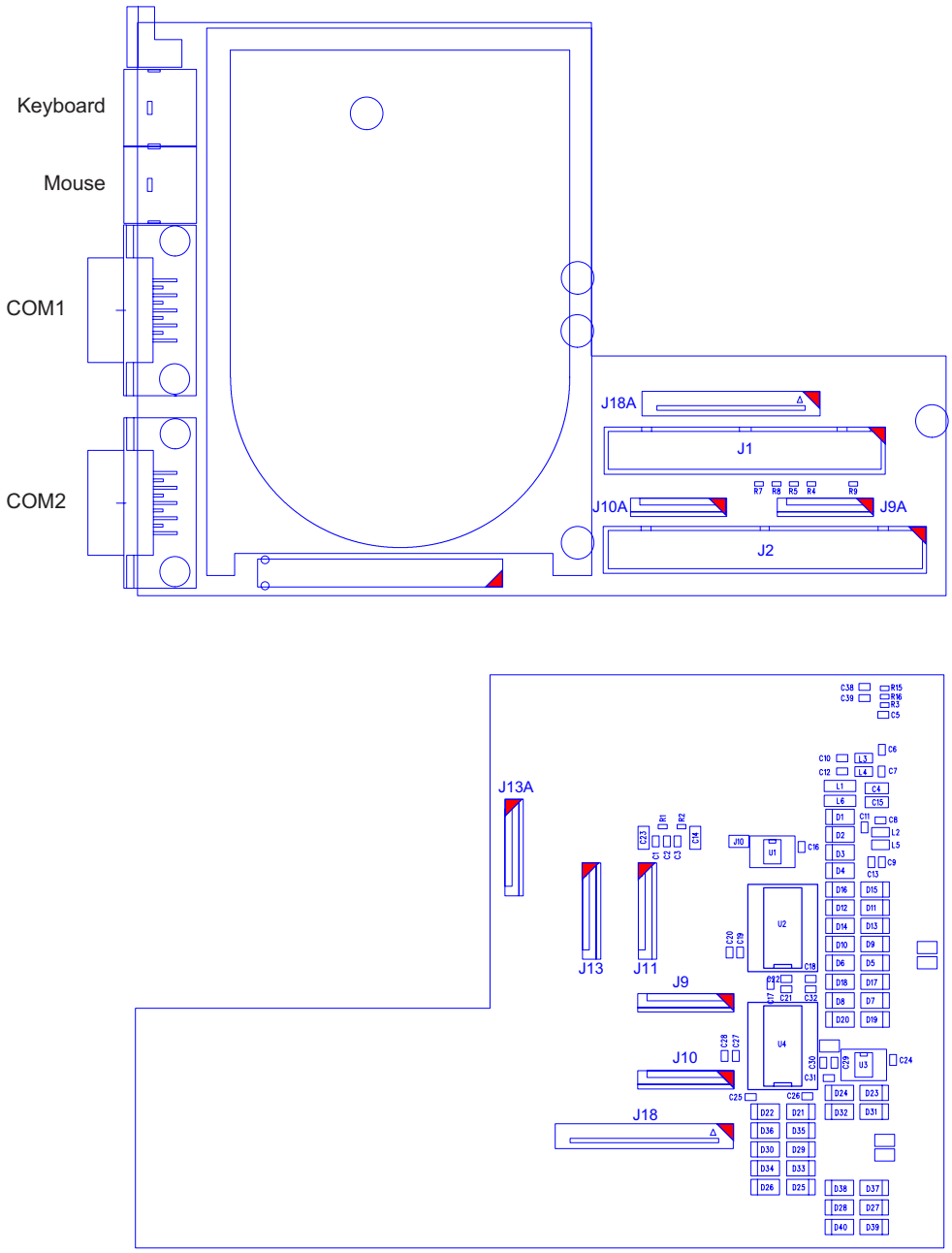
Note:
**** Tables B1.3 and B1.4 refer to J13 and J13a for the connection of COM2 and LPT1. Both the ICP-HD-1 and ICP-HDE8 possess COM2 which is accessed through J13 connected to the CPU board. If the Inova IPB-FPE12 piggy-back is used and connected to J13a then the COM2 on the IDE carriers ICP-HD-1 and ICP-HDE8MS will be disabled.***

Note:
Damage to the CPU board or the piggyback may result if the cables are incorrectly positioned. Inova will not accept responsibility for negligent actions!

B1.5 ICP-HDE8MS Description

As mentioned previously, the ICP-HDE8MS has a number of additional features compared to the standard ICP-HD-1 module. These extra features include HD and FD connection with both standard connectors and the Inova flex cables. This provides the user with additional system flexibility.

Figure B1.5 Top & Bottom Views of the ICP-HDE8MS



B1.6 Keyboard Interface

A front-panel with COM1, COM2 mouse and keyboard interfaces is either integrated into an 8HP standard CPU front-panel or available as a separate 4HP unit. The piggyback located behind these interfaces connects to the CPU-mounted J11 connector.

Figure B1.6 Keyboard Interface Pinout

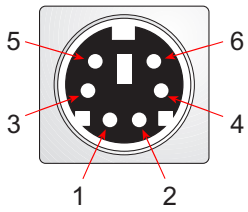


Table B1.6 Keyboard Connector Signals

Pin No.	Signal	Pin No.	Signal
1	Data	2	N/C
3	GND	4	+5V
5	CLK	6	N/C

B1.7 Mouse Interface

A front-panel with COM1, COM2 mouse and keyboard interfaces is either integrated into an 8HP standard CPU front-panel or available as a separate 4HP unit. The piggyback located behind these interfaces connects to the CPU-mounted J11 connector.

Figure B1.7 Mouse Interface Pinout

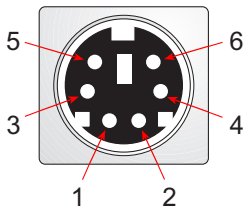


Table B1.7 Mouse Connector Signals

Pin No.	Signal	Pin No.	Signal
1	Data	2	N/C
3	GND	4	+5V
5	CLK	6	N/C

B1.8 COM1 & COM 2 Interfaces

The two COM ports feature a complete set of handshaking and modem control signals, maskable interrupt generation and high-speed data transfer rates. A front-panel with COM1, COM2, mouse and keyboard interfaces is either integrated into an 8HP standard CPU front-panel or available as a separate 4HP unit. The IDE carrier board located behind these interfaces connects to the CPU-mounted J11 and J13 connectors.

Figure B1.8 COM1 & COM2 Interface Pinout

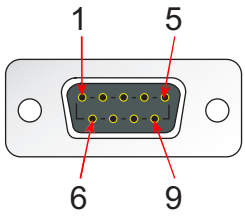


Table B1.8 COM1 & COM2 Connector Signals

Pin No.	Signal	
	RS232	RS485
1	DCD	
2	RxD	RxD, TxD +
3	TxD	RxD, TxD -
4	DTR	
5	GND	
6	DSR	
7	RTS	
8	CTS	
9	RI	

Note:

The standard CPU configuration has both COM ports set for RS232 communication.

However, this device can be configured to observe a two-wire, non galvanically separated, RS485 protocol. The data direction is governed by controlling the UART's RTS signal. Writing a hex value of 0B to this register allows data to be transmitted. Writing 1B to this register configures the device to receive data.

CompactPCI®

IPM-ATA

IPM-ATA

B

B1 IPM-ATA CPU Extension

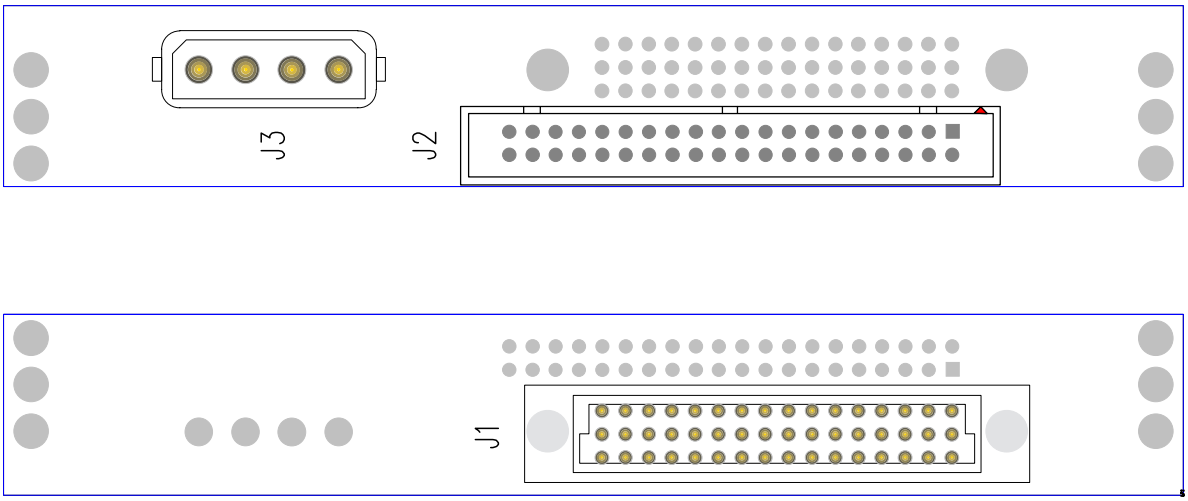
Inova Plug-In Module (IPM-) offers the user the ability to exchange a hard-disk for example without having to remove the CPU from the CompactPCI enclosure and then dismantle it etc. Currently, three units exist that provide industry with hard-disk, Compact FLASH, MicroDrive or ATA PCMCIA mass storage capability.

B1.1 J1 Interfaces

All IPM-ATA modules possess J1 for data communication between the CompactPCI backplane and the mass storage unit(s) in question. Figure B1.1a illustrates the dedicated IPM-ATA backplane and connectors.

Note:
The IPM-ATA modules can only be used in CompactPCI systems that have been prepared for rear I/O (C) or have the IDE signals available on the rear J2 connector that are in accordance with the specification for RIO(C). In addition, the rear J2 CompactPCI connector must be present.

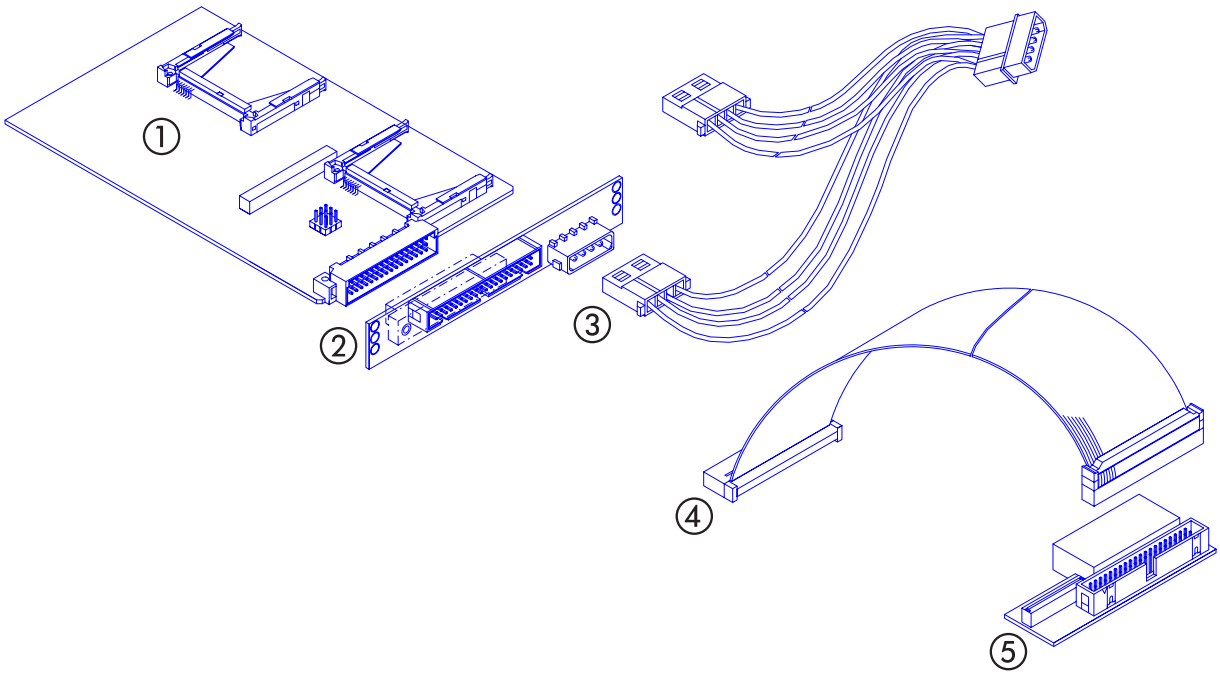
Figure B1.1a Dedicated IPM-ATA Backplane



B1.1 J1 Interfaces (Contd.)

Standard IDE ribbon-cable is used to connect J2 of the IPB-RIO-HD-FD module to the IPM's dedicated backplane. The use of ribbon cable permits the mass-storage device(s) to be positioned at any convenient location within the CompactPCI enclosure. Figure B1.1b shows the complete configuration (CompactPCI to IPM-)

Figure B1.1b The Complete Connection Picture



KEY:
1. IPM-ATA carrier board
2. Dedicated backplane with standard IDE ribbon cable and power cord interfaces
3. Y-Cable for bringing the power from the CompactPCI backplane and to this and another device
4. Standard IDE ribbon cable (30cm)
5. Inova rear I/O module (IPB-RIO-IDE-FD) with IDE and slim-line FD connections

B1.2 IPM-ATA-HD

The IPM-ATA-HD has provision for one standard notebook (2.5") EIDE device (FLASH or hard-disk) and one Compact FLASH or MicroDrive site. Figure B1.2 illustrates the significant connectors for this device while Table B1.2 indicates the jumper positions for the various Master/Slave device configurations.

Figure B1.2 IPM-ATA-HD Board Layout

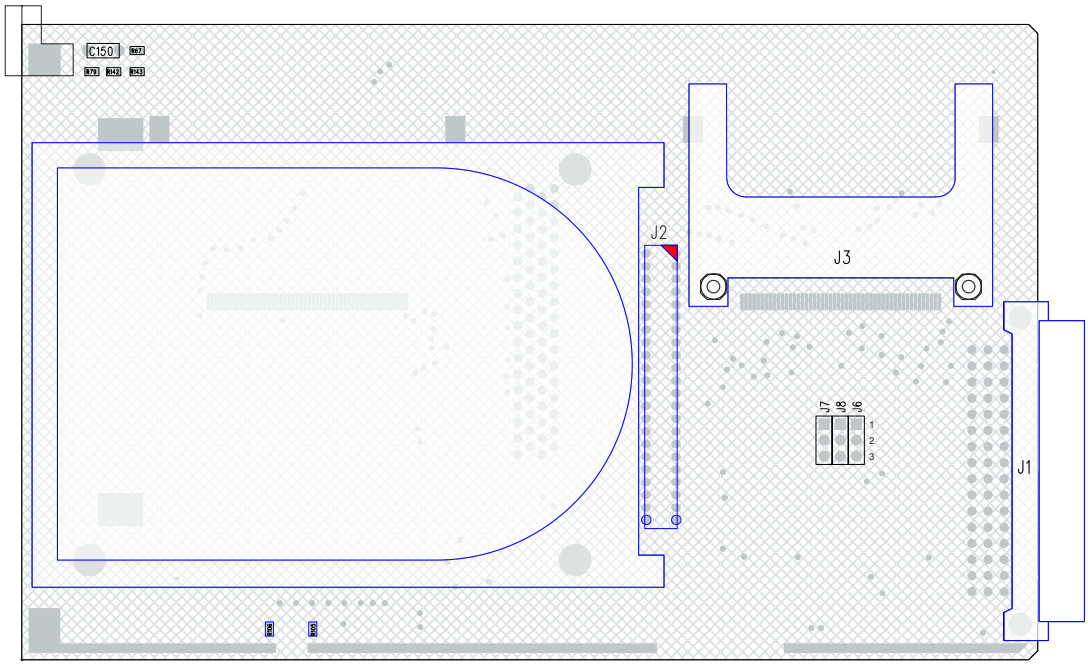


Table B1.2 IPM-ATA-HD Jumper Description

Compact FLASH or MicroDrive in J3		Jumper J6
Master	Slave	
X	-	2-3
-	X	Open
-	-	-

It should be noted that the secondary IDE channel only is available for use by the IPB-ATA-HD (the primary is on the CPU board itself). A Master device must be present either in the form of a hard-disk, Compact FLASH, MicroDrive or CD-ROM etc. Slave only configurations and multi Master configurations are not supported and will not work!

B1.3 IPM-ATA-CF

The IPM-ATA-CF has provision for one or two standard Compact FLASH or MicroDrive devices. Figure B1.3 illustrates the significant connectors for this device while Table B1.3 indicates the jumper settings for the various Master/Slave device configurations.

Figure B1.3 IPM-ATA-CF Board Layout

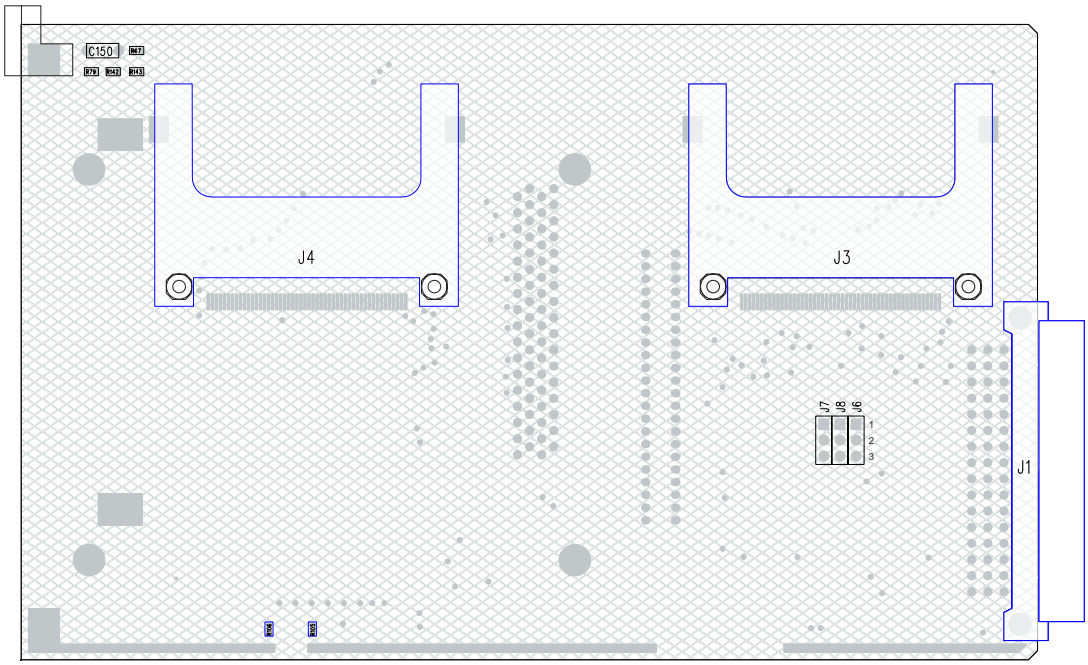


Table B1.3 IPM-ATA-CF Jumper Description

Compact FLASH or MicroDrive in J3		Jumper J6
Master	Slave	
X	-	2-3
-	X	Open
-	-	-

Compact FLASH or MicroDrive in J4		Jumper J7
Master	Slave	
X	-	2-3
-	X	Open
-	-	-

It should be noted that the secondary IDE channel only is available for use by the IPB-ATA-CF (the primary is on the CPU board itself). A Master device must be present either in the form of an external hard-disk, Compact FLASH, MicroDrive or CD-ROM etc. Slave only configurations and multi Master configurations are not supported and will not work!

B1.4 IPM-ATA-PCMCIA

The IPM-ATA-PCMCIA has provision for one standard ATA PCMCIA device and one Compact FLASH or MicroDrive site. Figure B1.4 illustrates the significant connectors for this device while Table B1.4 indicates the jumper settings for the various Master/Slave device configurations.

Figure B1.4 IPM-ATA-PCMCIA Board Layout

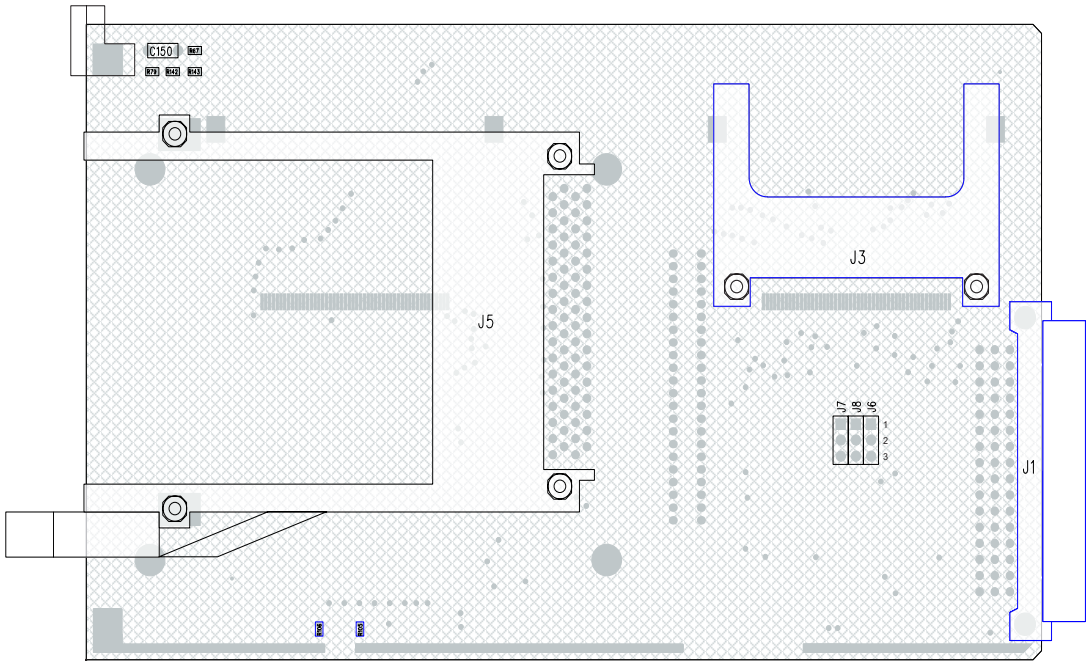


Table B1.4 IPM-ATA-PCMCIA Jumper Description

PCMCIA Device in J5		Jumper J8
Master	Slave	
X	-	2-3
-	X	Open
-	-	-

Compact FLASH or MicroDrive in J3		Jumper J6
Master	Slave	
X	-	2-3
-	X	Open
-	-	-

It should be noted that the secondary IDE channel only is available for use by the IPB-ATA-PCMCIA (the primary is on the CPU board itself). A Master device must be present either in the form of an external hard-disk, PCMCIA device, Compact FLASH, MicroDrive or CD-ROM etc. Slave only configurations and multi Master configurations are not supported and will not work!

B1.5 Device Compatibility

Because of the diversity of Compact FLASH devices available with different architectures and error recovery routines etc. there is a strong possibility that some Master / Slave combinations will fail to be recognised by the BIOS. To help highlight the problem, Inova have provided the test report shown in Table B1.5 which should be regarded as a guide when choosing to pick-and-mix devices. Should devices other than those from the manufacturers indicated in the table be chosen, then it may be prudent that Inova be contacted prior to commissioning.

Table B1.5 Compatibility List

Test	Position	Compact FLASH Card	Jumper	Result
1	J3	IBM Microdrive DMDM-10340	Master	Windows NT4.0 Passed
	J4	Empty	-	
2	J3	M-Systems 64MByte Compact FLASH	Master	Windows NT4.0 Passed
	J4	Empty	-	
3	J3	IBM Microdrive DMDM-10340	Slave	Windows NT4.0 Passed (incl. Strip Set Config.)
	J4	IBM Microdrive DMDM-10340	Master	
4	J3	IBM Microdrive DMDM-10340	Slave	Windows NT4.0 Passed
	J4	M-Systems 64MByte Compact FLASH	Master	
5	J3	IBM Microdrive DMDM-10340	Master	Failed: M-Systems not detected in BIOS
	J4	M-Systems 64MByte Compact FLASH	Slave	
6	J3	M-Systems 64MByte Compact FLASH	Master	Windows NT4.0 Passed
	J4	IBM Microdrive DMDM-10340	Slave	

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CompactPCI®

IPB-FPE12

IPB-FPE12 Contents

C

C1 IPB-FPE12 CPU Extension

The Inova IPB-FPE12 adds LPT and COM2 functionality to any Inova CPU. The piggyback is available as a stand-alone device with its own 4HP front-panel or integrated within a 12HP K6 or PPC front-panel. The information documented here is valid regardless of the connection choice.

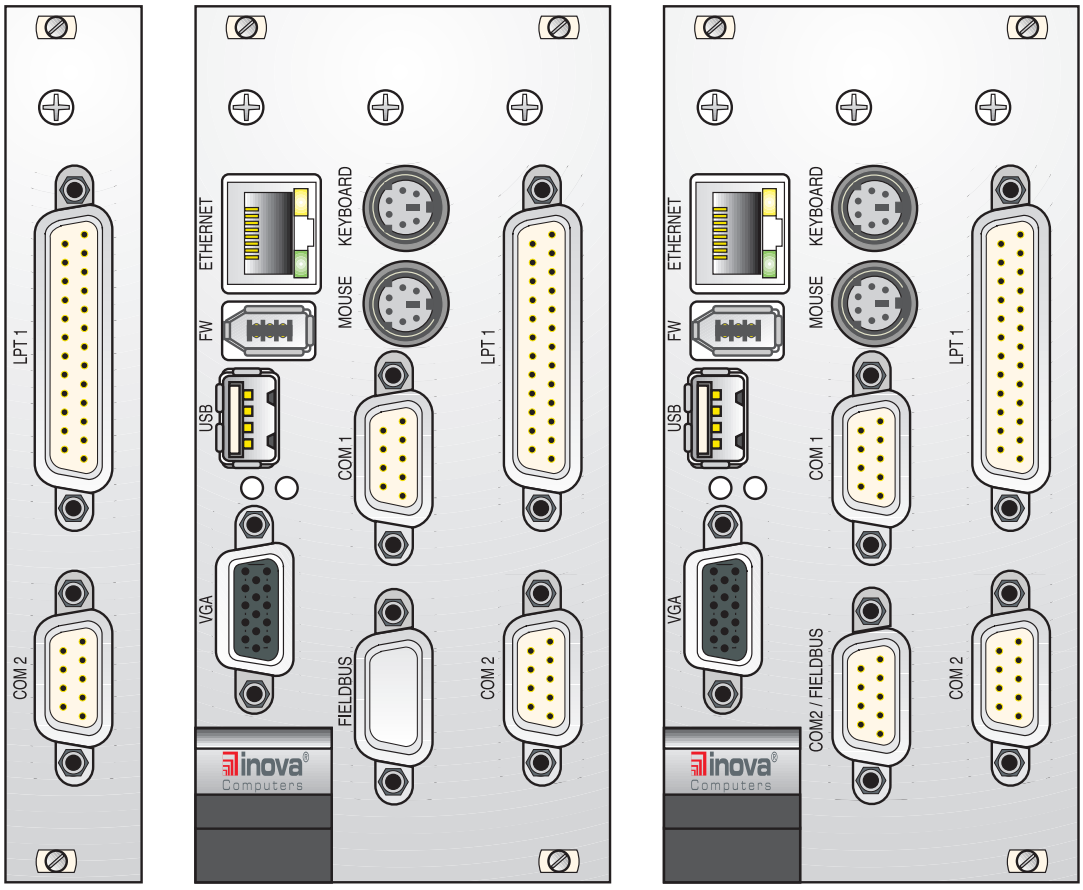
C1.1 J13 Interface for LPT1 & COM2

The control of the LPT and COM2 interfaces is performed through the J13 connector on the CPU base board. The location of this connector may be determined by referring to Section 1 - Product Overview of the CPU User's Manual. A flex cable from J13 connects to the interface board discussed in this section.

C1.2 IPB-FPE12 & Front-panel (4HP or 12HP)

The Inova IPB-FPE12 interface is a small piggyback available as a stand-alone device with its own 4HP front-panel or integrated with the CPU as in figure C1.2.

Figure C1.2 IPB-FPE12 Stand-Alone or Integrated with CPU

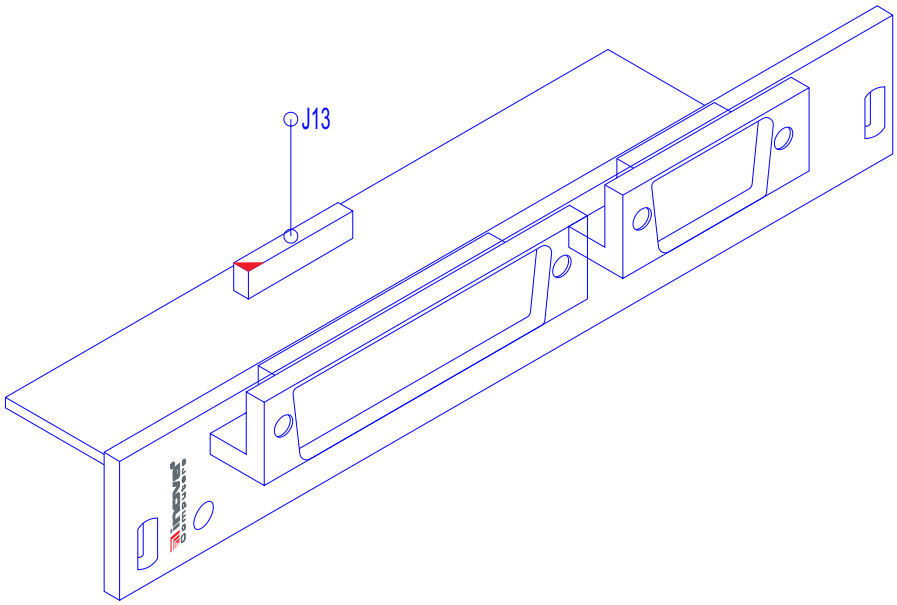


C1.3 LPT1 & COM2 Piggyback

Figure C1.3 illustrates the construction of the stand-alone IPB-FPE12 piggyback and the upperside location of the J13 connector. The same mechanical construction applies to the integrated version. Care should be taken to ensure that pin 1 of J13 on the CPU base board is linked by an appropriate length of flex cable to pin 1 on the piggyback. To help with the orientation, the connector flanks that are blue indicate the blue face of the flex-cable. Unmarked flanks indicate the metallic connection of the flex-cable. Also, pin 1 has been highlighted by a red triangle.

> ***Note:***
> ***Damage to the CPU board or the piggyback may result if the flex cable is positioned incorrectly. Inova will not accept responsibility for negligent actions!***

Figure C1.3 LPT1 & COM2 Piggyback Board IPB-FPE12



> ***Note:***
> ***The physical connection of the IPB-FPE12 is electrically identical regardless of the nature of connection (stand-alone or integrated!)***

Table C1.3 IPB-FPE12 Connector Description

Connector	Description
J13	LPT1 & COM2

Note:

Other Inova piggybacks (ICP-HD-1 & ICP-HDE8) provide J13a to "daisy-chain" the LPT1 / COM2 interfaces. If these connectors are used for the integration of the IPB-FPE12 then the COM2 port on these piggybacks is disabled.

C1.4 LPT1 Interface

A front-panel with LPT1 and COM2 interfaces is either integrated into a 12HP standard CPU front-panel or available as a separate 4HP unit. The piggyback located behind these interfaces connects to the CPU-mounted J13 connector.

Figure C1.6 LPT1 Interface Pinout

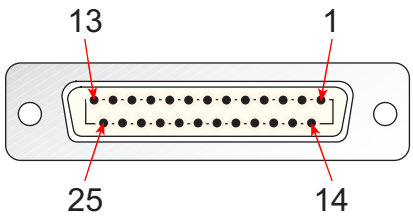


Table C1.6 LPT1 Connector Signals

Pin No.	Signal	Pin No.	Signal
1	STROBE	2	PD0
3	PD1	4	PD2
5	PD3	6	PD4
7	PD5	8	PD6
9	PD7	10	ACK
11	BUSY	12	PE
13	SLCT	14	AUTOED
15	ERROR	16	INIT
17	SLCTIN	18-25	GND

C1.5 COM2 Interface

The COM2 port features a complete set of handshaking and modem control signals, maskable interrupt generation and high-speed data transfer rates. A front-panel with LPT1 and COM2 interfaces is either integrated into a 12HP standard CPU front-panel or available as a separate 4HP unit. The piggyback located behind these interfaces connects to the CPU-mounted J13 connector.

Figure C1.5 COM2 Interface Pinout

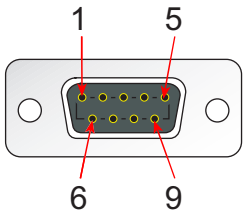


Table C1.5 COM2 Connector Signals

Pin No.	Signal	
	RS232	RS485
1	DCD	
2	RxD	RxD, TxD +
3	TxD	RxD, TxD -
4	DTR	
5	GND	
6	DSR	
7	RTS	
8	CTS	
9	RI	

Note:

The standard piggyback configuration has COM2 set for RS232 communication.

However, this device can be configured to observe a two-wire non galvanically separated RS485 protocol. The data direction is governed by controlling the UART's RTS signal. Writing a hex value of 0B to this register allows data to be transmitted. Writing 1B to this register configures the device to receive data.

CompactPCI®

IPB-RIO

IPB-RIO Contents

D

D1 IPB-RIO CPU Extension

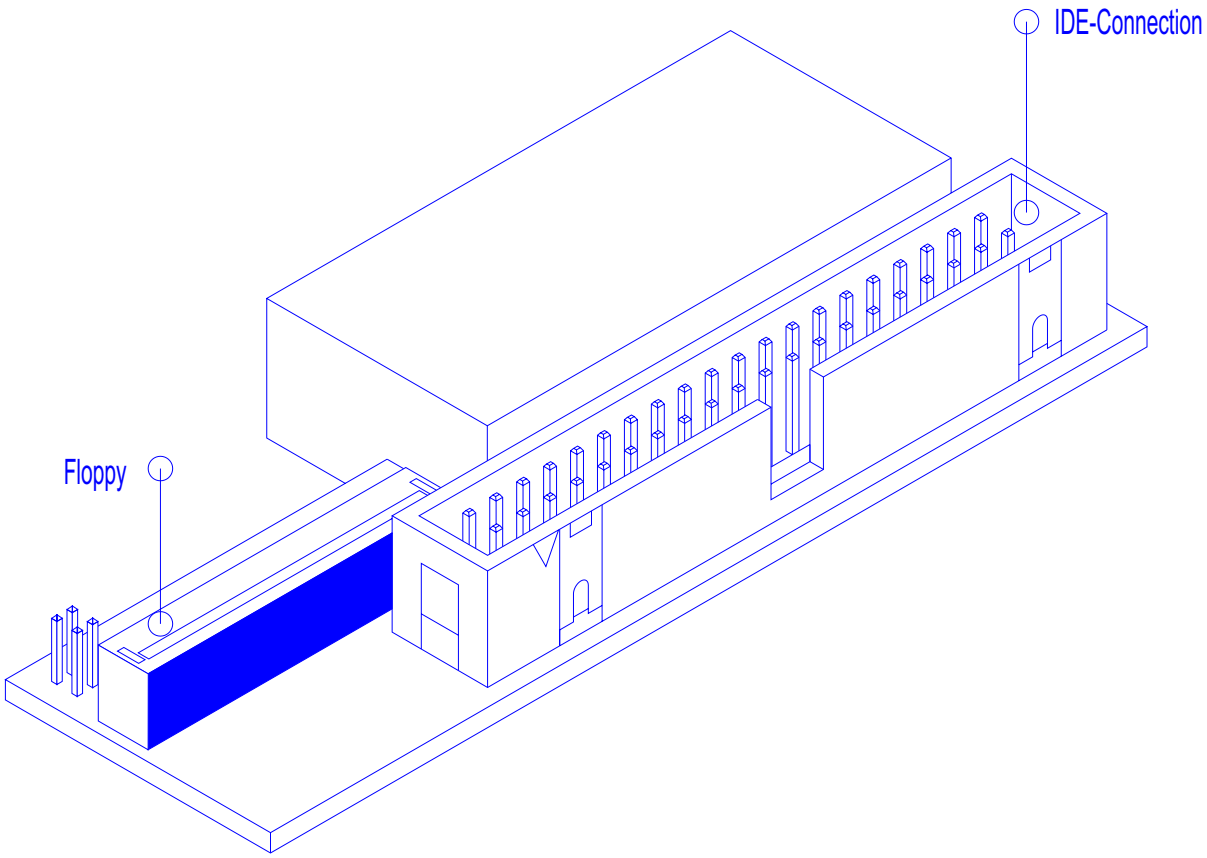
To enhance the I/O and serviceability of their CPUs, Inova have introduced rear I/O modules that connect to a CompactPCI connector on the rear of the Master Slot on the backplane. All standard Inova backplanes are equipped with this R2 connector so that even if the rear I/O functionality is not requested at time of order, it can be implemented at a later stage.

Currently, Inova have 4 rear I/O transition modules in their product range. Three of these are documented here.

D1.1 IPB-RIO-HD-FD

As its name suggests, this transition module recovers the embedded IDE and floppy signals from the CompactPCI backplane and presents them in a form ready for device connection. One of the advantages of this module is its ability to attach an IDE device without direct flex-cable connection to the CPU base board. This facilitates servicing and allows a CPU for example, to be switched without touching the software stored on the HD. Likewise, a hard-disk can be exchanged without having to disassemble the CPU!

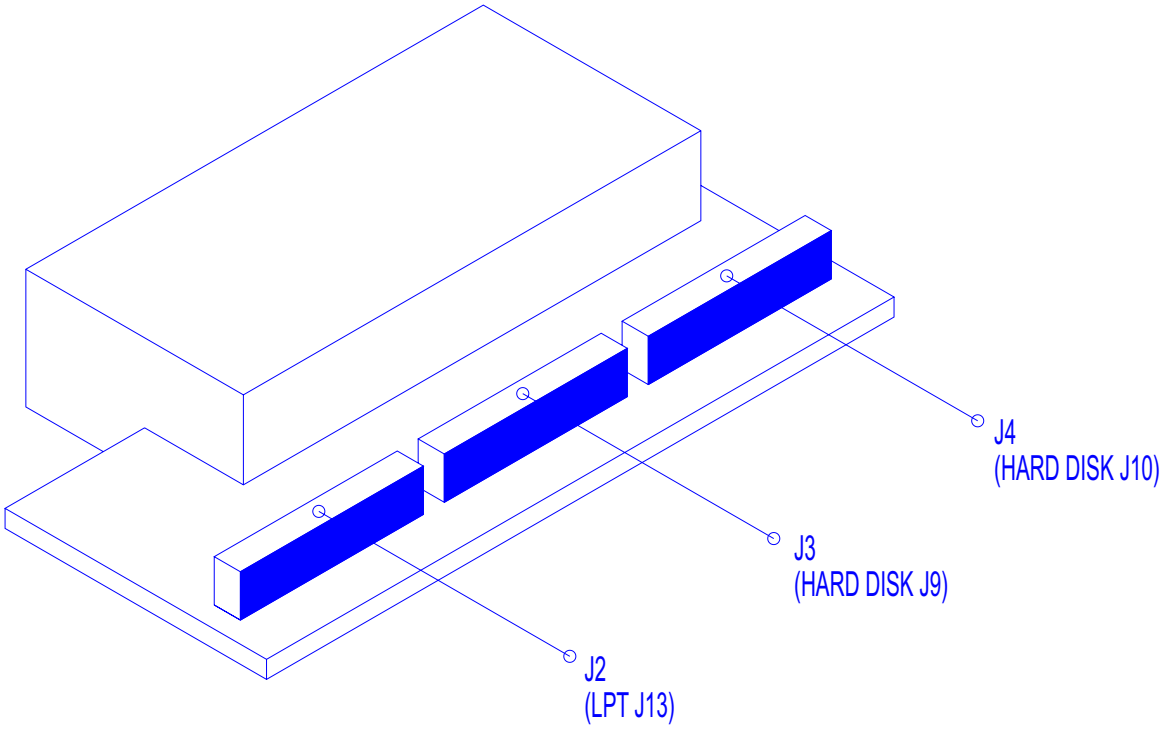
Figure D1.1 IPB-RIO-HD-FD



D1.2 IPB-RIO-HD-LPT-(FLEX)

Similar to the IPB-RIO-HD-FD, this transition module recovers the embedded IDE and LPT signals from the CompactPCI backplane and presents them in a form ready for device connection. This time, instead of a standard IDE header, the IDE device is connected using the familiar Inova flex cables. Also, a slim-line floppy disk may be attached using a suitable cable to the LPT connector (J13). A switch in BIOS allows the user to 'redefine' the signals!

Figure D1.2 IPB-RIO-HD-LPT-(FLEX)



Note:

If the LPT device is connected to this transition module then a connection cannot be made to the CPU base board. Doing so could render the hardware useless or cause any data communication to fail.

D

D1.3 IPB-RIO-C-SHORT

All Inova -RIO(C) compatible CPUs can take advantage of this transition module as it allows the signals shown in table D1.3 to be recovered (used). Figure D1.3 illustrates this piggyback and points to the available interfaces.

Figure D1.3 IPB-RIO-C-SHORT

Table D1.3 Rear I/O Type 'C'

REAR I/O OPTION	Rear I/O - 'C'
ETHERNET	Second Channel*
USB	Second Channel
FireWire	Second Channel
LPT 1 / FD	Yes
SPEAKER	Yes
EIDE	Yes

Note:

The Inova PIII CPU can have both Ethernet channels routed to the front-panel. Utilising the rear I/O option while communicating via the second Ethernet channel on the front-panel will result in data conflict.

D1.4 IPB-RIO-C-80MM

Similar to the -SHORT version, this transition module extends the signals shown in table D1.3 to a rear panel. Naturally, not all enclosures are suitable for this type of connection and the following must be considered.

- Inova Desktop systems have an integrated fan - will the transition module interfere with it?
- 84HP Inova *CoolBreeze* systems are too short to accept an 80mm transition module.
- Inova Industrial enclosures are available in 2 standard configurations:
  - Wall Mounting
  - Rack Mounting
- Wall mounted racks are not suitable for rear I/O
- The Inova rack mounted industrial enclosure must be delivered without rear panelling as the position of the transition module will vary depending on the chosen enclosure and backplane.

Figure D1.4 IPB-RIO-C-80MM

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