Intel® 21143 PCI/CardBus 10/100Mb/s Ethernet LAN Controller

Design Guide

July 2002

Order Number: 278588-001

Contents

Figures

Tables

Revision History

Date	Revision	Description
July 2002	001	First release.

This design guide provides a description of how to implement 100BASE-TX and 10BASE-T network connections using the 21143 PCI/CardBus 10/100 Mb/s Ethernet LAN Controller (referred to as the 21143).

While this document will not provide specific recommendations for physical layer devices, it will provide design recommendations and layout recommendations.

This application note provides a description of how to implement 100BASE-TX and 10BASE-T network connections using the 21143 PCI/CardBus 10/100 Mbs/s Ethernet LAN Controller (referred to as the 21143).

1.0 Functional Overview

This section provides an overview of the 21143 and the implementation of 100 Mb/s and 10 Mb/s network connections using MII-based or SYM-based PHY devices.

1.1 21143 Overview

The 21143 is a single-chip bus master Ethernet/Fast Ethernet device that supports direct memory access (DMA) and has direct interfaces to both the CardBus and the PCI local bus. The 21143 implements a direct interface to the CardBus or PCI bus through a single 50-pin connection, which consists of the control and address/data signals.

The 21143 provides a complete implementation of the IEEE 802.3 Ethernet specification. This includes the attachment unit interface (AUI), twisted-pair (10BASE-T) interface, MII SYM port interface, and the interface through the media access control (MAC) layer that creates a direct interface to the PCI bus.

The PCI interface utilizes only about 10% of the bus bandwidth during fully networked operation for 100 Mb/s Fast Ethernet reception or transmission. This bus master design results in high throughput between the system and the network.

1.2 Network Interface

The 21143 physical layer design supports AUI drop cable Ethernet and 10BASE-T twisted-pair (TP) Ethernet connections. The 21143 **gep<0>/aui_bnc** (pin 100), which is software controlled, provides for a connection of either the AUI (10BASE5) or BNC (10BASE2) network connector. Table 1 describes the function of this pin.

Table 1. Signal gep<0>/aui_bnc Description

Program State	Function
0	AUI port enabled; BNC port disabled.
1	BNC transceiver (or DC-to-DC converter) enabled; AUI port disabled

AUI signals interface with the Manchester encoder/decoder portion of the 21143. The 21143 supports 10BASE5 thickwire and 10BASE2 ThinWire connections. The 10BASE2 connection requires an external transceiver.

The 21143 implements the 100BASE-T MII layer and the 100/10 Mb/s Ethernet MAC layer. The 21143 provides a dual network interface for both a 100BASE-T and a 10 Mb/s Ethernet. At the 100BASE-T port, the 21143 supports the industry-standard MII for any 100BASE-T implementation.

The 21143 is fully compliant with the MII specifications (as defined in IEEE 802.3). The MII is a nibblewide, general interface, that can be used with various physical interfaces, such as 100BASE-TX, 100BASE-T4, shielded twisted-pair (STP), and fiber. It also supports dual rates of speed (10 Mb/s and 100 Mb/s).

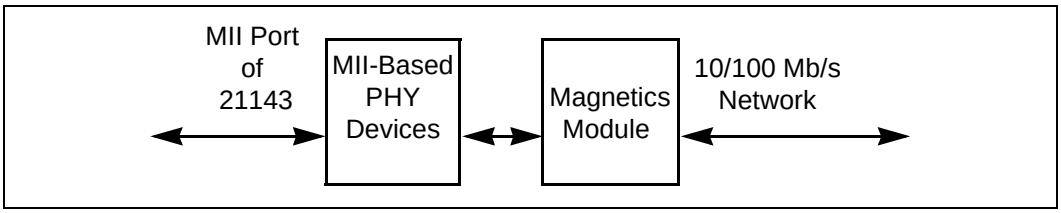
The 21143 includes special support for 100BASE-TX networks by including the PCS section (scrambler and 5B/4B coding/decoding). Integrating the 10BASE-T ENDEC with the 100 Mb/s-only SYM-based PHYs enables full support for a 10/100-implementation.

1.3 MII-Based PHY Block Diagram

Figure 1 is a block diagram of a 10BASE-T and 100BASE-T single-connector network connection using a MII-based PHY device with the 21143.

MII-based PHY devices are provided by Intel, Integrated Circuit Systems*, National Semiconductor*, Seeq*, and TDK*.

Figure 1. MII-Based PHY Design



The MII-based PHY design includes the following components:

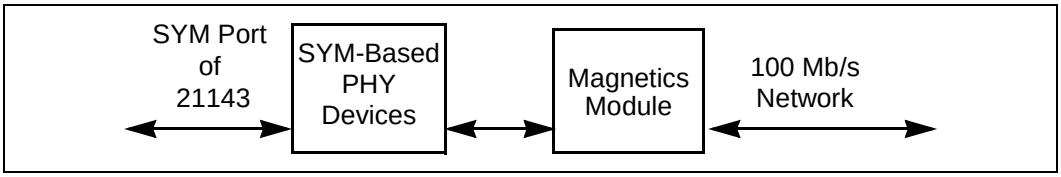
- The MII-based PHY devices, which have a direct interface to the MII port of the 21143 with dual-rate option (as specified in the MII specification) and a full interface to the 10/100 Mb/s magnetics module.
- The magnetics module, which is based on transformers and serial chokes enabling the network connection to the 100 Mb/s network (100BASE-TX or 100BASE-T4) and to the 10 Mb/s network (10BASE-T).

1.4 SYM-Based PHY Block Diagram

Figure 2 is a block diagram of a 100BASE-TX single-connector network connection using a SYM-based PHY device with the 21143. For a 10 Mb/s network connection, the network can be connected directly to the 21143 through filters and chokes.

SYM-based PHY devices are provided by GEC Plessey*, Quality Semiconductor*, and Micro Linear*.

Figure 2. SYM-Based PHY Design



The SYM-based PHY design includes the following components:

- The SYM-based PHY devices, which have a direct interface to the SYM port of the 21143 with an interface to the 100 Mb/s magnetics module.
- The magnetics module, which is based on transformers and serial chokes enabling the network connection to the 100 Mb/s-only network (100BASE-TX or 100BASE-T4).

2.0 21143 Ports

Table 2 lists the active AUI signals when the 21143 AUI port is selected.

Table 2. AUI Signals

Signal	Pin Number
aui_cd–	138
aui_cd+	137
aui_rd–	140
aui_rd+	139
aui_td–	143
aui_td+	142

Table 3 lists the active twisted-pair signals when the 21143 10BASE-T port is selected.

Table 3. Twisted-Pair Signals

Signal	Pin Number
tp_rd–	10
tp_rd+	9
tp_td–	5
tp_td– –	4
tp_td+	6
tp_td+ +	7

Table 4 lists the active MII signals when the 21143 MII port is selected.

Table 4. MII Signals

Signal	Pin Number
mii_clsn	118
mii_crs	117
mii_dv	129
mii_mdc	134
mii_mdio	135
mii_rclk	128
mii_rx_err	127
mii_rxd <3:0>	133:130
mii_tclk	124
mii_txd<3:0>	119:122
mii_txen	123

Table 5 lists the active SYM signals when the 21143 SYM port is selected.

Table 5. SYM Signals

Signal	Pin Number
sd	117
sel10_100	127
sym_rclk	128
sym_rxd<0>	130
sym_rxd<1>	131
sym_rxd<2>	132
sym_rxd<3>	133
sym_rxd<4>	118
sym_tclk	124
sym_txd<0>	122
sym_txd<1>	121
sym_txd<2>	120
sym_txd<3>	119
sym_txd<4>	123

3.0 Network Connection

The network connections of the 21143 can be used in 10BASE-T, AUI, MII, or SYM configurations. Different methods are used to connect each port to the actual cable connector.

3.1 10BASE-T Twisted-Pair Network Port

Figure 3, Figure 4, and Figure 5 show the network connection design options for 10BASE-T type implementations.

Figure 3 and Figure 4 show two ways of connecting the 10BASE-T network by using a standard 1:1 transformer module. This implementation type requires a swing compensator (to swing the 21143 output from 3.3 V to 5 V) to meet the standard requirements.

Figure 5 shows a direct connection to a $1:\sqrt{2}$ transformer module. This implementation type provides the lowest component count for 10BASE-T. The filter and transformer components minimize any potential electromagnetic interference and radio frequency interface problems.

Common-mode noise (when noise between two lines of the same polarity *add* rather than cancel) can radiate energy from the twisted-pair interface. Also, significant common-mode power supply noise can be generated on the board or adapter by other devices. Therefore, Intel recommends the use of filter and transformer modules that incorporate common-mode chokes.

Table 8 and Table 10 list the part numbers for each implementation. Figure 3 shows the 10BASE-T network connection with buffers. The required components for this configuration are as follows:

- Voltage swing compensator — 74ACT244
- Terminating and decoupling components
- Filter transformer and common-mode chokes
- RJ45 connector

Figure 3. 10BASE-T Network Connection with Buffers

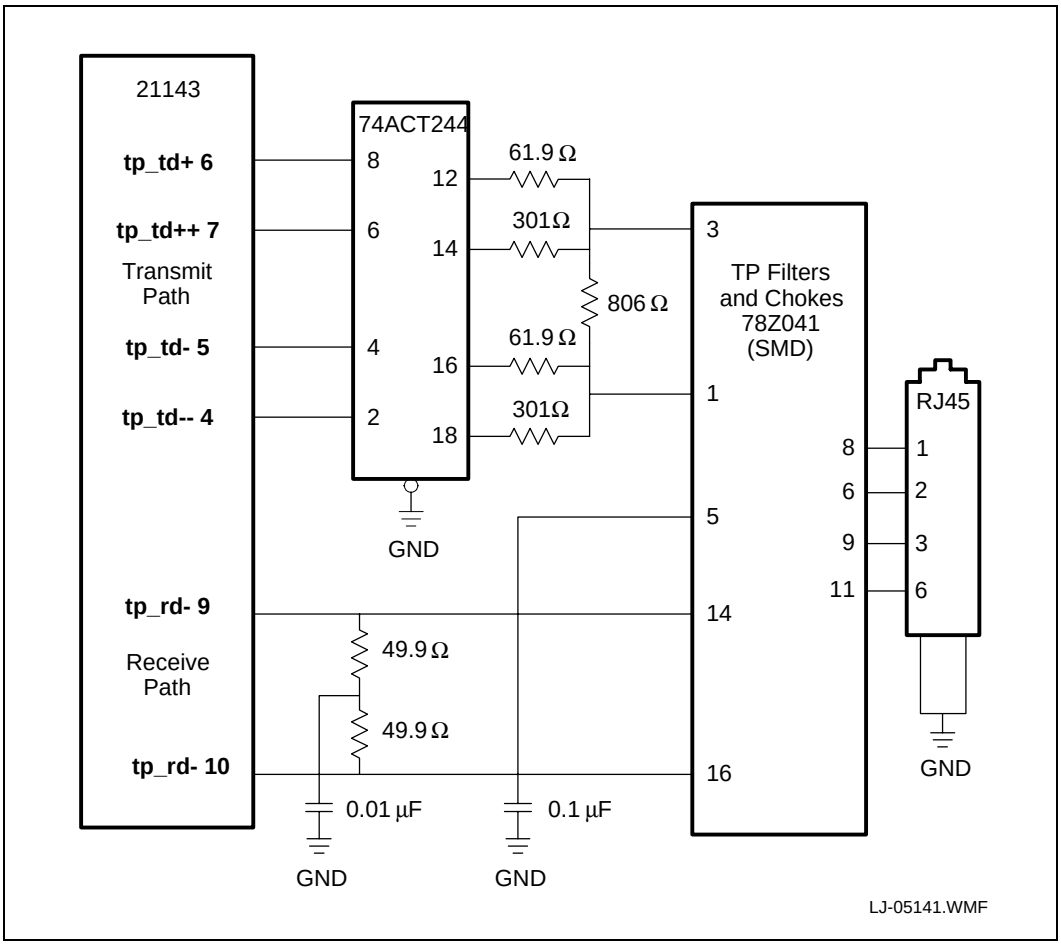


Figure 4 shows the 10BASE-T network connection without buffers. The required components for this configuration are as follows:

- Terminating and decoupling components
- Transformer module (ratio of $1:\sqrt{2}$ for swing compensation)
- Filter transformer and common-mode chokes
- RJ45 connector

Figure 4. 10BASE-T Network Connection Without Buffers

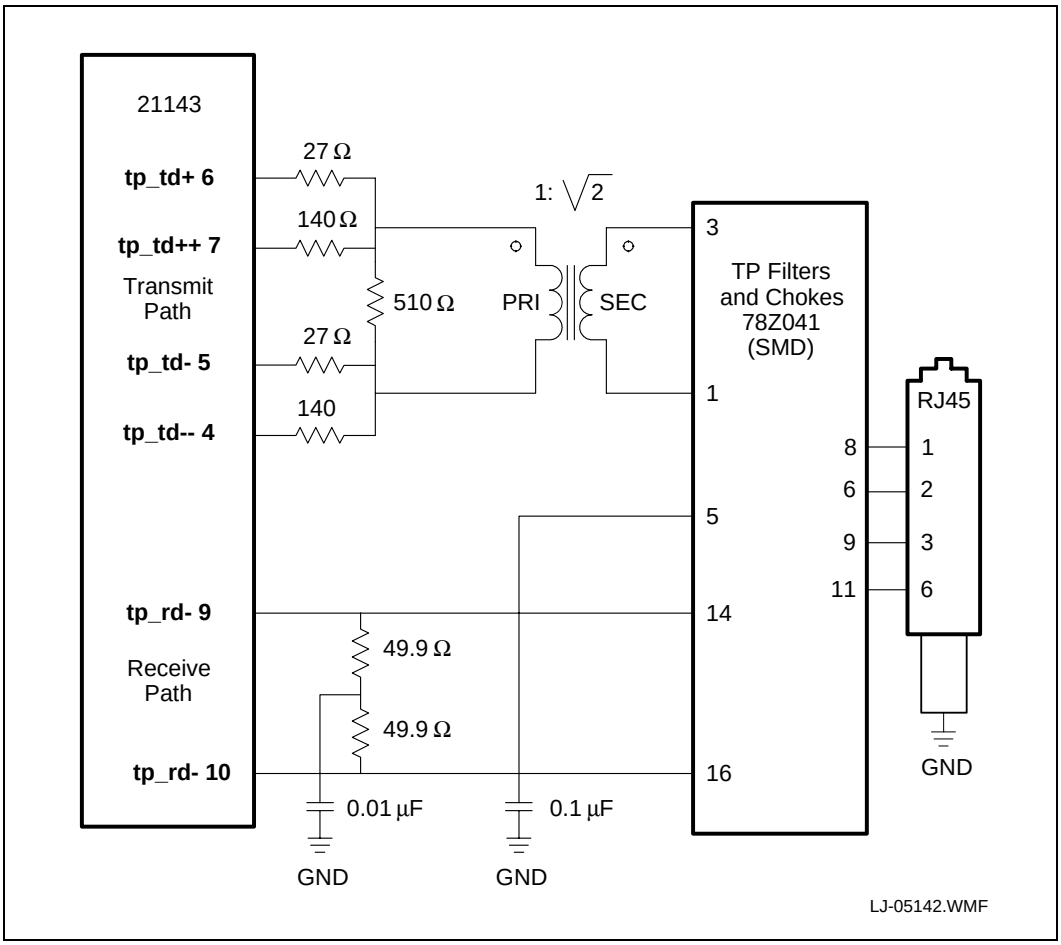
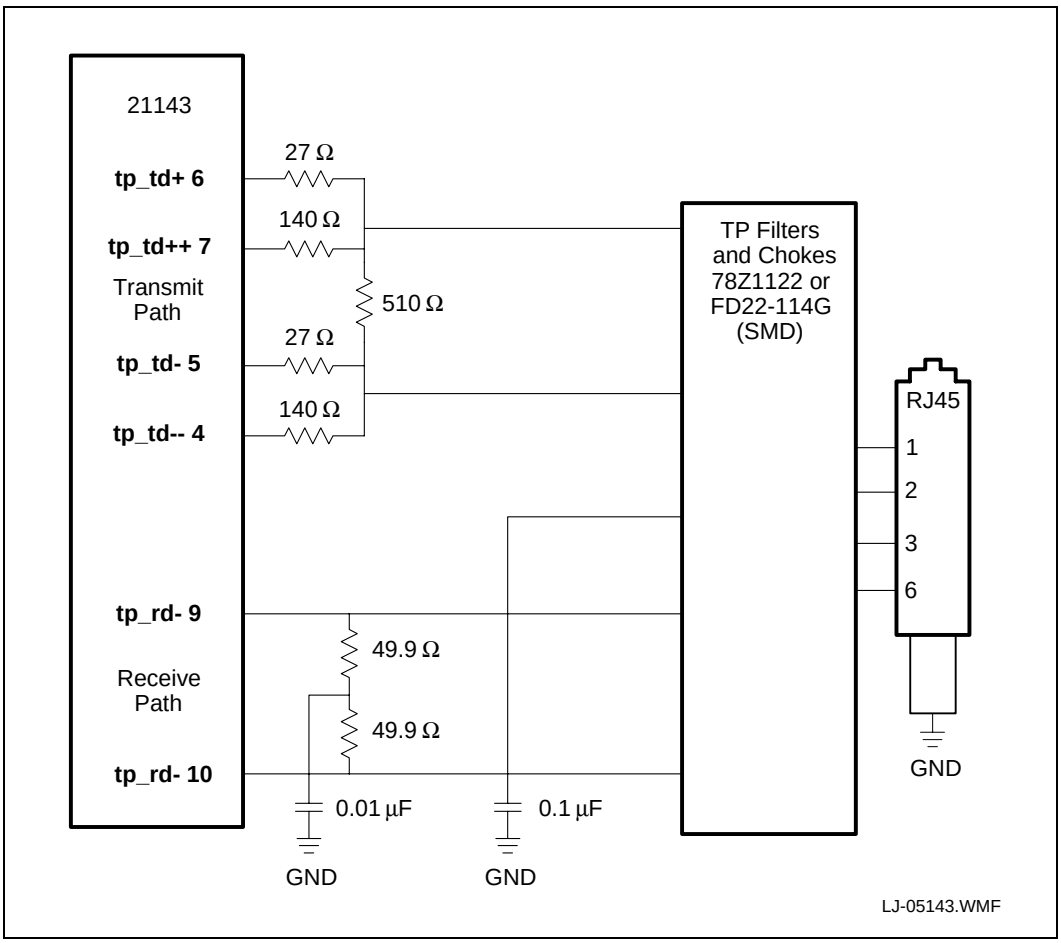


Figure 5 shows the minimum component requirement for the 10BASE-T network connection. This implementation uses a filter transformer module with a 1:$\sqrt{2}$ transformer on the transmit path to compensate for the voltage swing. The required components for this configuration are as follows:

- Terminating and decoupling components
- Filter, transformer, and common-mode chokes
- RJ45 connector

Figure 5. Minimum Components Required for 10BASE-T



3.2 100-Ready Designs

The 21143 can also be designed for systems that are “100-Ready.” The term “100-Ready” implies a system that has a 10 Mb/s network that can easily be upgraded to become a 10/100 Mb/s network. There are two methods for providing 100-Ready designs:

- Provide a connector for an internal optional daughtercard.
- Provide an MII connector for an external module that connects to the MII/SYM port.

These two methods are described in Table 6.

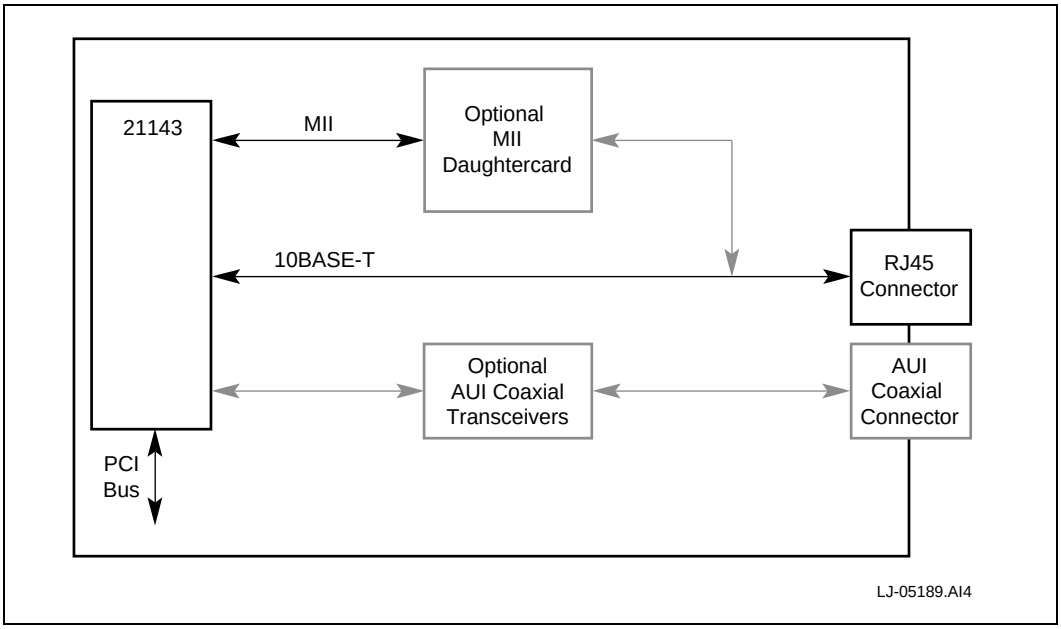
Table 6. Internal vs. External Design Features

Design	Features
Internal optional daughtercard	• Can be designed with an MII or any custom connector. • User opens cabinet to install 100 Mb/s daughtercard.
External MII/SYM module	• User connects module to external MII/SYM connector; user does not have to open cabinet for installation.

3.2.1 Internal Optional Daughtercard

Figure 6 shows a block diagram of a 100-Ready design using a daughter card.

Figure 6. 10BASE-T 100-Ready Daughtercard Block Diagram



3.2.2 Description of 100-Ready Daughtercard Block Diagram

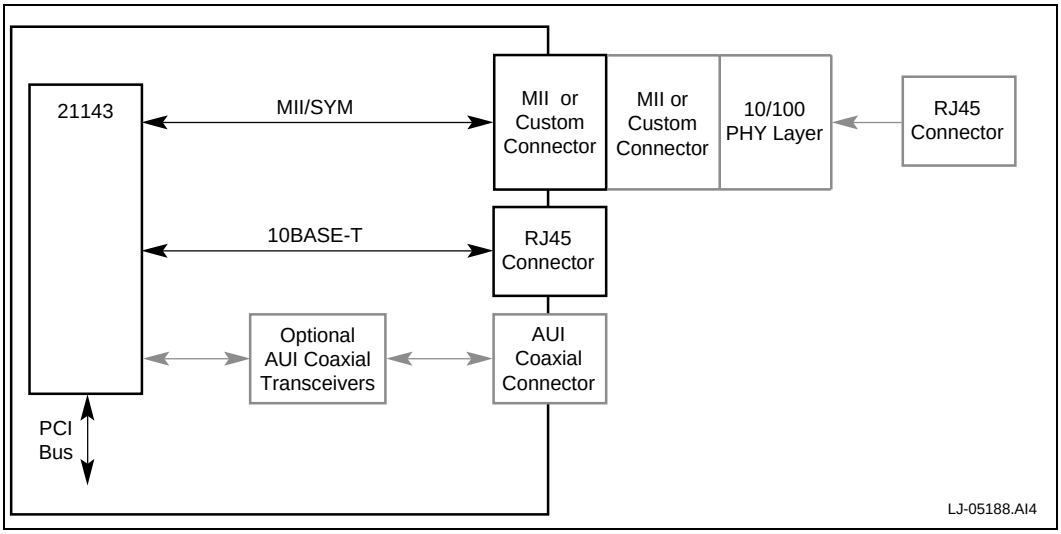
The blocks in the10BASE-T 100-Ready block diagram represent the following components:

- 21143 — A 21143 with all of the external components for operating the network connection (reference parts, XTAL, and so on). The 21143 can use the PCI bus, and the MII/SYM, 10BASE-T, and AUI coaxial ports for communication.
- Optional MII/SYM daughtercard — A daughtercard with a 100 Mb/s or 10/100 Mb/s PHY that interfaces with an MII connector or custom connector. The daughtercard can be designed to use the same RJ45 connector.
- RJ45 — A network connection.

3.2.3 100-Ready External Module Design

Figure 7 shows a block diagram of a 100-Ready design using an external module.

Figure 7. 10BASE-T 100-Ready External Module Block Diagram



3.2.4 Description of 100-Ready External Module Block Diagram

The blocks in the100-Ready external module block diagram represent the following components:

- 21143 — A 21143 with all of the external components for operating the network connection (reference parts, XTAL, and so on). The 21143 can use the PCI bus, and the MII/SYM, 10BASE-T, and AUI coaxial ports for communication.
- Optional external MII/SYM daughtercard — A daughtercard with a 100 Mb/s or 10/100 Mb/s PHY that interfaces with an MII connector or custom connector. The daughtercard uses the magnetics to connect to the RJ45 connector.
- MII connector — An MII or custom connector that connects with the MII/SYM port of the 21143.
- RJ45 — A network connection.

3.2.5 MII/SYM Pin Listing

Table 7 describes the MII/SYM pin multiplexing enabling the full flexibility for both network connections options using the same internal connector for the MII-based or the SYM-based PHY device (for detailed implementation notes, refer to the specific PHY device section in this document).

Table 7. MII/SYM Pinout (Sheet 1 of 2)

Pin Number	MII Interface Function	SYM Interface Function
117	**mii_crs**	**sd**
118	**mii_clsn**	**sym_rxd<4>**
119	**mi_txd<3>**	**sym_txd<3>**
120	**mi_txd<2>**	**sym_txd<2>**
121	**mi_txd<1>**	**sym_txd<1>**

Table 7. MII/SYM Pinout (Sheet 2 of 2)

Pin Number	MII Interface Function	SYM Interface Function
122	**mii_txd<0>**	**sym_txd<0>**
123	**mii_txen**	**sym_txd<4>**
124	**mii_tclk**	**sym_tclk**
127	**mii_rx_err**	**sel10_100**
128	**mii_rclk**	**mii_rclk**
129	**mii_dv**	N.C.
130	**mii_rxd<0>**	**sym_rxd<0>**
131	**mii_rxd<1>**	**sym_rxd<1>**
132	**mii_rxd<2>**	**sym_rxd<2>**
133	**mii_rxd<3>**	**sym_rxd<3>**
134	**mii_mdc**	N.C.
135	**mii_mdio**	N.C.

3.3 AUI Network Port

The 21143 is fully compliant with the AUI standard. The AUI can interface with an external medium-attachment unit (MAU) and connect to alternate media, such as 10BASE2 (ThinWire) and 10BASE5 (thickwire). Figure 8 and Figure 9 show the required connections.

Figure 8 shows the AUI 10BASE5 network connection and the pin connections between the 21143 and the isolation transformer. The required components for this configuration are as follows:

- Terminating and decoupling components
- Isolation transformer
- AUI connector

Figure 8. AUI 10BASE5 Network and Pin Connections

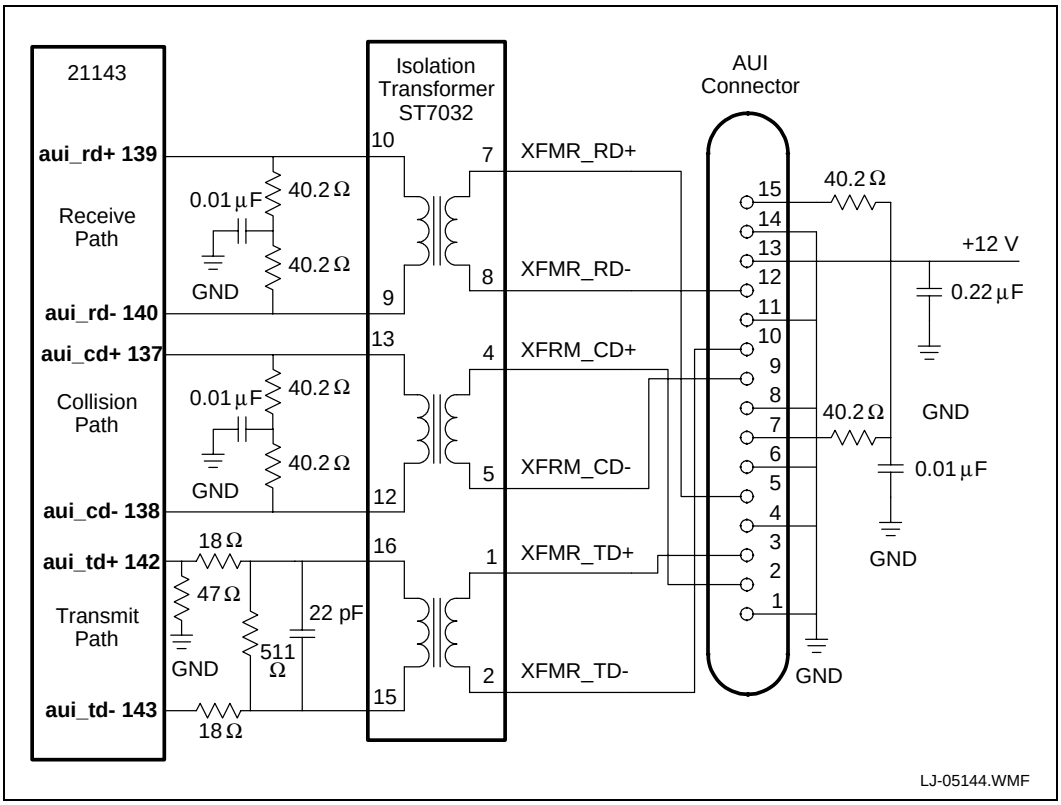
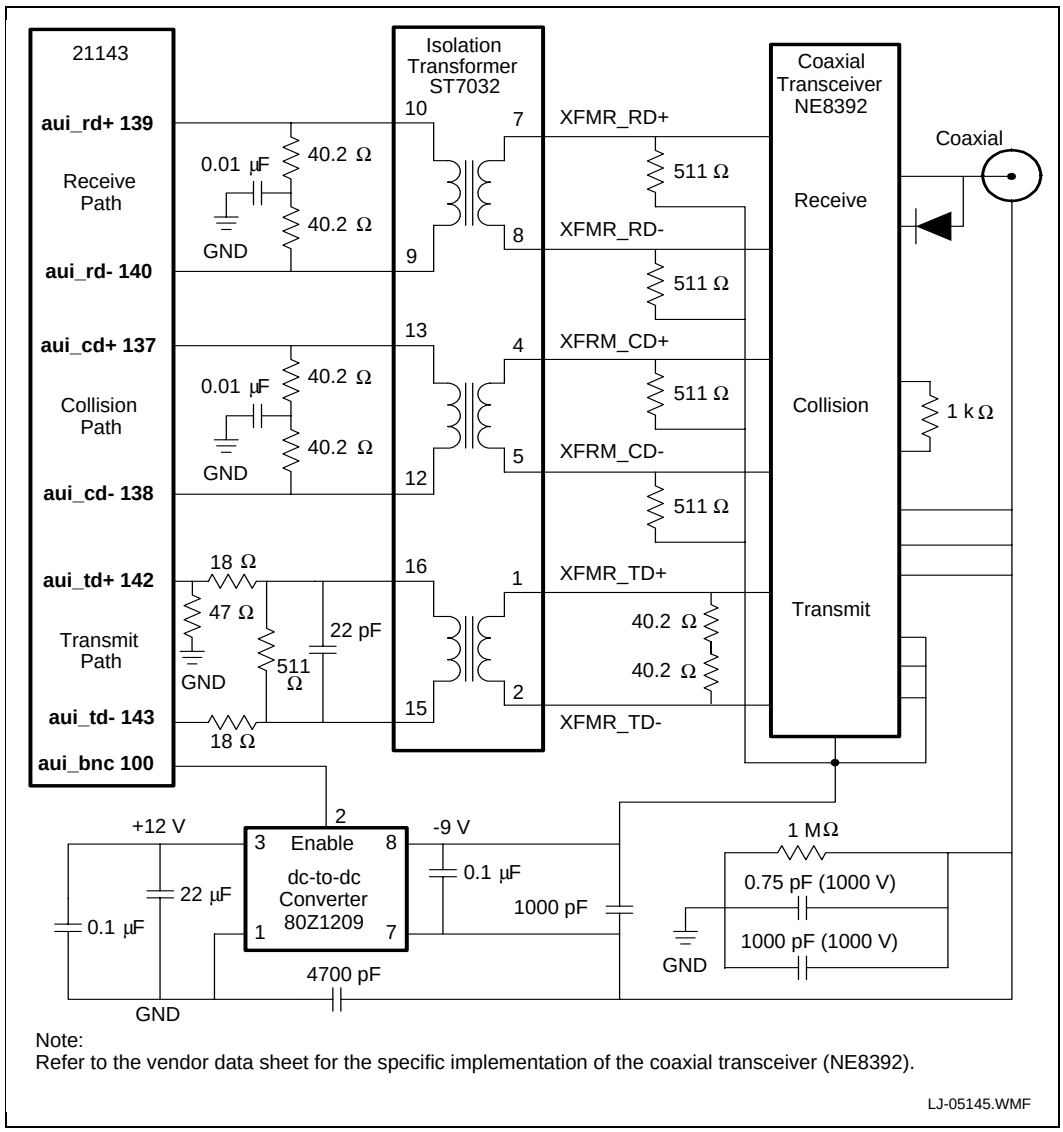


Figure 9 shows the AUI 10BASE2 network connection. In this configuration, the AUI is not externally exposed. The required components for this configuration are as follows:

- Isolation transformer
- Terminating and decoupling components
- DC-to-DC converter
- Coaxial transceiver and BNC connector

Figure 9. AUI 10BASE2 Network Connection



Note:
Refer to the vendor data sheet for the specific implementation of the coaxial transceiver (NE8392).

LJ-05145.WMF

In cases where 10BASE2 MAU is a module separate from the board, MAU can be implemented on a small add-in card. Ensure that the cable used to connect the board to MAU provides adequate shielding of the AUI signals from external noise. This MAU add-in card includes the following components:

- Transceiver chip and BNC connector
- DC-to-DC converter
- Discrete devices

3.4 Media-Specific Components

Table 8 lists the media-specific interface components for 10BASE-T access. Table 10 lists the media-specific interface components for 10BASE2 and 10BASE5 access.

Table 8. 10BASE-T Media-Specific Components

Access Type	Components	Available Part Numbers
10BASE-T	74ACT244 driver	74ACT244 or 74FCT244
	Filter and transformer module	Pulse Engineering* PE65745[1] Valor*PT4096[1] Valor* ST7011[1] Halo* TD42-2006Q[1] Halo* TG42-2006W1[1]
	Transformer filter and chokes	Pulse Engineering* PE65434 Valor* FL1012
	RJ45 wire jack connector	—

1. Surface-mount device.

Table 9. 10BASE2 and 10BASE5 Media-Specific Components

Access Type	Components	Available Part Numbers
10BASE2	DC-to-DC converter	Fil Mag* 80Z1209DSND
	Isolation transformer	Valor* ST7032[1] Pulse Engineering* PE65723[1] Valor* LT6032[1] Valor* ST6032/3[1] Halo* TD01-0756K[1] Halo* TG01-0756W[1]
	Coaxial transceiver	National Semiconductor* DP8392C
	Connector	—
10BASE5	Isolation transformer	Valor* ST7032[1] Pulse Engineering* PE65723[1] Valor* LT6032[1] Valor* ST6032/3[1] Halo* TD01-0756K[1] Halo* TG01-0756W[1]
	AUI connector	—

1. Surface-mount device.

4.0 21143 Requirements

This section provides information about the external component connections for the 21143, and describes the following requirements:

- Unused JTAG port requirements
- Current reference and capacitor input
- Crystal connection or crystal oscillator connection for the serial clock connection

4.1 Unused JTAG Port Requirements

Table 10 describes the 21143 signal pin requirements if you are *not* using the JTAG port.

Table 10. Pin Requirements When Not Using the JTAG Port

Leave the Following JTAG Pins Open	Pull the Following JTAG Pin Up or Down
tms (pin 1)	**tck** (pin 120)
tdi (pin 2)	
tdo (pin 4)	

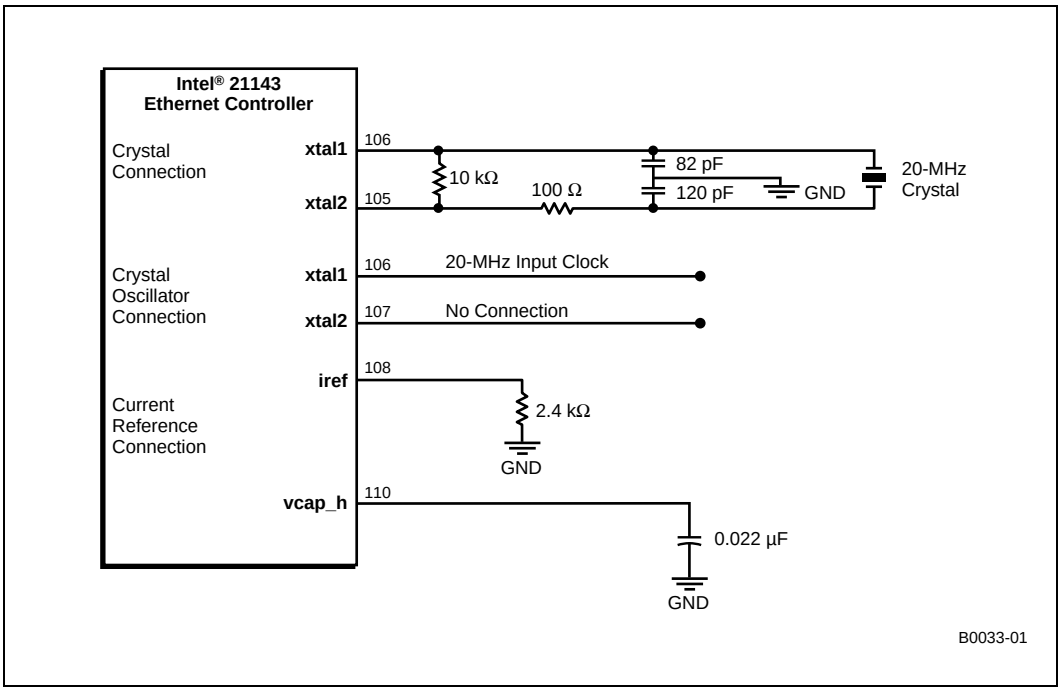
4.2 Current Reference and Capacitor Input Requirements

Table 11 describes the current reference and capacitor input requirements for the 21143, and Figure 10 shows the external component connections.

Table 11. Current Reference and Capacitor Inputs

Pin Name	Pin Number	Function	Connect This Pin...
iref	108	Current reference input for the analog phase-locked loop (PLL)	Through a 2.4 kΩ resistor to ground
vcap_h	110	Capacitor input	Through a 0.022 µF capacitor to ground

Figure 10. 21143 External Component Connections



4.3 Crystal and Crystal Oscillator Connections

Figure 10 shows two serial clock connections; select either the crystal connection or the crystal oscillator connection. According to the IEEE 802.3 standard, a 20 MHz crystal is required. The crystal frequency must not vary by more than 100 parts per million (PPM), or 0.01%. Place the crystal as close as possible to the 21143.

Because the frequency of crystals from different vendors can vary, test the crystals in the actual circuit. It may be necessary to vary the tuning of the surrounding components. However, after the capacitors have been tuned for the specific crystal, the design does not need to be altered on a board-by-board basis.

The 21143 also supports a crystal oscillator (Figure 10). This configuration requires no external component and **xtal2** should be left open.This is useful for applications with multiple network connections.

Table 12 lists the crystal specifications.

Table 12. Crystal Specifications

Specification	Value	Units
Crystal frequency	20.000	MHz
Frequency tolerance	±50	PPM
Load capacitance	50	pF
Frequency stability	±30	PPM
Maximum effective series resistance	40	Ohms (Ω)
Test condition drive level	100	µW

5.0 Signal Routing and Placement

The Ethernet circuitry should be kept free of interference from unrelated signal traces. Routing for other signals must be kept away from the space surrounding the grouped Ethernet components. Place the Ethernet circuitry at the perimeter of the board, as close as possible to the network connector.

The onchip crystal oscillator requires an external crystal and discrete components. For stable and noise-free operation, place the crystal and discrete components as close as possible to the 21143, keeping the etch length as short as possible. Do not route any noisy signals in this area.

The PCI pin ordering is fully compatible with the PCI specification recommendation and can be easily routed within the specified etch limits of the PCI signals. This includes shared signal lengths of up to 3.8 cm (1.5 in) and the clock signal length of 6.41 cm (2.5 in).

Keep all signal paths short and route them as directly as possible.

Systems using 10BASE-T nodes can be connected by cables up to 100 m (328 ft.). As a result, signals that reach the board can be noisy and low in amplitude. To minimize corrupting this data, route these signals, by most direct path, from the network connector and through the magnetics coupler to the 21143.

The length of this path should not exceed 8 cm (3 in) for the active AUI signals. The MII/SYM interface operates at 25 MHz (or 2.5 MHz). All routing of the MII/SYM signals to the MII/SYM device should be as short as possible and should not have significant differences of lengths and characteristics within signal groups. Examples of signal groups include **mii_rxd<4:0>** and **mii_txd<4:0>**.

Note: The routing of these signals should be done with caution. The preferred routing of these signals is in the external routing layers of the board. The MII/SYM device should be located between the 21143 and the magnetics port.

5.1 Ground and Power Planes

Up to four types of power signals require handling when implementing a design with the 21143:

- **Gnd** is adapter ground.
- **Vcc** (+5 V from PCI) drives the external components (boot ROM and Ethernet address ROM).
- **Vdd** (+3.3 V) drives the 21143.
- **Vee** (-9 V output) power from the DC-to-DC converter if the coaxial network connection is implemented. For information specific to the -9 V power supply, refer to the transceiver used to drive the coaxial network connection.

Intel recommends that at least two power planes be kept on the PCB: **Vcc** and **Gnd**. The **Vdd** power plane (+3.3 V) can be implemented either by a cut in the **Vcc** power plane, or by a power island under the 21143 on one of the signal routing layers.

Intel recommends that decoupling capacitors should be connected to all power supplies. These capacitors should be placed as close as possible to the power pins of the chips. The recommended values are as follows: 0.1 µF, 0.01 µF, 10 µF (tantalum), and 47 µF (tantalum).

For better noise-testing immunity, separate all power planes between the network connectors and the transformer from the logic and analog power planes of the adapter for the 10BASE-T, 10BASE2, 100BASE-T4, and 100BASE-TX connections.

Intel also recommends that the connector's shield of the adapter should be connected to the PC chassis.

5.1.1 3.3 V Power Supply

The 21143 operates with a power supply of 3.3 V. At least eight decoupling capacitors are recommended and should contain the following values:

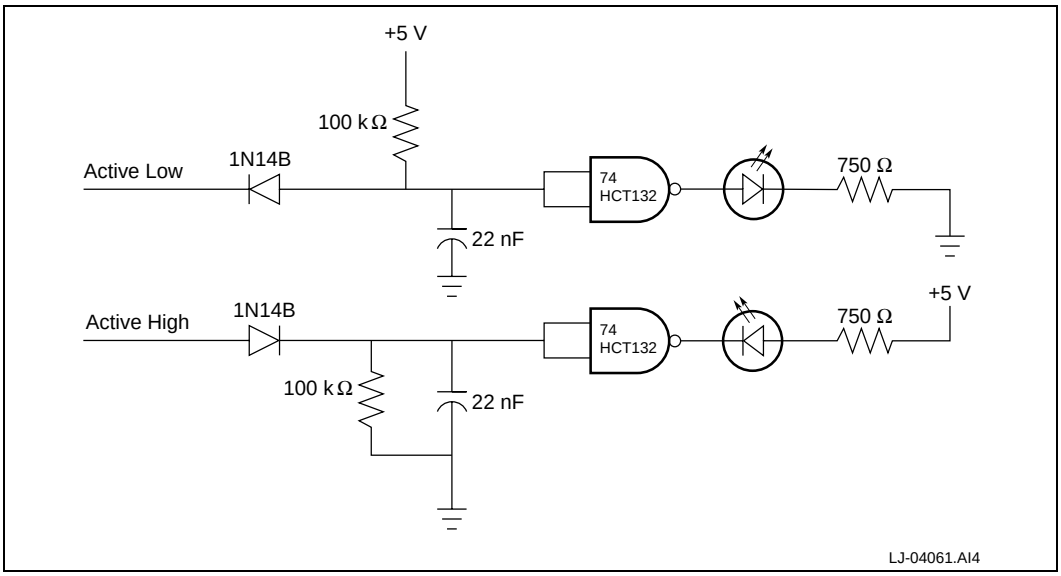
- Three each at 0.1 µF
- Three each at 0.01 µF
- One each at 10 µF (tantalum)
- One each at 47 µF (tantalum)

5.2 LED Status Signals

The LED connection requires a serial resistor that is connected to ground. This resistor value should be calculated according to the type of LED used. A typical 2 mA LED requires a 750 Ω resistor. For implementations using the boot ROM, the LED current should not exceed 2 mA. For LED indication and programming information, refer to the CSR15 definition in the *21143 PCI /CardBus 10/100 Mb/s Ethernet LAN Controller Hardware Reference Manual*.

The 21143 requires LED time-stretching logic for a visible indication of the activity signal. Figure 11 shows how to implement this circuit.

Figure 11. LED Time-Stretcher Circuit



6.0 Design Considerations

This section provides information to aid the user in designing Ethernet and Fast Ethernet capabilities onto a motherboard. In addition, it also includes design considerations for FCC compliance.

6.1 Designing the Ethernet Corner on Motherboards

This subsection provides a list of routing suggestions and a list of component placement suggestions.

The following list contains routing recommendations:

- Minimize the length of high-frequency signals.
- Route differential signal pairs together.
- Minimize the use of vias for high-frequency signals.

The following list contains component placement recommendations.

- Refer to the *PCI Local Bus Specification, Revision 2.1* for the placement of the 21143 with relation to the PCI bus.
- Place the 21143 as close to the PHY device as possible.
- Place the PHY device as close to the filters and magnetics as possible.
- Place the filters and magnetics as close to the RJ45 connector as possible.

6.2 Suggestions for FCC Compliance

Product designs and their associated applications are unique. Therefore, the designer must consider the total system or module implementation when determining a product design for FCC compliance.

The following information is provided as suggestions only to aid the designer in meeting FCC regulations.

6.2.1 Suggestions for Quiet Ground and Power Planes

For quiet ground and power planes, consider the following suggestions:

- Isolate power plane for PLL stability and noise isolation of audio digital-analog converters and amplifiers.
- Partition ground planes to isolate the I/O from common system noise. Do not route any etch across an isolated or partitioned ground plane.

Note: Ground plane splits can affect a signal's return path back to its source. If the signal return path is along the ground plane underneath the signal etch, any interruption in the ground plane increases the return path loop area, which in turn, increases its ability to radiate.

- Add common-mode chokes to the design at the output of the isolation transformer to isolate the I/O from common system noise.
- Place high-speed signals between power and ground planes to reduce board-level radiation.

The following books are recommended as additional references:

- *Fundamentals of Electromagnetic Capability,* by William G. Duff

- *Engineering Electromagnetic Capability*, by V. Prasad Kodali

6.2.2 Suggestions for Routing

For routing information, consider the following suggestions:

- Never route any etch (power or ground) across a partition or void because the signal loses its return-path integrity and contaminates the isolated plane.
- Avoid placing oscillators, phase-locked loops, and other clock-type devices near I/O connectors.
- Route all critical signals (for example; clocks, video output) directly in the etch and avoid, if possible, using vias (signal paths routed between planes in an etch board).

Note: Critical signals should be prioritized from the fastest to the slowest with respect to frequency and rise time. The fastest critical signals should be routed first.