82540EP Gigabit Ethernet Controller

Networking Silicon

Datasheet

Revision 1.2
April 2003

Revision History

Date	Revision	Notes
Apr 2002	0.25	Initial Release
Nov 2002	1.0	Changed document status to Intel Confidential.
Jan 2003	1.1	Section 1.0. Replaced Block Diagram Section 2.6. Added Table footnote Section 4.1, 4.2, 4.3. Replaced tables Section 5.1. Added Visual Pin Reference Section 4.4 Removed Power Supply Characteristics; added note to I/O Characteristics Section 5.0 Replaced Pinout Diagram
Apr 2003	1.2	Removed confidential status. Section 1.0. Added product ordering code.

Note: This page is intentionally left blank.

Contents

1.0 Introduction

The Intel® 82540EP Gigabit Ethernet Controller is a single, compact component with an integrated Gigabit Ethernet Media Access Control (MAC) and physical layer (PHY) functions. For desktop, workstation and mobile PC Network designs with critical space constraints, the Intel® 82540EP allows for a Gigabit Ethernet implementation in a very small area that is footprint compatible with current generation 10/100 Mbps Fast Ethernet designs

The Intel® 82540EP integrates Intel's fourth generation gigabit MAC design with fully integrated, physical layer circuitry to provide a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab). The controller is capable of transmitting and receiving data at rates of 1000 Mbps, 100 Mbps, or 10 Mbps. In addition to managing MAC and PHY layer functions, the controller provides a 32-bit wide direct Peripheral Component Interconnect (PCI) 2.2 compliant interface capable of operating at 33 or 66 MHz.

The 82540EP also incorporates the CLKRUN protocol and hardware supported downshift capability to two or three-pair 100 Mb/s operation. These features optimize mobile applications.

The Intel® 82540EP's on-board System Management Bus (SMB) port enables network manageability implementations required by information technology personnel for remote control and alerting via the LAN. With SMB, management packets can be routed to or from a management processor. The SMB port enables industry standards, such as Intelligent Platform Management Interface (IPMI) and Alert Standard Forum (ASF), to be implemented using the 82540EP. In addition, on chip ASF 1.0 circuitry provides alerting and remote control capabilities with standardized interfaces.

The 82540EP Gigabit Ethernet Controller architecture is designed to deliver high performance and PCI bus efficiency. Wide internal data paths eliminate performance bottlenecks by efficiently handling large address and data words. The 82540EP controller includes advanced interrupt handling features to limit PCI bus traffic and a PCI interface that maximizes the use of bursts for efficient bus usage. The 82540EP caches up to 64 packet descriptors in a single burst for efficient PCI bandwidth use. A large 64 KByte on-chip packet buffer maintains superior performance as available PCI bandwidth changes. In addition, using hardware acceleration, the controller offloads tasks from the host controller, such as TCP/UDP/IP checksum calculations and TCP segmentation.

The 82540EP is packaged in a 15 mm^2 196-ball grid array and is pin compatible with both the 82551QM 10/100 Mbps Fast Ethernet Multifunction PCI/CardBus Controller and the 82540EM Gigabit Ethernet Controller (which does not have added power saving features like CLKRUN).

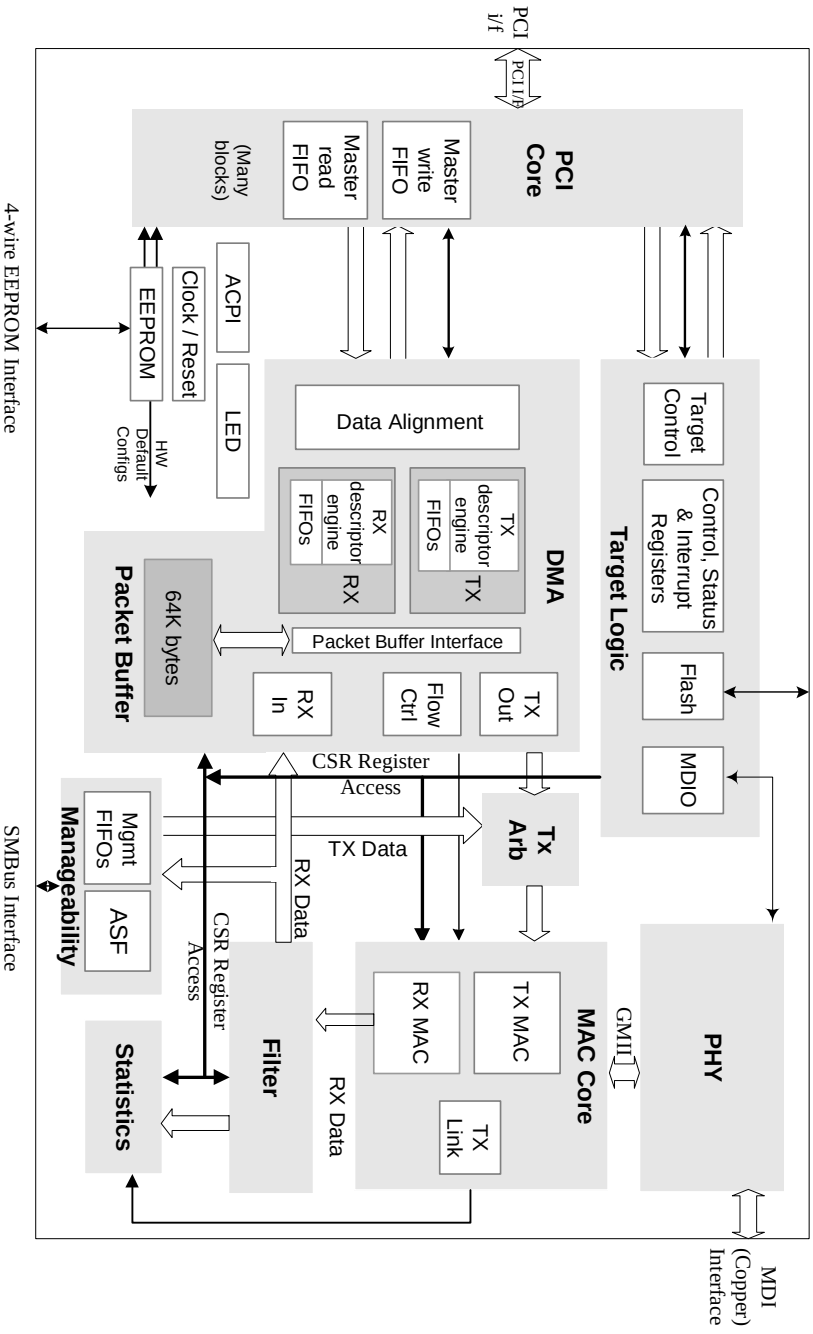


Figure 1. Gigabit Ethernet Controller Block Diagram

1.1 Document Scope

This document contains datasheet specifications for the 82540EP Gigabit Ethernet Controller, including signal descriptions, DC and AC parameters, packaging data, and pinout information.

1.2 Reference Documents

This application assumes that the designer is acquainted with high-speed design and board layout techniques. The following documents provide additional information:

- 82544EI/82544GC Gigabit Ethernet Controller Software Developer's Manual, Revision 0.25, Intel Corporation.
- PCI Local Bus Specification, Revision 2.3, PCI Special Interest Group.
- PCI Bus Power Management Interface Specification, Rev. 1.1, PCI Special Interest Group.
- IEEE Standard 802.3, 1996 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- IEEE Standard 802.3u, 1995 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- IEEE Standard 802.3x, 1997 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- IEEE Standard 802.3z, 1998 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- IEEE Standard 802.3ab, 1999 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- 82559 Fast Ethernet Controllers Timing Device Selection Guide, AP-419, Intel Corporation.
- PCI Mobile Design Guide, Rev. 1.1, PCI Special Interest Group

1.3 Product Code

The product ordering code for the 82540EP is: RC82540EP.

Note: This page is intentionally left blank.

2.0 Features of the 82540EP Gigabit Ethernet Controller

2.1 PCI Features

Features	Benefits
PCI Revision 2.3 support for 32-bit wide interface at 33 MHz and 66 MHz	• Application flexibility for LAN on Motherboard (LOM) or embedded solutions • 64-bit addressing for systems with more than 4 Gigabytes of physical memory • Support for new PCI 2.3 interrupt status/control
Algorithms that optimally use advanced PCI, MWI, MRM, and MRL commands	• Efficient bus operations
CardBus Information Services (CIS) Pointer	• Enables CardBus operation (when used with external FLASH device and series termination on PCI bus)
CLKRUN# Signal	• PCI clock suspension for low power mobile design

2.2 MAC Specific Features

Features	Benefits
Low-latency transmit and receive queues	• Network packets handled without waiting or buffer overflow.
IEEE 802.3x compliant flow control support with software controllable pause times and threshold values	• Control over the transmissions of pause frames through software or hardware triggering • Frame loss reduced from receive overruns
Caches up to 64 packet descriptors in a single burst	• Efficient use of PCI bandwidth
Programmable host memory receive buffers (256 Bytes to 16 KBytes) and cache line size (16 Bytes to 256 Bytes)	• Efficient use of PCI bandwidth
Wide, optimized internal data path architecture	• Low latency data handling • Superior DMA transfer rate performance
64 KByte configurable Transmit and Receive FIFO buffers	• No external FIFO memory requirements • FIFO size adjustable to application
Descriptor ring management hardware for transmit and receive	• Simple software programming model
Optimized descriptor fetching and write-back mechanisms	• Efficient system memory and use of PCI bandwidth
Mechanism available for reducing interrupts generated by transmit and receive operations	• Maximizes system performance and throughput
Support for transmission and reception of packets up to 16 KBytes	• Enables jumbo frames

2.3 PHY Specific Features

Features	Benefits
Integrated PHY for 10/100/1000 Mbps full and half duplex operation	• Smaller footprint and lower power dissipation compared to multi-chip MAC and PHY solutions
IEEE 802.3ab Auto-Negotiation support	• Automatic link configuration including speed, duplex, and flow control
IEEE 802.3ab PHY compliance and compatibility	• Robust operation over the installed base of Category-5 (CAT-5) twisted pair cabling
State-of-the-art DSP architecture implements digital adaptive equalization, echo cancellation, and cross-talk cancellation	• Robust performance in noisy environments • Tolerance of common electrical signal impairments
PHY ability to automatically detect polarity and cable lengths and MDI versus MDI-X cable at all speeds	• Easier network installation and maintenance • End-to-end wiring tolerance

2.4 Host Offloading Features

Features	Benefits
Transmit and receive IP, TCP and UDP checksum off-loading capabilities	• Lower CPU utilization
Transmit TCP segmentation	• Increased throughput and lower CPU utilization • Large send offload feature (in Microsoft* Windows* XP) compatible
Advanced packet filtering	• 16 exact matched packets (unicast or multicast) • 4096-bit hash filter for multicast frames • Promiscuous (unicast and multicast) transfer mode support • Optical filtering of invalid frames
IEEE 802.1q VLAN support with VLAN tag insertion, stripping and packet filtering for up to 4096 VLAN tags	• Ability to create multiple virtual LAN segments
Descriptor ring management hardware for transmit and receive	• Optimized fetching and write-back mechanisms for efficient system memory and PCI bandwidth usage
16 KByte jumbo frame support	• High throughput for large data transfers on networks supporting jumbo frames
Interrupt coalescing (multiple packets per interrupt)	• Increased throughput by reducing interrupts generated by transmit and receive operations

2.5 Manageability Features

Features	Benefits
Manageability features: SMB port, ASF 1.0, ACPI, Wake on LAN, and PXE	• Network management flexibility
On-board SMB port	• Enables IPMI and ASF implementations • Allows packets routing to and from either LAN port and a server management processor
Compliance with PCI Power Management 1.1 and ACPI 2.0 register set compliant including: • D0 and D3 power states • Network Device Class Power Management Specification 1.1 • PCI Specification 2.2	• PCI power management capability requirements for PC and embedded applications
SNMP and RMON statistic counters	• Easy system monitoring with industry standard consoles
SDG 3.0, WfM 2.0, and PC2001 compliance	• Remote network management capabilities through DMI 2.0 and SNMP software
Wake on LAN support	• Packet recognition and wake-up for NIC and LOM applications without software configuration
Two or three-pair cable downshift	• Assures link under adverse cable configurations

2.6 Additional Device Features

Features	Benefits
Four activity and link indication outputs that directly drive LEDs	• Link and activity indications (10, 100, and 1000 Mbps) on each port
Programmable LED functionality	• Software definable function (speed, link, and activity) and blinking allowing flexible LED implementations
Internal PLL for clock generation can use a 25 MHz crystal	• Lower component count and system cost
JTAG (IEEE 1149.1) Test Access Port built in silicon	• Simplified testing using boundary scan
On-chip power control circuitry[a]	• Reduced number of on-board power supply regulators • Simplified power supply design in less power-critical applications
Four software definable pins	• Additional flexibility for LEDs or other low speed I/O devices
Supports little endian byte ordering for both 32 and 64 bit systems and big endian byte ordering for 64 bit systems	• Portable across application architectures
Two or three-pair cable downshift	• Supports modular hardware accessories
Provides loopback capabilities	• Validates silicon integrity
Minimal ballout change from the 82540EM	• Pin Compatibility

a. If applying the “low-power” EEPROM setting for the 82540EP chip, then only external voltage regulator circuits should be used instead of the on-chip power control circuitry

2.7 Technology Features

Features	Benefits
196-pin Ball Grid Array (TFBGA) package	• 15 mm^2 component making LOM designs easier
Pin compatible with 82551QM and 82540EM controllers	• Enables 10/100 Mbps Fast Ethernet or 1000 Mbps Gigabit Ethernet implementations on the same board with only minor stuffing option changes
Implemented in 0.15u CMOS process	• Offers lowest geometry to minimize power and size while maintaining Intel quality reliability standards
Operating temperature: 0° C to 70° C (maximum) operating temperature Heat sink or forced airflow not required 65° C to 140° C storage temperature range	• Simple thermal design
PCI Signaling: 3.3 V (5 V tolerant) PCI signaling Typical targeted power dissipation: • 1.38W @ D0 1000 Mb/s • 386mW @ D3 100 Mb/s (wake-up enabled) • <20mW @ D3 wake-up disabled	• Lower power requirements for mobile applications

3.0 Signal Descriptions

Note: The targeted signal names are subject to change without notice. Verify with your local Intel sales office that you have the latest information before finalizing a design.

3.1 Signal Type Definitions

The signals of the 82540EP controller are electrically defined as follows:

Name	Definition
I	**Input.** Standard input only digital signal.
O	**Output.** Standard output only digital signal.
TS	**Tri-state.** Bi-directional three-state digital input/output signal.
STS	**Sustained Tri-state.** Sustained digital three-state signal driven by one agent at a time. An agent driving the STS pin low must actively drive it high for at least one clock before letting it float. The next agent of the signal cannot drive the pin earlier than one clock after it has been released by the previous agent.
OD	**Open Drain.** Wired-OR with other agents. The signaling agent asserts the OD signal, but the signal is returned to the inactive state by a weak pull-up resistor. The pull-up resistor may require two or three clock periods to fully restore the signal to the de-asserted state.
A	**Analog.** PHY analog data signal.
P	**Power.** Power connection, voltage reference, or other reference connection.

3.2 PCI Bus Interface

When the Reset signal (RST#) is asserted, the 82540EP will not drive any PCI output or bi-directional pins except the Power Management Event signal (PME#).

3.2.1 PCI Address, Data and Control Signals

Symbol	Type	Name and Function
AD[31:0]	TS	**Address and Data.** Address and data signals are multiplexed on the same PCI pins. A bus transaction includes an address phase followed by one or more data phases. The address phase is the clock cycle when the Frame signal (FRAME#) is asserted low. During the address phase AD[31:0] contain a physical address (32 bits). For I/O, this is a byte address, and for configuration and memory, a DWORD address. The 82540EP device uses little endian byte ordering. During data phases, AD[7:0] contain the least significant byte (LSB) and AD[31:24] contain the most significant byte (MSB).

Symbol	Type	Name and Function
CBE[3:0]#	TS	**Bus Command and Byte Enables.** Bus command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, CBE[3:0]# define the bus command. In the data phase, CBE[3:0]# are used as byte enables. The byte enables are valid for the entire data phase and determine which byte lanes contain meaningful data. CBE0# applies to byte 0 (LSB) and CBE3# applies to byte 3 (MSB).
PAR	TS	**Parity.** The Parity signal is issued to implement even parity across AD[31:0] and CBE[3:0]#. PAR is stable and valid one clock after the address phase. During data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted after a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. When the 82540EP controller is a bus master, it drives PAR for address and write data phases, and as a slave device, drives PAR for read data phases.
FRAME#	STS	**Cycle Frame.** The Frame signal is driven by the 82540EP device to indicate the beginning and length of an access and indicate the beginning of a bus transaction. While FRAME# is asserted, data transfers continue. FRAME# is de-asserted when the transaction is in the final data phase.
IRDY#	STS	**Initiator Ready.** Initiator Ready indicates the ability of the 82540EP controller (as bus master device) to complete the current data phase of the transaction. IRDY# is used in conjunction with the Target Ready signal (TRDY#). The data phase is completed on any clock when both IRDY# and TRDY# are asserted. During the write cycle, IRDY# indicates that valid data is present on AD[31:0]. For a read cycle, it indicates the master is ready to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. The 82540EP controller drives IRDY# when acting as a master and samples it when acting as a slave.
TRDY#	STS	**Target Ready.** The Target Ready signal indicates the ability of the 82540EP controller (as a selected device) to complete the current data phase of the transaction. TRDY# is used in conjunction with the Initiator Ready signal (IRDY#). A data phase is completed on any clock when both TRDY# and IRDY# are sampled asserted. During a read cycle, TRDY# indicates that valid data is present on AD[31:0]. For a write cycle, it indicates the target is ready to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. The 82540EP device drives TRDY# when acting as a slave and samples it when acting as a master.
STOP#	STS	**Stop.** The Stop signal indicates the current target is requesting the master to stop the current transaction. As a slave, the 82540EP controller drives STOP# to request the bus master to stop the transaction. As a master, the 82540EP controller receives STOP# from the slave to stop the current transaction.
IDSEL#	I	**Initialization Device Select.** The Initialization Device Select signal is used by the 82540EP as a chip select signal during configuration read and write transactions.
DEVSEL#	STS	**Device Select.** When the Device Select signal is actively driven by the 82540EP, it signals notifies the bus master that it has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.
VIO	P	**VIO.** The VIO signal is a voltage reference for the PCI interface (3.3 V or 5 V PCI signaling environment). It is used as the clamping voltage. Note: An external resistor is required between the voltage reference and the VIO pin. The target resistor value is 100 KΩ

3.2.2 Arbitration Signals

Symbol	Type	Name and Function
REQ#	TS	**Request Bus.** The Request Bus signal is used to request control of the bus from the arbiter. This signal is point-to-point.
GNT#	I	**Grant Bus.** The Grant Bus signal notifies the 82540EP that bus access has been granted. This is a point-to-point signal.
LOCK#	I	**Lock Bus.** The Lock Bus signal is asserted by an initiator to require sole access to a target memory device during two or more separate transfers. The 82540EP device does not implement bus locking.

3.2.3 Interrupt Signal

Symbol	Type	Name and Function
INTA#	TS	**Interrupt A.** Interrupt A is used to request an interrupt by port 1 of the 82540EP. It is an active low, level-triggered interrupt signal.

3.2.4 System Signals

Symbol	Type	Name and Function
CLK	I	**PCI Clock.** The PCI Clock signal provides timing for all transactions on the PCI bus and is an input to the 82540EP device. All other PCI signals, except the Interrupt A (INTA#) and PCI Reset signal (RST#), are sampled on the rising edge of CLK. All other timing parameters are defined with respect to this edge.
M66EN	I	**66 MHz Enable.** M66EN indicates whether the system bus is enabled for 66MHz.
RST#	I	**PCI Reset.** When the PCI Reset signal is asserted, all PCI output signals, except the Power Management Event signal (PME#), are floated and all input signals are ignored. The PME# context is preserved, depending on power management settings. Most of the internal state of the 82540EP is reset on the de-assertion (rising edge) of RST#.
CLKRUN#	I/O OD	**Clock Run.** This signal is used by the system to pause the PCI clock signal. It is used by the 82540EP controller to request the PCI clock. When the CLKRUN# feature is disabled, leave this pin unconnected.

3.2.5 Error Reporting Signals

Symbol	Type	Name and Function
SERR#	OD	**System Error.** The System Error signal is used by the 82540EP controller to report address parity errors. SERR# is open drain and is actively driven for a single PCI clock when reporting the error.
PERR#	STS	**Parity Error.** The Parity Error signal is used by the 82540EP controller to report data parity errors during all PCI transactions except by a Special Cycle. PERR# is sustained tri-state and must be driven active by the 82540EP controller two data clocks after a data parity error is detected. The minimum duration of PERR# is one clock for each data phase a data parity error is present.

3.2.6 Power Management Signals

Symbol	Type	Name and Function
LAN_ PWR_ GOOD	I	**Power Good (Power-on Reset).** The Power Good signal is used to indicate that stable power is available for the 82540EP. When the signal is low, the 82540EP holds itself in reset state and floats all PCI signals.
PME#	OD	**Power Management Event.** The 82540EP device drives this signal low when it receives a wake-up event and either the PME Enable bit in the Power Management Control/Status Register or the Advanced Power Management Enable (APME) bit of the Wake-up Control Register (WUC) is 1b.
AUX_PWR	I	**Auxiliary Power.** If the Auxiliary Power signal is high, then auxiliary power is available and the 82540EP device should support the D3cold power state.

3.2.7 Impedance Compensation Signals

Symbol	Type	Name and Function
ZN_COMP	I/O	**N Device Impedance Compensation.** This signal should be connected to an external precision resistor (to VDD) that is indicative of the PCI trace load. This cell is used to dynamically determine the drive strength required on the N-channel transistors in the PCI I/O cells.
ZP_COMP	I/O	**P Device Impedance Compensation.** This signal should be connected to an external precision resistor (to VSS) that is indicative of the PCI trace load. This cell is used to dynamically determine the drive strength required on the P-channel transistors in the PCI I/O cells.

3.2.8 SMB Signals

Symbol	Type	Name and Function
SMBCLK	I/O	**SMB Clock.** The SMB Clock signal is an open drain signal for serial SMB interface.
SMBDATA	I/O	**SMB Data.** The SMB Data signal is an open drain signal for serial SMB interface.
SMBALRT#	O	**SMB Alert.** The SMB Alert signal is open drain for serial SMB interface.

3.3 EEPROM and Serial FLASH Interface Signals

Symbol	Type	Name and Function
EE_DI	O	**EEPROM Data Input.** The EEPROM Data Input pin is used for output to the memory device.
EE_DO	I	**EEPROM Data Output.** The EEPROM Data Output pin is used for input from the memory device. The EE_DO includes an internal pull-up resistor.
EE_CS	O	**EEPROM Chip Select.** The EEPROM Chip Select signal is used to enable the device.
EE_SK	O	**EEPROM Serial Clock.** The EEPROM Shift Clock provides the clock rate for the EEPROM interface, which is approximately 1 MHz.

Symbol	Type	Name and Function
FL_CE#	O	**FLASH Chip Enable Output.** Used to enable FLASH device.
FL_SCK	O	**FLASH Serial Clock Output**. The clock rate of the serial FLASH interface is approximately 1 MHz.
FL_SI	O	**FLASH Serial Data Input.** This pin is an output to the memory device.
FL_SO	I	**FLASH Serial Data Output.** This pin is an input from the FLASH memory. It has an internal pullup device.

3.4 Miscellaneous Signals

3.4.1 LED Signals

Symbol	Type	Name and Function
LED0 / LINK#	O	**LED0 / LINK Up.** Programmable LED indication. Defaults to indicate link connectivity.
LED1 / ACT#	O	**LED1 / Activity.** Programmable LED indication. Defaults to flash to indicate transmit or receive activity.
LED2 / LINK100#	O	**LED2 / LINK 100.** Programmable LED indication. Defaults to indicate link at 100 Mbps.
LED3 / LINK1000#	O	**LED3 / LINK 1000.** Programmable LED indication. Defaults to indicate link at 1000 Mbps.

3.4.2 Other Signals

Symbol	Type	Name and Function
SDP[7:6] SDP[1:0]	TS	**Software Defined Pin.** The Software Defined Pins are reserved and programmable with respect to input and output capability. These default to input signals upon power-up but may be configured differently by the EEPROM. The upper four bits may be mapped to the General Purpose Interrupt bits if they are configured as input signals. Note: SDP5 is not included in the group of Software Defined Pins.

3.5 PHY Signals

3.5.1 Crystal Signals

Symbol	Type	Name and Function
XTAL1	I	**Crystal One.** The Crystal One pin is a 25 MHz +/- 50 ppm input signal. It can be connected to either an oscillator or crystal. If a crystal is used, Crystal Two (XTAL2) must also be connected.
XTAL2	O	**Crystal Two.** Crystal Two is the output of an internal oscillator circuit used to drive a crystal into oscillation. If an external oscillator is used in the design, XTAL2 must be disconnected.

3.5.2 Analog Signals

Symbol	Type	Name and Function
REF	P	**Reference.** This Reference signal should be connected to VSS through an external 2.49 KΩ resistor.
MDI[0]+/-	A	**Media Dependent Interface [0].** **1000BASE-T**: In MDI configuration, MDI[0]+/- corresponds to BI_DA+/-, and in MDI-X configuration, MDI[0]+/- corresponds to BI_DB+/-. **100BASE-TX**: In MDI configuration, MDI[0]+/- is used for the transmit pair, and in MDI-X configuration, MDI[0]+/- is used for the receive pair. **10BASE-T**: In MDI configuration, MDI[0]+/- is used for the transmit pair, and in MDI-X configuration, MDI[0]+/- is used for the receive pair.
MDI[1]+/-	A	**Media Dependent Interface [1].** **1000BASE-T**: In MDI configuration, MDI[1]+/- corresponds to BI_DB+/-, and in MDI-X configuration, MDI[1]+/- corresponds to BI_DA+/-. **100BASE-TX**: In MDI configuration, MDI[1]+/- is used for the receive pair, and in MDI-X configuration, MDI[1]+/- is used for the transit pair. **10BASE-T**: In MDI configuration, MDI[1]+/- is used for the receive pair, and in MDI-X configuration, MDI[1]+/- is used for the transit pair.
MDI[2]+/-	A	**Media Dependent Interface [2].** **1000BASE-T**: In MDI configuration, MDI[2]+/- corresponds to BI_DC+/-, and in MDI-X configuration, MDI[2]+/- corresponds to BI_DD+/-. **100BASE-TX**: Unused. **10BASE-T**: Unused.
MDI[3]+/-	A	**Media Dependent Interface [3].** **1000BASE-T**: In MDI configuration, MDI[3]+/- corresponds to BI_DD+/-, and in MDI-X configuration, MDI[3]+/- corresponds to BI_DC+/-. **100BASE-TX**: Unused. **10BASE-T**: Unused.

3.6 Test Interface Signals

Symbol	Type	Name and Function
JTAG_TCK	I	**JTAG Clock.**
JTAG_TDI	I	**JTAG TDI.**
JTAG_TDO	O	**JTAG TDO.**
JTAG_TMS	I	**JTAG TMS.**
JTAG_ TRST#	I	**JTAG Reset.** This is an active low reset signal for JTAG. This signal should be terminated using a pull-down resistor to ground. It must not be left unconnected.
TEST	I	**Factory Test Pin.**
CLKVIEW	O	**Clock View.** Output for GTX_CLK and RX_CLK during IEEE PHY conformance testing. The clock is selected by register programming.

3.7 Power Supply Connections

3.7.1 Digital Supplies

Symbol	Type	Name and Function
VDDO	P	**3.3 V I/O Power Supply.**
DVDD	P	**1.5 V Digital Core Power Supply.**

3.7.2 Analog Supplies

Symbol	Type	Name and Function
AVDDH	P	**3.3 V Analog Power Supply.**
AVDDL	P	**2.5 V Analog Power Supply.**

3.7.3 Ground and No Connects

Symbol	Type	Name and Function
GND	P	**Ground.**
NC	P	**No Connect.** Do not connect any circuitry to these pins. Pull-up or pull-down resistors should not be connected to these pins.

3.7.4 Control Signals

Symbol	Type	Name and Function
CTRL_15	A	**1.5V Control.** LDO voltage regulator output to drive external pass transistor. If 1.5V is already present in the system, leave output unconnected. To achieve optimal D_3 power consumption (<50 mw), leave the output unconnected and use a high-efficiency external switching regulator.
CTRL_25	A	**2.5V Control.** LDO voltage regulator output to drive external pass transistor. If 2.5V is already present in the system, leave output unconnected. To achieve optimal D_3 power consumption (<50 mw), leave the output unconnected and use a high-efficiency external switching regulator.

4.0 Voltage, Temperature, and Timing Specifications

Note: The specification values listed in this section are subject to change without notice. Verify with your local Intel sales office that you have the latest information before finalizing a design.

4.1 Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings[a]

Symbol	Parameter	Min	Max	Unit
V_{DD}	DC supply voltage	-0.3	7	V
V_{IN}	Input voltage	-1	V_{DD} + 0.3	V
I_{IN}	DC input pin current	-10	10	mA
T_{STG}	Storage temperature	-40	125	°C

a. Maximum ratings are referenced to ground (VSS). Permanent device damage is likely to occur if the ratings in this table are exceeded. These values should not be used as the limits for normal device operations.

4.2 Recommended Operating Conditions

Table 2. Recommended Operating Conditions[a] (Sheet 1 of 2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{OP}	Operating Temperature		0		70	°C
V_{IO}	VIO Voltage Range		3		5.25	V
V_{DD}	Periphery Voltage Range	**3.3V** ± 10%	3	3.3	3.6	V

Table 2. Recommended Operating Conditions[a] (Sheet 2 of 2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{AH}	Analog High VDD Range	**3.3V** ± 10%	3	3.3	3.6	V
V_D	Core Digital Voltage Range	**1.5V** ± 5%	1.425	1.5	1.575	V
V_{AL}	Analog Low VDD Range	**2.5V** ± 5%	2.375	2.5	2.625	V

a. Sustained operation of the device at conditions exceeding these values, even if they are within the absolute maximum rating limits, might result in permanent damage.

4.3 DC Specifications

Table 3. DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_{DD} (3.3)	DC supply voltage on VDDO or AVDDH	3.00	3.3	3.60	V
V_{DD} (2.5)	DC supply voltage on AVDDL	2.38	2.5	2.62	V
V_{DD} (1.5)	DC supply voltage on DVDD	1.43	1.5	1.57	V

Table 4. Power Specifications - D0a

	D0a							
	unplugged/no link		@10 Mbps		@100Mbps		@1000Mbps	
	Typ Icc (mA)	Max Icc (mA)	Typ Icc (mA)	Max Icc (mA)	Typ Icc (mA)	Max Icc (mA)	Typ Icc (mA)	Max Icc (mA)
3.3V	40	40	55	65	65	80	125	125
2.5V	20	20	30	35	55	60	145	150
1.5V	100	120	95	100	115	125	400	425
Total Device Power	325 mW		400 mW		525 mW		1.38 W	1.5 W

Table 5. Power Specifications - D3cold

	D3cold - wake-up enabled						D3cold - wake disabled - max power savings mode disabled		D3cold - wake disabled - max power savings mode enabled[a]	
	unplugged/no link		@10 Mbps		@100Mbps					
	Typ Icc (mA)	Max Icc (mA)	Typ Icc (mA)	Max Icc (mA)	Typ Icc (mA)	Max Icc (mA)	Typ Icc (mA)	Max Icc (mA)	Typ Icc (mA)	Max Icc (mA)
3.3V	40	40	55	55	50	50	40	40	6	8
2.5V	20	20	30	30	55	55	20	20	0.1	0.1
1.5V	40	40	30	35	55	60	10	10	1	1
Total Device Power	240 mW		300 mW		385 mW		195 mW		20 mW	

a. Special Note: To obtain the benefit of max power savings mode, do not use the internal voltage regulator control circuit and external pass transistors. Use external switching regulators for highest efficiency.

Table 6. Power Specifications D(r) Uninitialized

	D(r) Uninitialized (LAN_PWR_GOOD=0)	
	Typ Icc (mA)	Max Icc (mA)
3.3V	40	45
2.5V	40	45
1.5V	190	200
Total Device Power	520 mW	

Table 7. Power Specifications - Complete Subsystem

	Complete Subsystem (Reference Design) Including Magnetics, LED, Regulator Circuits									
	D3cold - wake disabled - max power savings mode disabled		D3cold wake-enabled @10Mbps		D3cold wake-enabled @100Mbps		D0 @1000Mbps active		D3cold - wake disabled - max power savings mode enabled	
	Typ Icc (mA)	Max Icc (mA)	Typ Icc (mA)	Max Icc (mA)	Typ Icc (mA)	Max Icc (mA)	Typ Icc (mA)	Max Icc (mA)	Typ Icc (mA)	Max Icc (mA)
3.3V	40	40	60	60	60	60	130	130	6	8

Table 7. Power Specifications - Complete Subsystem

2.5V	20	20	40	40	80	80	240	245	0.1	0.1
1.5V	10	10	30	35	55	60	400	425	1	1
Subsystem 3.3V current		70 mA		135 mA		200 mA		800 mA		10 mA

Table 8. I/O Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	Voltage input LOW		-0.5		0.8	V
V_{IH}	Voltage input HIGH		2		V_{DD} +0.3	V
V_{OL}	Voltage output LOW				0.4	V
V_{OH}	Voltage output HIGH		2.4			V
V_{SH}	Schmitt Trigger Hysterysis		0.1			V
I_{OL}[a]	Output current LOW 3mA drivers (TTL3) 6mA drivers (TTL6) 12mA drivers (TTL12)	 V_{OL} V_{OL} V_{OL}	 3 6 12			 mA mA mA
I_{OH}[a]	Output current HIGH 3mA drivers (TTL3) 6mA drivers (TTL6) 12mA drivers (TTL12)	 V_{OH} V_{OH} V_{OH}	 -3 -6 -12			 mA mA mA
I_{IN}	Input Current TTL inputs Inputs with pull-down resistors TTL inputs with pull-up resistors	$V_{IN} = V_{DD}$ or V_{SS} $V_{IN} = V_{DD}$ $V_{IN} = V_{SS}$	 -10 150 -150	±1	 10 480 -480	 µA µA µA
I_{OZ}	3-state output leakage current	$V_{OH} = V_{DD}$ or V_{SS}	-10	±1	10	µA
C_{IN}	Input capacitance	Any input and bi-directional buffer		2.5		pF
C_{OUT}	Output capacitance	Any output buffer		2		pF
C_{PUD}	Pull-up/down Resistor value		7.5		20	kΩ

a. TTL3 signals include: EE_DI, EE_SK, EE_CS, and JTAG_TDO.
TTL6 signals include: CLKRUN#, FL_CE#, FL_SCK, FL_SI, and CLK_VIEW.
TTL12 signals include: LED0 / LINK #, LED1 / ACT #, LED2 / LINK100 #, LED3 / LINK1000 #, SDP0, SDP1, SDP6, and SDP7.

4.4 AC Characteristics

Table 9. AC Characteristics: 3.3 V Interfacing

Symbol	Parameter	Min	Typ	Max	Unit
PCICLK	Clock frequency in PCI mode			66	MHz

Table 10. 25 MHz Clock Input Requirements

Symbol	Parameter[a]	Min	Typ	Max	Unit
fi_TX_CLK	TX_CLK_IN frequency	25 - 50 ppm	25	25 + 50 ppm	MHz

a. This parameter applies to an oscillator connected to the Crystal One (XTAL1) input. Alternatively, a crystal may be connected to XTAL1 and XTAL2 as the frequency source for the internal oscillator.

Table 11. Link Interface Clock Requirements

Symbol	Parameter	Min	Typ	Max	Unit
fGTX[a]	GTX_CLK frequency		125		MHz

a. GTX_CLK is used externally for test purposes only.

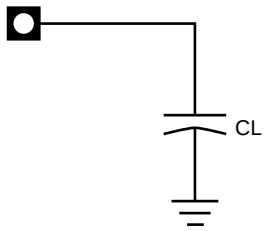
Table 12. EEPROM Interface Clock Requirements

Symbol	Parameter	Min	Typ	Max	Unit
fSK				1	MHz

Table 13. AC Test Loads for General Output Pins

Symbol	Signal Name	Value	Units
CL	TDO	10	pF
CL	PME#, SDP[7:0]	16	pF
CL	EE_DI, EE_SK	18	pF
CL	RX_ACTIVITY, TX_ACTIVITY, LINK_UP	20	pF

Figure 1. AC Test Loads for General Output Pins



4.5 Timing Specifications

Note: Timing specifications are subject to change. Verify with your local Intel sales office that you have the latest information before finalizing a design.

4.5.1 PCI Bus Interface

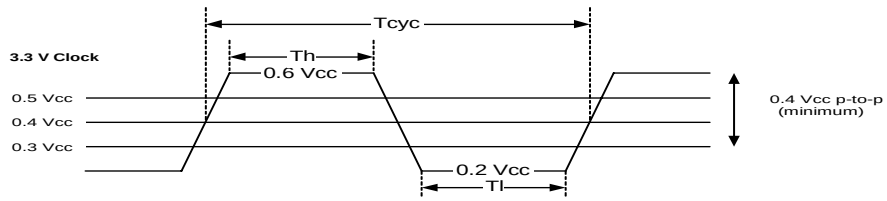
4.5.1.1 PCI Bus Interface Clock

Table 14. PCI Bus Interface Clock Parameters

Symbol	Parameter[a]	PCI 66 MHz		PCI 33 MHz		Units
		Min	Max	Min	Max	
TCYC	CLK cycle time	15	30	30		ns
TH	CLK high time	6		11		ns
TL	CLK low time	6		11		ns
	CLK slew rate	1.5	4	1	4	V/ns
	RST# slew rate[b]	50		50		mV/ns

a. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown.
b. The minimum RST# slew rate applies only to the rising (de-assertion) edge of the reset signal and ensures that system noise cannot render a monotonic signal to appear bouncing in the switching range.

Figure 2. PCI Clock Timing



4.5.1.2 PCI Bus Interface Timing

Table 15. PCI Bus Interface Timing Parameters

Symbol	Parameter	PCI 66MHz		PCI 33 MHz		Units
		Min	Max	Min	Max	
TVAL	CLK to signal valid delay: bussed signals	2	6	2	11	ns
TVAL(ptp)	CLK to signal valid delay: point-to-point signals	2	6	2	12	ns
TON	Float to active delay	2		2		ns
TOFF	Active to float delay		14		28	ns
TSU	Input setup time to CLK: bussed signals	3		7		ns
TSU(ptp)	Input setup time to CLK: point-to-point signals	5		10, 12		ns
TH	Input hold time from CLK	0		0		ns
TRRSU	REQ64# to RST# setup time	10*TCYC		10*TCYC		ns
TRRH	RST# to REQ64# hold time	0		0		ns

NOTES:
1. Output timing measurements are as shown.
2. REQ# and GNT# signals are point-to-point and have different output valid delay and input setup times than bussed signals. GNT# has a setup of 10 ns; REQ# has a setup of 12 ns. All other signals are bussed.
3. Input timing measurements are as shown.

Figure 3. PCI Bus Interface Output Timing Measurement

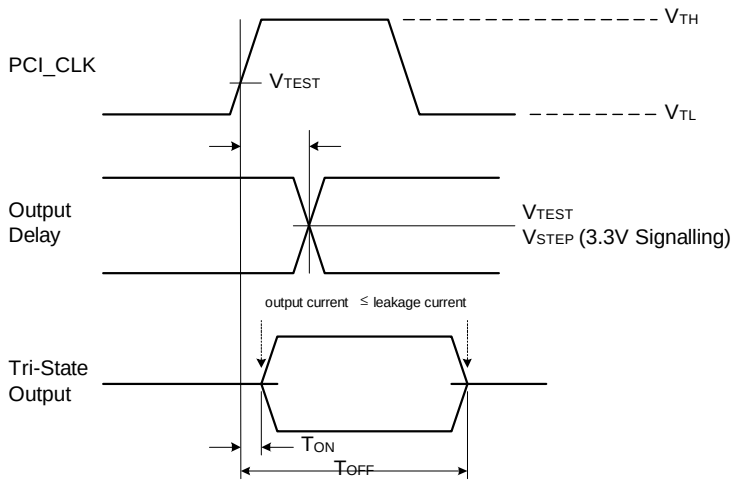


Figure 4. PCI Bus Interface Input Timing Measurement Conditions

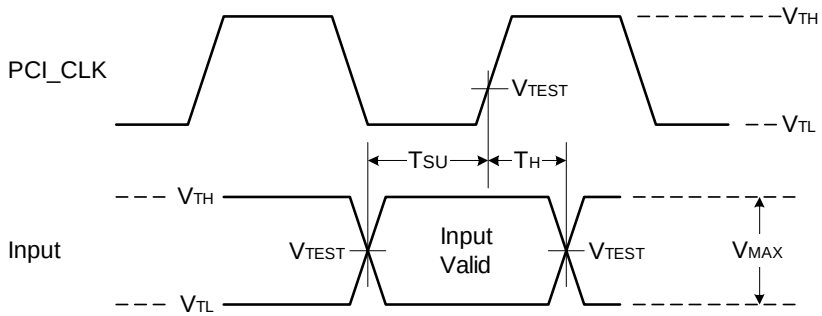


Table 16. PCI Bus Interface Timing Measurement Conditions

Symbol	Parameter	PCI 66 MHz 3.3 v	Unit
VTH	Input measurement test voltage (high)	0.6*VCC	V
VTL	Input measurement test voltage (low)	0.2*VCC	V
VTEST	Output measurement test voltage	0.4*VCC	V
	Input signal slew rate	1.5	V/ns

Figure 5. TVAL (max) Rising Edge Test Load

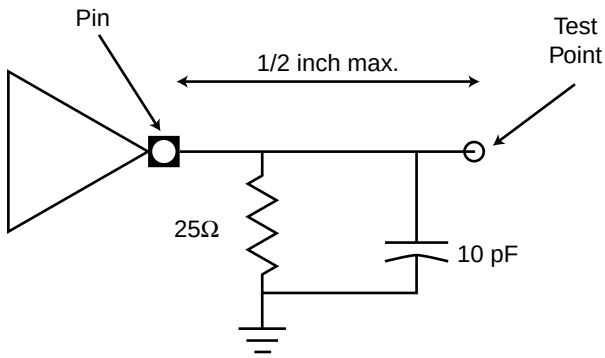


Figure 6. TVAL (max) Falling Edge Test Load

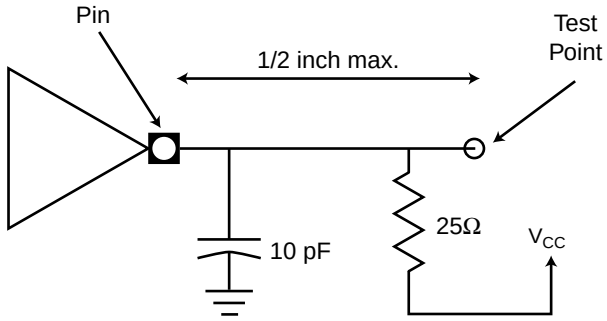


Figure 7. TVAL (min) Test Load

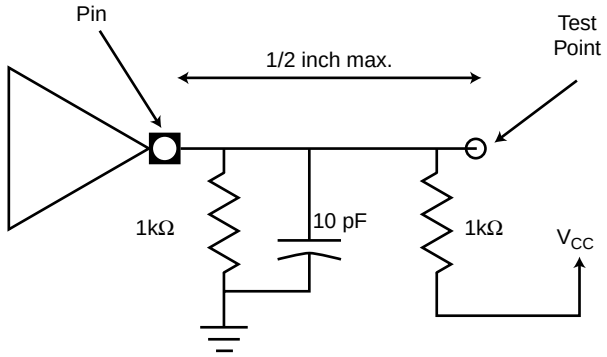
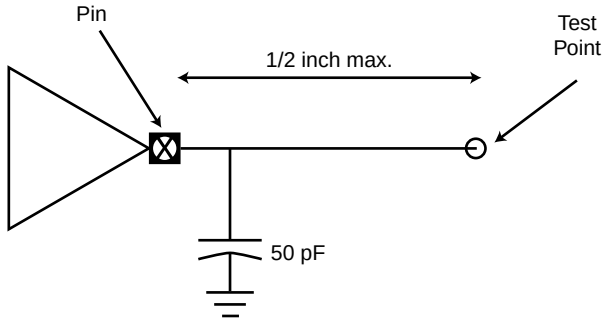


Figure 8. TVAL Test Load (PCI 5 V Signaling Environment)



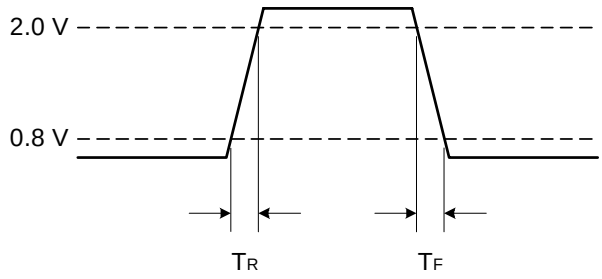
NOTE: Note: 50 pF load used for maximum times. Minimum times are specified with 0 pF load.

4.5.2 Link Interface Timing

Table 17. Rise and Fall Times

Symbol	Parameter	Condition	Min	Max	Unit
TR	Clock rise time	0.8 V to 2.0 V	0.7		ns
TF	Clock fall time	2.0 V to 0.8 V	0.7		ns
TR	Data rise time	0.8 to 2.0 V	0.7		ns
TF	Data fall time	2.0 V to 0.8 V	0.7		ns

Figure 9. Link Interface Rise/Fall Timing



4.5.3 EEPROM Interface

Table 18. Link Interface Clock Requirements

Symbol	Parameter	Min	Typ	Max	Unit
TPW	EE_SK pulse width		TPERIOD*128		ns

a. The EEPROM clock is derived from a 125 MHz internal clock.

Table 19. Link Interface Clock Requirements

Symbol	Parameter[a]	Min	Typ	Max	Unit
TDOS	EE_DO setup time	TCYC*2			ns
TDOH	EE_DO hold time	0			ns

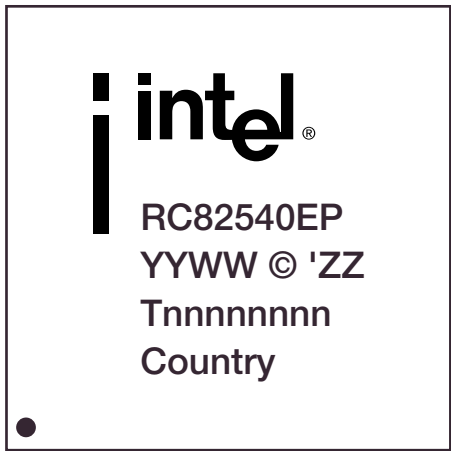
a. The EE_DO setup and hold time is a function of the PCI bus CLK cycle time but is referenced to O_EE_SK.

5.0 Package and Pinout Information

This section describes the 82540EP device, manufactured in a 196-lead ball grid array measuring 15mm X 15mm. External product identification is shown in Figure 10. The nominal ball pitch is 1mm. The pin number-to-signal mapping is indicated beginning with Table 19.

5.1 Device Identification

Figure 10. 82540EP Device Identification Markings



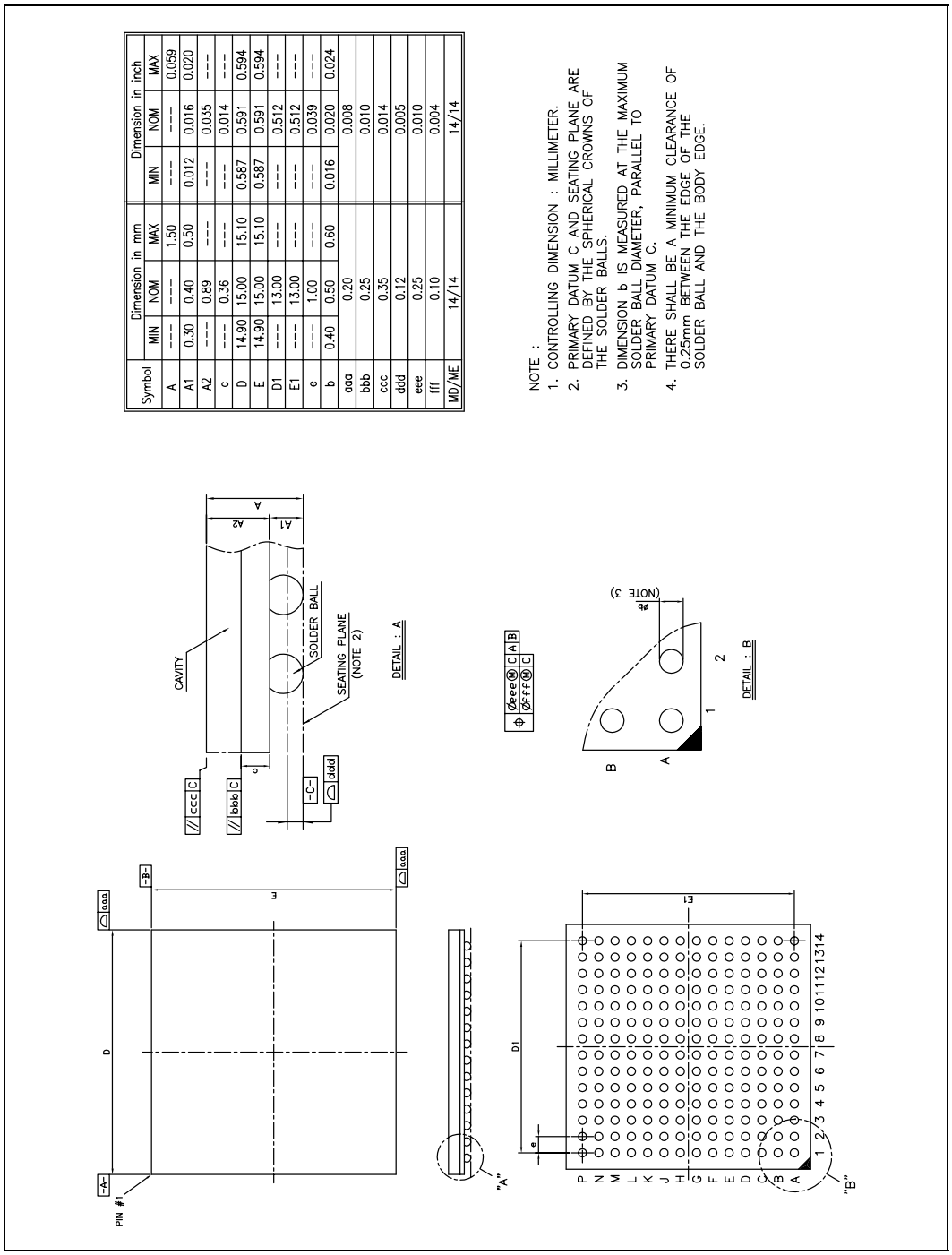
82540EP	Product Name
YYWW	Date Code
Tnnnnnnnn	Lot Trace Code
(c)’ZZ	Copyright Information
Country	Country of Origin Assembly

NOTE: “●“indicates the location of pin 1. It is not an actual mark on the device

5.2 Package Information

The 82540EP device is a 196-lead ball grid array (TFBGA) measuring 15 mm^2. The package dimensions are detailed in Figure 11. The nominal ball pitch is 1 mm.

Figure 11. 82540EP Mechanical Specifications



5.3 Thermal Specifications

The 82540EP device is specified for operation when the ambient temperature (TA) is within the range of 0° C to 70° C.

TC (case temperature) is calculated using the equation:

TC = TA + P (θJA - q JC)

TJ (junction temperature) is calculated using the equation:

TJ = TA + P θJA

P (power consumption) is calculated by using the typical ICC, as indicated inTable 4 of Section 4.0, and nominal VCC. The thermal resistances are shown in Table 18.

Table 18. Thermal Characteristics

Symbol	Parameter	Value at specified airflow (m/s)				Units
		0	1	2	3	
θJA	Thermal resistance, junction-to-ambient	28.1	25.0	23.7	22.8	°C/ Watt
θJC	Thermal resistance, junction-to-case	6.1	6.1	6.1	6.1	°C/ Watt

Thermal resistances are determined empirically with test devices mounted on standard thermal test boards. Real system designs may have different characteristics due to board thickness, arrangement of ground planes, and proximity of other components. The case temperature measurements should be used to assure that the 82540EP device is operating under recommended conditions.

5.4 Pinout Information

Table 19. PCI Address, Data, and Control Signals

Signal	Pin	Signal	Pin	Signal	Pin
PCI_AD[0]	N7	PCI_AD[16]	K1	CBE0#	M4
PCI_AD[1]	M7	PCI_AD[17]	E3	CBE1#	L3
PCI_AD[2]	P6	PCI_AD[18]	D1	CBE2#	F3
PCI_AD[3]	P5	PCI_AD[19]	D2	CBE3#	C4
PCI_AD[4]	N5	PCI_AD[20]	D3	PAR	J1
PCI_AD[5]	M5	PCI_AD[21]	C1	FRAME#	F2
PCI_AD[6]	P4	PCI_AD[22]	B1	IRDY#	F1
PCI_AD[7]	N4	PCI_AD[23]	B2	TRDY#	G3
PCI_AD[8]	P3	PCI_AD[24]	B4	STOP#	H1
PCI_AD[9]	N3	PCI_AD[25]	A5	DEVSEL#	H3
PCI_AD[10]	N2	PCI_AD[26]	B5	VIO	G2
PCI_AD[11]	M1	PCI_AD[27]	B6	IDSEL	A4
PCI_AD[12]	M2	PCI_AD[28]	C6		
PCI_AD[13]	M3	PCI_AD[29]	C7		
PCI_AD[14]	L1	PCI_AD[30]	A8		
PCI_AD[15]	L2	PCI_AD[31]	B8		

Table 20. PCI Arbitration Signals

Signal	Pin
REQ#	C3
GNT#	J3

Table 21. Interrupt Signals

Signal	Pin
INTA#	H2

Table 22. System Signals

Signal	Pin	Signal	Pin	Signal	Pin
CLK	G1	M66EN	C2	RST#	B9

Table 23. Error Reporting Signals

Signal	Pin	Signal	Pin
SERR#	A2	PERR#	J2

Table 24. Power Management Signals

Signal	Pin	Signal	Pin
LAN_PWR_GOOD	A9	AUX_PWR	J12
PME#	A6	CLKRUN#	C8

Table 25. Impedance Compensation Signals

Signal	Pin	Signal	Pin
ZN_COMP	H4	ZP_COMP	G4

Table 26. SMB Signals

Signal	Pin	Signal	Pin	Signal	Pin
SMBCLK	A10	SMBDATA	C9	SMBALRT#	B10

Table 27. EEPROM and Serial FLASH Interface Signals

Signal	Pin	Signal	Pin	Signal	Pin
EE_SK	M10	EE_DI	P10	FL_SCK	N9
EE_DO	N10	FL_CE#	M9	FLSO	P9
EE_CS	P7	FL_SI	M11		

Table 28. LED Signals

Signal	Pin	Signal	Pin
LED0 / LINK#	A12	LED2 / LINK100#	B11
LED1 / ACT#	C11	LED3 / LINK1000#	B12

Table 29. Other Signals

Signal	Pin	Signal	Pin	Signal	Pin
SDP0	N14	SDP6	N13	CTRL_15	P11
SDP1	P13	SDP7	M12	CTRL_25	B13

Table 30. IEEE Test Signals

Signal	Pin
CLK_VIEW	M8

Table 31. PHY Signals

Signal	Pin	Signal	Pin	Signal	Pin
XTAL1	K14	MDI0+	C13	MDI2+	F13
XTAL2	J14	MDI1-	E14	MDI3-	H14
REF	B14	MDI1+	E13	MDI3+	H13
MDI0-	C14	MDI2-	F14		

Table 32. Test Interface Signals

Signal	Pin	Signal	Pin	Signal	Pin
JTAG_TCK	L14	JTAG_TDO	M14	JTAG_RST#	L13
JTAG_TDI	M13	JTAG_TMS	L12	TEST	A13

Table 33. Digital Power Signals

Signal	Pin	Signal	Pin	Signal	Pin
DVDD (1.5V)	E11	DVDD (1.5V)	J8	DVDD (1.5V)	L9
DVDD (1.5V)	E12	DVDD (1.5V)	J9	DVDD (1.5V)	L10
DVDD (1.5V)	G5	DVDD (1.5V)	J10	VDDO (3.3V)	A3
DVDD (1.5V)	G6	DVDD (1.5V)	J11	VDDO (3.3V)	A7
DVDD (1.5V)	G13	DVDD (1.5V)	K5	VDDO (3.3V)	A11
DVDD (1.5V)	H5	DVDD (1.5V)	K6	VDDO (3.3V)	E1
DVDD (1.5V)	H6	DVDD (1.5V)	K7	VDDO (3.3V)	K3
DVDD (1.5V)	H7	DVDD (1.5V)	K8	VDDO (3.3V)	K4
DVDD (1.5V)	H8	DVDD (1.5V)	K9	VDDO (3.3V)	K13
DVDD (1.5V)	H11	DVDD (1.5V)	K10	VDDO (3.3V)	N6
DVDD (1.5V)	J5	DVDD (1.5V)	K11	VDDO (3.3V)	N8
DVDD (1.5V)	J6	DVDD (1.5V)	L4	VDDO (3.3V)	P2
DVDD (1.5V)	J7	DVDD (1.5V)	L5	VDDO (3.3V)	P12

Table 34. Analog Power Signals

Signal	Pin	Signal	Pin	Signal	Pin
AVDDL (2.5 V)	D9	AVDDL (2.5 V)	G12	AVDDL (2.5 V)	L8
AVDDL (2.5 V)	D11				

Table 35. Grounds and No Connect Signals

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
GND	B3	GND	E7	GND	G9	NC	A1
GND	B7	GND	E8	GND	G10	NC	A14
GND	C10	GND	E9	GND	G11	NC	C5
GND	C12	GND	E10	GND	G14	NC	D10
GND	D4	GND	F4	GND	H9	NC	D12
GND	D5	GND	F5	GND	H10	NC	D14
GND	D6	GND	F6	GND	K2	NC	F12
GND	D7	GND	F7	GND	K12	NC	H12
GND	D8	GND	F8	GND	L6	NC	J4
GND	D13	GND	F9	GND	L11	NC	J13
GND	E2	GND	F10	GND	M6	NC	L7
GND	E4	GND	F11	GND	N1	NC	N11
GND	E5	GND	G7	GND	N12	NC	P1
GND	E6	GND	G8	GND	P8	NC	P14

Table 36. Signal Names in Pin Order (Sheet 1 of 6)

Signal Name	Pin
NC	A1
SERR#	A2
VDDO (3.3V)	A3
IDSEL	A4
PCI_AD[25]	A5
PME#	A6
VDDO (3.3V)	A7
PCI_AD[30]	A8
LAN_PWR_GOOD	A9
SMBCLK	A10
VDDO (3.3V)	A11
LED0 / LINK#	A12
TEST	A13
NC	A14
PCI_AD[22]	B1
PCI_AD[23]	B2
GND	B3
PCI_AD[24]	B4

Table 36. Signal Names in Pin Order (Sheet 2 of 6) (Continued)

Signal Name	Pin
PCI_AD[26]	B5
PCI_AD[27]	B6
GND	B7
PCI_AD[31]	B8
RST#	B9
SMBALRT#	B10
LED2 / LINK100#	B11
LED3 / LINK1000#	B12
CTRL_25	B13
REF	B14
PCI_AD[21]	C1
M66EN	C2
REQ#	C3
CBE3#	C4
NC	C5
PCI_AD[28]	C6
PCI_AD[29]	C7
CLKRUN#	C8
SMBDATA	C9
GND	C10
LED1 / ACT#	C11
GND	C12
MDI0+	C13
MDI0-	C14
PCI_AD[18]	D1
PCI_AD[19]	D2
PCI_AD[20]	D3
GND	D4
GND	D5
GND	D6
GND	D7
GND	D8
AVDDL (2.5 V)	D9
NC	D10
AVDDL (2.5 V)	D11
NC	D12
GND	D13
NC	D14

Table 36. Signal Names in Pin Order (Sheet 3 of 6) (Continued)

Signal Name	Pin
VDDO (3.3V)	E1
GND	E2
PCI_AD[17]	E3
GND	E4
GND	E5
GND	E6
GND	E7
GND	E8
GND	E9
GND	E10
DVDD (1.5V)	E11
DVDD (1.5V)	E12
MDI1+	E13
MDI1-	E14
IRDY#	F1
FRAME#	F2
CBE2#	F3
GND	F4
GND	F5
GND	F6
GND	F7
GND	F8
GND	F9
GND	F10
GND	F11
NC	F12
MDI2+	F13
MDI2-	F14
CLK	G1
VIO	G2
TRDY#	G3
ZP_COMP	G4
DVDD (1.5V)	G5
DVDD (1.5V)	G6
GND	G7
GND	G8
GND	G9
GND	G10

Table 36. Signal Names in Pin Order (Sheet 4 of 6) (Continued)

Signal Name	Pin
GND	G11
AVDDL (2.5 V)	G12
DVDD (1.5V)	G13
GND	G14
STOP#	H1
INTA#	H2
DEVSEL#	H3
ZN_COMP	H4
DVDD (1.5V)	H5
DVDD (1.5V)	H6
DVDD (1.5V)	H7
DVDD (1.5V)	H8
GND	H9
GND	H10
DVDD (1.5V)	H11
NC	H12
MDI3+	H13
MDI3-	H14
PAR	J1
PERR#	J2
GNT#	J3
NC	J4
DVDD (1.5V)	J5
DVDD (1.5V)	J6
DVDD (1.5V)	J7
DVDD (1.5V)	J8
DVDD (1.5V)	J9
DVDD (1.5V)	J10
DVDD (1.5V)	J11
AUX_PWR	J12
NC	J13
XTAL2	J14
PCI_AD[16]	K1
GND	K2
VDDO (3.3V)	K3
VDDO (3.3V)	K4
DVDD (1.5V)	K5
DVDD (1.5V)	K6

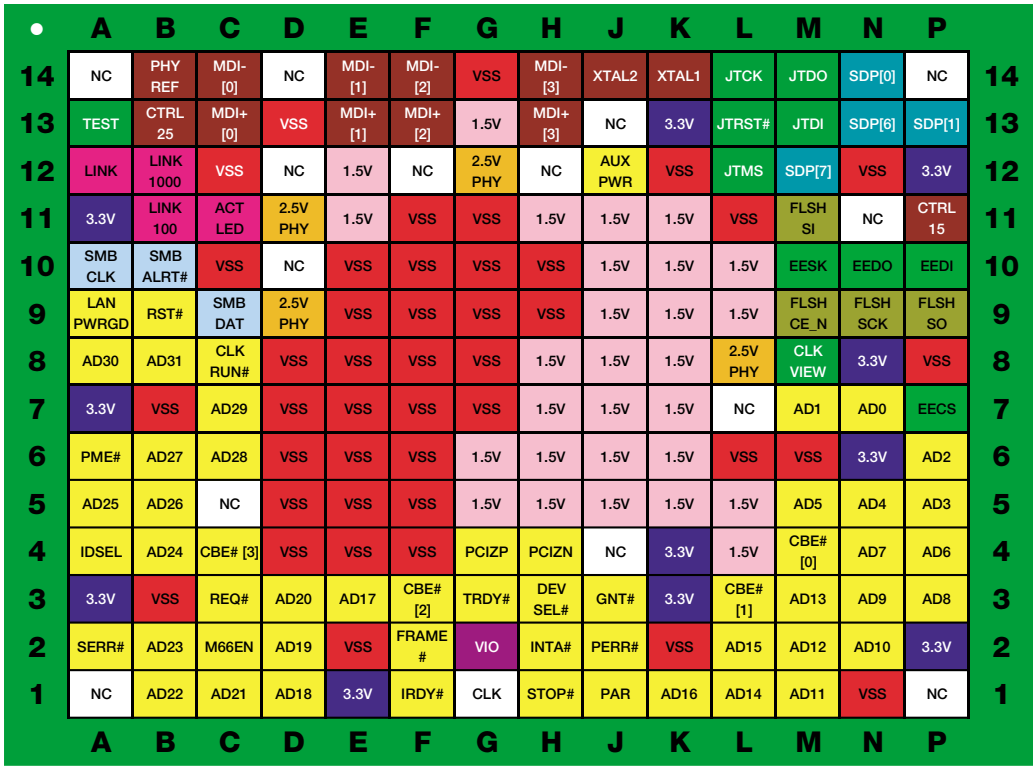
Table 36. Signal Names in Pin Order (Sheet 5 of 6) (Continued)

Signal Name	Pin
DVDD (1.5V)	K7
DVDD (1.5V)	K8
DVDD (1.5V)	K9
DVDD (1.5V)	K10
DVDD (1.5V)	K11
GND	K12
VDDO (3.3V)	K13
XTAL1	K14
PCI_AD[14]	L1
PCI_AD[15]	L2
CBE1#	L3
DVDD (1.5V)	L4
DVDD (1.5V)	L5
GND	L6
NC	L7
AVDDL (2.5 V)	L8
DVDD (1.5V)	L9
DVDD (1.5V)	L10
GND	L11
JTAG_TMS	L12
JTAG_RST#	L13
JTAG_TCK	L14
PCI_AD[11]	M1
PCI_AD[12]	M2
PCI_AD[13]	M3
CBE0#	M4
PCI_AD[5]	M5
GND	M6
PCI_AD[1]	M7
CLK_VIEW	M8
FL_CE#	M9
EE_SK	M10
FL_SI	M11
SDP7	M12
JTAG_TDI	M13
JTAG_TDO	M14
GND	N1
PCI_AD[10]	N2

Table 36. Signal Names in Pin Order (Sheet 6 of 6) (Continued)

Signal Name	Pin
PCI_AD[9]	N3
PCI_AD[7]	N4
PCI_AD[4]	N5
VDDO (3.3V)	N6
PCI_AD[0]	N7
VDDO (3.3V)	N8
FL_SCK	N9
EE_DO	N10
NC	N11
GND	N12
SDP6	N13
SDP0	N14
NC	P1
VDDO (3.3V)	P2
PCI_AD[8]	P3
PCI_AD[6]	P4
PCI_AD[3]	P5
PCI_AD[2]	P6
EE_CS	P7
GND	P8
FL_SO	P9
EE_DI	P10
CTRL_15	P11
VDDO (3.3V)	P12
SDP1	P13
NC	P14

5.5 Visual Pin Reference



•	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
14	NC	PHY REF	MDI-[0]	NC	MDI-[1]	MDI-[2]	VSS	MDI-[3]	XTAL2	XTAL1	JTCK	JTDO	SDP[0]	NC	14
13	TEST	CTRL 25	MDI+[0]	VSS	MDI+[1]	MDI+[2]	1.5V	MDI+[3]	NC	3.3V	JTRST#	JTDI	SDP[6]	SDP[1]	13
12	LINK	LINK 1000	VSS	NC	1.5V	NC	2.5V PHY	NC	AUX PWR	VSS	JTMS	SDP[7]	VSS	3.3V	12
11	3.3V	LINK 100	ACT LED	2.5V PHY	1.5V	VSS	VSS	1.5V	1.5V	1.5V	VSS	FLSH SI	NC	CTRL 15	11
10	SMB CLK	SMB ALRT#	VSS	NC	VSS	VSS	VSS	VSS	1.5V	1.5V	1.5V	EESK	EEDO	EEDI	10
9	LAN PWRGD	RST#	SMB DAT	2.5V PHY	VSS	VSS	VSS	VSS	1.5V	1.5V	1.5V	FLSH CE_N	FLSH SCK	FLSH SO	9
8	AD30	AD31	CLK RUN#	VSS	VSS	VSS	VSS	1.5V	1.5V	1.5V	2.5V PHY	CLK VIEW	3.3V	VSS	8
7	3.3V	VSS	AD29	VSS	VSS	VSS	VSS	1.5V	1.5V	1.5V	NC	AD1	AD0	EECS	7
6	PME#	AD27	AD28	VSS	VSS	VSS	1.5V	1.5V	1.5V	1.5V	VSS	VSS	3.3V	AD2	6
5	AD25	AD26	NC	VSS	VSS	VSS	1.5V	1.5V	1.5V	1.5V	1.5V	AD5	AD4	AD3	5
4	IDSEL	AD24	CBE# [3]	VSS	VSS	VSS	PCIZP	PCIZN	NC	3.3V	1.5V	CBE# [0]	AD7	AD6	4
3	3.3V	VSS	REQ#	AD20	AD17	CBE# [2]	TRDY#	DEV SEL#	GNT#	3.3V	CBE# [1]	AD13	AD9	AD8	3
2	SERR#	AD23	M66EN	AD19	VSS	FRAME #	VIO	INTA#	PERR#	VSS	AD15	AD12	AD10	3.3V	2
1	NC	AD22	AD21	AD18	3.3V	IRDY#	CLK	STOP#	PAR	AD16	AD14	AD11	VSS	NC	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	

Figure 12. Ball Grid Array / Pin Reference for 196-TFBGA (thru-the-top view)