82543GC Gigabit Ethernet Controller Specification Update

June 18, 2004

Revision 2.1

The 82543GC Gigabit Ethernet Controller may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

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REVISION HISTORY

82543GC Gigabit Ethernet Controller Specification Update

Date of Revision	Revision	Description
June 18, 2004	2.1	Initial Public Release

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PREFACE

This document is an update to published specifications. There are two current specification documents:

- 82543GC Gigabit Ethernet Controller Datasheet, Intel Corporation.
- OR-2710 82543GC Gigabit Ethernet Controller Developer's Manual, Intel Corporation.

This document is intended for hardware system manufactures and software developers of applications, operating systems or tools. It contains Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

The changes/errata/clarifications described in this document will be incorporated into the next release of 82543GC Gigabit Ethernet Controller Data Sheet, the 82543GC Gigabit Ethernet Controller Developer's Manual.

NOMENCLATURE

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause 82543GC device behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

COMPONENT IDENTIFICATION VIA PROGRAMMING INTERFACE

82543GC steppings can be identified by the following register contents:

82543GC Stepping	Vendor ID	Device ID	Revision Number
A0	8086h	1001h	00h
A1	8086h	1001h	01h
A2	8086h	1001h	02h

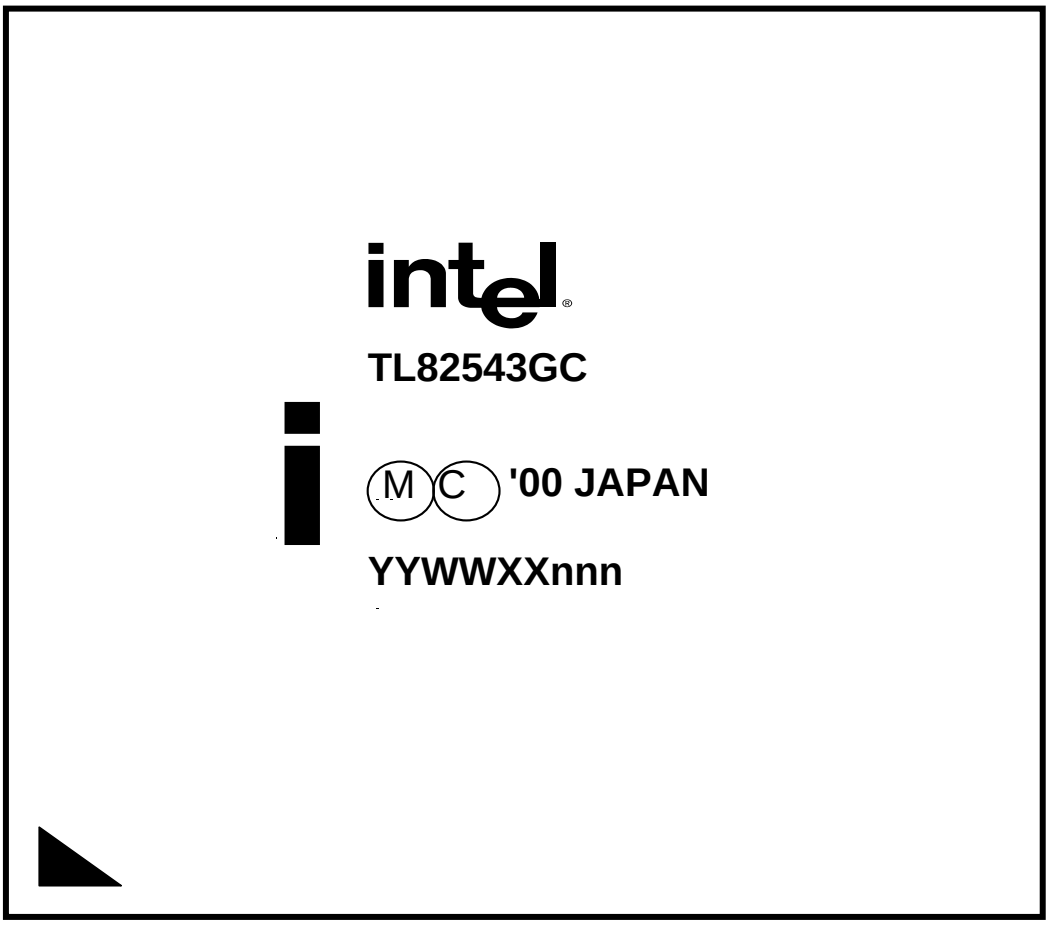
The device also provides an identification number through the Test Access Port.

GENERAL INFORMATION

This section covers the 82543GC device.

82543GC COMPONENT MARKING INFORMATION

Stepping	QDF Number	S- Spec Number	Top Marking	Notes
A0	Q415	S L3N8	FW82543GC	Engineering Samples. May be marked with either QDF number or S-spec number.
A1	Q416	S L3N9	FW82543GC	Engineering Samples. May be marked with either QDF number or S-spec number.
A2	Q417	N/A	FW82543GC or TL82543GC	Engineering Samples. May be marked two ways: with the QDF number and a top mark FW82543GC; or without any QDF or S-spec number, and a top mark TL82543GC.
	N/A	N/A	TL82543GC	Production Devices. Marked without QDF or S-spec numbers and bear a top mark TL82543GC.



The legend for the manufacturing code is as follows:

YY = Assembly input year

WW = Assembly workweek

XXnnn = Complete lot traceability code (use for issue reporting)

XX = Mask/assembly spec

nnn = Lot history code

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed 82543GC steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLES

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

No.	A0	A1	A2	Plans	SPECIFICATION CHANGES	Page	Affected Document
1	X	X	X	NoFix	GMII Setup and Hold Times	9	Datasheet
No.	**A0**	**A1**	**A2**	**Plans**	**ERRATA**	**Page**	**Notes**
1	X	X	X	NoFix	MDI Control Register Returns Incorrect Values	9	
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3	X			Fixed	Late Collision Statistics May Be Incorrect	9	
4	X			Fixed	Some Registers Cannot be Accessed During Reset	10	
5	X	X	X	NoFix	DAC Accesses May Not Be Interpreted Correctly	10	
6	X	X	X	NoFix	Flash Memory Functions Incorrectly in 64-Bit Address Space	10	
7	X			Fixed	Excessive Errors in 100Mb Half-Duplex Mode	10	
8	X			Fixed	48 Bit Preambles Sent in 10Mb and 100Mb Operation	11	
9	X			Fixed	CRS Detection Takes Too Long in MII Half-Duplex Mode	11	
10	X	X	X	NoFix	DMA Early Receive Function Does Not Work	11	
11	X			Fixed	ILOS Bit Copied Incorrectly from EEPROM to Speed Bits	11	
12	X	X	X	NoFix	Gigabit Half-Duplex Mode Operates Incorrectly	11	
13	X	X	X	NoFix	Zero-Byte PCI Bus Writes	12	
14	X	X	X	NoFix	TCP Segmentation Feature Operates Incorrectly	12	
15	X	X		Fixed	Incorrect Checksum Calculation and Indication	12	
16	X			Fixed	Transmitter Affected by Discarding Packets	12	
17	X			Fixed	Flash Memory Address Conflicts	13	
18	X	X	X	NoFix	Packet Buffer Memory Address Conflicts	13	
19	X			Fixed	Transmit Packet Corruption of Small Packets	13	
20	X			Fixed	Receive Packet Buffer Corruption When Nearly Full	13	
21	X	X		Fixed	Receive Packet Loss in 100Mb Half-Duplex Operation	14	
22	X	X	X	NoFix	TNCRS Statistic Register Has Live Count in Full-Duplex Mode	14	
23			X	NoFix	Receive IP Checksum Offload Disabled	14	
24	X	X	X	NoFix	EEPROM Initializes Software Defined Pins Incorrectly	14	
25	X	X	X	NoFix	Continuous XOFFs Transmitted When Receive Buffer Is Full	15	

26	X	X	X	NoFix	Default Speed Selection May Depend on EEPROM Presence	15	
27	X	X	X	NoFix	Link Status Change Interrupt Only Occurs If Link is Up	15	
28	X	X	X	NoFix	Early Transmit Feature Does Not Operate Correctly	15	
29	X	X	X	NoFix	TDO Output Not Floated When JTAG TAP Controller Inactive	16	
30	X	X	X	NoFix	Initialization Ignores Incorrect EEPROM Signature	16	
31	X	X	X	NoFix	Internal Loopback Difficulties	16	
32	X	X	X	NoFix	Collision Pin Not Ignored in TBI Mode	16	
33	X	X	X	NoFix	Receive Descriptor Writeback Problems for Packets Spanning Multiple Buffers	17	
34	X	X	X	NoFix	Illegal Oversize Packets Overflow Receive FIFO	17	
35	X	X	X	NoFix	Transmit Descriptor Writeback Problem with Non-Zero WTHRESH	17	
36	X	X	X	NoFix	Bus Initialization with Some Chipsets	17	
37	X	X	X	NoFix	Use of Receive Delay Timer Ring Register (RDTR) Causes Occasional Lockups	18	
38	X	X	X	NoFix	Transmit TCP Checksum Modified if Calculated as 0x0000	18	
No.	**A0**	**A1**	**A2**	**Plans**	**SPECIFICATION CLARIFICATIONS**	**Page**	**Affected Document**
1	X	X	X	Doc Change	0-70C Ambient Temperature Range	19	Datasheet
2	X	X	X	Doc Change	Receiver Enabling and Disabling	19	Developer's Manual
No.	**A0**	**A1**	**A2**	**Plans**	**DOCUMENTATION CHANGES**	**Page**	**Affected Document**
1	X	X	X	Doc Replaced	TX/RX Descriptor Register Addresses	19	Developer's Manual
2	X	X	X	Doc Replaced	Auto Speed Detect Function Requires CTRL.SLU Bit to Be Set	20	Developer's Manual
3	X	X	X	Doc Replaced	Values Programmed to Some Registers While in Reset Do Not Persist	20	Developer's Manual
4	X	X	X	Doc Change	JTAG Port Operation	20	Datasheet and Developer's Manual.
5	X	X	X	Doc Change	Register Summary Uses Improper Page Reference Format	20	Developer's Manual
6	X	X	X	Doc Change	Change O_EN_CDET output to NO_CONNECT	21	Datasheet
7	X	X	X	Doc Change	Change Recommended Tx IPG Programming Value for 10/100/1000BASE-T	21	Developer's Manual
8	X	X	X	Doc Change	Remove Transmit Report Status Sent Function	21	Developer's Manual
9	X	X	X	Doc Change	Remove Transmit DMA Pre-fetching and Preemption Functions (TXDMAC)	21	Developer's Manual
10	X	X	X	Doc Change	Remove Transmit Burst Timer Control Function (TBT)	22	Developer's Manual
11	X	X	X	Doc Change	Remove Adaptive IFS Throttle Function (AIT)	22	Developer's Manual

SPECIFICATION CHANGES

1. GMII Setup and Hold Times

Problem: The data sheet contains incorrect setup and hold time specifications for the GMII interface.

The old setup and hold times were 2.5ns minimum and 4ns. typical.

For the receive signals, the new setup time is 2.0ns. (min.) the new hold time is 0ns. (min.). For the transmit signals, the new setup time is 2.5ns. (min.) and the new hold time is 0.5ns. (min.) Documentation will change to show the new values.

Affected Specs: AC Timings section of 82543GC Gigabit Ethernet Controller Datasheet Rev. 2.02.

ERRATA

1. MDI Control Register Returns Incorrect Values

Problem: MDIO reads through the MDI control register return wrong values.

Implication: The Management Data Interface register is necessary for the controller to communicate serially with GMII/MII PHY devices through the B_MDIO pin.

Workaround: Route MDIO and MDC pins from an external PHY device to B_SDP (Software Defined) pins and add appropriate software to capture the MDI data.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

2. Descriptor Queue Maximum Size Limitation

Problem: When the 82543GC device initiates a PCI cycle to access data, it is possible for the target to issue a “retry”. A retry is a target disconnect without data transfer. In response, the 82543GC controller may attempt another read or write cycle to a different address instead of retrying the same memory location. In a PC environment, it is possible that the target chipset will hang, generate an NMI or exhibit other errors.

Implication: This erratum affects the 82543 device’s ability to access data correctly from the descriptor list using its DMA process.

Workaround: Do not allow the controller to have more than 256 active descriptors in either the receive descriptor ring or the transmit descriptor ring. In other words, program the device so the receive tail register does not exceed the receive head register by more than 0x100 and the transmit tail register does not exceed the transmit head register my more than 0x100. There are two ways to achieve this goal:

- Set up the software driver to never manage more than 256 descriptors per ring.
- Program the driver to actively calculate the difference between descriptor head and tail. This way, the software driver can manage many more total descriptors, but it never moves the tail pointer far enough to make excessive descriptors active.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

3. Late Collision Statistics May Be Incorrect

Problem: In gigabit half duplex mode, the late collision statistic register may not count late collision events correctly.

Implication: The actual number of late collisions in half duplex mode may be higher than reflected in the statistic register.

Workaround: None.

Status: This erratum was resolved in the A1 stepping of the 82543GC Gigabit Ethernet Controller.

4. Some Registers Cannot Be Accessed During Reset

Problem: PCI accesses to transmit descriptor registers will not succeed if the 82543GC controller is in a transmit reset state. Similarly, PCI accesses to receive descriptor registers will not succeed if the 82543GC controller is in a receive reset state. Affected registers include the transmit descriptor registers (offsets 0x420 – 0x440), receive descriptor registers, diagnostic packet buffer head/tail registers (offsets 0x8000 – 0x8018) and the flow control threshold registers (offsets 0x160 – 0x168).

Implication: Accesses to any of these registers during reset states will result in an infinite PCI retry state.

Workaround: Software can check that the 82543GC device is not in a reset state before accessing the registers.

Status: Intel resolved this erratum in the A1 stepping of the 82543GC Gigabit Ethernet Controller. However, software still should not attempt to write to these registers during reset states because the data written will not be retained. Documentation will be updated to specify which registers are held in reset during which conditions. See Documentation Change #3.

5. DAC Accesses May Be Interpreted Incorrectly

Problem: When the 82543GC device is mapped to a 64-bit PCI address space as a target device, it does not always handle dual-address cycle (DAC) accesses correctly.

Implication: The 82543GC Gigabit Ethernet Controller is designed to function with addresses above the 4 GByte PCI boundary and can advertise this capability in base address register 0. As a bus master, it can fully utilize this space and initiates all 64-bit DAC cycles correctly. However, it does not always respond to DAC cycles correctly as a target device. In addition, accesses to flash memory may work incorrectly. See Erratum #7, Flash Memory Functions Incorrectly in 64-Bit Address Space.

Workaround: Bit 0x0D in the EEPROM space at byte 0x0A denotes 64-bit address mapping if cleared to “0”. (This is the default configuration.) Program the bit to logic “1” to denote 32-bit address space. As an added precaution, software drivers can check this bit and render a shutdown with an error message if a “0” is detected.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

6. Flash Memory Interface Functions Incorrectly in 64-Bit Address Space

Problem: When the 82543GC controller is mapped to a 64-bit address space as a target, the flash memory space is also mapped to a 64-bit space. However, the flash memory interface hardware is implemented for 32 bit addressing and may fail in response to 64-bit addressing.

Implication: This erratum is directly related to Erratum #5 (DAC Accesses May Be Interpreted Incorrectly). Mapping flash memory to an address above 4 GBytes may result in PCI master aborts or other incorrect behavior.

Workaround: The workaround is identical to the workaround for Erratum #5, DAC Accesses May Be Interpreted Incorrectly. Bit 0x0D in the EEPROM space at byte 0x0A denotes 64-bit address space if cleared to “0”. (This is the default configuration.) Program this bit to logic “1” to denote 32-bit address space. As an added precaution, software drivers can check this bit and render a shutdown with an error message if a “0” is detected.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

7. Excessive Errors in 100Mb Half-Duplex Mode

Problem: When the 82543GC Gigabit Ethernet Controller operates in 100Mb mode and network traffic causes collisions, the device will experience excessive CRC, alignment and RX_ERR errors. Intel observed late collision situations where the 82543GC device attempted packet transmission while another station was transmitting and after the collision window expired. The observed error rates were approximately one error per 300 good received packets. Error rates this high cause excessive packet loss, which can lead to protocol timeouts. The problem occurs with multiple PHY devices and a variety of Ethernet hub and cabling configurations.

Implication: Data transfer performance is substantially reduced due to error packets.

Workaround: None.

Status: Intel resolved this erratum in the A1 stepping of the 82543GC Gigabit Ethernet Controller.

8. 48 Bit Preambles Sent in 10Mb and 100Mb Operation

Problem: The 82543GC device transmits 48 bit preambles instead of 56 bit preambles for 10Mb and 100Mb operation.

Implication: Certain 10Mb and 100Mb repeaters will only tolerate 56 bit preambles, so packets transmitted by the 82543GC controller will be incompatible. A product example is the Intel InBusiness 4 Port Fast Hub, which is based on a Broadcom 5205 repeater device.

Workaround: None.

Status: Intel resolved this erratum in the A1 stepping of the 82543GC Gigabit Ethernet Controller.

9. CRS Detection Takes Too Long in MII Half-Duplex Mode

Problem: When the 82543GC controller is operated in half-duplex mode, it can take up to 16 bit times to detect Carrier Sense (CRS) assertion.

Implication: The IEEE specification is 8 bit times. Functional problems are not anticipated in operating networks, however.

Workaround: None.

Status: Intel resolved this erratum in the A1 stepping of the 82543GC Gigabit Ethernet Controller.

10. DMA Early Receive Function Does Not Work

Problem: When DMA early receive operation is enabled on the 82543GC device and a DMA receive underrun occurs, the controller may erroneously place data into the packet descriptors.

Implication: The early receive function cannot be used.

Workaround: None.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

11. ILOS Bit Copied Incorrectly from EEPROM to Speed Bits

Problem: When the 82543GC controller loads configuration information from EEPROM, it maps the Invert Loss of Signal (ILOS) bit into the Speed Selection bits in the device control register.

Implication: Both the ILOS and Speed settings will be incorrect.

Workaround: Software should write correct bit values into the control register.

Status: Intel resolved this erratum in the A1 stepping of the 82543GC Gigabit Ethernet Controller.

12. Gigabit Half-Duplex Mode Operates Incorrectly

Problem: Several problems prevent proper gigabit half-duplex operation.

Implication: Do not use GMII half-duplex operation. GMII full-duplex and MII (10/100Mb) half-duplex modes are unaffected.

Workaround: None.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

13. Zero-Byte PCI Bus Writes

Problem: The 82543GC Gigabit Ethernet Controller can generate zero-byte writes on a 32-bit PCI bus because it is has a 64-bit internal architecture. A zero-byte access is defined as a data transfer with IRDY# and TRDY# asserted but none of the byte enables asserted.

Implication: Zero-byte writes are allowed by the PCI specification. However, an erratum in the 450GX PC chipset causes incompatibility with the 82543GC controller. The erratum is titled, #29 Hang with Zero-Byte Write Followed by a Nonzero-Byte Write. The erratum states, “If an inbound PCI zero-byte write is followed by a PCI nonzero-byte write, and a specific set of timing circumstances exist, the chipset can become out of sync.”

Workaround: In a 450GX chipset system, change the system’s IOQ depth from eight to one. In most systems, the IOQ depth parameter is accessible through the BIOS setup utility.

Status: Intel does not plan to resolve this problem in a future stepping of the 82543GC Gigabit Ethernet Controller.

14. TCP Segmentation Feature Operates Incorrectly

Problem: Several errata prevent proper TCP segmentation operation, in particular, concurrency with other DMA events and payload mismatch trapping. At least one of the errata can cause transmit operation to hang.

Implication: Do not use the TCP segmentation feature.

Workaround: None.

Status: Some of the errata were corrected in the A1 stepping. At least one severe transmit problem was not corrected. Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

15. Incorrect Checksum Calculation and Indication

Problem: Several errata can cause checksum calculations (packet, TCP, UDP, IP, etc.) to be performed incorrectly or to be misreported. These problems can occur on both transmitted and received packets and can also relate to packet size.

Implication: Checksum offloading is not reliable and should not be used.

Workaround: None. Checksums should be calculated in software rather than being offloaded to 82543GC hardware.

Status: Some of the problems were corrected in the A1 stepping, including the problem of incorrect UDP checksum indication. The remaining problems were corrected in the A2 stepping, with the exception of receive IP checksum. See erratum #23, “Receive IP Checksum Offload Disabled.”

16. Transmitter Affected by Discarding Packets

Problem: When the 82543GC device is forced to discard a transmit packet because of non-transmission, internal pointers may get corrupted and lead to bad packet transmission or a hang condition. The situations that can trigger this behavior are:

- **(a.)** Half-duplex operation and the number of collisions exceeds the programmed threshold.
- **(b.)** Half–duplex operation and a late collision occurs with re-transmit disabled for late collisions.
- **(c.)** Transmit underrun with re-transmit disabled for underruns.

Implication: Precautions must be taken so that the 82543GC device does not discard packets it cannot transmit.

Workaround: When using half-duplex mode, program the 82543GC Gigabit Ethernet Controller for a very high collision threshold and allow it to retransmit packets that encounter a late collision. Also, if the “early transmit” feature is used, configure the device to retransmit packets that encounter underruns.

Status: Intel resolved this erratum in the A1 stepping of the 82543GC Gigabit Ethernet Controller.

17. Flash Memory Address Conflicts

Problem: Accesses to certain flash memory addresses will not succeed because of address conflicts with registers in the 82543GC device. Example addresses include offsets 2000h or 3000h. This erratum is closely related to erratum #18, Packet Buffer Memory Address Conflicts.

Implication: The flash memory interface cannot be used.

Workaround: None.

Status: Intel resolved this erratum in the A1 stepping of the 82543GC Gigabit Ethernet Controller.

18. Packet Buffer Memory Address Conflicts

Problem: Accesses to certain packet buffer memory addresses will not succeed because of address conflicts with registers in the 82543GC device. Example addresses include offsets 12000h or 13000h. This erratum is closely related to erratum #17, Flash Memory Address Conflicts.

Implication: Software cannot directly access packet buffer memory. Such accesses are typically performed only for diagnostic purposes.

Workaround: None.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

19. Transmit Packet Corruption of Small Packets

Problem: When the 82543GC Ethernet Controller is transmitting and receiving simultaneously, it is possible that short packets will be corrupted before transmission. In systems with a 64-bit, 66 MHz PCI bus, packets up to 148 bytes can be affected. In systems with a 32-bit and/or 33 MHz bus, packets up to 64 bytes can be affected. In both cases, the corrupted data will appear in the last 16 bytes of data. The data corruption occurs before CRC calculation.

Implication: Since the CRC is calculated after the problem occurs, corrupted short packets can be transmitted on the wire without indication of corruption (except for any protocol checksum embedded in the packet).

Workaround: For systems with a 64-bit, 66 MHz PCI bus, software should pad all packets equal to 148 or less bytes with an additional 16 bytes of pad data. The value of the data does not matter, since the data may be “sacrificed” to the corruption problem and the protocol stack at the receiving end station will ignore it anyway. For systems with a 32-bit and/or 33 MHz bus, software should pad the packets up to the Ethernet minimum of 64 bytes (including CRC).

Status: Intel resolved this erratum in the A1 stepping of the 82543GC Gigabit Ethernet Controller.

20. Receive Packet Buffer Corruption When Nearly Full

Problem: When the size of a received packet comes within a 64-bit word of filling up all the space in the packet buffer memory, internal header information may not get updated properly for the packet. Subsequent DMA cycles may transfer corrupted data from the packet buffer into the host system memory. The corrupted packets may be of random length, frequently exceeding the maximum Ethernet size.

When the size of a received packet exceeds the space in the packet buffer memory, the 82543GC Gigabit Ethernet Controller will drop the packet. This behavior is normal and is not affected by the erratum.

Implication: Software cannot directly access packet buffer memory. Such accesses are typically performed only for diagnostic purposes.

Workaround: It may not be possible to prevent the problem, requiring software to screen for packets that exceed maximum Ethernet frame size. When such a packet is found, software should reset the device.

In addition, a combination of techniques may be required to effectively reduce occurrences:

(a.) Place the device on a high-bandwidth PCI bus (64 bits @ 66 MHz) if possible. Use a dedicated slot if one is available.

(b.) Increase allocation of buffers and receive descriptors to start.

(c.) Enable flow control.

Status: Intel resolved this erratum in the A1 stepping of the 82543GC Gigabit Ethernet Controller.

21. Receive Packet Loss in 100Mb Half-Duplex Operation

Problem: When the 82543GC Ethernet Controller is operating in half-duplex mode at 100Mb, a good packet may get dropped following a collision with reception of a very short collision fragment. In this situation, a portion of the preamble from the collision fragment gets appended to the incoming good packet. The good packet will then be dropped because it has an invalid CRC. It will also be likely not to pass through an address filter.

This erratum is affected by the link partner's behavior after collisions. The problem may not be seen with some link partners, particular those that are not in strict IEEE compliance with respect to collisions.

Implication: The 82543GC Gigabit Ethernet Controller cannot be used in half-duplex 100Mb operation.

Workaround: None.

Status: Intel resolved this erratum in the A1 stepping of the 82543GC Gigabit Ethernet Controller.

22. TNCRS Statistic Register Has Live Count in Full-Duplex Mode

Problem: The Transmit with No Carrier Sense Statistic (TNCRS) has no meaning in full-duplex operation. However, it has been observed to contain an incrementing value.

Implication: The TNCRS counter is defined to indicate the number of half-duplex frame transmissions in which the Carrier Sense input (I_CRS) was not asserted by a PHY. This operation is unaffected by the erratum.

Workaround: Software should ignore the TNCRS statistic in full-duplex mode.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

23. Receive IP Checksum Offload Disabled

Problem: When Intel resolved Erratum #15, "Incorrect Checksum Calculation and Indication," it was not possible to resolve a problem affecting receive IP checksums. To ensure against user problems, the receive IP checksum offload function was completely disabled.

Implication: The 82543GC controller will ignore the IP Checksum Offload Enable Bit (RXCSUM.IPOFL). IP Checksum Error Bits in the receive descriptors (RDESC.ERRORS Bit 6) will always read "0". This erratum does not affect any other checksum calculation.

Workaround: None. Receive IP checksums should be calculated in software.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

24. EEPROM Initializes Software Defined Pins Incorrectly

Problem: Bits SWDPIO_EXT[7:4] of Initialization Control Word 2 in the EEPROM are supposed to map to bits SWDPIOHI[11:8] in the Extended Device Control Register at offset 0x00018. Instead, the bits map to SWDPINSHI[7:4] of that register.

Implication: The input/output characteristic of some of the software-defined pins could be assigned incorrectly.

Workaround: Program these bits in the Extended Device Control Register correctly in software.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

25. Continuous XOFFs Transmitted When Receive Buffer Is Full

Problem: When the receive FIFO is full (or within a quad word of full), the 82543GC controller will send XOFFs continuously. The receive buffer will fill up if there are insufficient receive descriptors or insufficient memory buffers. This condition can occur under heavy network traffic loads.

Implication: When the controller is sending continuous XOFFs, it cannot transmit any data packets in the transmit FIFO.

Workaround: Set up a watchdog timer in the software driver to monitor that packets given to the 82543GC device are actually transmitted. If packet transmission is not acknowledged after 2-3 seconds, the host system should be notified to reset the Ethernet controller. At this time, the driver should return memory resources to the operating system for reallocation.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

26. Default Speed Selection May Depend on EEPROM Presence

Problem: When the controller is configured for GMII operation and auto-speed detection is disabled, the default speed setting (CTRL.SPEED) will depend on whether a valid EEPROM is present, as determined by the signature bits. If a legitimate EEPROM is determined not to be present, the controller will use 10b as the speed selection bits in the Device Control Register, resulting in a speed of 1000 Mb/s. If an EEPROM is determined to be present, the controller will use 00b as the speed selection bits, resulting in a speed of 10 Mb/s.

Implication: This erratum could cause the 82543GC controller to initially be configured at the wrong speed if it is being used in an application for twisted pair copper wiring. Note that the 82543GC device has another erratum related to EEPROM detection (Erratum #29, “Initialization Ignores Wrong EEPROM Signature”). Employing the workaround to Erratum #29 requires an EEPROM to be present in all 82543GC designs. Thus, the default speed setting is most likely to be seen as 10 Mb/s.

Workaround: Software should program the CTRL.SPEED bits to the desired speed and not expect the controller to default to gigabit.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

27. Link Status Change Interrupt Only Occurs If Link is Up

Problem: If link is lost, the controller may not always generate a link status change interrupt. This erratum only applies to the TBI (fiber) mode of operation.

Implication: The system may fail to notice loss of link if it relies solely on receiving an interrupt as notification.

Workaround: The Interrupt Cause Status Register will correctly indicate a link status change event even if the interrupt does not occur. The software driver can query this register. The software driver can also look for sequence errors as an indication that link has been lost.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

28. Early Transmit Feature Does Not Operate Correctly

Problem: Use of the early transmit function may cause hangs in 10/100 Mb/s operation.

Implication: The early transmit feature is only applicable to 10/100 Mbps operation, where it was expected to improve overall data transfer rates. With the feature enabled, the 82543GC controller may lock up or exhibit other problems; insignificant performance gains were observed.

Workaround: None. Do not use the early transmit function.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller. Documentation will change to remove text referring to this feature and its associated registers.

29. TDO Output Not Floated When JTAG TAP Controller Inactive

Problem: When the TAP controller is inactive, the TDO output remains driven. This behavior does not meet the IEEE 1149.1 (JTAG) specification.

Implication: The TDO output should float when the TAP controller is not being scanned. The specification requires the ability to float the TDO output in order to allow multiple scan chains to be connected in parallel.

Workaround: Do not connect the 82543GC device's TAP controller in parallel with other JTAG chains. Note that the 82543GC device does not support the JTAG scan or bypass instructions. These limitations prevent series connections of the TAP controller as well.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

30. Initialization Ignores Incorrect EEPROM Signature

Problem: When the 82543GC controller powers up, it reads initialization values from EEPROM space. If Initialization Control Word 1 bits 15:14 (the signature bits) equal 01b, the controller senses that an EEPROM is present and continues processing the initialization values. If the controller detects any other value, it Is supposed to abort processing initialization data and use its defaults instead. With this erratum, the controller continues processing the EEPROM initialization values even if the signature bits are incorrect.

Implication: This operation could lead to improper initialization from a corrupt EEPROM or from a non-existant EEPROM. Note that Erratum #26 also

Workaround: Ensure that an EEPROM is always present and that the signature bits are correct. EEPROMs should also always be present to work around Erratum #5, "DAC Accesses May Be Interpreted Incorrectly".

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

31. Internal Loopback Difficulties

Problem: Link must be present for internal loopback, and loopback operation varies among MII, GMII and TBI modes. Loopback cannot be entered directly from 10 Mb/s operation because the loopback data is sampled by 100 Mb/s clocks.

Implication: Internal loopback testing may be impractical when a real link partner is not present or when a cable is not present. Extra software coding may be required to develop satisfactory test routines.

Workaround: The internal loopback path is the same for all modes, but the link requirements differ. In all cases the controller must sense that link is up prior to entering loopback. To enter loopback from 100 Mb/s operation when an active link partner is not present, toggle the ILOS (Invert Loss of Signal) bit in the Device Control Register to "trick" the controller into sensing link is up. For GMII mode (1000 Mb/s), force link if a working gigabit link partner is not present. For TBI mode, if a link partner is not present, it is also possible to toggle the ILOS bit to simulate link acquisition. In some cases it may be more practical to use external (PHY or transceiver) loopback instead of internal loopback.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

32. Collision Pin Not Ignored in TBI Mode

Problem: Asserting the collision input signal (COL) can cause the transmitter to hang intermittently in TBI mode.

Implication: When the 82543GC Gigabit Ethernet Controller is in TBI mode, the collision signal is meaningless because receive and transmit channels each have their own dedicated optical fibers. Nevertheless, the pin must be tied off carefully.

Workaround: For TBI mode operation, use a pulldown resistor on the COL input hold it in the deasserted state.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

33. Receive Descriptor Writeback Problems for Packets Spanning Multiple Buffers

Problem: Receive descriptors are typically written back to memory either upon receive interrupts or opportunistically in between writing data buffers. When a received Ethernet packet exceeds the size of a single receive buffer, corrupted receive descriptor writebacks may occur and the controller may hang. The conditions for this erratum are specific:

- The controller is programmed to write back receive descriptors upon a receive interrupt, the interrupt has not yet been triggered, and
- The controller has a programmed descriptor writeback threshold (RXDCTL.WTHRESH), the number of receive descriptors consumed thus far by the packet is equal to or greater than the threshold.

Implication: Corrupted descriptor writebacks may include writing back unconsumed descriptors, descriptor writebacks to incorrect addresses, or writebacks missed altogether. In addition, the device may cease to access the PCI bus or cease packet reception. If the device hangs, a full software or hardware reset is needed.

Workaround: If the system uses buffers smaller than the maximum allowed packet size, take the following precautions:

- Configure the receive interrupt to occur immediately on end-of-packet by programming RDTR = 0.
- Configure the descriptor writeback threshold WTHRESH to a value that will not result in a writeback in the middle of a packet. Packets may be 1514 bytes or up to 16K bytes if long packets are enabled. It is recommended that the RXDCTL.GRAN bit be set to 1 descriptor and WTHRESH set to the maximum number of descriptor buffers the maximum size packet will consume.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

34. Illegal Oversize Packets Overflow Receive FIFO

Problem: The controller should drop invalid Ethernet packets, but frames exceeding the maximum legal size can overflow the receive FIFO, causing a lock up. This problem has only been reported in a test environment with an IXIA packet generator.

Implication: The 82543GC controller can receive frames up to the size of the receive packet buffer without difficulty. If the 82543GC controller locks up due to an oversize packet, a full software or hardware reset is needed.

Workaround: Driver software should ensure that a minimum of 16K is allocated to the receive FIFO. Packets larger than this size should not be present on the LAN.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

35. Transmit Descriptor Writeback Problems with Non-Zero WTHRESH

Problem: Transmit descriptors are typically written back to memory either upon transmit interrupts or opportunistically in between reading data buffers. When the controller has a programmed writeback threshold (TXDCTL.WTHRESH), it will attempt to write back full descriptors instead of just a status byte. The controller may incorrectly calculate the length of the writeback operation, causing corrupted descriptor writebacks. This erratum is closely related to Erratum #33. “Receive Buffer Writeback Problems for Packets Spanning Multiple Buffers.”

Implication: Corrupted descriptor writebacks may include writing back unconsumed descriptors, descriptor writebacks to incorrect addresses, or writebacks missed altogether. In addition, the device may cease to access the PCI bus or cease packet transmission. If the device hangs, a full software or hardware reset is needed.

Workaround: Leave WTHRESH at its default value of 0. Descriptors will be written back immediately.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

36. Bus Initialization with Some Chipsets

Problem: Upon initialization, the 82543GC controller samples the REQ64# signal on the rising (inactive) edge of RST#. If REQ64# is sampled low (asserted), the controller starts up with a 64-bit bus width.

The PCI Local Bus Specification calls for 0 ns. minimum input hold time on this signal. However, the 82543GC controller requires 1 ns. input hold time.

Implication: If the signal does not have sufficient hold time, the 82543GC controller could power up with incorrect bus width (64 versus 32 bits).

Many bridges and chipsets drive the REQ64# signal with a full clock of hold time past the rising edge of RST# and this problem will not be encountered. Other loads on the PCI bus may affect the severity of the problem.

Workaround: For embedded designs, verify that the system bridge will deliver a full clock of hold time. If the problem is encountered on an add-in board, try moving the board to a connector on another bus segment.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82545EM/82546EB Gigabit Ethernet Controllers.

37. Use of Receive Delay Timer Ring Register (RDTR) Causes Occasional Lockups

Problem: The 82543GC Controller Receive Delay Timer Ring Register (RDTR) is used to delay interrupt notification until a number of microseconds elapse past the last receive packet in a sequence of packets. Under high traffic conditions, this function can occasionally lead to lockups of both receive and transmit. The lockups are due to a request queue problem in the DMA control logic.

Implication: If lockup occurs, either a hardware or software reset will be required. Ethernet performance under some OSes (e.g., Linux) will be reduced if the feature is disabled.

Workaround: Do not use the receive delay timer ring. Leave RDTR at its 0x00000000 default. Other techniques can be used to moderate receive interrupts: not using descriptor writebacks, or querying the receive descriptor head pointer (approximate indication of descriptors used).

Intel's Linux driver continues to use RDTR, but documentation warns to turn it off if problems are seen. Other Intel drivers did not previously use the feature.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

38. Transmit TCP Checksum Incorrectly Modified if Calculated as 0x0000

Problem: If the controller calculates a transmit TCP checksum as 0x0000, it will automatically change the checksum to 0xFFFF.

Specifications call for 0xFFFF be substituted for 0x0000 for UDP packets to distinguish UDP packets that carry no checksum. However, the modification does not apply to TCP packets.

Implication: If the receiving station is running MS-DOS and calculates a receive checksum of 0x0000, it will flag an error if the checksum contained in the packet is 0xFFFF. Other operating systems treat 0x0000 and 0xFFFF as equivalent in one's complement math. UDP checksums are correct.

Workaround: Intel modified the DOS Ethernet driver to check for a received checksum of 0xFFFF on a TCP/IP packet and change it back to 0x0000 before passing the packet to the operating system.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82543GC Gigabit Ethernet Controller.

SPECIFICATION CLARIFICATIONS

1. 0-70C Ambient Temperature Range

Problem: The data sheet contains conflicting information on the controller's rated temperature range. The recommended temperature range is given as 0-55C both in a specification table and Section 5.3, Thermal Specifications. Elsewhere, the data sheet indicates a recommended maximum junction temperature of 100C and mentions 0-70C as a test footnote.

Intel validated the 82543GC Gigabit Ethernet Controller for the full commercial ambient temperature range of 0-70C. The overriding specification is the 100C maximum junction temperature. Multiplying the typical 1.5W power by the 17C/W thermal coefficient, then adding the product to 70, yields approximately 96C, which falls under the 100C limit.

Affected Specs: Recommended Operating Conditions and the Thermal Specifications section of OR-2711 82543GC Gigabit Ethernet Controller Advance Information Datasheet Rev. 2.01. Documentation will change to uniformly indicate 0-70C.

2. Receiver Enabling and Disabling

Problem: The 82543GC controller does not support "throttled" reception by repeatedly disabling/enabling the receiver by programming the Enable (EN) Bit in the Receive Control Register (RCTL). The reason is that the disabling/enabling operation does not re-initialize packet filter logic that demarcates packet start and end locations in the FIFO.

A note will be added to the RCTL register description reminding users to reset at least the receiver before re-enabling it.

Affected Specs: RCTL register description in OR-2710 82543GC Gigabit Ethernet Controller Developer's Manual Rev. 2.01.

DOCUMENTATION CHANGES

1. TX/RX Descriptor Register Addresses

Problem: The 82543GC Gigabit Ethernet Controller cannot use address offsets assigned for the previous generation 82542 Gigabit Ethernet Controller. Affected registers include the transmit descriptor registers (incorrect offset range 0x420 – 0x440), receive descriptor registers, diagnostic packet buffer head/tail registers (incorrect offset range 0x8000 – 0x8018) and the flow control threshold registers (incorrect offset range 0x160 – 0x168).

Offsets for these registers will change in documentation to reflect the correct 82543GC device values. Refer to the following table for specific changes.

Register Name	Incorrect Offsets (Based on 82542 Controller)	Corrected Offsets (Based on 82543GC Controller)
RX_DELAY_TIMER	00108	02820
RX_DESC_BASE_ADDR	00110	02800
RX_RING_LENGTH	00118	02808
RX_DESC_HEAD	00120	02810
RX_DESC_TAIL	00128	02818
TX_DESC_BASE_ADDR	00420	03800

TX_RING_LENGTH	00428	03808
TX_DESC_HEAD	00430	03810
TX_DESC_TAIL	00438	03818
TX_INTERRUPT_DELAY	00440	03820
RX_PB_HEAD	08000	02410
RX_PB_TAIL	08008	02418
TX_PB_HEAD	08010	03410
TX_PB_TAIL	08018	03418
FLOW_CONTROL RX THRESH HI	00160	02168
FLOW_CONTROL RX THRESH LO	00168	02160

Affected Docs: 82543GC Gigabit Ethernet Controller Developer's Manual, Order #751596-001. Note: this is an obsolete document. It has been replaced by the combined data sheet/developer's manual documents indicated in the preface of this spec update.

2. Auto Speed Detect Function Requires CTRL.SLU Bit to Be Set

Problem: Setting the Set Link Up (SLU) bit is a prerequisite for the Auto Speed Detect Enable (ASDE) bit in the Device Control Register to operate correctly. Asserting CTRL.SLU does not actually force link-up unless the link indication input indicates that the 82543GC device is connected to a PHY device with valid link.

Documentation will change to explain the complete behavior.

Affected Docs: 82543GC Gigabit Ethernet Controller Developer's Manual, Order #751596-001. Note: this is an obsolete document. It has been replaced by the combined data sheet/developer's manual documents indicated in the preface of this spec update.

3. Values Programmed to Some Registers While in Reset Do Not Persist

Problem: This behavior is related to erratum #4, Some Registers Cannot Be Accessed During Reset. The erratum was corrected, preventing infinite PCI retries, but values in certain registers will not be retained after the reset state ends. Documentation will change to explain which registers are affected.

Affected Docs: 82543GC Gigabit Ethernet Controller Developer's Manual, Order #751596-001. Note: this is an obsolete document. It has been replaced by the combined data sheet/developer's manual documents indicated in the preface of this spec update.

4. JTAG Port Operation

Problem: The JTAG interface as described in the Developer's Manual is not compliant to the IEEE 1149.1 specification and only supports the IDCODE instruction. However, the pin description tables in the datasheet (also the text in the Developer's Manual) does not describe the capabilities of this interface and some readers may think that full boundary scan is supported.

The pin description tables and text will change so the function is described as the "Test Access Port (IDCODE function)" instead of "JTAG".

Affected Docs: OR-2711 82543GC Gigabit Ethernet Controller Advance Information Datasheet Rev. 2.01 and OR-2710 82543GC Gigabit Ethernet Controller Developer's Manual Rev. 2.01.

5. Register Summary Uses Improper Page Reference Format

Problem: The 82543GC Register Summary refers to page numbers in the format (11-182, 11-186, 11-188, …) and (10-162, 10-166, 10-166, …).

The pagination will change to the format (182, 186, 188, …) and (162, 166, 186, …). The actual page numbers are correct.

Affected Docs: OR-2710 82543GC Gigabit Ethernet Controller Developer's Manual Rev. 2.01.

6. Change O_EN_CDET Output to NO_CONNECT

Problem: The output labeled O_EN_CDET should be relabeled to NO_CONNECT. The Enable Comma Detect function is not present on the 825543GC Gigabit Ethernet Controller. This change affects the Pin Description Tables and Signal Name to Electrical Connection Lists.

Comma detection triggers a SERDES device (present in 1000BASE-SX designs) to re-acquire byte synchronization, and is used primarily during Auto-negotiation. Comma detection can be asserted on the SERDES by permanently connecting the SERDES input to Vcc through an approximately 1K pullup resistor. The SERDES will perform the realignment every time it detects a comma character.

Affected Docs: OR-2711 82543GC Gigabit Ethernet Controller Advance Information Datasheet Rev. 2.01.

7. Change Recommended Transmit IPG Programming Value for 10/100/1000BASE-T

Problem: The IEEE standard minimum transmit inter-packet gap is 96 bit times. To achieve that gap requires a programmed setting to the IPGT Field in the Transmit Inter packet Gap (TIPG) Register. The actual inter-packet gap in MAC data clocks) is the sum of the programmed value and a variable logic synchronization time within the device. Use a recommended programming value of 10 for TBI applications and 10 for 10/100/1000BASE-T applications to assure that the minimum IPG gap will be met under all synchronization conditions.

The Developer's Manual currently indicates a programming value of 6 for both fiber and copper implementations. This value will change to 10. In addition to the register listing, section 12.5 Transmit Initialization text should change.

Affected Docs: OR-2710 82543GC Gigabit Ethernet Controller Developer's Manual Rev. 2.01.

8. Remove Transmit Report Status Sent Function

Problem: The Transmit Report Status Sent function is not implemented to write back descriptor status when packet data goes out on the wire. The Report Packet Sent (RPS) Bit in the transmit descriptor (Bit 4 in TDESC.CMD) is Reserved and should be programmed to 0. The related Report Status function (Bit 3 in TDESC.CMD) may be used to force transmit descriptor status bytes to be written back to memory as the packet data reaches the transmit queue.

Affected text includes 4.3.2 Transmit Descriptor Writeback and references in numerous other sections, including the interrupt description text.

Affected Docs: OR-2710 82543GC Gigabit Ethernet Controller Developer's Manual Rev. 2.01.

9. Remove Transmit DMA Pre-fetching and Preemption Functions

Problem: The controller does not implement the ability to start transmit descriptor data fetches before finishing the previous descriptor. In addition, it does not have the ability to disable DMA preemptions during TCP

segmentation. The Transfer DMA Control Register (TXDMAC) will be removed from the developer's manual and text in 12.6 Reset should change.

Note: Erratum #14 prohibits using TCP segmentation regardless of the preemption function.

Affected Docs: OR-2710 82543GC Gigabit Ethernet Controller Developer's Manual Rev. 2.01.

10. Remove Gigabit Half-Duplex Transmit Burst Timer Control Function (TBT)

Problem: The controller does not have the capability to control transmit burst length for Gigabit half-duplex operation through register programming. The Transmit Burst Timer Register (TBT) will be removed from the developer's manual.

Note: Erratum #12 prohibits Gigabit half-duplex mode operation.

Affected Docs: OR-2710 82543GC Gigabit Ethernet Controller Developer's Manual Rev. 2.01.

11. Remove Adaptive IFS Throttle Function (AIT)

Problem: The controller does not have the ability to increase inter-packet gap (beyond TIPG control) during back-to-back transmit operation and Gigabit half-duplex operation. The Adaptive IFS Throttle Register (AIT) will be removed from the developer's manual. Affected sections of the developer's manual include 9.2.2.2 Packet Bursting, 9.4.1 Adaptive IFS and 9.4.2 Burst Mode IFS.

Note: Erratum #12 prohibits Gigabit half-duplex mode operation.

Affected Docs: OR-2710 82543GC Gigabit Ethernet Controller Developer's Manual Rev. 2.01.