PD672X/30/32/33 — ZV Port Implementation

Application Note

May 2001

As of May 2001, this document replaces the Basis Communications Corp. document *AN-PD10*.

Application Note

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1.0 Introduction

The PD6710, PD6722, and PD6729 are single-chip PCMCIA interface controllers capable of controlling one or two PCMCIA or compact Flash sockets, respectively. They are designed for use in embedded applications and notebook systems where reduced form factor and low power consumption are critical design objectives.

Current typical application examples include:

- Routers
- Access network servers
- PBXs
- Vending machines
- Portable handheld systems
- Data acquisition systems
- Settop boxes
- Integrated access devices
- DSLAMs
- Terminal servers
- Point of Sale terminals
- Navigation systems
- Measurement equipment

With the PD6710, a complete single-socket PCMCIA solution with power-control circuitry can occupy less than 1.5 square inches (10 square centimeters) of board space. Similarly, with the PD6722 and PD6729, a complete dual-socket PCMCIA solution with power-control circuitry can occupy less than 2 square inches (13 square centimeters) of board space.

The PD67XX controllers are completely compatible with the standards of PCMCIA (Personal Card Memory International Association) Release 2.0 Standard as well as JEIDA (Japan Electronic Industry Development Association) Version 4.1 Standard (PD6729 is compliant with the PCI 2.1 Specification. The PD67XX controllers also offer special power-saving features such as Automatic Low-power Dynamic Mode and Suspend Mode. Both controllers are true mixed-voltage devices that can operate at +5 volts, +3.3 volts, or a combination of these at various interfaces. The controllers have full internal buffering and require no additional circuitry to interface to the ISA (or ISA-like) Bus for the PD6710 and PD6722, and the PCI Bus for PD6729, or to PCMCIA sockets.

Note: In this document, PD67XX represents the PD6710, PD6722, and PD6729.

2.0 Overview

This application note discusses system design considerations associated with the implementation of the ZV (Zoomed Video) Port when using the PD6722/’29/’30, or PD6832 controller devices. Intended to assist the system designer, this document highlights how various aspects of the PC Card relate to the ZV Port implementation. Since the ZV Port implementation overlaps PC Card, graphics, and audio technologies, consulting with appropriate applications/product groups is recommended.

3.0 Zoomed Video (ZV)

ZV is a cost-effective method of accessing live video through a PC Card. The ZV Port provides a direct connection between a PC Card and a VGA controller and an audio DAC. It allows the PC Card to directly write video data to an input port of a graphics controller and audio data to a digital-to-analog converter. Intel offers a family of PC Card (PCMCIA) Controllers that support the ZV Port standard.

4.0 A Typical ZV Port Implementation

Figure 1 on page 7 illustrates a typical ZV Port implementation with PD6722/’29/’30 and PD6832 controller devices. These devices support the ZV Port in the ‘bypass’ mode during which the signals are directly rerouted from the PC Card bus to the Video ZV Port (the video port of the GD7XXX device is also referred to as the V-Port). This rerouting is accomplished by tristating specific PC Card Bus signals from the PC Card (PCMCIA) Controller. Once these signals are tristated by the host controller during the ZV Port operation, the ZV Port-compliant PC Card drives video and audio data on the same signals. Video signals from the PC Card are routed to the ZV Port-capable video controller; audio signals from the PC Card are routed to the ZV Port-compliant audio DAC in the host system. This mechanism provides an inexpensive means of adding video/audio capability to a notebook or desktop system without any additional burden on the host bus.

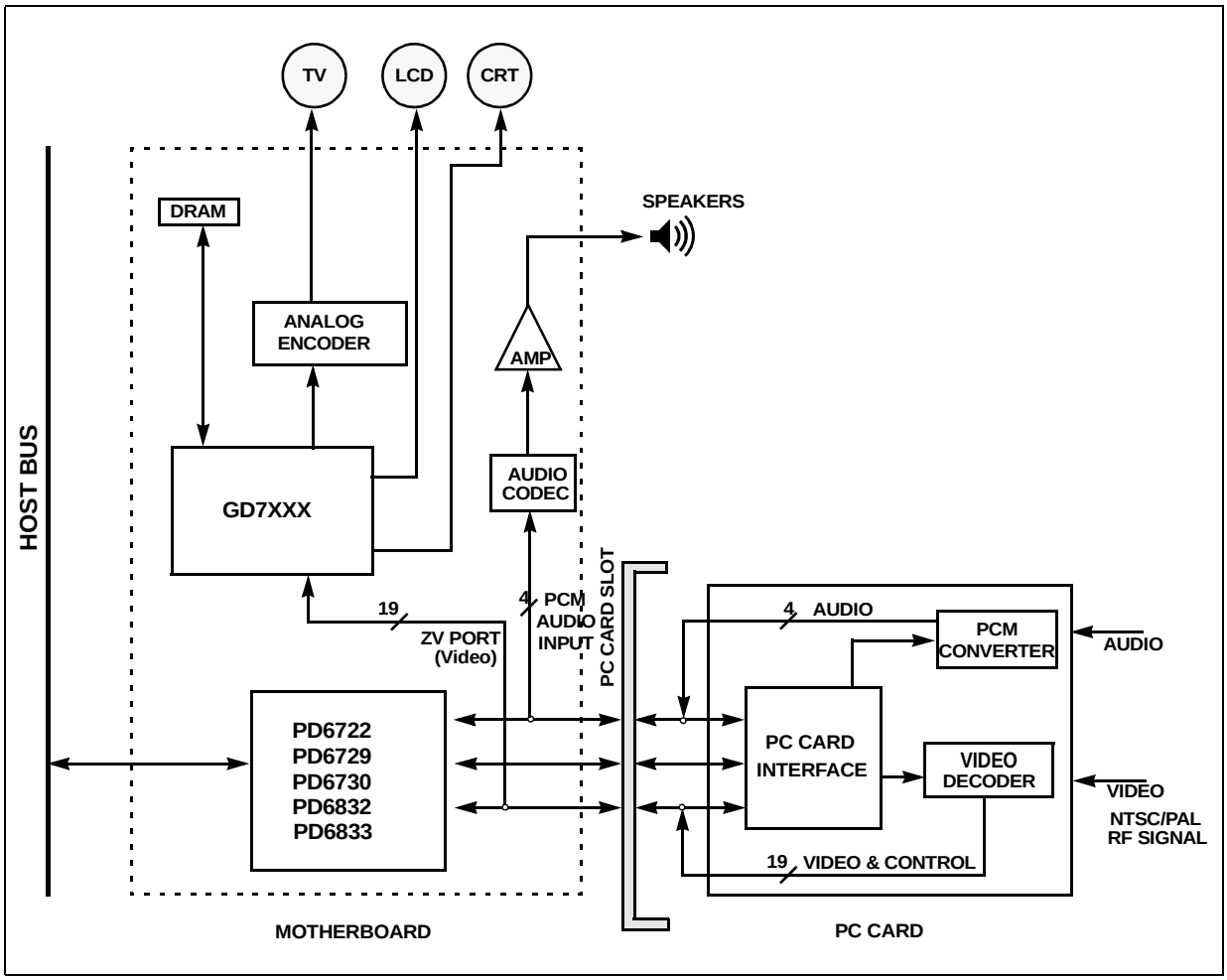
As specified in the PC Card standard, a ZV Port-compliant PC Card, when inserted into a PC Card slot, is initialized the same way as a PC Card 16. It is then recognized as a ZV Port card and programmed accordingly by Card Services. As shown in Figure 1, the PD6722/’29/’30/’6832 enters the ZV Port mode by tristating address pins A[25:4] of the PC Card bus when the Multimedia Enable bit (bit 0 of the Misc. Control register 1 at index 16h in the PD6722/’29/’30 and PD6832; in the PD6832 it can also be at memory offset 816h) is set. These address pins are outputs from the PD6722/’29/’30/’6832 during normal PC Card operation. The tristating of the address pins by the adapter allows the A[25:4] signals to simultaneously carry video data and video capture timing control signals directly to a video controller, and the audio signals to the audio DAC. The PD6832 has a Multimedia Arm bit (bit 7 of the Misc. Control register 3; this register is at I/O index 2Fh, extended index 25h, or memory offset 925h) that works as the overriding control bit. Until the Multimedia Arm bit is set, the Multimedia Enable bit does not tristate the address bit as previously described. When the Multimedia Expand bit (bit 6 of Misc. Control register 3) is set to ‘1’, CE2 and D[15:8] are tristated on the 16-bit PC Card bus, in addition to the tristating of the address signals A[25:4]. The Multimedia Expand bus allows 24-bit video from the ZV Port-compliant PC Card.

Note that ZV Port implementation is likely to vary depending on the platform; the Socket Services software *must* be customized to address these variances. Controlling the OE (output enable) inputs of the external buffers depends upon specific hardware design and software needs to be aware of specifics, such as the I/O Port addresses.

When the PC Card Multimedia mode is used, Intel recommends that the ZV Port pins be connected as shown in Tables 1–3 for the various controller devices. The pin assignments provided in the tables ensure signal integrity and compliance with the ZV Port standard. By disabling or powering down the ZV Port, this connection between the GD7XXX and the PC Card bus does not interfere with the normal (non-multimedia) PC Card bus operation.

When the ZV Port is disabled, VPM (Video Port Manager) software or other client drivers must program the VGA controller so as not to adversely affect the video port of the VGA controller. A bus switch, turned off during normal PC Card bus operation, may be needed to reduce the load on the PC Card bus.

Figure 1. Typical ZV Port Implementation



A buffer circuit placed between the PC Card bus and the VGA video port reduces the trace length to lower the loading effect. The ZV Port standard requires that the length of the trace between the PC Card connector and the buffer (if used) must be less than two inches. Buffers are also needed to support ZV Port PC Cards in either socket.

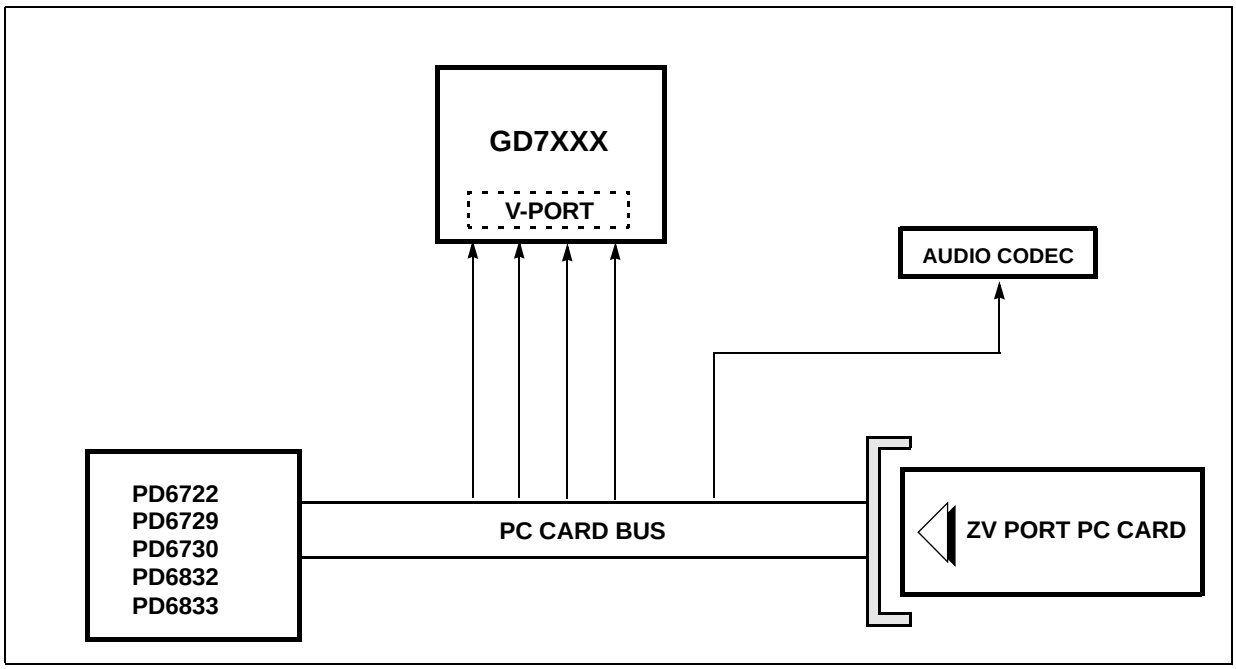
In a full implementation of the ZV Port, multiple PC Card slots can be used to implement the ZV Port. This implies that the user inserts the multimedia PC Card into either slot and the system is able to recognize and respond to this event appropriately. To allow the multimedia PC Card to be inserted into either slot, the individual PC Card bus must be isolated from the other bus by using buffers in the system. The following block diagrams illustrate possible ZV Port implementations.

Note that the control signal inputs to the buffers can be controlled by different methods. For the GD7XXX, the buffer control comes from the I/O pins of the GD7XXX that are labeled VPCNTL and TVON. For further information, refer to the application note titled, *"V-Port Implementation for the GD7548 Super VGA Controller"*.

5.0 Dedicated Socket Approach to ZV Port Implementation

Figure 2 shows a solution using the PD6722/'29/'30/'6832 Controller and the GD7XXX Super VGA controller to support a single dedicated ZV Port slot. This simple implementation does not require any external buffer or glue logic; the only limitation is that one socket must be dedicated to the ZV Port. Also, depending upon the audio controller used, a buffer may be required between the PC Card bus and the audio controller. The designer must ensure that while in R2 PC Card mode (non-ZV operation), the traffic over the bus does not cause the audio input to be driven or the video port of the VGA controller to be adversely affected. If the audio controller or VGA controller do not support a shutdown mode, buffers are required in each path. Also refer to "Layout Guidelines" on page 15 to determine if buffers are required for the video path.

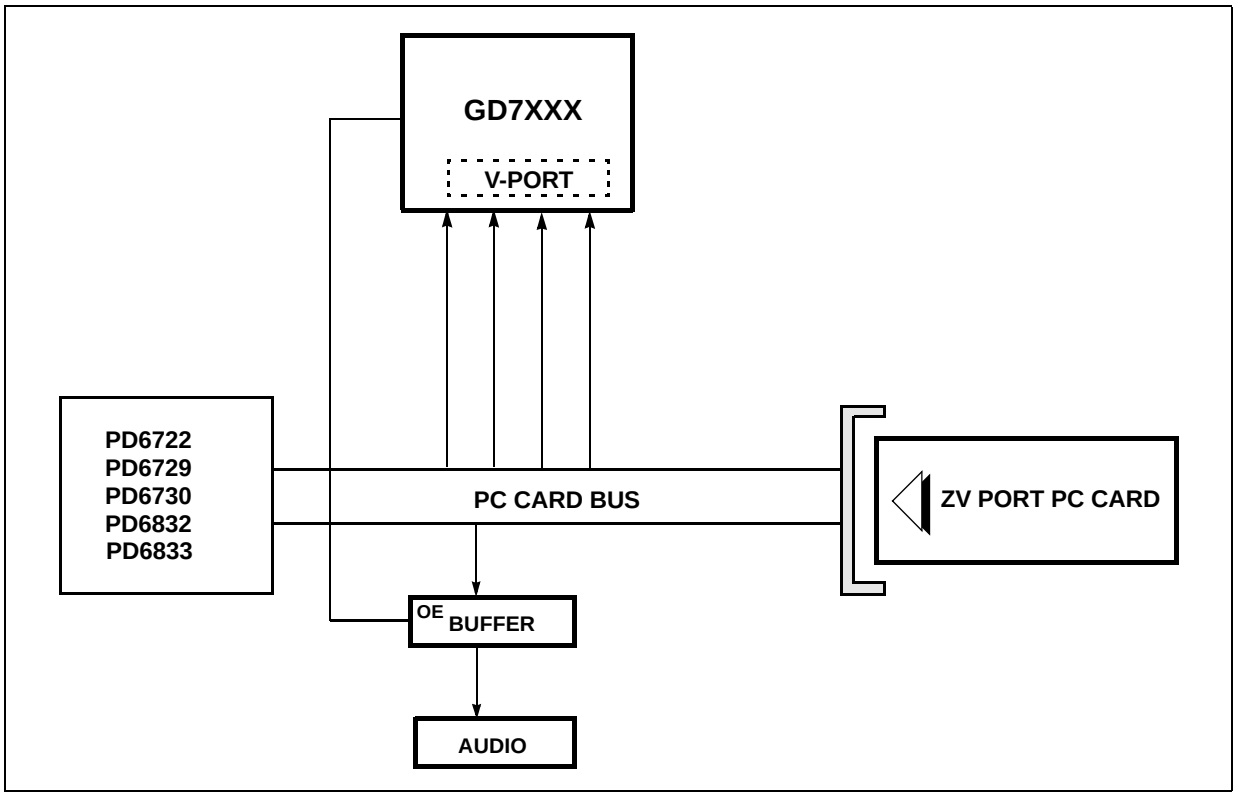
Figure 2. Dedicated Socket Approach to ZV Port Implementation



6.0 Buffer Implementation for Audio DAC

A buffer solution to isolate the audio controller when the socket is not configured in ZV Port mode is shown in Figure 3. This illustrates how to control the buffer enable; if the GD7XXX is used, then one of the GPO pins can control the buffer enable.

Figure 3. Buffer Implementation for Audio DAC



7.0 ZV Port Implementation for Socket A and B

Figure 4 shows the ZV Port support for socket A and B. If using the GD7XXX, two of the GPO pins can control the buffer output enables. Since there is only one V-Port, a ZV Port PC Card can be inserted in either Socket A or Socket B.

Figure 4. ZV Port Implementation for Socket A and B

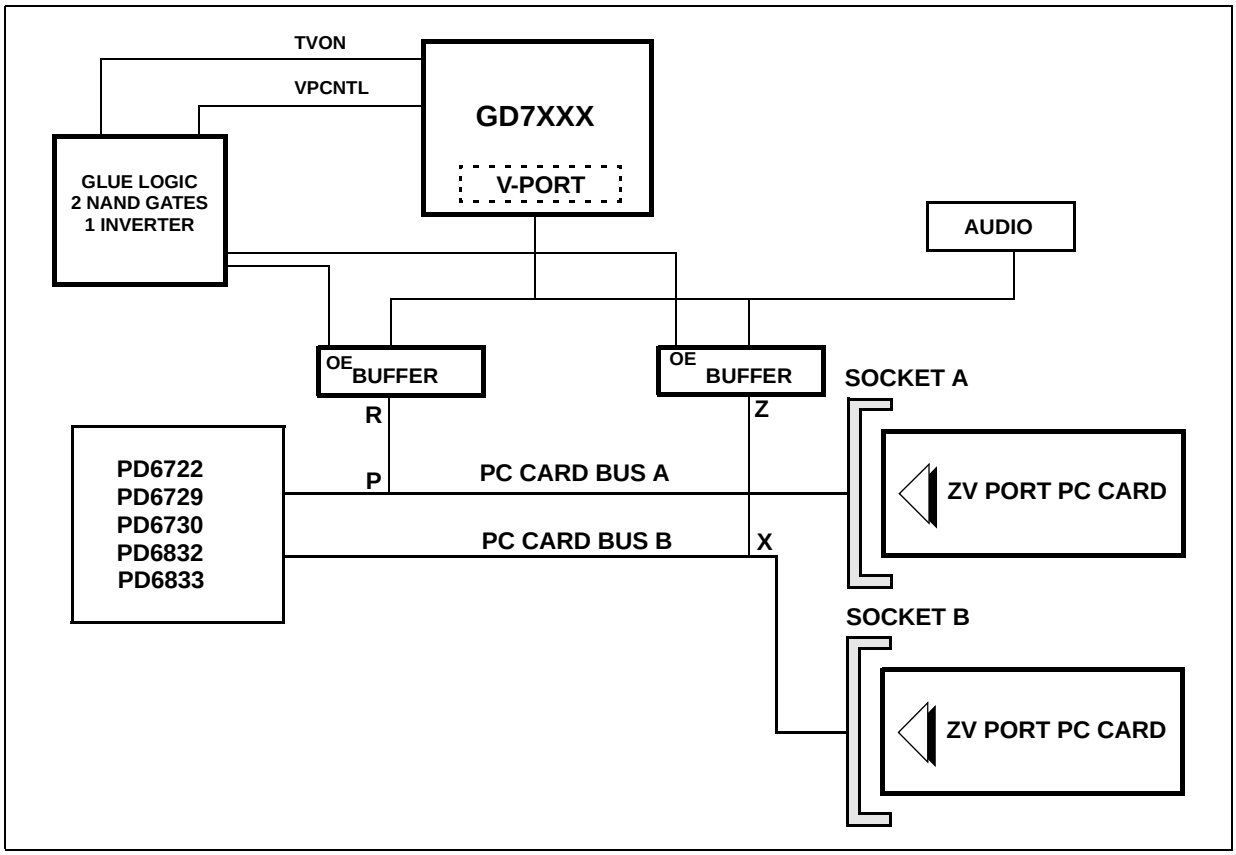


Table 1. PC Card, ZV Port, and PD6722 Pin Assignment (Sheet 1 of 2)

PC Card Pin Number	PC Card Pin	I/O in PC Card Mode	ZV Port Pin Name	I/O in ZV Port Mode	PD6722Socket A	PD6722Socket B	Comments
8	A10	I	HREF	O	21	85	Horizontal sync to ZV Port
10	A11	I	VSYNC	O	25	89	Vertical sync to ZV Port
11	A9	I	Y0	O	28	91	Video data to ZV Port
12	A8	I	Y2	O	30	93	Video data to ZV Port
13	A13	I	Y4	O	33	95	Video data to ZV Port
14	A14	I	Y6	O	35	97	Video data to ZV Port
NOTE: 'I' indicates that the signal is an input to the PC Card; 'O' indicates that the signal is an output from the PC Card. Controller ignores BVD2/SPKR#, IOIS16#, and INPACK# during ZV Port operation.							

Table 1. PC Card, ZV Port, and PD6722 Pin Assignment (Sheet 2 of 2)

PC Card Pin Number	PC Card Pin	I/O in PC Card Mode	ZV Port Pin Name	I/O in ZV Port Mode	PD6722Socket A	PD6722Socket B	Comments
19	A16	I	UV2	O	41	103	Video data to ZV Port
20	A15	I	UV4	O	43	105	Video data to ZV Port
21	A12	I	UV6	O	45	107	Video data to ZV Port
22	A7	I	SCLK	I	47	109	Audio SCLK PCM signal
23	A6	I	MCLK	I	49	112	Audio MCLK PCM signal
24–25	A[5:4]	I	RESERVED	RFU	50,53	113,115	Tristated by Controller; no connection in PC Card
26–29	A[3:0]	I	ADDRESS[3:0]	I	55,57,58,60	118,120, 121,123	Used for accessing PC Card
33	IOIS16#	O	PCLK	O	68	131	Pixel clock to ZV Port
46	A17	I	Y1	O	32	94	Video data to ZV Port
47	A18	I	Y3	O	34	96	Video data to ZV Port
48	A19	I	Y5	O	36	98	Video data to ZV Port
49	A20	I	Y7	O	38	100	Video data to ZV Port
50	A21	I	UV0	O	40	102	Video data to ZV Port
53	A22	I	UV1	O	42	104	Video data to ZV Port
54	A23	I	UV3	O	44	106	Video data to ZV Port
55	A24	I	UV5	O	46	108	Video data to ZV Port
56	A25	I	UV7	O	48	110	Video data to ZV Port
60	INPACK#	O	LRCLK	O	56	119	Audio LRCLK PCM signal
62	SPKR#	O	SDATA	O	59	122	Audio PCM Data signal

NOTE: 'I' indicates that the signal is an input to the PC Card; 'O' indicates that the signal is an output from the PC Card. Controller ignores BVD2/SPKR#, IOIS16#, and INPACK# during ZV Port operation.

Table 2. PC Card, ZV Port, and PD6729 Pin Assignment (Sheet 1 of 2)

PC Card Pin Number	PC Card Pin	I/O in PC Card Mode	ZV Port Pin Name	I/O in ZV Port Mode	PD6729Socket A	PD6729Socket B	Comments
8	A10	I	HREF	O	77	153	Horizontal sync to ZV Port
10	A11	I	VSYNC	O	82	157	Vertical sync to ZV Port
11	A9	I	Y0	O	84	159	Video data to ZV Port
12	A8	I	Y2	O	86	162	Video data to ZV Port
13	A13	I	Y4	O	88	164	Video data to ZV Port
14	A14	I	Y6	O	90	166	Video data to ZV Port
19	A16	I	UV2	O	97	172	Video data to ZV Port
20	A15	I	UV4	O	99	174	Video data to ZV Port

NOTE: 'I' indicates that the signal is an input to the PC Card; 'O' indicates that the signal is an output from the PC Card. Controller ignores BVD2/SPKR#, IOIS16#, and INPACK# during ZV Port operation.

Table 2. PC Card, ZV Port, and PD6729 Pin Assignment (Sheet 2 of 2)

PC Card Pin Number	PC Card Pin	I/O in PC Card Mode	ZV Port Pin Name	I/O in ZV Port Mode	PD6729Socket A	PD6729Socket B	Comments
21	A12	I	UV6	O	101	176	Video data to ZV Port
22	A7	I	SCLK	I	104	179	Audio SCLK PCM signal
23	A6	I	MCLK	I	106	181	Audio MCLK PCM signal
24–25	A[5:4]	I	RESERVED	RFU	108, 110	183, 185	Tristated by Controller; no connection in PC Card
26–29	A[3:0]	I	ADDRESS[3:0]	I	112, 114, 115, 117	187,190, 191, 193	Used for accessing PC Card
33	IOIS16#	O	PCLK	O	125	201	Pixel clock to ZV Port
46	A17	I	Y1	O	87	163	Video data to ZV Port
47	A18	I	Y3	O	89	165	Video data to ZV Port
48	A19	I	Y5	O	92	167	Video data to ZV Port
49	A20	I	Y7	O	94	169	Video data to ZV Port
50	A21	I	UV0	O	96	171	Video data to ZV Port
53	A22	I	UV1	O	98	173	Video data to ZV Port
54	A23	I	UV3	O	100	175	Video data to ZV Port
55	A24	I	UV5	O	103	178	Video data to ZV Port
56	A25	I	UV7	O	105	180	Video data to ZV Port
60	INPACK#	O	LRCLK	O	113	189	Audio LRCLK PCM signal
62	SPKR#	O	SDATA	O	116	192	Audio PCM data signal

NOTE: 'I' indicates that the signal is an input to the PC Card; 'O' indicates that the signal is an output from the PC Card. Controller ignores BVD2/SPKR#, IOIS16#, and INPACK# during ZV Port operation.

Table 3. PC Card, ZV Port, and PD6730/'6832 Pin Assignment (Sheet 1 of 2)

PC Card Pin No.	PC Card Pin	I/O in PC Card Mode	ZV Port Pin Name	I/O in ZV Port Mode	PD6730 or PD6832 Socket A	PD6730 or PD6832 Socket B	Comments
8	A10	I	HREF	O	73	149	Horizontal sync to ZV Port
10	A11	I	VSYNC	O	77	153	Vertical sync to ZV Port
11	A9	I	Y0	O	80	155	Video data to ZV Port
12	A8	I	Y2	O	82	157	Video data to ZV Port
13	A13	I	Y4	O	84	159	Video data to ZV Port
14	A14	I	Y6	O	86	162	Video data to ZV Port
19	A16	I	UV2	O	93	169	Video data to ZV Port
20	A15	I	UV4	O	95	171	Video data to ZV Port
21	A12	I	UV6	O	97	173	Video data to ZV Port
22	A7	I	SCLK	I	100	175	Audio SCLK PCM signal

NOTE: 'I' indicates that the signal is an input to the PC Card; 'O' indicates that the signal is an output from the PC Card. Controller ignores BVD2/SPKR#, IOIS16#, and INPACK# during ZV Port operation.

Table 3. PC Card, ZV Port, and PD6730/'6832 Pin Assignment (Sheet 2 of 2)

PC Card Pin No.	PC Card Pin	I/O in PC Card Mode	ZV Port Pin Name	I/O in ZV Port Mode	PD6730 or PD6832 Socket A	PD6730 or PD6832 Socket B	Comments
23	A6	I	MCLK	I	103	178	Audio MCLK PCM signal
24–25	A[5:4]	I	RESERVED	RFU	105, 107	181, 183	Tristated by Controller; no connection in PC Card
26–29	A[3:0]	I	ADDRESS [3:0]	I	109,111, 113,116	185,187, 189, 191	Used for accessing PC Card
33	IOIS16#	O	PCLK	O	125	201	Pixel clock to ZV Port
46	A17	I	Y1	O	83	158	Video data to ZV Port
47	A18	I	Y3	O	85	161	Video data to ZV Port
48	A19	I	Y5	O	88	164	Video data to ZV Port
49	A20	I	Y7	O	90	166	Video data to ZV Port
50	A21	I	UV0	O	92	168	Video data to ZV Port
53	A22	I	UV1	O	94	170	Video data to ZV Port
54	A23	I	UV3	O	96	172	Video data to ZV Port
55	A24	I	UV5	O	99	174	Video data to ZV Port
56	A25	I	UV7	O	102	176	Video data to ZV Port
60	INPACK#	O	LRCLK	O	110	186	Audio LRCLK PCM signal
62	SPKR#	O	SDATA	O	114	190	Audio PCM Data signal

NOTE: 'I' indicates that the signal is an input to the PC Card; 'O' indicates that the signal is an output from the PC Card. Controller ignores BVD2/SPKR#, IOIS16#, and INPACK# during ZV Port operation.

8.0 Layout Guidelines

The VGA controller, the PC Card (PCMCIA) Controller, and the PC Card Sockets must be in close proximity to one another. This requirement is particularly important when the PD6832 or PD6833 device is used along with the ZV Port for Card bus implementation. According to tests conducted by PCMCIA ZV Port subcommittee, the stubs to the GD7548 device or any other VGA controller must be no longer than two inches. As shown in Figure 4 on page 11, the stub length is the distance between points P and R for PC Card bus A and between points X and Z for PC Card bus B. Vias have already been included in this recommended stub length.

- Maximum total capacitive loading for each Card bus signal = 22 pF
- Maximum input capacitance of each host controller pin = 10 pF
- Maximum input capacitance of the buffer pin = 5 pF

A total of 7 pF remains for the PC Card connector-to-buffer input pin trace. A maximum trace length of two inches satisfies CardBus requirements.

System designers must check the V_{CC} bounce, ground bounce, and crosstalk on CardBus/ZV Port prototypes to ensure that the effect is minimal. The CCLK signal on the CardBus must be thick with sufficient gap from adjacent traces and series termination must be used. Guidelines for CCLK signal are included in the latest PC Card specifications.

Note: Intel recommends that designers contact the PCMCIA organization for the latest revision of the ZV Port standard.