

Reference Manual

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EPM-4 (Lynx)

AMD ÉlanSC520 processor
module with 10/100 Ethernet,
and PC/104-*Plus* interface.



EPM-4

AMD ÉlanSC520 processor
module with 10/100 Ethernet,
and PC/104-*Plus* interface



MEPM4

Product Release Notes

This page includes recent changes or improvements that have been made to this product. These changes may affect its operation or physical installation in your application. Please read the following information.

Rev 5 Release

- EPM-4h model release – RoHS extended temperature version.

Rev 4 Release

- PC/104 (ISA) connector keyed to better comply with standard. PC/104 connector soldered instead of press-fit.
- Physically smaller fuse at F1 with same protection value.
- 3.0V battery.

Rev 3 Release

- EPM-4g model release – Initial RoHS version.

Rev 2 Release

- Initial public release.

Support Page

The **EPM-4 Support Page**, at <http://www.VersaLogic.com/private/lynxsupport.asp> contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Operating system information and software drivers
- Data sheets and manufacturers' links for chips used in this product
- BIOS information and upgrades
- Utility routines and benchmark software

Note: This is a private page for EPM-4 users only. It cannot be reached through our web site. You must enter this address directly to find the support page.

Model EPM-4
AMD Élan processor module with 10/100 Ethernet,
and PC/104-*Plus* interface

REFERENCE MANUAL



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Description

The EPM-4 (Lynx) is a 486-based processor board in a compact PC/104-*Plus* format. It is specifically designed for OEM control projects requiring compact size, high reliability, and long product lifespan / availability. Its features include:

- AMD ÉlanSC520 microcontroller
 - 133 MHz
- 64 MB system RAM
- 10/100 dual-speed Ethernet
- Battery Backed SRAM Option
- Real time clock
- PC/104, PC/104-*Plus* expansion interface
- IDE controller
- Two general purpose timer inputs
- Watchdog timer
- Reconfigurable BIOS defaults
- Console redirected to COM port if no VGA
- Keyboard, mouse, AT motherboard peripherals
- CompactFlash Socket
- Four COM ports
 - Two RS-232
 - Two RS-422/485
- Parallel Port/Floppy Interface
- Vcc sensing reset circuit
- Flash BIOS with OEM enhancements
- Ethernet Remote boot capability
 - 3rd party boot code not included
- Single supply (+5V) operation
- Customizing available
- Batteryless operation (possible)
- Extended temperature options (100MHz)
- Transient Voltage Suppressor Devices
- RoHS-compliant version available

The EPM-4 is a complete computer system in one board. It may be used alone or with expansion modules. It features a PC/104-*Plus* expansion interface for fast PCI-based interface to a wide variety of PC/104 and PC/104-*Plus* stacking modules. This card is designed to be used primarily as an Ethernet node processor card.

It is fully compatible with popular operating systems including Windows 95/98/NT/NTE/, CE, QNX, Linux, RT-Linux, and other Real Time Operating Systems (see the [VersaLogic OS Compatibility Chart](#)).

On-board I/O includes 10/100 Mbit Ethernet, IDE, four COM ports, floppy and two general-purpose timer inputs.

This exceptional processor card was designed from the ground up for OEM applications with longevity and reliability as the main focus. It is fully supported by the VersaLogic design team. Both hardware and software (BIOS) customization are available in quantities as low as 25 pieces. Each board is subjected to 100% functional testing and is backed by a limited two-year warranty.

Technical Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

Board Size:

3.55" x 3.775" (PC/104 standard).

Storage Temperature:

-40° C to 85° C

Operating Temperature:

EPM-4c, g 0° C to +60° C (100 FPM airflow)

EPM-4e, h -40° C to +85° C (free air, extended temperature versions)

Power Requirements: (with keyboard, mouse, and hard drive running DOS)

EPM-4c, g 133 MHz +5V ±5% @ 0.94A

EPM-4e, h 100 MHz +5V ±5% @ 0.84A, extended temperature versions

+3.3V or ±12V may be required by some expansion modules

System Reset:

V_{CC} sensing, resets below 4.70V typ.

Watchdog timeout

BBSRAM Interface:

2 MB option mapped into high memory

IDE Interface:

Industry standard 2mm 44-pin non-latching style, CompactFlash socket.

LPT/Floppy Interface:

Supports one floppy drive or parallel port.

Ethernet Interface:

Autodetect 10BaseT/100BaseTX based on Intel 82551ER. 12K transmit/receive buffer.

COM1 and COM2 Interface:

RS-232, 16C550 compatible, 115K baud max.

COM3 and COM4 Interface:

RS-422/485, 16C550 compatible, 460K baud max.

Connectors:

Utility: 2mm 50-pin shrouded

IDE: 2mm 44-pin

Floppy/LPT: 2mm 20-pin shrouded

Ethernet: RJ45

Power: 0.1" 10-pin

CompactFlash Type II socket

BIOS: General Software embedded BIOS with OEM enhancements

Field upgradeable with Flash BIOS Upgrade Utility

Bus Speed:

PCI, PC/104-Plus: 33 MHz, Revision 2.0

PC/104: 8 MHz, Revision 2.5

Compatibility:

PC/104 – Fully functional with most PC/104 devices. See the Expansion Bus section for details.

Embedded-PCI (PC/104-Plus) – Full compliance, 3.3V or 5V modules

RoHS: EPM-4g, h – Full compliance

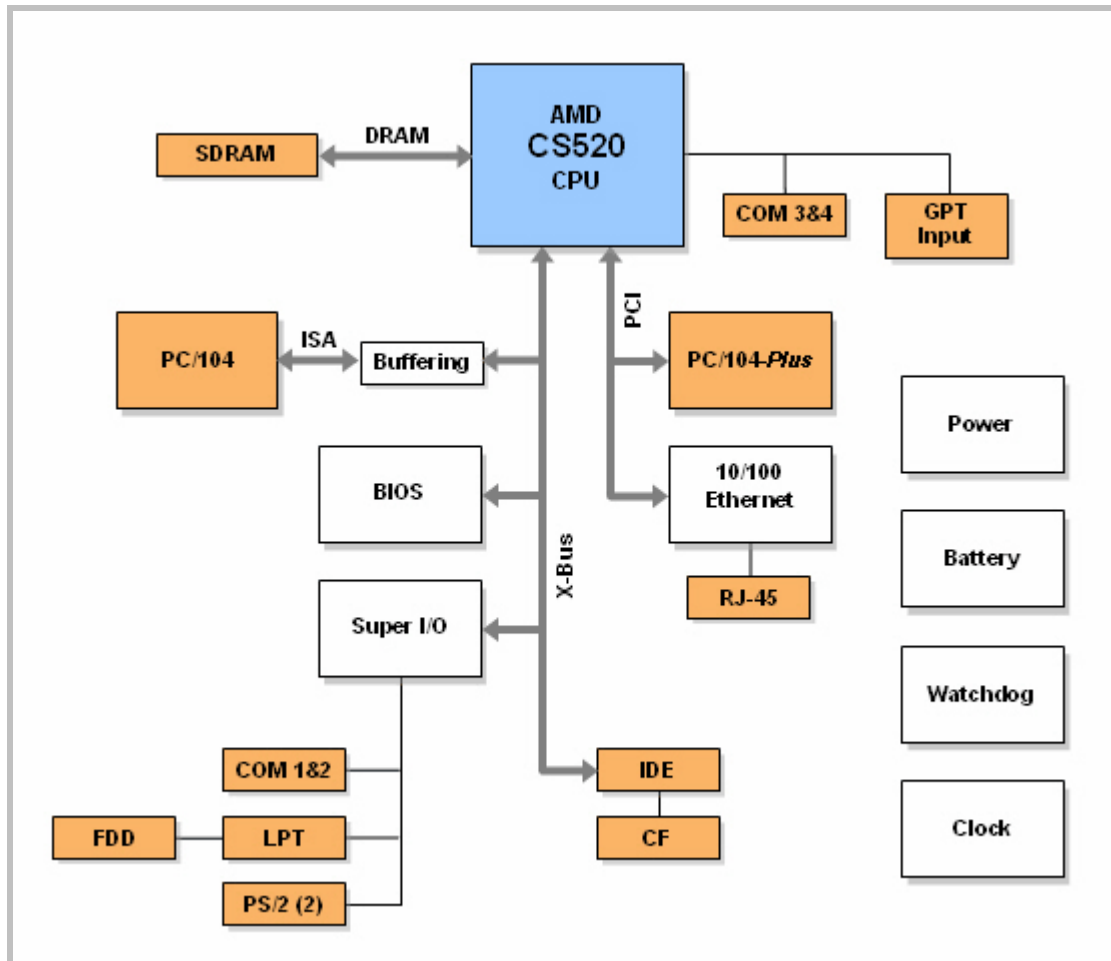
Weight:

EPM-4c, g – 0.117 kg (0.275 lbs)

EPM-4e, h – 0.116 kg (0.255 lbs)

Specifications are subject to change without notice.

EPM-4 Block Diagram



RoHS-Compliant Version

The EPM-4g and EPM-4h are RoHS-compliant. These models are functionally identical to the non-RoHS version of the boards.

ABOUT ROHS

In 2003, the European Union issued Directive 2002/95/EC regarding the Restriction of the use of certain Hazardous Substances (RoHS) in electrical and electronic equipment.

The RoHS directive requires producers of electrical and electronic equipment to reduce to acceptable levels the presence of six environmentally sensitive substances: lead, mercury, cadmium, hexavalent chromium, and the presence of polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) flame retardants, in certain electrical and electronic products sold in the European Union (EU) beginning July 1, 2006.

VersaLogic Corporation is committed to supporting customers with high-quality products and services meeting the European Union's RoHS directive.

ROHS COMPLIANT CABLES

Adapter cables for the EPM-4 are available in RoHS compliant and RoHS noncompliant versions. Compliance or noncompliance is indicated by the part number prefix. "CBR" indicates RoHS compliance. "CBL" indicates RoHS noncompliance. For applications that require RoHS compliance, use only the RoHS compliant ("CBR" version) cables. Availability of RoHS noncompliant cables may be limited.

Technical Support

If you have problems that this manual can't help you solve, first visit the EPM-4 Product Support web page below. If you have further questions, contact VersaLogic for technical support at (541) 485-8575. You can also reach our technical support engineers via e-mail at Support@VersaLogic.com.

EPM-4 Support Website

<http://www.VersaLogic.com/private/lynxsupport.asp>

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (541) 485-8575.

Please provide the following information:

- Your name, the name of your company, and your phone number
- The name of a technician or engineer who we can contact if we have questions
- Quantity of items being returned
- The model and serial number (bar code) of each item.
- A description of the problem
- Steps you have taken to resolve or repeat the problem
- The return shipping address

Warranty Repair

All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair

All non-warranty repairs are subject to diagnosis and labor charges, parts charges, and return shipping fees. We will need to know what shipping method you prefer for return back to your facility, and we will need to secure a purchase order number for invoicing the repair.

Note:

Please mark the RMA number clearly on the outside of the box before returning. Failure to do so can delay the processing of your return.

Overview

ELECTROSTATIC DISCHARGE

Warning! Electrostatic discharge (ESD) can damage boards, disk drives, and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded anti-static wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an anti-static foam pad if available.

The board should also be protected during shipment or storage by keeping inside a closed metallic anti-static envelope.

Note: The exterior coating on some metallic anti-static bags is sufficiently conductive to cause excessive battery drain if the bag comes in contact with the bottom side of the EPM-4.

LITHIUM BATTERY

Warning! To prevent shorting, premature failure, or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam, or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble, or dispose of in fire. Dispose of used batteries promptly.

Initial Configuration and Setup

The following list describes the components recommended for setting up a typical development system.

RECOMMENDED COMPONENTS

- EPM-4 Board and cable kit
- ATX Power Supply
- EPM-VID-3 for video support
- Keyboard with PS/2 connector, mouse
- Ethernet Network
- IDE Hard Drive
- Floppy Drive

CMOS Setup / Boot Procedure

- Turn power on.
- Press the DEL key the instant that video is displayed (during the memory test).
- Verify default CMOS Setup information as shown below.
- Insert bootable floppy disk into floppy drive.
- Reset computer using push button reset.
- See VersaLogic KnowledgeBase article [VT1476 – EPM-4 CMOS Setup Reference](#) for more information about these parameters.

Basic CMOS Configuration

System Bios Setup - Basic CMOS Configuration (C) 2002 General Software, Inc. All rights reserved		
DRIVE ASSIGNMENT ORDER:	Date:>JAN 1, 1980	Typematic Delay : 250 ms
Drive A: Floppy 0	Time: 00 : 00 : 00	Typematic Rate : 30 cps
Drive B: (None)	NumLock: Disabled	Seek at Boot : None
Drive C: IDE 0/Pri Master		Show "Hit Del" : Enabled
Drive D: (None)	BOOT ORDER:	Config Box : Enabled
Drive E: (None)	Boot 1st: Drive A:	F1 Error Wait : Enabled
Drive F: (None)	Boot 2nd: Drive C:	Parity Checking : (Unused)
Drive G: (None)	Boot 3rd: (None)	Memory Test Tick : Enabled
Drive H: (None)	Boot 4th: (None)	Debug Breakpoints: (Unused)
Drive I: (None)	Boot 5th: (None)	Debugger Hex Case: Upper
Drive J: (None)	Boot 6th: (None)	Memory Test : StdLo FastHi
Drive K: (None)		
(Loader): (Unused)	ATA DRV ASSIGNMENT: Sect Hds Cyls	Memory Base:
	Ide 0: 3 = AUTOCONFIG, LBA	633KB
FLOPPY DRIVE TYPES:	Ide 1: 3 = AUTOCONFIG, LBA	Ext:
Floppy 0: 1.44 MB, 3.5"	Ide 2: Not installed	63MB
Floppy 1: Not installed	Ide 3: Not installed	

Custom Configuration

System BIOS Setup - Custom Configuration (C) 2002 General Software, Inc. All rights reserved		
D0000h 64k page function	: ISA bus	COM1 (3F8h) RS-232 : IRQ4
PLD register base I/O	: 0E0h	COM2 (2F8h) RS-232 : IRQ3
Force Ethernet 10-Baset	: Disabled	COM3 (3E8h) RS-422/485 : Disabled
PS/2 Mouse (IRQ12)	: Enabled	COM4 (2E8h) RS-422/485 : Disabled
LPT1 (378h)	: Disabled	GP Timer 0 : Disabled
Parallel Port Mode	: FDD	GP Timer 1 : Disabled
CPU Speed	: 133 MHz	Watchdog Timer : Disabled
Cache Mode	: Wr-back	PCI Int A : IRQ11
Write Buffer	: Enabled	PCI Int B : IRQ11
GP Bus Timings	: Normal	PCI Int C (Ethernet) : IRQ11
Console Redirection	: Auto	PCI Int D : IRQ11

Note: Due to changes and improvements in the system BIOS, the information on your monitor may differ from that shown above.

Console Redirection

If there is no video device detected during boot up, BIOS keyboard and screen I/O can be redirected to the COM2 RS-232 serial port. CMOS configuration can be modified over this redirected console. ANSI or VT102 terminal emulation is recommended.

When console redirection is enabled, press CTRL-C on the terminal emulator to enter CMOS Setup; the BIOS ignores DEL from a PS/2 keyboard. This is normal operation of the Lynx.

COM2 is configured for standard serial port communication:

- 9600 Baud
- Parity: None
- Flow Control: None
- Data Bits: 8
- Stop Bits: 1

Console redirection remains active when POST completes and the operating system boots. Text-based operating systems such as DOS and Linux can be controlled over this connection.

To enable console redirection, there must be no video device detected, the console redirection option in Custom Configuration must be set to Auto, and there must be a terminal (such as Windows HyperTerm) detected at COM2.

CMOS Setup / IDE Configuration

IDE

The Lynx has a single IDE channel to connect up to two hard disks, CompactFlash modules or CD-ROM drives. This basic IDE interface operates using PIO mode 0, resides on the ISA bus, and does not support the drive address register at I/O address 3F7h. It has been tested successfully on a wide variety of operating systems.

IDE SETUP

IDE devices include hard disk drives, CD-ROM drives, and some CompactFlash modules.

There are 3 fields in the Basic CMOS Configuration screen that are relevant to IDE setup: IDE Drive Geometry, Drive Assignment Order, and Boot Order.

IDE Drive Geometry

Most desktop PCs have two IDE channels, each capable of supporting two IDE devices in a slave/master configuration or a single IDE device in a single (or master only) configuration.

In the IDE Drive Geometry list:

IDE 0 corresponds to primary channel, master/single drive.

IDE 1 corresponds to primary channel, slave drive.

IDE 2 corresponds to secondary channel, master/single drive.

IDE 3 corresponds to secondary channel, slave drive.

The Lynx uses the first IDE channel only. IDE 2 and IDE 3 are unused

All modern IDE devices use LBA mode. When setting up an IDE device, leave the drive geometry set to LBA mode unless your hard drive requires a different mode.

CD-ROM drives that will be used as boot devices should be set accordingly in the Drive Geometry list.

Drive Assignment Order

After a hard drive has been declared in the IDE Drive Geometry field, it must be assigned a DOS drive letter, even if you are not using the DOS operating system. Normally, "Drive C:" will be assigned to the IDE device that you wish to boot from.

Do not attempt to assign a drive letter to a CD-ROM drive. The drivers required to use these devices will automatically assign a drive letter to the device when loaded.

Boot Order

This field allows you to specify the order in which the BIOS looks for boot devices.

Usually, the drive you specify here corresponds to the declaration in the Drive Assignment Order field.

A CD-ROM drive can be inserted into the boot order by selecting “CDROM” at the desired boot order position.

CMOS Setup / Advanced Configuration

D0000H 64K PAGE FUNCTION

Default: ISA bus

ISA bus

Memory accesses to the D0000h page will be sent to the ISA bus for use by PC/104 expansion modules. This setting is required when flashing the BIOS with the FBU utility.

BIOS Ext

The D0000h page is mapped to sector 1 in the flash chip, which may contain 3rd party Ethernet boot code or any other BIOS extension (not included). If there is a such an extension present, it will be called by the BIOS. The BIOS extension can be programmed into the flash chip with the FBU utility. For remote booting via Ethernet, the recommended boot ROM is Managed PC Boot Agent from Argon Technology Corporation.

RAM

System RAM is exposed in the D0000h page.

PLD REGISTER BASE I/O

Default: 0E0h

Specifies the location of the PLD register in I/O space. It can be moved to 1E0h in case of an address conflict within add-in module.

FORCE ETHERNET 10-BASET

Default: Disabled

When enabled, this will disable the Ethernet media data rate auto-negotiation and force it to 10-BaseT mode.

Note: Some drivers will put the Ethernet back into auto-negotiation mode.

PS/2 MOUSE (IRQ12)**Default: Enabled**

When disabled, IRQ12 is freed for other devices.

LPT1 (0378H)**Default: IRQ7**

Allows you to disable or specify the IRQ used by LPT1 on the SMSC FDC37B727 Super I/O. When disabled, the IRQ and I/O space are freed.

PARALLEL PORT MODE**Default: SPP**

This option allows the user to change the communication mode of the parallel port. The options are: SPP, SPP/EPP1.9, ECP, ECP/EPP1.9, Printer, SPP/EPP1.7, ECP/EPP1.7, and FDD. The FDD option must be set if a floppy drive is used.

CPU SPEED**Default: 133 MHz**

The maximum clock rate for the ÉlanSC520 Microcontroller is 133 MHz. It can optionally be set to 100 MHz for a slight power savings. If an extended temperature board version is detected, the default will change to 100 MHz.

CACHE MODE**Default: Write-Back**

The 16 kb L1 cache can be configured for either write-through or write-back mode. This option controls the CACHE_WR_MODE in the CPUCTL register (MMCR offset 02h).

WRITE BUFFER**Default: Enabled**

When the write buffer is enabled, it buffers all write activity from the CPU, PCI bus, or GP bus. This option controls the WB_ENB bit in the DBCTL register (MMCR offset 40h).

GP BUS TIMINGS**Default: Normal**

The GP (ISA) bus timings may need to be slowed to accommodate ISA Plug-n-Play cards. This option modifies registers in the GP Bus Controller, MMCR offsets C08h through C10h.

COM1 (03F8H) RS-232

Default: IRQ4

Allows you to disable or specify the IRQ used by internal UART1 on the ÉlanSC520 Microcontroller. When disabled, the IRQ and I/O space are freed.

COM2 (02F8H) RS-232

Default: IRQ3

Allows you to disable or specify the IRQ used by internal UART2 on the ÉlanSC520 Microcontroller. When disabled, the IRQ and I/O space are freed.

COM3 (03E8H) RS-422/485

Default: Disabled

Allows you to disable or specify the IRQ used by UART1 on the SMSC FDC37B727 Super I/O. When disabled, the IRQ and I/O space are freed.

COM4 (02E8H) RS-422/485

Default: Disabled

Allows you to disable or specify the IRQ used by UART2 on the SMSC FDC37B727 Super I/O. When disabled, the IRQ and I/O space are freed.

GP TIMER 0, GP TIMER 1, WATCHDOG TIMER

Default: Disabled

These internal SC520 devices can be disabled or enabled by assigning an IRQ. Enabling these devices only sets up the IRQ assignment; it is up to the user to set up device operation. Refer to the ÉlanSC520 Microcontroller User's Manual for details.

PCI INTERRUPT A, B, C, AND D

Default: IRQ11

These options allow manual IRQ routing of PCI devices.

Note: PCI devices can share an interrupt. In most cases, the cost of doing this is slightly decreased system performance and slightly increased interrupt response time.

Using Custom CMOS Defaults

The Lynx BIOS has the capability to store CMOS defaults in the on-board flash chip. This storage area is non-volatile, enabling the Lynx to run with user-specified CMOS defaults without a battery installed.

If custom defaults are specified, they will be used instead of the factory defaults any time CMOS memory needs to be reset. CMOS is reset when any of the following occur:

- CMOS memory is found to be corrupt or uninitialized at boot time
- CMOS contents are erased by FBU during a BIOS upgrade
- The Lynx was powered on without a battery, or without a sufficiently charged battery

There are 4 options on the main BIOS setup screen that control CMOS defaults.

- *Save CMOS as custom defaults*

Saves the current CMOS settings to the custom defaults. These settings will be used any time CMOS is reset. If there are already custom defaults specified, they will be overwritten.
- *Reset CMOS to custom defaults*

Discards the current CMOS settings and uses the saved custom defaults. This operation will fail if no custom defaults have been previously saved.
- *Clear custom defaults (use factory defaults)*

Deletes custom CMOS settings stored in flash. Factory default settings will be used any time CMOS is reset.
- *Reset CMOS to factory defaults*

Discards the current CMOS settings and uses factory defaults, even if custom defaults have been specified. If CMOS is later reset, custom defaults will be used if available.

Warning! Take care in saving custom CMOS defaults, as you must be able to get back to the main BIOS setup screen to undo any mistakes. For example, it would be a mistake to disable a COM port that is required for console redirection when there is no video device available.

Physical Dimensions

The EPM-4 complies with all PC/104-Plus standards. Dimensions are given below to help with pre-production planning and layout.

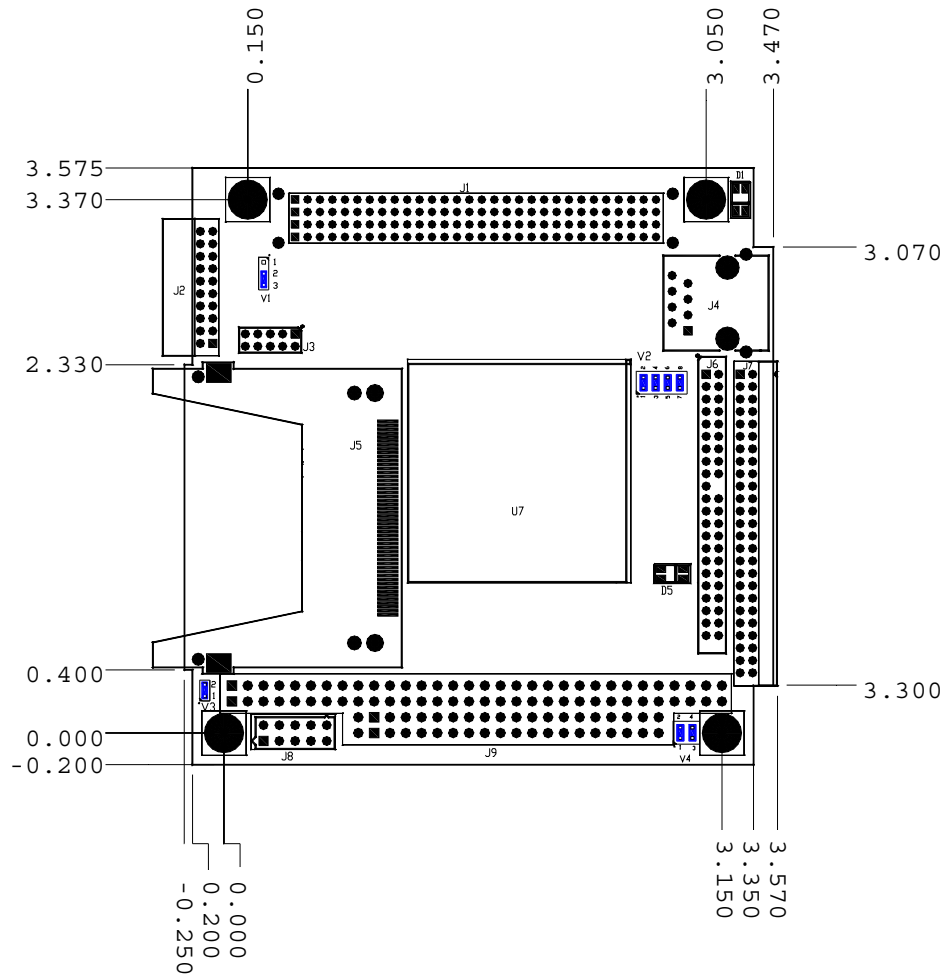


Figure 1. Dimensions
(Not to scale. All dimensions in inches.)

HEIGHT DIMENSIONS

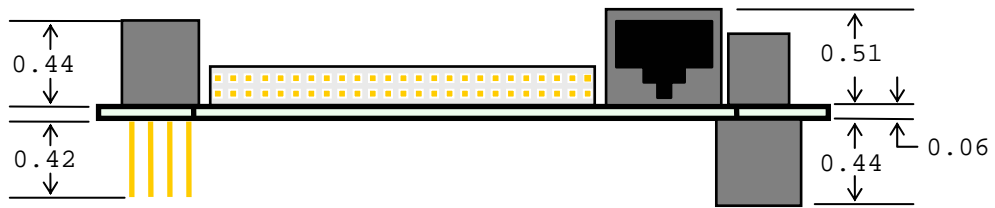


Figure 2. Height Dimensions
(Not to scale. All dimensions in inches.)

HARDWARE ASSEMBLY

The EPM-4 uses pass-through PC/104 and PC/104-*Plus* connectors so that expansion modules can be added to the top or bottom of the stack. PC/104 (ISA) modules must NOT be positioned between the Lynx and any PC/104-*Plus* (PCI) modules on the stack. The PC/104 pass-through connector on the EPM-4 Rev 4 is keyed (pins B10 and C19 missing) to provide greater compatibility with other PC/104 compliant devices.

The entire assembly can sit on a tabletop or it can be secured to a base plate. When bolting the unit down, make sure to secure all four standoffs to the mounting surface to prevent circuit board flexing. Standoffs are secured to the top circuit board using four pan head screws. Refer to the drawing on page 17 for dimensional details.

An extractor tool is available (part number VL-HDW-201) to separate the modules from the stack.

STACK ARRANGEMENT

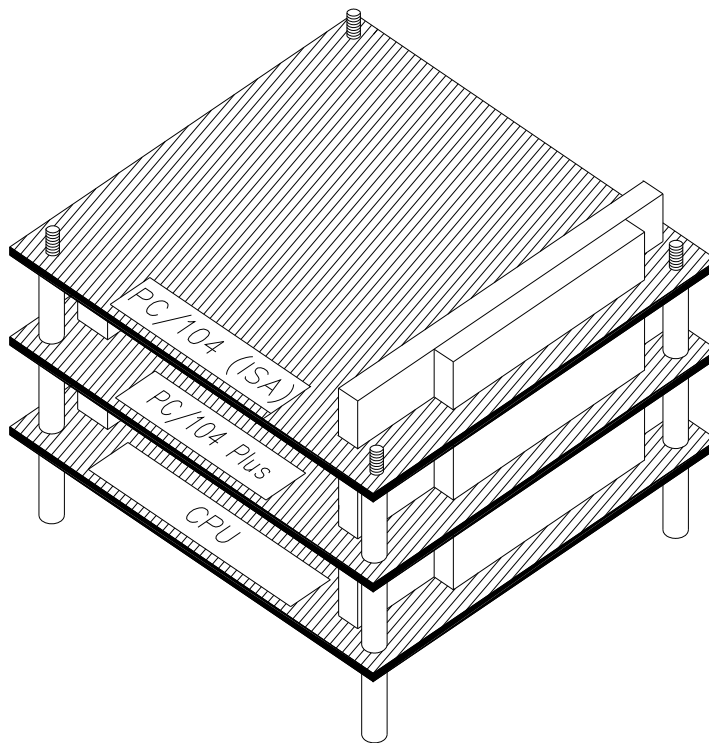


Figure 3. PC/104 Card Added to Top of Stack

External Connectors

CONNECTOR LOCATION DIAGRAM

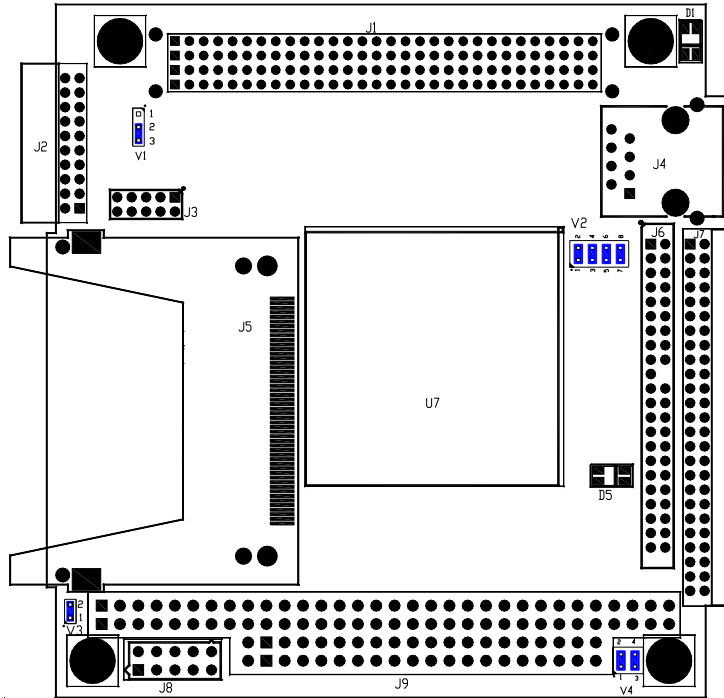
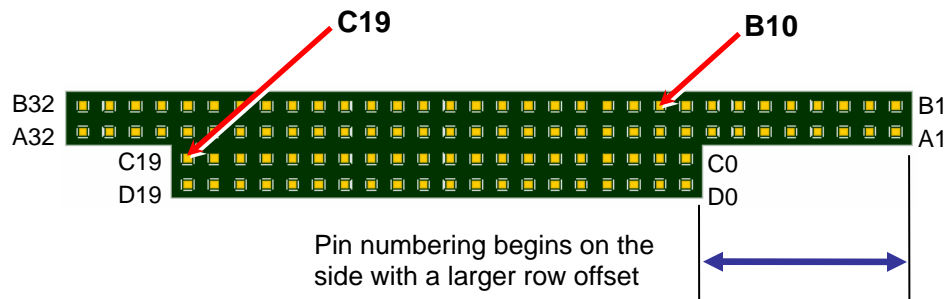


Figure 4. Connector Locations

On the EPM-4 Rev 4 and above, the pass-through PC/104 (ISA) connector is keyed (pins B10 and C19 missing) for greater compatibility with PC/104 devices, as shown in the figure below.

Pin Side of ISA Connector



Note: For rows A and B, pin numbers begin at 1.
For rows C and D, pin numbers begin at 0.

Figure 5. PC/104 (ISA) Connector Keying

CONNECTOR FUNCTIONS AND INTERFACE CABLES

The table below notes the function of each connector, as well as mating connectors and cables, and the page where a detailed pinout or further information is available.

Note: VersaLogic adapter cables for the EPM-4 are available in RoHS compliant and RoHS noncompliant versions. Compliance or noncompliance is indicated by the part number prefix. “CBR” indicates RoHS compliance. “CBL” indicates RoHS noncompliance. For applications that require RoHS compliance, use only the RoHS compliant (“CBR” version). Availability of RoHS noncompliant cables may be limited.

Table 1: Connector Functions and Interface Cables

Connector	Function	Mating Connector	Transition Cable	Cable Description	Page	‡Pin 1 Location X Coord. Y Coord.
J1	PC/104-Plus	AMP 1375799-1	—	—	34	.450 3.139
J2	LPT / Floppy	FCI 89947-720 DB-25 to floppy	CBL/CBR-2003 CBL/CBR-2501	12" 2mm latching LPT Floppy adapter cable	31	-0.071 2.465
J3	PLD Reprogramming Port (<i>Factory use Only</i>)	—	—	—	—	.450 2.525
J4	Ethernet	RJ45	—	—	32	3.935 2.545
J5	CompactFlash Type I & II	—	—	—	28	— —
J6	IDE Interface	FCI 89947-144 (IDC)	CBL/CBR-4404 CBL/CBR-4405	12" 2mm IDE cable 2mm to 0.1" adapter	28	3.050 2.247
J7	COM Ports, Keyboard, Mouse, GP Timer inputs, Power LED, Push-button reset, PC speaker, LED	FCI 89947-350LF	CBL/CBR-5009A	12" 2mm latching 50- pin to 50-pin	29	3.265 2.270
J8	Main Power Input	Berg 69176-010 (Housing) + Berg 47715-000 (Pins)	CBL/CBR-1008	Interface from industry standard ATX power supply	24	.0250 -0.050
J9	PC/104	AMP 1375795-2	—	—	34	.050 0.200

‡ Relative to lower left hand mounting hole. See page 17.

Jumper Block Locations

Note: The diagram below shows the as-shipped configuration for jumpers on Rev. 4.xx and earlier boards. On Rev. 5.xx and later boards, no jumper is installed on V3.

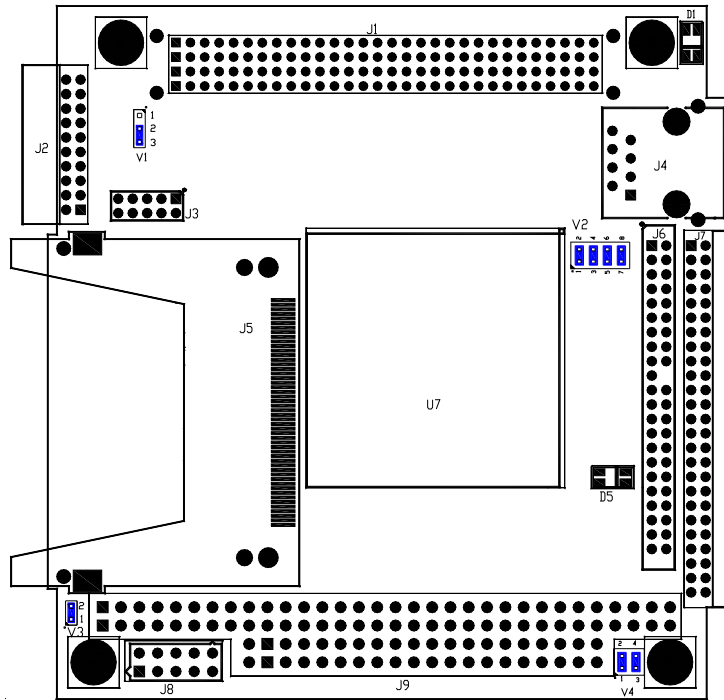


Figure 6. Jumper Block Locations

JUMPER SUMMARY

Table 2: Jumper Summary

Jumper Block	Description	As Shipped	Page
V1	Battery Power Jumper [1-2] In – Discharge CMOS Memory [2-3] In – Standard Operation	[2-3] In	26
V2	COM3 configuration [1-2] In and [3-4] In – RS-485 Endpoint [1-2] In and [3-4] Out – RS-485 Intermediate [1-2] Out and [3-4] In – RS-422	[1-2] In [3-4] In	27
V2	COM4 configuration [5-6] In and [7-8] In – RS-485 Endpoint [5-6] In and [7-8] Out – RS-485 Intermediate [5-6] Out and [7-8] In – RS-422	[5-6] In [7-8] In	27
V3 Rev. 4.xx and earlier	CompactFlash Master/Slave Section In — Master IDE Device Out — Slave IDE Device	In	28
V3 Rev. 5.xx and later	CompactFlash Master/Slave Section In — Slave IDE Device Out — Master IDE Device	Out	28
V4[1-2]	System BIOS Selector In — Run Time System BIOS occupies E0000h to FFFFFh Out — Master System BIOS occupies E0000h to FFFFFh Note: The Run Time System BIOS is field upgradeable using the BIOS upgrade utility. See www.VersaLogic.com/private/lynxsupport.asp for further information.	In	—
V4[3-4]	General Purpose Input Bit In — Bit D0 in SCR register reads as 1 Out — Bit D0 in SCR register reads as 0	In	—

Power Supply

POWER CONNECTORS

Main power is applied to the EPM-4 through a 10-pin polarized connector. Mating connector Berg 69176-010 (Housing) + Berg 47715-000 (Pins). See the table below for connector pinout and page 20 location information.

Warning! To prevent severe and possibly irreparable damage to the system, it is critical that the power connectors be wired correctly. Make sure to use all three +5VDC pins and all four ground pins to prevent excess voltage drop. Some suppliers include a pin-1 indicator on the crimp housing that corresponds to pin-10 of the pinout.

Table 3: Main Power Connector Pinout

J8 Pin	Signal Name	Description
1	Ground	Ground
2	+5VDC	Power Input
3	Ground	Ground
4	+12VDC	Power Input
5	Ground	Ground
6	-12VDC	Power Input
7	+3.3VDC	Power Input
8	+5VDC	Power Input
9	Ground	Ground
10	+5VDC	Power Input

Note: The +3.3VDC, +12VDC, and -12VDC inputs are only required for expansion modules that require these voltages.

Some manufacturers include a pin-1 indicator on the crimp housing that corresponds to pin-10 of the J8 power connector.

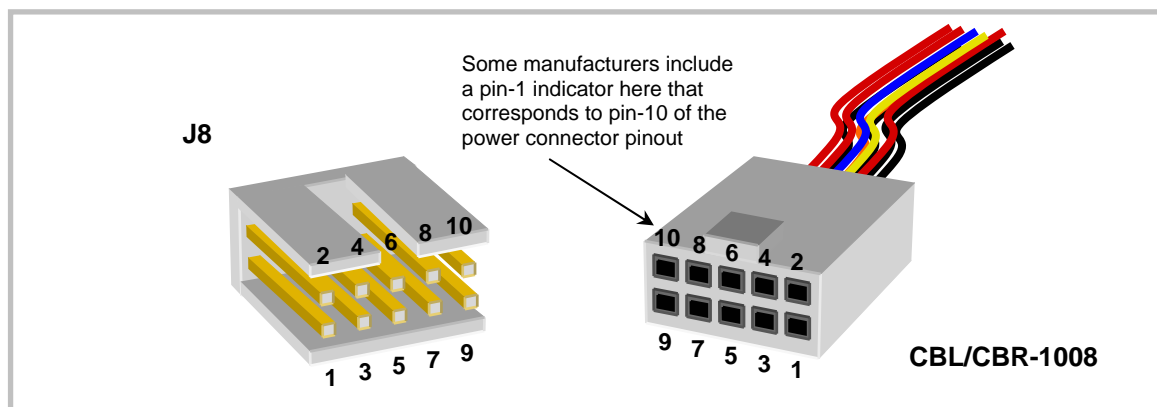


Figure 7. J8 and CBL/CBR-1008 Pin Numbering

POWER REQUIREMENTS

The EPM-4 only requires +5 volts ($\pm 5\%$) for proper operation. The voltage required for the RS-232 ports is generated with an on-board DC/DC converter. A variable low-voltage supply circuit provides power to the CPU and other on-board devices.

The exact power requirement of the EPM-4 depends on several factors peripheral connections, type and number of expansion modules, and attached devices. For example, AT keyboards typically draw their power directly from the EPM-4, and driving long RS-232 lines at high speed can increase power demand. Reducing the CPU speed from 133 MHz to 100 MHz via the BIOS settings will save approximately 0.5 W.

LITHIUM BATTERY

Warning! To prevent shorting, premature failure, or damage to the lithium battery, do not place the unit on a conductive surface such as metal, black conductive foam, or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble, or dispose of in fire. Dispose of used batteries promptly.

Batteries of different voltages are used on different revisions of the EPM-4, as shown below:

EPM-4 Revision	Battery Type	Min. Operating Voltage	Reorder Part No.
Rev 4 and above	3.0V	2.5V	T-HB3/5-2
Rev 2	3.5V	3.0V	T-HB3/5-3

If the operating voltage drops below the minimum, contact the factory for a replacement. Life expectancy under normal use is approximately 10 years.

CPU

The ÉlanSC520 Microcontroller has a 32-bit, low-voltage AMD Am5x86 microprocessor at its core. The maximum clock rate is 133 MHz. The Am5x86 has 16 kb of unified cache that supports write-back and write-through policies. It is a high-performance 486 CPU achieving performance results equal to a Pentium 75.

System RAM

MEMORY

The EPM-4 has 64MB of SDRAM soldered on board.

- Storage Capacity 64 MB
- Voltage 3.3 Volt
- Error Detection Code Not supported
- Error Correction Not supported
- Speed 66 MHz, 60 ns

CMOS RAM

CLEARING CMOS RAM

Jumper V1 can be moved to position [1-2] for 30 seconds to erase the contents of the CMOS RAM. Be sure to move the jumper back to position [2-3] for normal operation.

Note: Operation of the board with jumper V1 in the erase position [1-2] is not supported or recommended.

DEFAULT CMOS RAM SETUP VALUES

After the CMOS RAM is cleared, the system will load default CMOS RAM parameters the next time the board is powered on. The default CMOS RAM setup values will be used in order to boot the system whenever the main CMOS RAM values are blank, or when the system battery is dead or has been removed from the board.

Real Time Clock

The EPM-4 features a year 2000 compliant, battery-backed 146818 compatible real time clock/calendar chip. Under normal battery conditions, the clock will maintain accurate timekeeping functions during periods when the board is powered off.

SETTING THE CLOCK

The CMOS Setup utility (accessed by pressing the [DEL] key during a system boot) can be used to set the time/date of the real time clock.

Battery Backed Static RAM

The EPM-4 can be ordered with an optional 2 MB of Battery Backed Static RAM (BBSRAM). This BBSRAM is powered by the boards RTC battery when main power is turned off. Jumper V1, which is used to clear CMOS RAM, does not affect the BBSRAM.

The BBSRAM is located at the absolute address of (0x08000000) in one continuous 2 MB block.

Serial Ports

The EPM-4 features two on-board 16550 based serial channels located at standard PC I/O addresses. COM1 and COM2 are RS-232 (115.2K baud) serial ports.

COM3 and COM4 can be operated in RS-422 or RS-485 modes. Two additional non-standard baud rates are also available (programmable in the normal baud rate registers), up to 460K baud.

Interrupt assignment for each COM port is handled in CMOS Setup, and each port can be independently enabled or disabled.

All four serial ports are protected against ESD damage. This protection exceeds 15KV human body model.

COM PORT CONFIGURATION

There are no configuration jumpers for COM1 and COM2 because it only operates in RS-232 mode.

Jumper V2 is used to configure COM3 and COM4 for RS-422/485 operation. See page 23 for jumper configuration details.

COM3 AND COM4 RS-485 MODE LINE DRIVER CONTROL

The TxD+/TxD- differential line driver can be turned on and off by manipulating the DTR handshaking line.

The following code example shows how to turn the line driver for COM3 on and off:

```

mov    dx,03ECh    ; Point to COM3 Modem Control register
in     al,dx      ; Fetch existing value
or     al,01h     ; Clear bit D0
out    dx,al      ; Turn DTR on (enables line driver)

in     al,dx      ; Fetch existing value
and    al,0FEh    ; Set bit D0
out    dx,al      ; Turn DTR off (disables line driver)

```

IDE Hard Drive / CompactFlash / CD-ROM Interface

One IDE interface is available to connect up to two IDE devices, such as hard disks, CD-ROM drives or CompactFlash (CF) media. Use CMOS Setup to specify the drive parameters of the attached drives.

An activity indication LED is provided on the EPM-4. The yellow LED of D5 (See page 22) will show that activity is detected on the IDE interface.

A 2mm 44-pin connector (J6) and a CF socket (J5) are provide on the board. Jumper V3 determines if the CF media plugged into J5 is the IDE Master or slave (see Table 2).

Note: The IDE port is a simple interface compatible with PIO mode 0.

Warning! Cable length must be 18" or less to maintain proper signal integrity. The grounds in this connector should not be used to carry motor current.

Table 4: IDE Hard Drive Connector Pinout

J6 Pin	Signal Name	IDE Signal Name	Function
1	HRST*	Host Reset	Reset signal from CPU
2	Ground	Ground	Ground
3	IDE7	DATA 7	Data bit 7
4	ID8	DATA 8	Data bit 8
5	ID6	DATA 6	Data bit 6
6	ID9	DATA 9	Data bit 9
7	ID5	DATA 5	Data bit 5
8	ID10	DATA 10	Data bit 10
9	ID4	DATA 4	Data bit 4
10	ID11	DATA 11	Data bit 11
11	ID3	DATA 3	Data bit 3
12	ID12	DATA 12	Data bit 12
13	ID2	DATA 2	Data bit 2
14	ID13	DATA 13	Data bit 13
15	ID1	DATA 1	Data bit 1
16	ID14	DATA 14	Data bit 14
17	ID0	DATA 0	Data bit 0
18	ID15	DATA 15	Data bit 15
19	Ground	Ground	Ground
20	NC	NC	No connection
21	IDEDRQ	IDEDRQ	DMA/Request
22	Ground	Ground	Ground
23	IOWR*	HOST IOW*	I/O write
24	Ground	Ground	Ground
25	IORD*	HOST IOR*	I/O read
26	Ground	Ground	Ground
27	RDY	Ready	Wait control
28	HAEN	ALE	Address latch enable
29	IDEDACK	IDEACK	DMA/Ack.
30	Ground	Ground	Ground
31	HINT	HOST IRQ10	IRQ10
32	XI16*	HOST IOCS16*	Drive register enabled
33	PA1	HOST ADDR1	Address bit 1
34	NC	NC	No connection
35	PA0	HOST ADDR0	Address bit 0
36	PA2	HOST ADDR2	Address bit 2
37	ECS0*	HOST CS0*	Reg. Access chip select 0
38	ECS1*	HOST CS1*	Reg. Access chip select 1
39	NC	NC	No connection
40	Ground	Ground	Ground
41	5V	Power	Power
42	5V	Power	Power
43	Ground	Ground	Ground
44	NC	NC	No connection

KEYBOARD/MOUSE INTERFACE

A standard PS/2 keyboard and mouse interface is accessible through connector J7.

This device is protected against ESD damage by IC 61000-402 rated transient voltage suppressor components.

PROGRAMMABLE LED

The high-density I/O connector J7 includes an output signal for attaching a software controlled LED. Connect the cathode of the LED to J7[48]; anode to J7[47]. An on-board resistor limits the current to 15 mA when the circuit is turned on.

The 5V supply for this feature is protected by a self resetting fuse. This 1 Amp fuse is used to protect KB, mouse, speaker, and LED.

The programmable LED is controlled by the PIO24 pin on the ÉlanSC520 microcontroller. It can be turned on and off by writing the word 0100h to MMCR offsets 0C3Ah and 0C36h, respectively.

The MMCR base address defaults to DF00:0 (segment : offset address).

The external LED is duplicated with an on-board LED. The green LED in D5 (See page 22) is also controlled by the PIO24 pin.

Note: The LED is turned on by the BIOS during system startup. This causes the light to function as a "power on" indicator if it is not otherwise controlled by user code.

EXTERNAL SPEAKER

A miniature 8 ohm speaker can be connected between J7[49] and J7[50].

The 5V supply for this feature is protected by a self resetting fuse. This 1 Amp fuse is used to protect KB, mouse, speaker, and LED.

PUSH-BUTTON RESET

A normally open, momentary action push-button reset switch can be connected between J7[37] and J7[38]. Shorting J7[37] to ground will cause the EPM-4 to reboot.

GENERAL-PURPOSE TIMER INPUTS

Two flexible general-purpose timer inputs can be used for timing and counting applications. Each timer is capable of generating an interrupt, selectable via the BIOS Custom Configuration screen. For more information, see chapter 17 in the ÉlanSC520 Microcontroller User's Manual.

Parallel / Floppy Port

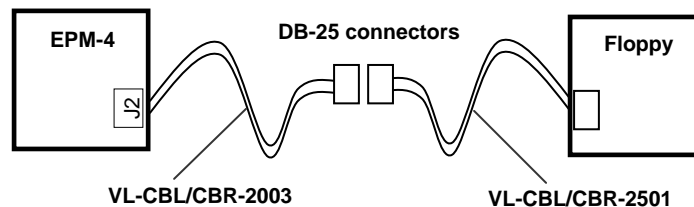
PARALLEL PORT OPERATION

The EPM-4 includes a standard bi-directional/EPP/ECP compatible LPT port which resides at the PC standard address of 378h. The port can be enabled or disabled and interrupt assignments can be made via the CMOS setup screen. The LPT mode is also set via the CMOS setup screen.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

FLOPPY PORT OPERATION

The parallel port can be used as a floppy disk interface. Select "FDD" as the LPT mode in CMOS Setup and connect a floppy disk drive to the parallel port cable (CBL/CBR-2003) using the floppy disk cable (CBL/CBR-2501). The diagram below shows how to connect the drive.



PARALLEL / FLOPPY PORT PINOUT

Table 6: LPT1 Parallel / Floppy Port Pinout

J2 Pin	Centronics Signal	Floppy Signal	Signal Direction
1	Strobe	DS0*	Out
2	Auto feed	RPM	Out
3	Data bit 1	INDEX*	In/Out
4	Printer error	HDSEL*	In
5	Data bit 2	TRK0*	In/Out
6	Reset	FDIR	Out
7	Data bit 3	WP*	In/Out
8	Select input	STEP*	Out
9	Data bit 4	RDATA*	In/Out
10	Data bit 5	DSKCHG	In/Out
11	Data bit 6	N.C.	In/Out
12	Data bit 7	MTR0*	In/Out
13	Data bit 8	N.C.	In/Out
14	Ground	GND	—
15	Acknowledge	DS1*	In
16	Ground	GND	—
17	Port Busy	MTR1*	In
18	Ground	GND	—
19	Paper End	WDATA*	In
20	Select	WGATE*	In

Ethernet Interface

The EPM-4 features an industry-standard 10baseT / 100baseTX Ethernet interface based on the Intel 82551ER Ethernet controller. This PCI based interface chip is widely supported. Drivers are readily available to support a variety of operating systems such as QNX, VxWorks and other RTOS vendors.

BIOS CONFIGURATION

The Ethernet interface shares PC/104-Plus interrupt "INTC". The CMOS Setup screen is used to select the IRQ line routed to INTC*.

STATUS LED

Two colored LEDs (D1) located next to the RJ-45 connector provide an indication of the Ethernet status as follows:

Green LED (Link / Activity)

- ON Active Ethernet cable plugged into J4.
No Tx/Rx data activity.
- OFF Cable not plugged into J4
Cable not plugged into active hub
- BLINKING Active Ethernet cable plugged into J4.
Tx or Rx data activity detected on the cable

Yellow LED (Speed)

- ON 100baseTx (Fast) detected on Ethernet cable.
- OFF 10BaseTx (Slow) detected on Ethernet cable.

ETHERNET CONNECTOR

A board-mounted RJ-45 connector is provided to make connection with category 5 Ethernet cable. The Ethernet controller will autodetect 10BaseT/100BaseTX connections.

Table 7: RJ45 Ethernet Connector

J4 Pin	Signal Name	Function
4	IGND	Isolated Ground
5	IGND	Isolated Ground
6	R-	Receive Data -
3	R+	Receive Data +
7	IGND	Isolated Ground
8	IGND	Isolated Ground
2	T-	Transmit Data -
1	T+	Transmit Data +

This device is protected against ESD damage by IEC 61000-4-2 rated transient voltage suppressor components.

Watchdog Timer

There is a flexible watchdog timer integrated into the ÉlanSC520 Microcontroller. It supports a time-out period up to 30 seconds, and can generate an interrupt, NMI, or system reset when time-out occurs. The watchdog registers are protected by write key sequences.

See the following pseudo code as a simple example of watchdog operation.

```

MMCR_base = DF00:0h      ; segment:offset address
WDTMRCTL = MMCR_base + 0CB0h
MemWrite WDTMRCTL, 03333h ; Key sequence to allow write access to
                          ; control
MemWrite WDTMRCTL, 0CCCCh ; register. These are 16-bit memory writes.
MemWrite WDTMRCTL, 0C010h ; Enable watchdog timer. 4 second timer.
                          ; Reset on timeout.

Begin program loop
                          ; perform useful instructions here that
                          ; will never take more than 4
                          ; seconds to complete.

MemWrite WDTMRCTL, 0AAAAh ; Key sequence to reset the timer
                          ; countdown

MemWrite WDTMRCTL, 05555h ; These are 16-bit memory writes.

End program loop

```

For detailed programming instructions for the integrated watchdog timer, see chapter 19 of the ÉlanSC520 Microcontroller User's Manual, and chapter 16 of the Register Set Manual.

Expansion Bus

The EPM-4 will accept up to eight expansion modules, up to four of which can be PC/104-Plus (PCI) expansion modules. The EPM-4 uses 3.3V PCI signaling but is 5V tolerant.

PC/104-PLUS (PCI Bus)

PC/104-Plus modules can be secured directly to the top or bottom of the EPM-4. Make sure to correctly configure the "slot position" jumpers on each PC/104-Plus module appropriately. PC/104 modules must not be positioned between the EPM-4 and any PC/104-Plus modules on the stack.

The EPM-4 is compliant with revision 2.0 of the PC/104-Plus spec. and can support four bus master capable PC/104-Plus modules.

The BIOS automatically allocates I/O and memory resources. However, manual PCI Interrupt routing will be used.

PC/104 (ISA Bus)

PC/104 modules are stacked on top the EPM-4. 16-bit modules first followed by 8-bit PC/104 modules.

The ÉlanSC520 Microcontroller uses a General-Purpose (GP) bus that is implemented as the ISA bus on the Lynx. The GP bus is similar in function to the ISA bus, but not functionally identical. Nearly all PC/104 devices in use today will work on the Lynx without modification.

Here is a summary of the differences between a legacy ISA bus and the GP bus implementation on the Lynx.

- Only DMA channels 5 and 6 are available to PC/104 devices
- IRQ15 is not available to PC/104 devices
- PC/104 bus devices cannot initiate bus access cycles. The ÉlanSC520 Microcontroller is always the master of the ISA bus.
- Address pipelining is not supported.
- IOCHK, REFRESH, and NOWS signals are not supported.
- MEMR and SMEMR are tied together. MEMW and SMEMW are tied together.

For a more detailed description of the GP bus and its differences from a standard ISA bus, see chapter 13 in the ÉlanSC520 Microcontroller User's Manual.

Note: On the EPM-4 Rev 4 and above, the pass-through PC/104 (ISA) connector is keyed (pins B10 and C19 missing) for greater compatibility with the PC/104 standard. See Figure 5 for details.

I/O CONFIGURATION

PC/104-Plus Modules

No hardware configuration is necessary except to jumper the expansion module for the correct slot number.

PC/104 Modules

PC/104 I/O modules should be addressed in the 104h – 3FFh address range. Care must be taken to avoid the I/O addresses shown in the *On-Board I/O Devices* table on page 37. These ports are used by on-board peripherals and video devices.

Memory and I/O Map

ÉLANSC520 MEMORY MAPPED CONFIGURATION REGION (MMCR) REGISTERS

Much of the functionality incorporated into the ÉlanSC520 Microcontroller, such as the watchdog timer, CPU speed control, and general-purpose timer, can be controlled and monitored through the Memory Mapped Configuration Region (MMCR) registers. The MMCR registers occupy 4KB of memory space. For convenience, these registers are made available at boot time in the first megabyte of system RAM, at DF000h.

Wherever the MMCR is located, its 4KB footprint will cover and take precedence over the underlying memory space function. For example, when the D0000h page function is set to ISA bus, DF000h through DFFFFh will instead be occupied by the MMCR. For this reason, the maximum BIOS extension size is reduced from 64KB to 60KB.

In the event of an address conflict, the MMCR base address can be moved at any time with an I/O write to the Configuration Base Address Register (CBAR), located at I/O address FFFCh. Refer to the ÉlanSC520 Register Set Manual for further details.

MEMORY MAP

The lower 1 MB memory map of the EPM-4 is arranged as shown in the following table.

Table 8: Memory Map

Start Address	End Address	Comment
E0000h	FFFFFh	System BIOS
DF000h	DFFFFh	MMCR Registers (see note)
D0000h	DEFFFh	ISA memory, BIOS extension, or RAM
C0000h	CFFFFh	Reserved for Video BIOS
A0000h	BFFFFh	Reserved for Video RAM
00000h	9FFFFh	System DRAM

Note: Default location. If MMCR is relocated, this memory space is allocated to ISA memory, BIOS extension, or RAM, depending on how the D0000h page function is set in CMOS Setup.

I/O MAP

The following table lists the common I/O devices in the EPM-4 I/O map. User I/O devices should be added in the 104h – 3FFh range, using care to avoid the devices already in the map as shown below.

Table 9: On-Board I/O Devices

I/O Device	Standard I/O Addresses
See ÉlanSC520 register set manual	000h-0FFh
Special Control Register	0E0h
Revision Indicator Register	0E1h
Map and Paging Control Register	0E3h
Primary IDE Controller	1F0h – 1F6h
COM 4 Serial Port	2E8h – 2EFh
COM 2 Serial Port	2F8h – 2FFh
COM 3 Serial Port	3E8h – 3EFh
Floppy Disk Controller	3F0h – 3F7h
COM1 Serial Port	3F8h – 3FFh
CBAR	FFFCh-FFFFh

Note: I/O ports occupied by on-board devices are freed up when the device is disabled in CMOS Setup.

Interrupt Configuration

Default interrupt settings on the Lynx have been selected to maintain PC/AT compatibility. They can be re-routed to satisfy customer constraints. Use the custom configuration screen in BIOS setup to configure IRQ's on the Lynx. Not all devices can use all IRQ's. Refer to Figure 8 for a description of allowable IRQ assignments for each device.

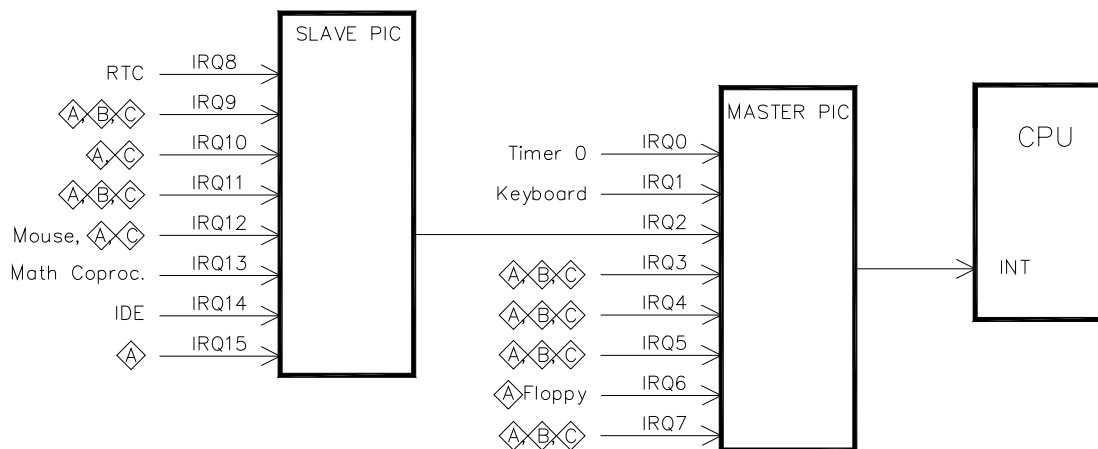


Figure 8. Interrupt Circuit Diagram

Components Group:	
A	COM1, COM2, GP Timers, Watchdog, PCI Interrupts.
B	COM3, COM4, LPT1
C	Available on PC/104 (ISA) bus

Default IRQ assignments:	
0	Timer 0
1	Keyboard
2	Slave PIC cascade
3	COM2
4	COM1
5	Unused
6	Floppy drive
7	Unused
8	Real-Time Clock
9	Unused
10	Unused
11	PCI Interrupt A,B,C,D
12	PS/2 Mouse
13	Math Co-processor
14	IDE controller
15	Unused

Special Control Register

SCR (READ/WRITE) 00E0h

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	SB-SEL	Reserved	Reserved	Reserved	Reserved	GPI

Table 10: Special Control Register Bit Assignments

Bit	Mnemonic	Description
D7-D6	—	Reserved — These bits have no function.
D5	SB-SEL	BIOS Selector Input — Indicates the status of jumper V4[1-2] SB-SEL = 0 Jumper V4 [1-2] = Out (Master BIOS) SB-SEL = 1 Jumper V4 [1-2] = In (Run Time BIOS) <i>Note: This general purpose bit is read-only.</i>
D4-D1	—	Reserved — These bits have no function.
D0	GPI	General Purpose Input — Indicates the status of TTL input GPI = 0 Jumper V4 [3-4] = Out GPI = 1 Jumper V4 [3-4] = In <i>Note: This bit is a read-only bit.</i>

Revision Indicator Register

REVIND (READ ONLY) 00E1h

D7	D6	D5	D4	D3	D2	D1	D0
PC4	PC3	PC2	PC1	PC0	REV1	REV0	ET

This register is used to indicate the revision level of the EPM-4 product.

Bit	Mnemonic	Description															
D7-D3	PC4-PC0	<p>Product Code — These bits are hard coded to represent the product type. The EPM-4 will always read as 11011. Other codes are reserved for future products.</p> <table> <tr> <td>PC4</td> <td>PC3</td> <td>PC2</td> <td>PC1</td> <td>PC0</td> <td>Product Code</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>EPM-4</td> </tr> </table> <p><i>Note: These bits are read-only.</i></p>	PC4	PC3	PC2	PC1	PC0	Product Code	1	1	0	1	1	EPM-4			
PC4	PC3	PC2	PC1	PC0	Product Code												
1	1	0	1	1	EPM-4												
D2-D1	REV1-REV0	<p>Revision Level — These bits are represent the EPM-4 circuit revision level.</p> <table> <tr> <td>REV1</td> <td>REV0</td> <td>Revision Level</td> </tr> <tr> <td>0</td> <td>0</td> <td>Current product release</td> </tr> <tr> <td>0</td> <td>1</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>1</td> <td>Reserved</td> </tr> </table> <p><i>Note: These bits are read-only.</i></p>	REV1	REV0	Revision Level	0	0	Current product release	0	1	Reserved	1	0	Reserved	1	1	Reserved
REV1	REV0	Revision Level															
0	0	Current product release															
0	1	Reserved															
1	0	Reserved															
1	1	Reserved															
D0	ET	<p>Extended Temperature — This bit indicates whether the board is an extended temperature version or not.</p> <p>0 – EPM-4c – Standard Temperature 1 – EPM-4e – Extended Temperature</p> <p><i>Note: This bit is read-only.</i></p>															

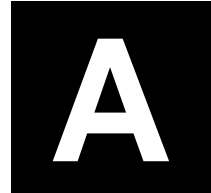
Map and Paging Control Register

MPCR (READ/WRITE) 00E3H

D7	D6	D5	D4	D3	D2	D1	D0
FPGEN	Reserved	Reserved	Reserved	Reserved	PG2	PG1	PG0

Table 11: Map and Paging Control Register Bit Assignments

Bit	Mnemonic	Description																																				
D7	FPGEN	<p>FLASH Paging Enable — Enables a 64KB page frame from E0000h to EFFFFh. Used to gain access to the on-board FLASH memory.</p> <p>FPGEN = 0 FLASH page frame disabled. FPGEN = 1 FLASH page frame enabled.</p> <p><i>Note: When FPGEN = 1, the Page Select bits are used to access various blocks within the FLASH. The "D0000h 64k page function" in CMOS Setup must be set to "ISA Bus".</i></p>																																				
D6-D3	—	Reserved — These bits have no function.																																				
D2-D0	PG2-PG0	<p>Page Select — Selects which 64K block of FLASH will be mapped into the page frame.</p> <table border="1"> <thead> <tr> <th>PG2</th> <th>PG1</th> <th>PG0</th> <th>Memory Range within FLASH</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>000000h to 00FFFFh</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>010000h to 01FFFFh</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>020000h to 02FFFFh</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>030000h to 03FFFFh</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>040000h to 04FFFFh</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>050000h to 05FFFFh</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>060000h to 06FFFFh</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>070000h to 07FFFFh</td> </tr> </tbody> </table>	PG2	PG1	PG0	Memory Range within FLASH	0	0	0	000000h to 00FFFFh	0	0	1	010000h to 01FFFFh	0	1	0	020000h to 02FFFFh	0	1	1	030000h to 03FFFFh	1	0	0	040000h to 04FFFFh	1	0	1	050000h to 05FFFFh	1	1	0	060000h to 06FFFFh	1	1	1	070000h to 07FFFFh
PG2	PG1	PG0	Memory Range within FLASH																																			
0	0	0	000000h to 00FFFFh																																			
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1	1	0	060000h to 06FFFFh																																			
1	1	1	070000h to 07FFFFh																																			



CBL/CBR-5009 Connectors

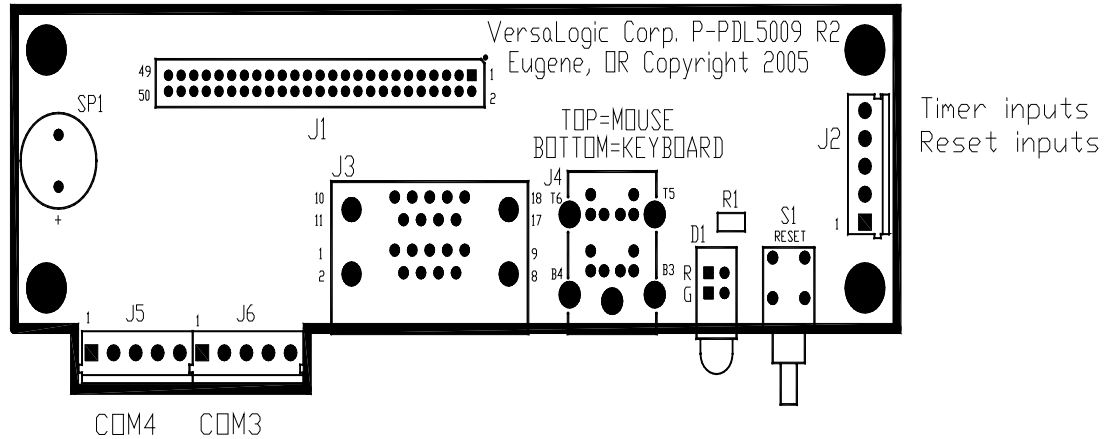


Figure 9. CBL/CBR-5009 Connector and Component Locations

Table 12: Connector/Component Functions, and Interface Cables

Connector / Component	Function	Part Number	Description
D1	Power and Programmable LEDs	Dialight 552-0211	LEDx2 T1 3/4 PC Mount Red/Red
J1	High Density Connector	FCI 98414-F06-50U	2mm, 50 pins, keyed, latching header
J2	Timer and Reset input	Conta-Clip 10250.4	5 pin screw terminal
J3	COM1, COM2	Kycon K42-E9P/P-A4N	Dual stacked DB-9 male
J4	PS/2 Keyboard and Mouse	Kycon KMDG-6S/6S-S4N	Dual stacked PS/2 female
J5	COM4	Conta-Clip 10250.4	5 pin screw terminal
J6	COM3	Conta-Clip 10250.4	5 pin screw terminal
R1	Resistor	DigiKey P332CCT-ND	332 ohms
S1	Reset Button	E-Switch 800SP9B7M6RE	Right angle momentary switch
SP1	Speaker	Challenge Electronics DBX05	Miniature speaker

CBL/CBR-5009 Dimensions and Mounting

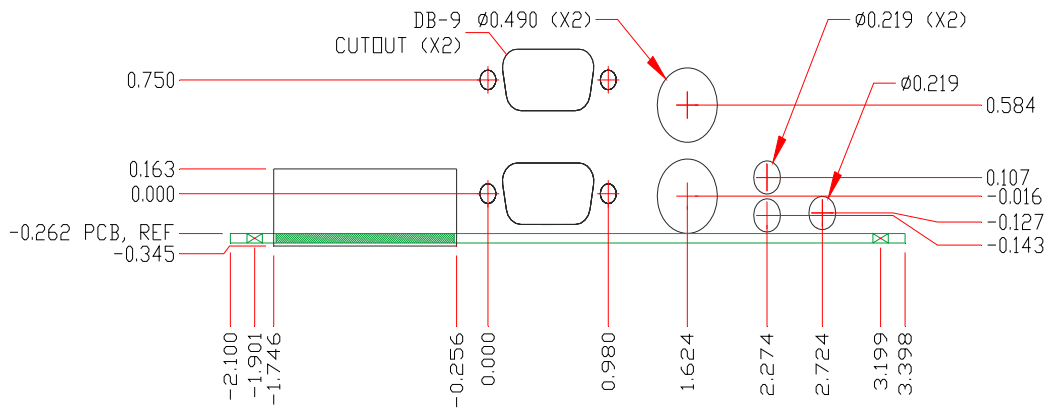


Figure 10. CBL-5009 Dimensions and Mounting

CBL/CBR-5009 Schematic

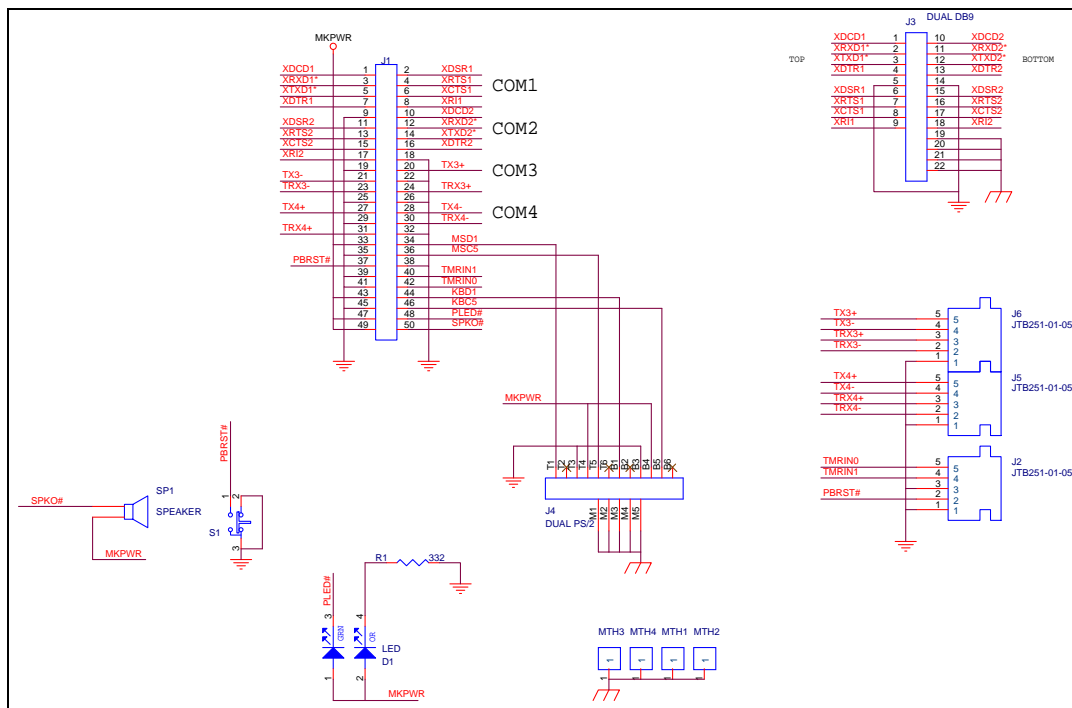


Figure 11. CBL/CBR-5009 Schematic

Appendix B — References

B

- | | |
|---|--|
| Integrated 32-bit CPU
<i>ÉlanSC520</i> | Advanced Micro Devices , (www.amd.com/epd) |
| Ethernet Controller
<i>82551ER</i> | Intel Corporation , (www.intel.com/design) |
| PC/104 Specification
<i>PC/104 Resource Guide</i> | PC/104 Consortium , (www.pc104.org) |
| PC/104-Plus Specification
<i>PC/104 Resource Guide</i> | PC/104 Consortium , (www.pc104.org) |
| General PC Documentation
<i>The Programmer's PC Sourcebook</i> | Microsoft Press (www.microsoft.com/learning/books) |
| General PC Documentation
<i>The Undocumented PC</i> | Powell's Books (www.powells.com) |

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