88F6281

Integrated Controller

Hardware Specifications

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Marvell. Moving Forward Faster

Document Conventions

	**Note:** Provides related information or information of special importance.
	**Caution:** Indicates potential damage to hardware or software, or loss of data.
	**Warning:** Indicates a risk of personal injury.

Document Status

Doc Status: Preliminary	Technical Publication: 0.xx

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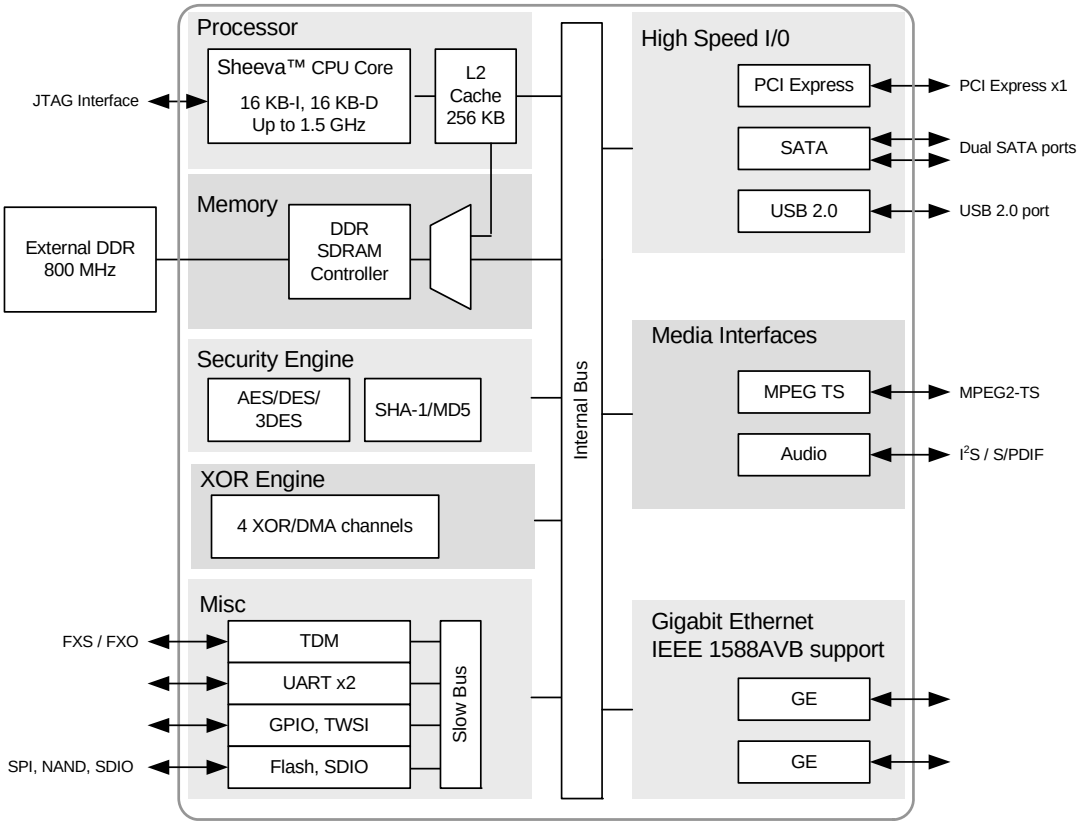
PRODUCT OVERVIEW

The Marvell® 88F6281 is a high-performance, highly integrated controller. The 88F6281 is based on the Marvell proprietary, ARMv5TE-compliant, high-speed Sheeva™ CPU core. The CPU core integrates a 256 KB L2 cache.



88F6281 Functional Block Diagram

FEATURES

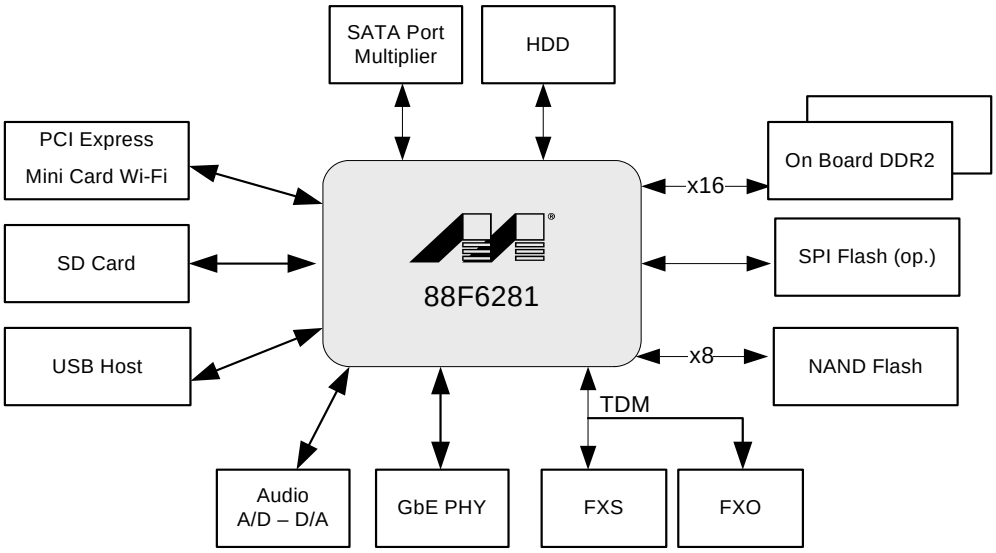
- **The 88F6281 includes:**
  - High-performance CPU core, running at up to 1.5 GHz, with integrated, four-way, set-associative L1 16-KB I-cache/16-KB D-cache and unified, 256-KB, four-way, set-associative L2 cache
  - High-bandwidth dual-port DDR2 memory interface (16-bit DDR2 SDRAM @ up to 800 MHz data rate)
  - PCI Express (x1) port with integrated PHY
  - Two Gigabit Ethernet (10/100/1000 Mbps) MACs
  - USB 2.0 port with integrated PHY
  - Two SATA 2.0 ports with integrated 3 Gbps SATA II PHY
  - Security Cryptographic engine
  - S/PDIF (Sony/Philips Digital Interconnect Format) / I^2S (Integrated Interchip Sound) Audio in/out interface
  - SD/SDIO/MMC interface
  - TDM SLIC/SLAC Codec interface
  - Two XOR engines, each containing two XOR/DMA channels (a total of four XOR/DMA channels)
  - MPEG Transport Stream (TS) interface
  - SPI port with SPI flash boot support
  - 8-bit NAND flash interface with boot support
  - Two 16550 compatible UART interfaces
  - TWSI port
  - 50 multi-purpose pins
  - Internal Real Time Clock (RTC)
  - Interrupt controller
  - Timers
  - 128-bit eFuse (one-time programmable memory)
- **Sheeva™ CPU core**
  - Up to 1.5 GHz
  - 32-bit and 16-bit RISC architecture
  - Compliant with v5TE architecture, as published in the *ARM Architect Reference Manual*, Second Edition
  - Includes MMU to support virtual memory features
  - 256-KB, four-way, set-associative L2 unified cache
  - 16-KB, four-way, set-associative I-cache
  - 16-KB, four-way, set-associative D-cache
  - 64-bit internal data bus
  - Branch Prediction Unit
  - Supports JTAG/ARM ICE
  - Supports both Big and Little Endian modes
- **DDR2 SDRAM controller**
  - 16-bit interface
  - Up to 400 MHz clock frequency (800 MHz data rate)
  - DDR SDRAM with a clock ratio of 1:N and 2:N between the DDR SDRAM and the CPU core, respectively
  - SSTL 1.8V I/Os
  - Auto calibration of I/Os output impedance
  - Supports four DRAM chip selects
  - Supports all DDR devices densities up to 2 Gb
  - Supports up to 32 open pages (page per bank)
  - Up to 2 GB total address space
  - Supports on-board DDR designs (no DIMM support)
  - Supports 2T mode, to enable high-frequency operation under heavy load configuration
  - Supports DRAM bank interleaving
  - Supports up to a 128-byte burst per single memory access
- **PCI Express interface (x1)**
  - PCI Express Base 1.1 compatible
  - Integrated low-power SERDES PHY, based on proven Marvell® SERDES technology
  - Serves as a Root Complex or an Endpoint port
  - x1 link width
  - 2.5 Gbps data rate
  - Lane polarity reversal support
  - Maximum payload size of 128 bytes
  - Single Virtual Channel (VC-0)
  - Replay buffer support
  - Extended PCI Express configuration space
  - Advanced Error Reporting (AER) support
  - Power management: L0s and software L1 support
  - Interrupt emulation message support
  - Error message support
- **PCI Express master specific features**
  - Single outstanding read transaction
  - Maximum read request of up to 128 bytes
  - Maximum write request of up to 128 bytes
  - Up to four outstanding read transactions in Endpoint mode
- **PCI Express target specific features**
  - Supports up to eight read request transactions
  - Maximum read request size of 4 KB
  - Maximum write request of 128 bytes
  - Supports PCI Express access to all of the controller's internal registers
- **Two Integrated GbE (10/100/1000) MAC ports**
  - Supports 10/100/1000 Mbps
  - Dedicated DMA for data movement between memory and port

- Priority queuing on receive based on Destination Address (DA), VLAN Tag, and IP TOS
- Layer 2/3/4 frame encapsulation detection
- TCP/IP checksum on receive and transmit
- Supports proprietary 200 Mbps Marvell MII (MMII) interface
- Supports four modes:
  - Port 0 RGMII, Port 1 RGMII
  - Port 0 RGMII, Port 1 MII/MMII
  - Port 0 MII/MMII, port 1 RGMII
  - Port 0 GMII, Port 1 N/A

•DA filtering

- **Precise Timing Protocol (PTP)**
  - Supports precise time stamping for packets, as defined in IEEE 1588 PTP v1 and v2 and IEEE 802.1AS draft standards
  - Supports Flexible Time Application interface to distribute PTP clock and time to other devices in the system
  - Optionally accepts an external clock input for time stamping
- **Audio Video Bridging networks**
  - Supports IEEE 802.1Qav draft Audio Video Bridging networks
  - Supports time- and priority-aware egress pacing algorithm to prevent bunching and bursting effects—suitable for audio/video applications
  - Supports Egress Jitter Pacer for AVB-Class A and AVB-Class B traffic and strict priority for legacy traffic queues
- **USB 2.0 port**
  - Serves as a peripheral or host
  - USB 2.0 compliant
  - Integrated USB 2.0 PHY
  - Enhanced Host Controller Interface (EHCI) compatible as a host
  - As a host, supports direct connection to all peripheral types (LS, FS, HS)
  - As a peripheral, connects to all host types (HS, FS) and hubs
  - Up to four independent endpoints, supporting control, interrupt, bulk, and isochronous data transfers
  - Dedicated DMA for data movement between memory and port
- **Two Integrated Marvell 3 Gbps (Gen2i) SATA PHYs**
  - Compliant with SATA II Phase 1 specifications
    - Supports SATA II Native Command Queuing (NCQ), up to 128 outstanding commands per port
    - Fully supports first party DMA (FPDMA)
    - Backwards compatible with SATA I devices
  - Supports SATA II Phase 2 advanced features
    - 3 Gbps (Gen2i) SATA II speed
    - Port Multiplier (PM)—Performs FIS-based switching, as defined in SATA working group PM definition
    - Port Selector (PS)—Issues the protocol-based Out-Of-Band (OOB) sequence for selecting the active host port
  - Supports device 48-bit addressing
  - Supports ATA Tag Command Queuing
- **SATA II Host Controller**
  - Enhanced-DMA (EDMA) for the SATA ports
  - Automatic command execution, without host intervention
  - Command queuing support, for up to 32 outstanding commands
  - Separate SATA request/response queues
  - 64-bit addressing support for descriptors and data buffers in system memory
  - Read ahead
  - Advanced interrupt coalescing
  - Target mode operation—supports attaching two 88F6281 controllers through their Serial-ATA ports, enabling data communication between the 88F6281 controllers
  - Advanced drive diagnostics via the ATA SMART command
- **Cryptographic engine**
  - Hardware implementation on encryption and authentication engines, to boost packet processing speed
  - Dedicated DMA to feed the hardware engines with data from the internal SRAM memory or from the DDR memory
  - Implements AES, DES, and 3DES encryption algorithms
  - Implements SHA1 and MD5 authentication algorithms
- **S/PDIF / I^2S Audio In/Out interface**
  - Either S/PDIF or I^2S inputs can be active at one time
  - Both S/PDIF and I^2S outputs can be simultaneously active, transferring the same PCM data
- **S/PDIF-specific features**
  - Compliant with 60958-1, 60958-3, and IEC61937 specifications
  - Sample rates of 44.1/48/96 kHz
  - 16/20/24-bit depths

- **I²S-specific features**
  - Sample rates of 44.1/48/96 kHz
  - I²S input and I²S output operate at the same sample rate
  - 16/24-bit depths
  - I²S in and I²S out support independent bit depths (16 bit/24 bit)
  - Supports plain I²S, right-justified and left-justified formats
- **SD/SDIO/MMC host interface**
  - 1-bit/4-bit SDmem, SDIO, and MMC cards
  - Up to 50 MHz
  - Hardware generate/check CRC, on all command and data transactions on the card bus
- **TDM SLIC/SLAC Codec interface**
  - Generic interface to standard SLIC/SLAC codec devices
  - Compatible with standard PCM highway formats
  - TDM protocol support for two channels, up to 128 time slots
  - Dedicated SPI interface for codec management
  - Integrated DMA to transfer voice data to/from memory buffer
- **Two XOR engines and DMA**
  - Two XOR/DMA channels per XOR engine (for a total of four XOR/DMA channels)
  - Chaining via linked-lists of descriptors
  - Moves data from source interface to destination interface
  - Supports increment or hold on both Source and Destination Addresses
  - Supports XOR operation, on up to eight source blocks—useful for RAID applications
  - Supports iSCSI CRC-32 calculation
- **NAND flash controller**
  - 8-bit NAND flash interface
  - Glueless interface to CE Care and CE Don't Care NAND flash devices
  - Boot support
- **Serial Peripheral Interface (SPI) controller**
  - Up to 50 MHz clock
  - Supports direct boot from external SPI serial flash memory
- **MPEG Transport Stream (TS) interface**
  - ISO/IEC 13818-1 standard compliant
  - Supports any one of the following modes:
    - Parallel (8 bit) input
    - Parallel output
    - Two independent serial interfaces
  - Data rate up to 80 Mbps
- **Two UART Interfaces**
  - 16550 UART compatible
  - Two pins for transmit and receive operations
  - Two pins for modem control functions
- **Two-Wire Serial Interface (TWSI)**
  - General purpose TWSI master/slave port
  - Can also be used for serial ROM initialization
- **50 dedicated Multi-Purpose Pins (MPPs) for peripheral functions and general purpose I/O**
  - Each pin can be configured independently.
  - GPIO inputs can be used to register interrupts from external devices, and to generate maskable interrupts.
  - Only two of the following multiplexed interfaces may be configured simultaneously:
    - Audio
    - TS
    - TDM
    - GbE Port 0 in GMII mode or GbE Port 1
- **Interrupt Controller**
  Maskable interrupts to CPU core
  (and PCI Express for a PCI Express endpoint)
- **Two general purpose 32-bit timers/counters**
- **Internal architecture**
  - Mbus-L bus for high-performance, low-latency CPU core to DDR SDRAM connectivity
  - Advanced Mbus architecture
  - Dual port DDR SDRAM controller connectivity to both CPU and Mbus
- **Bootable from**
  - SPI flash
  - SATA device
  - NAND flash
  - PCI Express
  - UART (for debug purpose)
- **288-pin HSBGA package, 19 x 19 mm, 1 mm ball pitch**



Usage Model Example: VoIP Gateway

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Preface

About this Document

This datasheet provides the hardware specifications for the 88F6281 integrated controller. The hardware specifications include detailed pin information, configuration settings, electrical characteristics and physical specifications.

This datasheet is intended to be the basic source of information for designers of new systems.

In this document, the “88F6281” is often referred to as the “device”.

Related Documentation

The following documents contain additional information related to the 88F6281:

- *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*, Doc No. MV-S104860-U0
- *Sheeva™ 88SV131 ARM v5TE Processor Core with MMU and L1/L2 Cache Datasheet*, Doc No. MV-S104950-U0
- *Unified Layer 2 (L2) Cache for Sheeva™ CPU Cores Addendum*, Doc No. MV-S104858-U0
- *88F6180, 88F6190, 88F6192, and 88F6281 Functional Errata, Interface Guidelines, and Restrictions*, Doc No. MV-S501157-U0
- *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide*, Doc No. MV-S301398-00[1]
- *AN-63: Thermal Management for Marvell Technology Products* Doc No. MV-S300281-00[1]
- *AN-179: TWSI Software Guidelines for Discovery™, Horizon™, and Feroceon® Devices*, Doc No. MV-S300754-00[1]
- *AN-183: 88F5181 and 88F5281 Big Endian and Little Endian Support*, Doc No. MV-S300767-00[1]
- *AN-249: Configuring the Marvell® SATA PHY to Transmit Predefined Test Patterns*, Doc No. MV-S301342-00[1]
- *AN-260 System Power-Saving Methods for 88F6180, 88F6190, 88F6192, and 88F6281*, Doc No. MV-S301454-00[1]
- *TB-227: Differences Between the 88F6190, 88F6192, and 88F6281 Stepping Z0 and A0*, Doc No. MV-S105223-00[1]
- White Paper, *ThetaJC, ThetaJA, and Temperature Calculations,* Doc No. MV-S700019-00
- *ARM Architecture Reference Manual*, Second Edition
- *PCI Express Base Specification*, Revision 1.1
- *Universal Serial Bus Specification*, Revision 2.0, April 2000, Compaq, Hewlett-Packard, Intel, Lucent, Microsoft, NEC, Philips
- *Enhanced Host Controller Interface Specification for Universal Serial Bus*, Revision 0.95, November 2000, Intel Corporation
- *ARC USB-HS OTG High-Speed Controller Core reference V 4.0.1*
- Federal Information Processing Standards (FIPS) 46-2 (Data Encryption Standard)
- FIPS 81 (DES Modes of Operation)
- FIPS 180-1 (Secure Hash Standard)
- FIPS draft - Advanced Encryption Standard (Rijndeal)

1. This document is a Marvell proprietary, confidential document, requiring an NDA and can be downloaded from the Marvell Extranet.

- RFC 1321 (The MD5 Message-Digest Algorithm)
- RFC 1851 – The ESP Triple DES Transform
- RFC 2104 (HMAC: Keyed-Hashing for Message Authentication).
- RFC 2405 – The ESP DES-CBC Cipher Algorithm With Explicit IV
- IEEE standard, 802.3-2000 Clause 14
- ANSI standard X3.263-1995

See the Marvell Extranet website for the latest product documentation.

Document Conventions

The following conventions are used in this document:

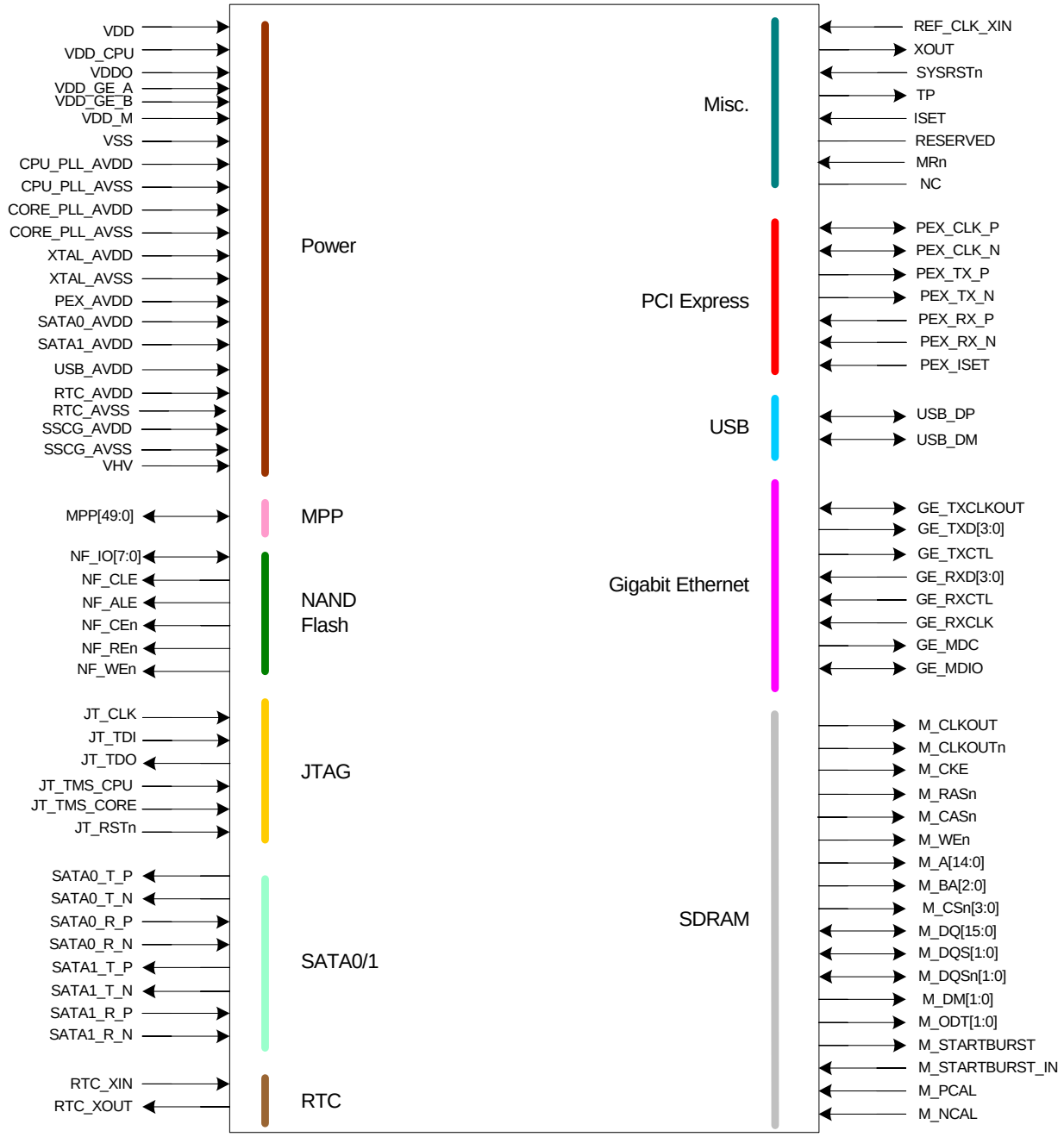
Signal Range	A signal name followed by a range enclosed in brackets represents a range of logically related signals. The first number in the range indicates the most significant bit (MSb) and the last number indicates the least significant bit (LSb). Example: DB_Addr[12:0]
Active Low Signals #	An n letter at the end of a signal name indicates that the signal's active state occurs when voltage is low. Example: INTn
State Names	State names are indicated in *italic* font. Example: *linkfail*
Register Naming Conventions	Register field names are indicated by angle brackets. Example: <RegInit> Register field bits are enclosed in brackets. Example: Field [1:0] Register addresses are represented in hexadecimal format. Example: 0x0 Reserved: The contents of the register are reserved for internal use only or for future use. A lowercase <n> in angle brackets in a register indicates that there are multiple registers with this name. Example: Multicast Configuration Register<n>
Reset Values	Reset values have the following meanings: 0 = Bit clear 1 = Bit set
Abbreviations	Kb: kilobit KB: kilobyte Mb: megabit MB: megabyte Gb: gigabit GB: gigabyte
Numbering Conventions	Unless otherwise indicated, all numbers in this document are decimal (base 10). An 0x prefix indicates a hexadecimal number. An 0b prefix indicates a binary number.

1 Pin and Signal Descriptions

This section provides the pin logic diagram for the 88F6281 device and a detailed description of the pin assignments and their functionality.

1.1 Pin Logic

Figure 1: 88F6281 Pin Logic Diagram



NOTE: The GE_TXCLKOUT pin is an input only when used as the MII/MMII Transmit Clock.

For details about MPP configuration options see Section 4.1, Multi-Purpose Pins Functional Summary, on page 51.

1.2 Pin Descriptions

This section details all the pins for the different interfaces providing a functional description of each pin and pin attributes.

Table 1<Default ¬¹ Font> defines the abbreviations and acronyms used in the pin description tables.

Table 1: Pin Functions and Assignments Table Key

Term	Definition
[n]	n - Represents the SERDES pair number
<n>	Represents port number when there are more than one ports
Analog	Analog Driver/Receiver or Power Supply
Calib	Calibration pad type
CML	Common Mode Logic
CMOS	Complementary Metal-Oxide-Semiconductor
DDR	Double Data Rate
GND	Ground Supply
HCSL	High-speed Current Steering Logic
I	Input
I/O	Input/Output
O	Output
o/d	Open Drain pin The pin allows multiple drivers simultaneously (wire-OR connection). A pull-up is required to sustain the inactive value.
Power	VDD Power Supply
SSTL	Stub Series Terminated Logic for 1.8V
t/s	Tri-State pin
XXXn	n - Suffix represents an Active Low Signal

Table 2: Interface Pin Prefix Codes

Interface	Prefix
Misc	N/A
DDR SDRAM	M_
PCI Express	PEX_
SATA	SATA0_ SATA1_
Gigabit Ethernet	GE_
USB 2.0	USB_
JTAG	JT_

Table 2: Interface Pin Prefix Codes (Continued)

Interface	Prefix
RTC	RTC_
NAND Flash	NF_
MPP	N/A
TWSI	TW_
UART	UA0_ UA1_
Audio	AU_
SPI	SPI_
SDIO	SD_
TDM	TDM_
PTP	PTP_

1.2.1 Power Supply Pins

Table 3 provides the voltage levels for the various interface pins. These do not include the analog power supplies for the PLLs or PHYs which are explicitly mentioned in the other pin description tables.

Table 3: Power Pin Assignments

Pin Name	I/O	Pin Type	Description
VDD	I	Power	1.0V Digital core voltage
VDD_CPU	I	Power	1.1V Digital CPU voltage
VDDO	I	Power	3.3V I/O power for MPP[49:36],MPP[19:0] and JTAG pins
VDD_GE_A	I	Power	1.8V or 3.3V I/O supply voltage for RGMII and SMI interfaces 3.3V I/O supply voltage for GMII, MII/MMII, and SMI interfaces
VDD_GE_B	I	Power	I/O power for MPP[35:20] 1.8V or 3.3V I/O supply voltage for RGMII interfaces 3.3V I/O supply voltage for GMII and MII/MMII interfaces
VDD_M	I	Power	1.8V I/O supply voltage for the DDR2 SDRAM interface
VSS	I	GND	VSS
CPU_PLL_AVDD	I	Power	1.8V analog quiet power to CPU PLL **NOTE:** See the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide* for power supply filtering recommendations.
CPU_PLL_AVSS	I	GND	CPU PLL ground
CORE_PLL_AVDD	I	Power	1.8V analog quiet power to Core PLL **NOTE:** See the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide* for power supply filtering recommendations.
CORE_PLL_AVSS	I	GND	Core PLL ground
SSCG_AVDD	I	Power	1.8V quiet power supply to the internal Spread Spectrum Clock Generator
SSCG_AVSS	I	GND	Ground for the internal Spread Spectrum Clock Generator
XTAL_AVDD	I	Power	1.8V analog quiet power to on-chip clock inverter for supporting external crystal, and on-chip current reference for SATA and USB PHYs **NOTE:** See the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide* for power supply filtering recommendations.
XTAL_AVSS	I	GND	Ground for supporting external crystal, and on-chip current reference for SATA and USB PHYs
VHV	I	Power	I/O supply voltage for eFuse: • 2.5V for eFuse burning only • 1.0V for eFuse reading only

Table 3: Power Pin Assignments (Continued)

Pin Name	I/O	Pin Type	Description
PEX_AVDD	I	Power	PCI Express PHY quiet power supply 1.8V **NOTE:** See the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide* for power supply filtering recommendations.
SATA0_AVDD SATA1_AVDD	I	Power	SATA II port0/1 quiet 3.3V power supply **NOTE:** See *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide* for power supply filtering recommendation.
USB_AVDD	I	Power	USB 2.0 PHY quiet 3.3V power supply **NOTE:** See the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide* for power supply filtering recommendation.
RTC_AVDD	I	Power	1.5V (via battery) or 1.8V (via the board) RTC interface voltage
RTC_AVSS	I	GND	RTC ground

1.2.2 Miscellaneous Pin Assignment

The Miscellaneous signal list contains clock and reset, test, and related signals.

Table 4: Miscellaneous Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
REF_CLK_XIN	I	Analog	XTAL_AVDD	Reference clock input from external oscillator or input from external crystal. Used as input to core, CPU, SATA, and USB PLLs.
XOUT	O	Analog	XTAL_AVDD	XTAL_OUT Feedback signal to external crystal. When not used, leave this pin floating.
SYSRSTn	I	CMOS	VDDO	System reset Main reset signal of the device clock. Used to reset all units to their initial state. When in the reset state, most output pins are in Tri-State.
SYSRST_OUTn	O	CMOS	VDDO	Reset request from the device to the board reset logic. This pin is multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 51).
PEX_RST_OUTn	O	CMOS	VDDO	Optional PCI Express Endpoint card reset output This pin is multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 51).
TP	O	Analog		Analog Test Point for SATA, USB, and PCI Express interfaces For internal use. Leave this pin unconnected.
ISET	I	Analog		Current reference for both the USB and SATA PHYs. Terminate this pin with a 6.04 kΩ resistor, pulled down.
MRn	I	CMOS	VDD_GE_A	Active-Low, Manual Reset Input SYSRST_OUTn is asserted low as long as the MRn input signal is asserted low, and for additional 20 ms after MRn (manual reset) de-assertion This pin is internally pulled up.
RESERVED				Reserved for Marvell¬Æ future usage. Leave unconnected externally.
NC				Reserved for Marvell¬Æ future usage. Leave unconnected externally.

1.2.3 DDR SDRAM Interface Pin Assignments

Table 5: DDR SDRAM Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
M_CLKOUT M_CLKOUTn	O	SSTL	VDD_M	SDRAM Differential Clock Pair
M_CKE	O	SSTL	VDD_M	Driven high to enable SDRAM clock. Driven low when setting the SDRAM to Self-refresh mode.
M_RASn	O	SSTL	VDD_M	SDRAM Row Address Select Asserted to indicate an active ROW address driven on the SDRAM address lines.
M_CASn	O	SSTL	VDD_M	SDRAM Column Address Select Asserted to indicate an active column address driven on the SDRAM address lines.
M_WEn	O	SSTL	VDD_M	SDRAM Write Enable Asserted to indicate a write command to the SDRAM.
M_A[14:0]	O	SSTL	VDD_M	SDRAM Address Driven with M_BA[2:0] during RASn and CASn cycles to generate the SDRAM address.
M_BA[2:0]	O	SSTL	VDD_M	Driven during M_RASn and M_CASn cycles to select one of the eight SDRAM virtual banks. **NOTE:** If an SDRAM device does not support the BA[2] pin, leave the M_BA[2] unconnected.
M_CSn[3:0]	O	SSTL	VDD_M	SDRAM Chip Selects Asserted to select a specific SDRAM Physical bank.
M_DQ[15:0]	t/s I/O	SSTL	VDD_M	SDRAM Data Bus Driven during write. Driven by SDRAM during reads.
M_DQS[1:0], M_DQSn[1:0]	t/s I/O	SSTL	VDD_M	SDRAM Data Strobe Driven by the 88F6281 during write. Driven by SDRAM during reads.
M_DM[1:0]	O	SSTL	VDD_M	SDRAM Data Mask Asserted by the 88F6281 to select the specific byte out of the 16-bit data to be written to the SDRAM.
M_ODT[1:0]	O	SSTL	VDD_M	SDRAM On Die Termination control Driven high to connect the SDRAM on die termination. Driven low to disconnect the SDRAM's termination. **NOTE:** For the recommended setting, refer to the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide*.

Table 5: DDR SDRAM Interface Pin Assignments (Continued)

Pin Name	I/O	Pin Type	Power Rail	Description
M_STARTBURST	O	SSTL	VDD_M	Start Burst 88F6281 indication of starting a burst read transaction. Asserted with the first M_CASn cycle of SDRAM access. **NOTE:** Must be routed on board to the SDRAM, and back to the 88F6281 as M_STARTBURST_IN. For the recommended length calculation for this routing and termination requirements, see the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide*.
M_START BURST_IN	I	SSTL	VDD_M	Start Burst Input
M_PCAL	I	Calib		SDRAM interface P channel output driver calibration. Connect to VSS through a resistor. The resistor value can vary between 30–70 ohm. **NOTE:** See the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide* for the recommended values of the calibration resistors.
M_NCAL	I	Calib		SDRAM interface N channel output driver calibration. Connect to M_VDD through a resistor. The resistor value can vary between 30–70 ohm. **NOTE:** See the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide* for the recommended values of the calibration resistors.

1.2.4 PCI Express Interface Pin Assignments

Table 6: PCI Express Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
PEX_CLK_P/N	I/O	HCSL	PEX_AVDD	PCI Express Reference Clock 100 MHz, differential This clock can be configured as input or output according to the reset strap (see Table 32, Reset Configuration, on page 67). **NOTE:** For Output mode, 50-ohm, pull-down resistors are required.
PEX_TX_P/N	O	CML	PEX_AVDD	Transmit Lane Differential pair of PCI Express transmit data
PEX_RX_P/N	I	CML	PEX_AVDD	Receive Lane Differential pair of PCI Express receive data
PEX_ISET	I	Analog		Current reference. Pull down to VSS through a 5 kΩ resistor. See the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide* for the recommended resistor value.

1.2.5 SATA Interface Pin Assignments

Table 7: SATA Port Interface Pin Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
SATA0_T_P/N SATA1_T_P/N	O	CML	SATA0/1_AVDD	Transmit Data: Differential analog output of SATA II port0/1
SATA0_R_P/N SATA1_R_P/N	I	CML	SATA0/1_AVDD	Receive Data: Differential analog input of SATA II port0/1
SATA0_PRESENTn SATA1_PRESENTn	O	CMOS	VDDO/ VDD_GE_B	When this signal is asserted there is an active link between the SATA II port and the external device (disk). **NOTE:** These signals are multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 51).
SATA0_ACTn SATA1_ACTn	O	CMOS	VDDO/ VDD_GE_B	When this signal is asserted, there is an active and used link between the SATA II port and the external device (disk). **NOTE:** These signals are multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 51).

1.2.6 Gigabit Ethernet Port Interface Pin Assignments

For additional information about the Gigabit Ethernet port pin functions refer to Section 4.2, Gigabit Ethernet (GbE) Pins Multiplexing on MPP, on page 57.

Table 8: Gigabit Ethernet Port0/1 Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
Port0—Dedicated GbE Pins				
GE_TXCLKOUT	t/s O	CMOS	VDD_GE_A	RGMII Transmit Clock RGMII transmit reference output clock for GE_TXD[3:0] and GE_TXCTL. Provides 125 MHz, 25 MHz or 2.5 MHz clock. Not used in MII/MMII mode.
	I			MII/MMII Transmit Clock MII/MMII transmit reference clock from PHY. Provides the timing reference for the transmission of the MII transmit clock, transmit enable, and GE_TXD[3:0] signals. This clock operates at 2.5 MHz or 25 MHz.
	t/s O			GMII Transmit Clock Provides the timing reference for the transfer of the transmit enable, transmit error and transmit data signals. This clock operates at 125 MHz.
GE_TXD[3:0]	t/s O	CMOS	VDD_GE_A	RGMII Transmit Data Contains the transmit data nibble outputs that run at double data rate with bits [3:0] driven on the rising edge of GE_TXCLKOUT and bits [7:4] driven on the falling edge.
				MII/MMII Transmit Data Contains the transmit data nibble outputs that are synchronous to the transmit clock input.
				GMII Transmit Data Contains the transmit data nibble outputs.
GE_TXCTL	t/s O	CMOS	VDD_GE_A	RGMII Transmit Control Transmit control synchronous to the GE_TXCLKOUT output rising/falling edge. GE_TXEN is driven on the rising edge of GE_TXCLKOUT. A logical derivative of transmit enable and transmit error is driven on the falling edge of GE_TXCLKOUT.
				MII/MMII Transmit Enable Indicates that the packet is being transmitted to the PHY. It Is synchronous to transmit clock.
				GMII Transmit Enable Indicates that the packet is being transmitted to the PHY. It Is synchronous to GE_TXCLKOUT.

Table 8: Gigabit Ethernet Port0/1 Interface Pin Assignments (Continued)

Pin Name	I/O	Pin Type	Power Rail	Description
GE_RXD[3:0]	I	CMOS	VDD_GE_A	RGMII Receive Data Contains the receive data nibble inputs that are synchronous to GE_RXCLK input rising/falling edge.
				MII/MMII Receive Data Contains the receive data nibble inputs that are synchronous to GE_RXCLK input.
				GMII Receive Data Contains the receive data nibble inputs.
GE_RXCTL	I	CMOS	VDD_GE_A	RGMII Receive Control GE_RXCTL is presented on the rising edge of GE_RXCLK. A logical derivative of receive data valid and receive data error is presented on the falling edge of RXCLK.
				MII/MMII Receive Data Valid
				GMII Receive Data Valid.
GE_RXCLK	I	CMOS	VDD_GE_A	RGMII Receive Clock The receive clock provides a 125 MHz, 25 MHz, or 2.5 MHz reference clock derived from the received data stream.
				MII/MMII Receive Clock Provides the timing reference for the reception of the receive data valid, receive error, and GE_RXD[3:0] signals. This clock operates at 2.5 MHz or 25 MHz.
				GMII Receive Clock Provides the timing reference for the reception of the GE_RXDV, receive error and receive data signals. This clock operates at 125 MHz
Port1—Multiplexed GbE Pins				
MPP[23:20]/ GE1[3:0]	t/s O	CMOS	VDD_GE_B	RGMII Transmit Data Contains the transmit data nibble outputs that run at double data rate with bits [3:0] presented on the rising edge of GE_TXCLKOUT and bits [7:4] presented on the falling edge.
				MII/MMII Transmit Data Contains the transmit data nibble outputs that are synchronous to the transmit clock input.
				GMII Transmit Data Contains the transmit data nibble outputs.

Table 8: Gigabit Ethernet Port0/1 Interface Pin Assignments (Continued)

Pin Name	I/O	Pin Type	Power Rail	Description
MPP[27:24]/ GE1[7:4]	I	CMOS	VDD_GE_B	RGMII Receive Data Contains the receive data nibble inputs that are synchronous to GE_RXCLK input rising/falling edge.
				MII/MMII Receive Data Contains the receive data nibble inputs that are synchronous to GE_RXCLK input.
				GMII Receive Data Contains the receive data nibble inputs.
MPP[28]/GE1[8]	I	CMOS	VDD_GE_B	MII/MMII Collision Detect Indicates a collision has been detected on the wire. This input is ignored in full-duplex mode. Collision detect is not synchronous to any clock.
				GMII Collision Detect
MPP[29]/GE1[9]	I	CMOS	VDD_GE_B	MII/MMII Transmit Clock MII/MMII transmit reference clock from PHY. Provides the timing reference for the transmission of the MII transmit clock, transmit enable, and GE_TXD[3:0] signals. This clock operates at 2.5 MHz or 25 MHz.
	t/s O			GMII Transmit Clock Provides the timing reference for the transfer of the transmit enable, transmit error and transmit data signals. This clock operates at 125 MHz.
MPP[30]/GE1[10]	I	CMOS	VDD_GE_B	RGMII Receive Control GE_RXCTL is presented on the rising edge of GE_RXCLK. A logical derivative of receive data valid and receive data error is presented on the falling edge of RXCLK.
				MII/MMII Receive Data Valid
				GMII Receive Error
MPP[31]/GE1[11]	I	CMOS	VDD_GE_B	RGMII Receive Clock The receive clock provides a 125 MHz, 25 MHz, or 2.5 MHz reference clock derived from the received data stream.
				MII/MMII Receive Clock Provides the timing reference for the reception of the receive data valid, receive error, and GE_RXD[3:0] signals. This clock operates at 2.5 MHz or 25 MHz.

Table 8: Gigabit Ethernet Port0/1 Interface Pin Assignments (Continued)

Pin Name	I/O	Pin Type	Power Rail	Description
MPP[32]/GE1[12]	I/O	CMOS	VDD_GE_B	RGMII Transmit Clock RGMII transmit reference output clock for GE_TXD[3:0] and GE_TXCTL Provides 125 MHz, 25 MHz or 2.5 MHz clock. Not used in MII/MMII mode.
				MII/MMII Carrier Sense Indicates that the receive medium is non-idle. In half-duplex mode, GE_CRS is also asserted during transmission. Carrier sense is not synchronous to any clock.
				GMII Carrier Sense
MPP[33]/GE1[13]	t/s O	CMOS	VDD_GE_B	RGMII Transmit Control Transmit control synchronous to the GE_TXCLKOUT output rising/falling edge. GE_TXEN is presented on the rising edge of GE_TXCLKOUT. A logical derivative of transmit enable transmit error is presented on the falling edge of GE_TXCLKOUT.
				MII/MMII Transmit Error It is synchronous to transmit clock. **NOTE:** Multiplexed on MPP.
				GMII Transmit Error It Is synchronous to GE_TXCLKOUT. **NOTE:** Multiplexed on MPP.
MPP[34]/GE1[14]	O	CMOS	VDD_GE_B	MII/MMII Transmit Enable Indicates that the packet is being transmitted to the PHY. It Is synchronous to transmit clock.
MPP[35]/GE1[15]	I	CMOS	VDD_GE_B	MII/MMII Receive Error Indicates that an error symbol, a false carrier, or a carrier extension symbol is detected on the cable. It is synchronous to GE_RXCLK input. **NOTE:** Multiplexed on MPP.

1.2.7 Serial Management Interface (SMI) Interface Pin Assignments

Table 9: Serial Management Interface (SMI) Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
GE_MDC	t/s O	CMOS/	VDD_GE_A	Management Data Clock MDC is derived from TCLK divided by 128. Provides the timing reference for the transfer of the MDIO signal.
GE_MDIO	t/s I/O	CMOS	VDD_GE_A	Management Data In/Out Used to transfer control and status information between PHY devices and the GbE controller. **NOTE:** An external pullup is required.

1.2.8 USB 2.0 Interface Pin Assignments

Table 10: USB 2.0 Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
USB_DP USB_DM	I/O	CML	USB_AVDD	USB 2.0 Data Differential Pair

1.2.9 JTAG Interface Pin Assignment

Table 11: JTAG Pin Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
JT_CLK	I	CMOS	VDDO	JTAG Clock Clock input for the JTAG controller. **NOTE:** This pin is internally pulled down to 0.
JT_RSTn	I	CMOS	VDDO	JTAG Reset When asserted, resets the JTAG controller. **NOTE:** This pin is internally pulled down to 0.[1]
JT_TMS_CPU	I	CMOS	VDDO	CPU JTAG Mode Select Controls CPU JTAG controller state. Sampled with the rising edge of JT_CLK. **NOTE:** This pin is internally pulled up to 1.
JT_TMS_CORE	I	CMOS	VDDO	Core JTAG Mode Select Controls the Core JTAG controller state. Sampled with the rising edge of JT_CLK. **NOTE:** This pin is internally pulled up to 1.
JT_TDO	O	CMOS	VDDO	JTAG Data Out Driven on the falling edge of JT_CLK.
JT_TDI	I	CMOS	VDDO	JTAG Data In JTAG serial data input. Sampled with the JT_CLK rising edge. **NOTE:** This pin is internally pulled up to 1.

1. If this pull-down conflicts with other devices, the JTAG tool must not use this signal. This signal is not mandatory for the JTAG interface, since the TAP (Test Access Port) can be reset by driving the JT_TMS signal HIGH for 5 JT_CLK cycles.

1.2.10 Real Time Clock (RTC) Interface Pin Assignments

Table 12: RTC Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
RTC_XIN	I	Analog	RTC_AVDD	RTC Crystal Clock Input
RTC_XOUT	O	Analog	RTC_AVDD	RTC Crystal Clock Feedback

1.2.11 NAND Flash Interface Pin Assignment

Table 13: NAND Flash Interface Pin Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
NF_IO[7:0]	I/O	CMOS	VDDO	Data Input/Output Used to output command, address and data, and to input data during read operations. **NOTE:** All of the NF_IO pins are multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 51)
NF_CLE	O	CMOS	VDDO	Command Latch Enable Controls the activating path for commands sent to the command register.
NF_ALE	O	CMOS	VDDO	Address Latch Enable Controls the activating path for the address to the internal address registers.
NF_CEn	O	CMOS	VDDO	Chip Enable Controls the device selection.
NF_REn	O	CMOS	VDDO	Read Enable Controls the serial data-in.
NF_WEn	O	CMOS	VDDO	Write Enable Controls writes to the NF_IO[7:0] ports.

1.2.12 MPP Interface Pin Assignment

Table 14: MPP Interface Pin Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
MPP[19:0]	t/s I/O	CMOS	VDDO	Multi Purpose Pin Various functionalities
MPP[35:20]	t/s I/O	CMOS	VDD_GE_B	Multi Purpose Pin Various functionalities
MPP[49:36]	t/s I/O	CMOS	VDDO	Multi Purpose Pin Various functionalities

Note

The various functionalities of the MPP pins are detailed in Section 4, Pin Multiplexing, on page 51.

1.2.13 Two-Wire Serial Interface (TWSI) Interface

Note All of the TWSI signals are multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 51).

Table 15: Two-Wire Serial Interface (TWSI) Interface Pin Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
TW_SDA	o/d I/O	CMOS	VDDO	TWSI Port Serial Data Address or write data driven by the TWSI master or read response data driven by the TWSI slave. **NOTE:** Requires a pull-up resistor to VDDO.
TW_SCK	o/d I/O	CMOS	VDDO	TWSI Port Serial Clock Serves as output when acting as an TWSI master. Serves as input when acting as an TWSI slave. **NOTE:** Requires a pull-up resistor to VDDO.

1.2.14 UART Interface

Note

All of the UART signals are multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 51).

Table 16: UART Port 0/1 Interface Pin Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
UA0/1_RXD	I	CMOS	VDDO	UART Port 0/1 RX Data
UA0/1_TXD	O	CMOS	VDDO	UART Port 0/1 TX Data
UA0/1_CTS	I	CMOS	VDDO	Clear to Send
UA0/1_RTS	O	CMOS	VDDO	Request to Send

1.2.15 Audio (S/PDIF / I²S) Interface

Note

- All of the Audio signals are multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 51).
- If the Audio interface is not used, leave all of the signals unconnected.
- The Audio signals are powered on VDDO or on VDD_GE_B, based on the pin multiplexing option.

Table 17: Audio (S/PDIF / I²S) Interface Signal Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
AU_SPDIFI	I	CMOS	VDDO/ VDD_GE_B	S/PDIF In
AU_SPDIFO	O	CMOS	VDDO/ VDD_GE_B	S/PDIF Out
AU_ SPDFRMCLK	O	CMOS	VDDO/ VDD_GE_B	S/PDIF Recovered Master Clock (256 x F_S)[1] For the frequency of this clock, see the Audio External Reference Clock section of Table 45, Reference Clock AC Timing Specifications, on page 86.
AU_I2SBCLK	O	CMOS	VDDO/ VDD_GE_B	I²S Bit Clock (64 x F_S)
AU_I2SDO	O	CMOS	VDDO/ VDD_GE_B	Transmitter Data Out
AU_I2SLRCLK	O	CMOS	VDDO/ VDD_GE_B	I²S Left/Right Clock (1 x F_S)
AU_I2SMCLK	O	CMOS	VDDO/ VDD_GE_B	I²S Master Clock (256 x F_S)
AU_I2SDI	I	CMOS	VDDO/ VDD_GE_B	I²S Receiver Data In
AU_EXTCLK	I	CMOS	VDDO/ VDD_GE_B	External Audio Clock For the frequency of this clock, see the Audio External Reference Clock section of Table 45, Reference Clock AC Timing Specifications, on page 86.

1. F_S is the audio sample rate.

1.2.16 Serial Peripheral Interface (SPI) Interface

Note

All of the SPI signals are multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 51).

Table 18: Serial Peripheral Interface (SPI) Interface Signal Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
SPI_MOSI[1]	O	CMOS	VDDO	SPI Data Output Data is output from the master and input to the slave.
SPI_MISO[2]	I	CMOS	VDDO	SPI Data Input Data is input to the master and output from the slave.
SPI_SCK	O	CMOS	VDDO	SPI Clock
SPI_CSn	O	CMOS	VDDO	SPI Chip Select **NOTE:** This pin requires an external pull up.

1. MOSI = Master Out Slave In.
2. MISO = Master In Slave Out.

1.2.17 Secure Digital Input/Output (SDIO) Interface

Note All of the SDIO signals are multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 51).

Table 19: Secure Digital Input/Output (SDIO) Interface Signal Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
SD_CLK	O	CMOS	VDDO	SDIO Clock
SD_CMD	I/O	CMOS	VDDO	SDIO Command Used to transfer a command serially from the SDIO host to the SDIO device. Used to transfer a command response serially from the SDIO device to the SDIO host. **NOTE:** This pin requires a pull up on board.
SD_D[3:0]	I/O	CMOS	VDDO	SDIO Data Input/Output Used to transfer data from the SDIO host to the SDIO device or vice versa. **NOTE:** These pins require a pull up on board.

1.2.18 Time Division Multiplexing (TDM) Interface

Note

- All of the TDM signals are multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 51).
- The TDM signals are powered on VDDO or on VDD_GE_B, based on the pin multiplexing option (see Section 4, Pin Multiplexing, on page 51).

Table 20: Time Division Multiplexing (TDM) Interface Signal Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
TDM_CH0_TX_QL	O	CMOS	VDDO/ VDD_GE_B	TDM Channel0 Transmit Qualifier
TDM_CH2_TX_QL	O	CMOS	VDDO/ VDD_GE_B	TDM Channel2 Transmit Qualifier
TDM_CH0_RX_QL	O	CMOS	VDDO/ VDD_GE_B	TDM Channel0 Receive Qualifier
TDM_CH2_RX_QL	O	CMOS	VDDO/ VDD_GE_B	TDM Channel2 Receive Qualifier
TDM_CODEC_INTn	I	CMOS	VDDO/ VDD_GE_B	Interrupt Signal FROM the SLIC/codec
TDM_CODEC_RSTn	O	CMOS	VDDO/ VDD_GE_B	SLIC/codec Reset Signal
TDM_PCLK	I/O	CMOS	VDDO/ VDD_GE_B	PCM Audio Bit Clock
TDM_FS	I/O	CMOS	VDDO/ VDD_GE_B	TDM Frame Sync Signal
TDM_DRX	I	CMOS	VDDO/ VDD_GE_B	PCM Audio Input Data (for recording)
TDM_DTX	O	CMOS	VDDO/ VDD_GE_B	PCM Audio Output Data (for playback)
TDM_SPI_CS[1:0]	O	CMOS	VDDO/ VDD_GE_B	Active low SPI chip selects driven by the host to the codec for register access. Always asserted for eight SCLK cycles at a time. Only Byte-by-Byte mode codec register read/write is supported.
TDM_SPI_SCK	O	CMOS	VDDO/ VDD_GE_B	Serial SPI clock from the host to the codec for register access. This is an RTO (return to one) clock. It toggles for eight cycles at a time (for 1 byte transfer) during codec register access, then it returns to high. The host drives write data on TDM_SPI_MOSI on the negative edge of TDM_SPI_SCK, and captures read data from the codec on the positive edge of TDM_SPI_SCK.

Table 20: Time Division Multiplexing (TDM) Interface Signal Assignment (Continued)

Pin Name	I/O	Pin Type	Power Rail	Description
TDM_SPI_MOSI	O	CMOS	VDDO/ VDD_GE_B	Serial SPI data from the host to the codec for register access. When TDM_SPI_CS is asserted low, the data is driven from the host on the negative edge of TDM_SPI_SCK. It is always driven for eight TDM_SPI_SCK cycles at a time. In a byte, the data can be driven MSB or LSB first.
TDM_SPI_MISO	I	CMOS	VDDO/ VDD_GE_B	Serial SPI read data from the CODEC to the host for register access. When TDM_SPI_CS is asserted low, this data is driven from CODEC on negative edge of TDM_SPI_SCK. It is always driven for eight TDM_SPI_SCK cycles at a time. The CODEC drives data on this line only for a read operation, when it gets command and address in previous bytes from the host on TDM_SPI_MOSI In a byte, the data can be driven MSB or LSB first.

1.2.19 Transport Stream (TS) Interface

Note

- All of the TS signals are multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 51).
- The TS signals are powered on VDDO or on VDD_GE_B based on the pin multiplexing option (see Section 4, Pin Multiplexing).

Table 21: Transport Stream (TS) Interface Signal Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
TSMP[0]	I	CMOS	VDDO/ VDD_GE_B	EXT_CLK External clock that can be used to drive the TS0_CLK and TS1_CLK
TSMP[1]	I/O	CMOS	VDDO/ VDD_GE_B	TS0_CLK Port0 TS clock. • If TS0_VAL is used, the clock may be continuous. • If TS0_VAL is not used, the clock may toggle only when valid data is available on TS0_DATA.
TSMP[2]	I/O	CMOS	VDDO/ VDD_GE_B	TS0_SYNC Port0 Sync/Frame Start Indicator or Packet Clock. The TS0_SYNC in parallel mode is a pulse that is active during the first (Sync) byte of the TS packet. In serial mode, the TS0_SYNC pulse may be active for the entire byte or only for the first bit. The polarity is programmable to be either active high or active low.
TSMP[3]	I/O	CMOS	VDDO/ VDD_GE_B	TS0_VAL Port0 Valid Data Indicator When this signal is used and is valid, it indicates that valid data is present on TS0_DATA. TS0_VAL is active during the TS frame packet data and inactive when there is no TS synchronization. In output mode, the polarity of TS0_VAL is programmable to be either active high or active low.
TSMP[4]	I/O	CMOS	VDDO/ VDD_GE_B	TS0_ERR Port0 Uncorrectable Packet Error When this signal is used, an error indicates that the packet contains an uncorrectable error, and therefore should not be used. In output mode, the TS0_ERR is active during the entire TS frame.
TSMP[5]	I/O	CMOS	VDDO/ VDD_GE_B	TS0_DATA[0] Port0 TS Data bit 0 in both parallel and serial modes. In Serial mode TS0_DATA[0] is used as data input or output.
TSMP[6]	I/O	CMOS	VDDO/ VDD_GE_B	• Parallel Mode: TS0_DATA[1]: Port0 TS Data bit 1 • Serial Mode: TS1_CLK: Port1 TS clock. - If TS1_VAL is used, the clock may be continuous. - If TS1_VAL is not used, the clock may toggle only when valid data is available on TS1_DATA

Table 21: Transport Stream (TS) Interface Signal Assignment (Continued)

Pin Name	I/O	Pin Type	Power Rail	Description
TSMP[7]	I/O	CMOS	VDDO/ VDD_GE_B	• Parallel Mode: TS0_DATA[2]: Port0 TS Data bit 2 • Serial Mode: TS1_SYNC: Port1 Sync/Frame Start Indicator or Packet Clock. The TS1_SYNC pulse may be active for the entire byte or only for the first bit. The polarity is programmable to be either active high or active low
TSMP[8]	I/O	CMOS	VDDO/ VDD_GE_B	• Parallel Mode: TS0_DATA[3]: Port0 TS Data bit 3 • Serial Mode: TS1_VAL: Port1Valid Data Indicator When this signal is used and is valid, it indicates that valid data is present on TS1_DATA[0]. TS1_VAL is active during the TS frame packet data and inactive when there is no TS synchronization. In output mode, the polarity of TS1_VAL is programmable to be either active high or active low.
TSMP[9]	I/O	CMOS	VDDO/ VDD_GE_B	• Parallel Mode: TS0_DATA[4]: Port0 TS Data bit 4 • Serial Mode: TS1_ERR: Port1 Uncorrectable Packet Error When this signal is used, an error indicates that the packet contains an uncorrectable error, and, therefore, should not be used. In output mode the TS1_ERR is active during the entire TS frame.
TSMP[10]	I/O	CMOS	VDDO/ VDD_GE_B	• Parallel Mode: TS0_DATA[5]: Port0 TS Data bit 5 • Serial Mode: TS1_DATA[0]: Port1 TS Data bit 0, used as data input or output.
TSMP[11]	I/O	CMOS	VDDO/ VDD_GE_B	TS0_DATA[6] Port0 TS Data bit 6 This pin is only valid in Parallel mode.
TSMP[12]	I/O	CMOS	VDDO/ VDD_GE_B	TS0_DATA[7] Port0 TS Data bit 7 This pin is only valid in Parallel mode.

1.2.20 Precise Timing Protocol (PTP) Interface

Note

All of the PTP signals are multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 51).

Table 22: Precise Timing Protocol (PTP) Interface Signal Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
PTP_CLK	I	CMOS	VDDO	PTP Clock
PTP_EVENT_REQ	I	CMOS	VDDO	Trigger generation to the PTP core.
PTP_TRIG_GEN	O	CMOS	VDDO	Trigger generated by the PTP core.

1.3 Internal Pull-up and Pull-down Pins

Some pins of the device package are connected to internal pull-up and pull-down resistors. When these pins are Not Connected (NC) on the system board, these resistors set the default value for input and sample at reset configuration pins.

The internal pull-up and pull-down resistor value is 50 kΩ. An external resistor with a lower value can override this internal resistor.

Table 23: Internal Pull-up and Pull-down Pins

Pin Name	Pin Number	Pull up/Pull down
GE_TXD[0]	H02	Pull down
GE_TXD[1]	H01	Pull down
GE_TXD[2]	H03	Pull up
GE_TXD[3]	H04	Pull up
GE_TXCTL	J04	Pull down
GE_MDC	L03	Pull up
JT_TMS_CORE	T14	Pull up
JT_RSTn	T15	Pull down
JT_TDI	R14	Pull up
JT_TMS_CPU	V15	Pull up
NF_ALE	R10	Pull up
NF_REn	U11	Pull down
NF_CLE	R11	Pull down
NF_CEn	V11	Pull up
NF_WEn	V12	Pull up
MRn	F04	Pull up
MPP[1]	V08	Pull down
MPP[2]	V07	Pull down
MPP[3]	V09	Pull down
MPP[4]	T09	Pull up
MPP[5]	T10	Pull up
MPP[7]	R06	Pull up
MPP[10]	R07	Pull down
MPP[11]	T07	Pull up
MPP[12]	U12	Pull down
MPP[14]	V13	Pull up
MPP[18]	V10	Pull up
MPP[19]	U10	Pull up
MPP[33]	N03	Pull down

2 Unused Interface Strapping

Table 24 lists the signal strapping to be used for systems in which some of the device interfaces are unused (not connected).

Table 24: Unused Interface Strapping

Unused Interface	Strapping
Ethernet SMI	Pull up GE_MDIO.
MPP	Configure any unused MPP pin to GPIO output. Leave the power supply connected. • If the related power supply is VDDO, leave it connected to 3.3V. • If the related power supply is VDD_GE_B, leave it connected to either 3.3V or 1.8V.
USB	Discard the power filter. Leave USB_AVDD connected to 3.3V. All other signals can be left unconnected.
PCI Express	Discard the analog power filters. Leave PEX_AVDD connected to 1.8V. Pull down the PEX_CLK_N signal through a 50 kΩ resistor to GND. Pull up the PEX_CLK_P signal through a 16 kΩ resistor to 1.8V. All other signals can be left unconnected. Configure the PEX_CLK_P and PEX_CLK_N signals as inputs, as indicated in Table 32, Reset Configuration, on page 67.
SATA	Discard the analog power filters. SATA0_AVDD/SATA1_AVDD can be left unconnected.
RTC	Connect RTC_AVDD, RTC_AVSS, RTC_XIN, and RTC_XOUT to GND.
SSCG	Discard the power filter. Leave SSCG_AVDD connected to 1.8V.
eFuse	Connect VHV to VDD

3 88F6281 Pin Map and Pin List

The 88F6281 pin list is provided as an Excel file attachment.

To open the attached Excel pin list file, double-click the pin icons below:

88F6281 Pin Map and Pin List.xls

Note

File attachments are only supported by Adobe Reader 6.0 and above.

To download the latest version of free Adobe Reader go to http://www.adobe.com.

4 Pin Multiplexing

4.1 Multi-Purpose Pins Functional Summary

The 88F6281 device contains 50 Multi-Purpose Pins (MPP). Each one can be assigned to a different functionality through the MPP Control register.

- General Purpose pins: MPP[5:0] and MPP[49:7]:
  - GPIO (input/output): MPP[0], MPP[4], MPP[9:8], MPP[11], MPP[17:13], MPP[32:20], and MPP[49:34]
  - GPO (output): MPP[3:1], MPP[5], MPP[7], MPP[10], MPP[12], MPP[19:18], and MPP[33]
- SYSRST_OUTn: Reset request from the device to the board reset logic. This pin is an output. SYSRST_OUTn is the default setting for MPP[6].
- PEX_RST_OUTn: Optional PCI Express Endpoint card reset output.
- MII/MMII/GMII/RGMII interface signals
- SATA0/1_ACTn/SATA0/1_PRESENTn (port 0 and port 1): SATA active and SATA present indications—see the SATA section in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*.
- NF_IO[7:0] (NAND Flash data [7:0])
- SPI interface: SPI_MOSI, SPI_MISO, SPI_SCK, SPI_CSn
- UART interface (port 0 and port 1): Transmit and receive functions: UA0_TXD, UA0_RXD, UA1_TXD, UA1_RXD, and Modem control functions: UA0_RTSn, UA0_CTSn, UA1_RTSn, UA1_CTSn
- SDIO interface: SD_CLK, SD_CMD, SD_D[3:0]
- Audio interface signals: AU_SPDIFI, AU_SPDIFO, AU_SPDIFRMCLK, AU_I2SBCLK, AU_I2SDO, AU_I2SLRCLK, AU_I2SMCLK, AU_I2SDI, AU_EXTCLK
- TS (Transport Stream) interface signals: TSMP[12:0]
- TDM/SPI interface signals: TDM_CH0/2_TX_QL, TDM_CH0/2_RX_QL, TDM_SPI_CS0/1, TDM_SPI_SCK, TDM_SPI_MOSI, TDM_SPI_MISO, TDM_CODEC_INTn, TDM_CODEC_RSTn, TDM_PCLK, TDM_FS, TDM_DRX, TDM_DTX
- PTP signals: PTP_EVENT_REQ, PTP_TRIG_GEN, PTP_CLK
- TWSI signals: TW_SDA, TW_SCK

MPP pins can be assigned to different functionalities through the MPP Control register, as shown in Table 25.

Table 25: MPP Functionality

MPP[19:0]:	MPP[35:20]:	MPP[49:36]:
GPIO	GPIO	GPIO
SATA LEDs	SATA LEDs	Audio
NAND flash	GbE	TDM
TWSI	Audio	TS
UART	TDM	
SPI	TS	
PTP	PTP	
SDIO		

Table 26 lists the functionality of the MPP pins, as determined by the MPP Multiplex register, see the Pins Multiplexing Interface Registers section in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*.

Table 26: MPP Function Summary

Pin name	0x0	0x1	0x2	0x3	0x4	0x5	0xC	0xD
MPP[0]	GPIO[0] (in/out)	NF_IO[2] (in/out)	SPI_SCn (out)	-	-	-	-	-
MPP[1]	GPO[1] (out only)	NF_IO[3] (in/out)	SPI_MOSI (out)	-	-	-	-	-
MPP[2]	GPO[2] (out only)	NF_IO[4] (in/out)	SPI_SCK (out)	-	-	-	-	-
MPP[3]	GPO[3] (out only)	NF_IO[5] (in/out)	SPI_MISO (in)	-	-	-	-	-
MPP[4]	GPIO[4] (in/out)	NF_IO[6] (in/out)	UA0_RXD (in)	-	-	SATA1_ACTn (out)	-	PTP_CLK (in)
MPP[5]	GPO[5] (out only)	NF_IO[7] (in/out)	UA0_TXD (out)	-	PTP_TRIG_GEN (out)	SATA0_ACTn (out)	-	-
MPP[6]	-	SYSRST_OUTn (out)	SPI_MOSI (out)	PTP_TRIG_GEN (out)	-	-	-	-
MPP[7]	GPO[7] (out only)	PEX_RST_OUTn (out)	SPI_SCn (out)	PTP_TRIG_GEN (out)	-	-	-	-
MPP[8]	GPIO[8] (in/out)	TW_SDA (in/out)	UA0_RTS (out)	UA1_RTS (out)	MII0_RXERR (in)	SATA1_PRESENTn (out)	PTP_CLK (in)	MII0_COL (in)
MPP[9]	GPIO[9] (in/out)	TW_SCK (in/out)	UA0_CTS (in)	UA1_CTS (in)	-	SATA0_PRESENTn (out)	PTP_EVENT_REQ (in)	MII0_CRS (in)
MPP[10]	GPO [10] (out only)	-	SPI_SCK (out)	UA0_TXD (out)	-	SATA1_ACTn (out)	PTP_TRIG_GEN (out)	-
MPP[11]	GPIO[11] (in/out)	-	SPI_MISO (in)	UA0_RXD (in)	PTP_EVENT_REQ (in)	SATA0_ACTn (out)	PTP_TRIG_GEN (out)	PTP_clk (in)
MPP[12]	GPO[12] (out only)	SD_CLK (out)	-	-	-	-	-	-
MPP[13]	GPIO[13] (in/out)	SD_CMD (in/out)	-	UA1_TXD (out)	-	-	-	-
MPP[14]	GPIO[14] (in/out)	SD_D[0] (in/out)	-	UA1_RXD (in)	SATA1_PRESENTn (out)	-	-	MII0_COL (in)
MPP[15]	GPIO[15] (in/out)	SD_D[1] (in/out)	UA0_RTS (out)	UA1_TXD (out)	SATA0_ACTn (out)	-	-	-
MPP[16]	GPIO[16] (in/out)	SD_D[2] (in/out)	UA0_CTS (in)	UA1_RXD (in)	SATA1_ACTn (out)	-	-	MII0_CRS (in)
MPP[17]	GPIO[17] (in/out)	SD_D[3] (in/out)	-	-	SATA0_PRESENTn (out)	-	-	-

Table 26: MPP Function Summary (Continued)

Pin name	0x0	0x1	0x2	0x3	0x4	0x5	0xC	0xD
MPP[18]	GPO[18] (out only)	NF_IO[0] (in/out)	-	-	-	-	-	-
MPP[19]	GPO[19] (out only)	NF_IO[1] (in/out)	-	-	-	-	-	-
MPP[20]	GPIO[20] (in/out)	TSMP[0] (in/out)	TDM_CH0_TX_QL (out)	GE1[0]	AU_SPDIFI (in)	SATA1_ACTn (out)	-	-
MPP[21]	GPIO[21] (in/out)	TSMP[1] (in/out)	TDM_CH0_RX_QL (out)	GE1[1]	AU_SPDIFO (out)	SATA0_ACTn (out)	-	-
MPP[22]	GPIO[22] (in/out)	TSMP[2] (in/out)	TDM_CH2_TX_QL (out)	GE1[2]	AU_SPDIFRMCLK(out)	SATA1_PRESENTn (out)	-	-
MPP[23]	GPIO[23] (in/out)	TSMP[3] (in/out)	TDM_CH2_RX_QL (out)	GE1[3]	AU_I2SBCLK (out)	SATA0_PRESENTn (out)	-	-
MPP[24]	GPIO[24] (in/out)	TSMP[4] (in/out)	TDM_SPI_CS0 (out)	GE1[4]	AU_I2SDO (out)	-	-	-
MPP[25]	GPIO[25] (in/out)	TSMP[5] (in/out)	TDM_SPI_SCK (out)	GE1[5]	AU_I2SLRCLK (out)	-	-	-
MPP[26]	GPIO[26] (in/out)	TSMP[6] (in/out)	TDM_SPI_MISO (in)	GE1[6]	AU_I2SMCLK (out)	-	-	-
MPP[27]	GPIO[27] (in/out)	TSMP[7] (in/out)	TDM_SPI_MOSI (out)	GE1[7]	AU_I2SDI (in)	-	-	-
MPP[28]	GPIO[28] (in/out)	TSMP[8] (in/out)	TDM_CODEC_INTn (in)	GE1[8]	AU_EXTCLK (in)	-	-	-
MPP[29]	GPIO[29] (in/out)	TSMP[9] (in/out)	TDM_CODEC_RSTn (out)	GE1[9]	-	-	-	-
MPP[30]	GPIO[30] (in/out)	TSMP[10] (in/out)	TDM_PCLK (in/out)	GE1[10]	-	-	-	-
MPP[31]	GPIO[31] (in/out)	TSMP[11] (in/out)	TDM_FS (in/out)	GE1[11]	-	-	-	-
MPP[32]	GPIO[32] (in/out)	TSMP[12] (in/out)	TDM_DRX (in)	GE1[12]	-	-	-	-
MPP[33]	GPO[33] (out only)	-	TDM_DTX (out)	GE1[13]	-	-	-	-
MPP[34]	GPIO[34] (in/out)	-	TDM_SPI_CS1 (out)	GE1[14]	-	SATA1_ACTn (out)	-	-
MPP[35]	GPIO[35] (in/out)	-	TDM_CH0_TX_QL (out)	GE1[15]	-	SATA0_ACTn (out)	MII0_RXERR (in)	-

Table 26: MPP Function Summary (Continued)

Pin name	0x0	0x1	0x2	0x3	0x4	0x5	0xC	0xD
MPP[36]	GPIO[36] (in/out)	TSMP[0] (in/out)	TDM_SPI_CS1 (out)	-	AU_SPDIFI (in)	-	-	-
MPP[37]	GPIO[37] (in/out)	TSMP[1] (in/out)	TDM_CH2_TX_QL (out)	-	AU_SPDIFO (out)	-	-	-
MPP[38]	GPIO[38] (in/out)	TSMP[2] (in/out)	TDM_CH2_RX_QL (out)	-	AU_SPDIFRMCLK (out)	-	-	-
MPP[39]	GPIO[39] (in/out)	TSMP[3] (in/out)	TDM_SPI_CS0 (out)	-	AU_I2SBCLK (out)	-	-	-
MPP[40]	GPIO[40] (in/out)	TSMP[4] (in/out)	TDM_SPI_SCK (out)	-	AU_I2SDO (out)	-	-	-
MPP[41]	GPIO[41] (in/out)	TSMP[5] (in/out)	TDM_SPI_MISO (in)	-	AU_I2SLRCLK (out)	-	-	-
MPP[42]	GPIO[42] (in/out)	TSMP[6] (in/out)	TDM_SPI_MOSI (out)	-	AU_I2SMCLK (out)	-	-	-
MPP[43]	GPIO[43] (in/out)	TSMP[7] (in/out)	TDM_CODEC_INTn (in)	-	AU_I2SDI (in)	-	-	-
MPP[44]	GPIO[44] (in/out)	TSMP[8] (in/out)	TDM_CODEC_RSTn (out)	-	AU_EXTCLK (in)	-	-	-
MPP[45]	GPIO[45] (in/out)	TSMP[9] (in/out)	TDM_PCLK (in/out)	-	-	-	-	-
MPP[46]	GPIO[46] (in/out)	TSMP[10] (in/out)	TDM_FS (in/out)	-	-	-	-	-
MPP[47]	GPIO[47] (in/out)	TSMP[11] (in/out)	TDM_DRX (in)	-	-	-	-	-
MPP[48]	GPIO[48] (in/out)	TSMP[12] (in/out)	TDM_DTX (out)	-	-	-	-	-
MPP[49]	GPIO[49] (in/out)	-	TDM_CH0_RX_QL (out)	-	-	PTP_CLK (in)	-	-

Note

- For MPPs assigned as NAND flash and SPI flash, wake-up mode after reset depends on Boot mode (see the Boot Device field in Table 32, Reset Configuration, on page 67):
  - When Boot mode is NAND Flash, MPP[5:0] and MPP[19:18] wake up after reset in NAND Flash mode.
  - When Boot mode is SPI Flash, either MPP[3:0] or {MPP[3:1] and MPP[7]} wake up after reset in SPI mode, (according to boot mode configured by reset strap pins).
- Pin MPP[6] wakes up after reset in 0x1 mode (SYSRST_OUTn)
- Pin MPP[7] wakes up after reset:
  - As SPI_CSn, if the boot device—selected according to boot device reset strapping—is 0x2 (boot from SPI flash, SPI_CSn on MPP[7]).
  - As PEX_RST_OUTn, if the boot device—selected according to boot device reset strapping—is any option other than 0x2.
- When TWSI serial ROM initialization is enabled (see TWSI Serial ROM Initialization in Table 32, Reset Configuration, on page 67), MPP[8] and MPP[9] wake up as TWSI data and clock pins, respectively.
- All other MPP interface pins wake up after reset in 0x0 mode (GPIO/GPO) and are default set to Data Output disabled (Tri-State). Therefore, those MPPs that are GPIO are in fact inputs, and those that are GPO are Tri-State.
- The SPI interface can be configured using one of the following sets of MPP pins:
  - MPP[3:0]
  - MPP[11], MPP[10], MPP[7], and MPP[6]
  - MPP[3:1] and MPP[7]
- Do not configure *both* MPP[3] and MPP[11] as SPI_MISO.
- UART0 and UART1 signals are duplicated on a few MPPs. The UART0 or UART1 signals must not be configured to more than one MPP.
- When selecting the MII/MMII interface (MPP[35:20]) and the TDM interface (MPP[49:35]), the TDM signal TDM_CH0_TX_QL and the MII/MMII signal MII1_RXERR are both multiplexed on MPP[35]. However, MPP[35] can only be configured to one of these functions at a time.
- Some of the MPP pins are sampled during SYSRSTn de-assertion to set the device configuration. These pins must be set to the correct value during reset (see Section 6.5, Pins Sample Configuration, on page 66).
- Pins that are left as GPIO and are not connected should be set to output after SYSRSTn de-assertion.

4.2 Gigabit Ethernet (GbE) Pins Multiplexing on MPP

The 88F6281 has 14 dedicated pins for its GbE port. (12 RGMII pins, an MDC pin, and an MDIO pin).

For the 88F6281, additional GbE interface pins are multiplexed on the MPPs, to serve as the following interfaces to an external PHY or switch.

- Two RGMII ports
- One RGMII port and one MMII/MII port
  (either port 0 as RGMII and port 1 as MMII/MII or port 0 as MMII/MII and port 1 as RGMII)
- One GMII port (port 0)

Table 27 summarizes the GbE port pins multiplexing.

Table 27: Ethernet Ports Pins Multiplexing

Pin Name	1xGMII	RGMII0+MII1/ MMII1	2xRGMII	MII0/MMII0+ RGMII1
GE_TXCLKOUT	GMII0_TXCLKOUT (out)	RGMII0_TXCLKOUT (out)	RGMII0_TXCLKOUT (out)	MII0_TXCLK (in)
GE_TXD[3:0]	GMII0_TXD[3:0] (out)	RGMII0_TXD[3:0] (out)	RGMII0_TXD[3:0] (out)	MII0_TXD[3:0] (out)
GE_TXCTL	GMII0_TXEN (out)	RGMII0_TXCTL (out)	RGMII0_TXCTL (out)	MII0_TXEN (out)
GE_RXD[3:0]	GMII0_RXD[3:0] (in)	RGMII0_RXD[3:0] (in)	RGMII0_RXD[3:0] (in)	MII0_RXD[3:0] (in)
GE_RXCTL	GMII0_RXDV (in)	RGMII0_RXCTL (in)	RGMII0_RXCTL (in)	MII0_RXDV (in)
GE_RXCLK	GMII0_RXCLK (in)	RGMII0_RXCLK (in)	RGMII0_RXCLK (in)	MII0_RXCLK (in)
MPP[8] or MPP[35]	NA	NA	NA	MII0_RXERR (in)
MPP[8] or MPP[14]	NA	NA	NA	MII0_COL (in)
MPP[9] or MPP[16]	NA	NA	NA	MII0_CRS (in)
MPP [23:20] / GE1[3:0]	GMII0_TXD[7:4] (out)	MII1_TXD[3:0] (out)	RGMII1_TXD[3:0] (out)	RGMII1_TXD[3:0] (out)
MPP_[27:24] / GE1[7:4]	GMII0_RXD[7:4] (in)	MII1_RXD[3:0] (in)	RGMII1_RXD[3:0] (in)	RGMII1_RXD[3:0] (in)
MPP_28 / GE1[8]	GMII0_COL (in)	MII1_COL (in)	NA	NA
MPP_29 / GE1[9]	GMII0_TXCLK (in)	MII1_TXCLK (in)	NA	NA
MPP_30 / GE1[10]	GMII0_RXERR (in)	MII1_RXDV (in)	RGMII1_RXCTL (in)	RGMII1_RXCTL (in)
MPP_31 / GE1[11]	NA	MII1_RXCLK (in)	RGMII1_RXCLK (in)	RGMII1_RXCLK (in)
MPP_32 / GE1[12]	GMII0_CRS (in)	MII1_CRS (in)	RGMII1_TXCLKOUT (out)	RGMII1_TXCLKOUT (out)
MPP_33 / GE1[13]	GMII0_TXERR (out)	MII1_TXERR (out)	RGMII1_TXCTL (out)	RGMII1_TXCTL (out)

Table 27: Ethernet Ports Pins Multiplexing (Continued)

Pin Name	1xGMII	RGMII0+MII1/ MMII1	2xRGMII	MII0/MMII0+ RGMII1
MPP_34 / GE1[14]	NA	MII1_TXEN (out)	NA	NA
MPP_35 / GE1[15]	NA	MII1_RXERR (in)	NA	NA

Note When using Gigabit Ethernet signals on MPPs, all relevant Gigabit Ethernet signals (except those marked as NA) must be implemented. For example, if using MII, and the chosen PHY does not have an MII_RXERR out signal, the MII_RX_ERR (in) (MPP[35]) must still be configured accordingly and must have a pull-down resistor.

4.3 TSMP (TS Multiplexing Pins) on MPP

The TS interface can be configured to one of five modes:

- One or two serial in interfaces
- One or two serial out interfaces
- Serial in and serial out interface
- Parallel in interface
- Parallel out interface

In parallel in or serial in mode, all TS signals are inputs.

In parallel out or serial out mode, all TS signals are outputs.

Table 28 summarizes the TS port pins multiplexing.

Table 28: TS Port Pin Multiplexing

Pin Name	Functionality in TS serial modes 2x in/2x out/in+out	Functionality in TS parallel in/out mode
TSMP[0]	EXT_CLK (in)	EXT_CLK (in)
TSMP[1]	TS0_CLK (in/out))	TS0_CLK (in/out))
TSMP[2]	TS0_SYNC(in/out))	TS0_SYNC(in/out))
TSMP[3]	TS0_VAL (in/out))	TS0_VAL (in/out))
TSMP[4]	TS0_ERR (in/out))	TS0_ERR (in/out))
TSMP[5]	TS0_DATA[0] (in/out)	TS0_DATA[0] (in/out)
TSMP[6]	TS1_CLK (in/out))	TS0_DATA[1] (in/out))
TSMP[7]	TS1_SYNC(in/out))	TS0_DATA[2] (in/out))
TSMP[8]	TS1_VAL (in/out))	TS0_DATA[3] (in/out))
TSMP[9]	TS1_ERR (in/out))	TS0_DATA[4] (in/out))
TSMP[10]	TS1_DATA[0] (in/out)	TS0_DATA[5] (in/out))
TSMP[11]	NA	TS0_DATA[6] (in/out))
TSMP[12]	NA	TS0_DATA[7] (in/out))

5 Clocking

Table 29 lists the clocks in the 88F6281.

Table 29: 88F6281Clocks

Clock Type	Description
CPU PLL	• Reference clock: REF_CLK_XIN (25 MHz) • Derivative clocks: - CPU clock - L2 cache clock - DDR Clock (the Mbus-L uses the DDR clock.) **NOTE:** See Table 32, Reset Configuration, on page 67 for CPU, L2 cache and DDR frequency configuration. L2 cache clock frequency must be equal or higher then DDR clock frequency. If the SSCG enable bit in the Sampled at Reset register is set, then the SSCG circuit is applied for the CPU PLL reference clock (refer to the Sampled at Reset register in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*).
Core PLL	• Reference clock: REF_CLK_XIN (25 MHz) • Derivative clocks: - TCLK (core clock, 200 MHz) - SDIO Clock (100 MHz) - Gigabit Ethernet Clock (125 MHz) - TS unit Clock(100/91/83/77MHz) - SPI clock (TCLK/30–TCLK/4 MHz) - SMI clock (TCLK/128 MHz) - TWSI clock (up to TCLK/1600) **NOTE:** See Table 32, Reset Configuration, on page 67 for TCLK frequency configuration. **NOTE:** See the TS Interface Configuration register in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications* for TS clock frequency configuration.
PEX PHY	There are two options for the reference clock configuration, depending on the PCI Express clock 100 MHz differential clock: • The device uses an external source for PCI Express clock. The PEX_CLK_P pin is an input. • The device uses an internal generated clock for PCI Express clock. The PEX_CLK_P pin is an output, driving out the PCI Express differential clock.
USB PHY PLL	• Reference clock: REF_CLK_XIN (25 MHz)

Table 29: 88F6281Clocks (Continued)

Clock Type	Description
SATA PHY PLL	• Reference clock: REF_CLK_XIN (25 MHz) • Derivative clock: SATA Clock (150 MHz)
RTC	• Reference clock: RTC_XIN (32.768 kHz) Used for real time clock functionality, see the Real Time Clock section in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*.
PTP	• Reference clock: PTP_CLK (125 MHz) The PTP_CLK can be used for the following functions: • PTP time stamp clock Two options for reference clock: - PTP_CLK - Gigabit Ethernet Clock (125 MHz) • TS unit clock Two options for reference clock: - PTP_CLK/2 - Core PLL • Audio unit clock Two options for reference clock: - PTP_CLK - REF_CLK_XIN (25 MHz) For clocking configuration registers, see the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*.

The following table lists the supported combinations of the CPU_CLK Frequency select, CPU_CLK to DDR CLK ratio, and to CPU_CLK to CPU L2 clock ratio (see Section 6.5, Pins Sample Configuration, on page 66).

Table 30: Supported Clock Combinations

DDR Clock (MHz)	CPU to DDR Clock Ratio	CPU Clock (MHz)	CPU to L2 Clock Ratio	L2 Clock (MHz)
333 250 200	3:1 4:1 5:1	1000	3:1	333
400 300 267 200	3:1 4:1 4.5:1 6:1	1200	3:1	400
375	4:1	1500	3:1	500

5.1 Spread Spectrum Clock Generator (SSCG)

The SSCG (Spread Spectrum Clock Generator) may be used to generate the spread spectrum clock for the PLL input. See SSCG Disable in Table 32, Reset Configuration, on page 67, for SSCG enable/bypass configuration settings.

The SSCG block can be configured to perform up spread, down spread and center spread.

The modulation frequency is configurable. Typical frequency is 30 kHz.

The spread percentage can also be configured up to 1%.

For additional details, see the SSCG Configuration Register description in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*.

6 System Power Up/Down and Reset Settings

This section provides information about the device power-up/down sequence and configuration at reset.

6.1 Power-Up/Down Sequence Requirements

6.1.1 Power-Up Sequence Requirements

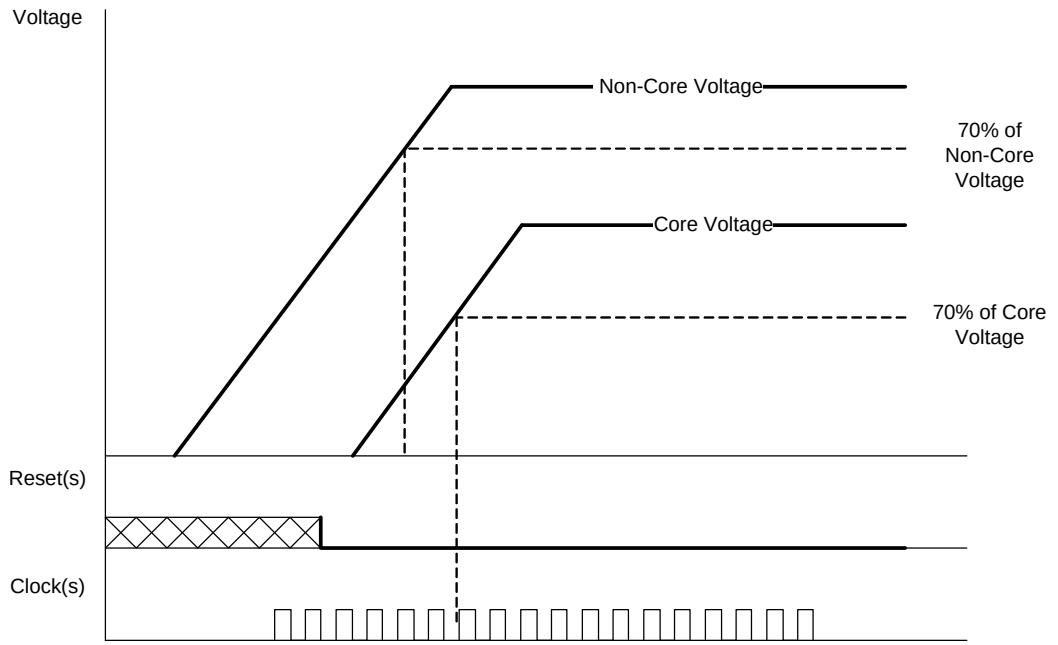
These guidelines must be applied to meet the 88F6281 device power-up requirements:

- The non-core voltages (I/O and Analog) as listed in Table 31 must reach 70% of their voltage level before the core voltages reach 70% of their voltage level.
  The order of the power-up sequence between the non-core voltages is unimportant so long as the non-core voltages power up before the core voltages reach 70% of their voltage level (shown in Figure 2).
  The order of the power-up sequence between the core voltages (VDD and VDD_CPU) is unimportant.
- The reset signal(s) must be asserted before the core voltages reach 70% of their voltage level (shown in Figure 2).
- The reference clock(s) inputs must toggle with their respective voltage levels before the core voltages reach 70% of their voltage level (shown in Figure 2).
- If VHV is set to burning mode (2.5V), which is a higher voltage than the VDD voltage, VDD must be powered before VHV, to prevent the fuse from being accidentally burned.

Table 31: I/O and Core Voltages

Non-Core Voltages		Core Voltages
I/O Voltages	**Analog Power Supplies**	
VDD_GE_A VDD_GE_B VDD_M VDDO	CPU_PLL_AVDD CORE_PLL_AVDD PEX_AVDD RTC_AVDD SATA0_AVDD SATA1_AVDD SSCG_AVDD XTAL_AVDD USB_AVDD	VDD VDD_CPU

Figure 2: Power-Up Sequence Example



Note

- It is the designer's responsibility to verify that the power sequencing requirements of other components are also met.
- Although the non-core voltages can be powered up any time before the core voltages, allow a reasonable time limitation (for example, 100 ms) between the **first** non-core voltage power-up and the **last** core voltage power-up.

6.1.2 Power-Down Sequence Requirements

There are no special requirements for the core supply to go down before non-core power, or for reset assertion when powering down (except for VHV, as described below). However, allow a reasonable time limitation (no more than 100 ms) between the **first** and **last** voltage power-down.

When using the eFuse in Burning mode, VHV must be powered down before VDD.

6.2 Hardware Reset

The device has one reset input pin—SYSRSTn. When asserted, the entire chip is placed in its initial state. Most outputs are placed in high-z, except for the following output pins, that are still active during SYSRSTn assertion:

- M_CLKOUT, M_CLKOUTn
- M_CKE
- M_ODT[1:0]
- M_STARTBURST
- SYSRST_OUTn

Note Reset (SYSRSTn signal) must be active for a minimum length of 5 ms. core power, I/O power, and analog power must be stable (VDD +/- 5%) during that time and onward.

6.2.1 Reset Out Signal

The device has an optional SYSRST_OUTn output signal, multiplexed on an MPP pin, that is used as a reset request from the device to the board reset logic. SYSRST_OUTn is the default option for that MPP pin.

This signal is asserted low for 20 ms, when one of the following **maskable** events occurs:

- Received hot reset indication from the PCI Express link (only relevant when used as a PCI Express endpoint), and bit <PexRstOutEn> is set to 1 in the RSTOUTn Mask Register (see the Reset register section of the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*).
- PCI Express link failure (only relevant when used as a PCI Express endpoint), and bit <PexRstOutEn> is set to 1 in the RSTOUTn Mask Register.
- Watchdog timer expiration and bit <WDRstOutEn> is set to 1 in the RSTOUTn Mask Register.
- Bit <SystemSoftRst> is set to 1 in System Soft Reset Register and bit <SoftRstOutEn> is set to 1 in RSTOUTn Mask Register.

This signal is asserted low for 20 ms, when one of the following **non-maskable** events occurs:

- Power on reset (The device includes a power-on-reset (POR) circuit for VDD power.)
- SYSRST_OUTn is asserted low as long as the MRn input signal is asserted low and for an additional 20 ms after MRn de-assertion. (This is useful for implementations that include a manual reset button.)

6.2.2 Power On Reset (POR)

The SYSRST_OUTn output signal is asserted low for 20 ms, when the power-on-reset (POR) circuit is triggered.

POR is triggered when VDD power up (digital core voltage) reaches a VDD threshold (threshold maximum value 0.8V).

Hysteresis: Another trigger will only occur after the power first drops to 50 mV, and then a power up occurs.

6.2.3 SYSRSTn Duration Counter

When SYSRSTn is asserted low, a SYSRSTn duration counter is running.

- The counter clock is the 25 MHz reference clock.
- It is a 29-bit counter, yielding a maximum counting duration of 2^29/25 MHz (21.4 seconds).
- The host software can read the counter value and reset the counter.
- When the counter reach its maximum value, it remains at this value until counter reset is triggered by software.

Note The SYSRSTn duration counter is useful for implementing manufacturer/factory reset. Upon a long reset assertion, greater than a pre-configured threshold, the host software may reset all settings to the factory default values.

6.3 PCI Express Reset

6.3.1 PCI Express Root Complex Reset

As a Root Complex, the device may generate a Hot Reset to the PCI Express port. Upon CPU setting the PCI Express Control register's <conf_mstr_hot_reset> bit, the PCI Express unit sends a Hot Reset indication to the Endpoint, see the PCI Express Interface section in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*.

6.3.2 PCI Express Endpoint Reset

When a Hot Reset packet is received:

- A maskable interrupt is asserted.
- If the <conf_dis_hot_rst_reg_rst> field in the PCI Express Debug Control register is cleared, the device also resets the PCI Express register file to its default values.
- The device triggers an internal reset, if not masked by the <conf_msk_hot_reset> field in the PCI Express Debug Control register.

Link failure is detected if the PCI Express link was up (LTTSSM L0 state) and dropped back to an inactive state (LTSSM Detect state). When Link failure is detected:

- A maskable interrupt is asserted.
- If the <conf_dis_link_fail_reg_rst> field in the PCI Express Debug Control register is cleared, the device also resets the PCI Express register file to its default values.
- The device triggers an internal reset, if the <conf_msk_link_fail> field is not masked by PCI Express Debug Control register.

Both link fail and hot reset conditions trigger a chip internal reset (if not masked in the PCI Express interface). All the chip logic is reset to the default values, except for sticky registers and the sample on reset logic. In addition, these events can trigger reset to the board, using one of the following:

- PEX_RST_OUTn signal (multiplexed on MPP).
- SYSRST_OUTn output (multiplexed on MPP)—if not masked by the <PexRstOutEn> bit.

The external reset logic (on the board) may assert the SYSRSTn input pin and reset the entire chip.

6.4 Sheeva™ CPU TAP Controller Reset

The Sheeva™ CPU Test Access Port (TAP) controller is reset when JT_RSTn is set and JT_TMS_CPU is active.

6.5 Pins Sample Configuration

The following pins are sampled during SYSRSTn de-assertion:

- Internal pull up/down resistors set the default mode (see Section 1.3, Internal Pull-up and Pull-down Pins, on page 48).
- Higher value, external pull up/down resistors are required to change the default mode of operation.

These signals must remain pulled up or down until SYSRSTn de-assertion (zero hold time in respect to SYSRSTn de-assertion).

Note

- If external logic is used instead of pull-up and pull-down resistors, the logic must drive all of these signals to the desired values during SYSRSTn assertion. To prevent bus contention on these pins, the external logic must float the bus no later than the third TCLK cycle after SYSRSTn de-assertion.
- All reset sampled values are registered in the Sample at Reset register (see the MPP Registers in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*). This is useful for board debug purposes and identification of board and system settings for the host software.
- If a signal is pulled up on the board, it must be pulled to the proper voltage level. Certain reset configuration pins are powered by VDD_GE_A and VDD_GE_B. Those pins have multiple voltage options (see Table 36, Recommended Operating Conditions, on page 77).

In each row of Table 32, the order of the pins is from MSb to LSb (e.g., for in the row CPU_CLK Frequency Select, MPP[2] is the MSB and MPP[10] is the LSB).

Table 32: Reset Configuration

Pin	Configuration Function
MPP[1]	TWSI Serial ROM Initialization
	0 = Disabled 1 = Enabled **NOTE:** Internally pulled down to 0x0. When this pin is set to 0x1, MPP[8] and MPP[9] wake up as TWSI data and clock pins, respectively (see Section 4.1, Multi-Purpose Pins Functional Summary, on page 51).
MPP[2],MPP[5], MPP[19], MPP[10]	CPU_CLK Frequency Select
	0x0–0x6 = Reserved 0x7 = 1000 MHz 0x8 = Reserved 0x9 = 1200 MHz 0xA–0xB = Reserved 0xC = 1500 MHz 0xD–0xF = Reserved **NOTE:** Internally pulled to 0x6. The supported combination for CPU_CLK Frequency select, CPU_CLK to DDR CLK ratio, and CPU_CLK to CPU L2 clock ratio are listed in Table 30, Supported Clock Combinations, on page 61.

Table 32: Reset Configuration (Continued)

Pin	Configuration Function
MPP[33], NF_ALE, NF_REn, NF_CLE	CPU_CLK to DDR CLK Ratio
	0x0–0x3 = Reserved 0x4 = 3:1 0x5 = Reserved 0x6 = 4:1 0x7 = 4.5:1 0x8 = 5:1 0x9 = 6:1 0xA–0xF = Reserved **NOTE:** Internally pulled to 0x4. The supported combination for CPU_CLK Frequency select, CPU_CLK to DDR CLK ratio, and CPU_CLK to CPU L2 clock ratio are listed in Table 30, Supported Clock Combinations, on page 61.
MPP[3], MPP[12], NF_WEn	CPU_CLK to CPU L2 Clock Ratio
	0x0 = Reserved 0x1 = 2:1 0x2 = Reserved 0x3 = 3:1 0x4–0x7 = Reserved **NOTE:** Internally pulled to 0x1. The supported combination for CPU_CLK Frequency select, CPU_CLK to DDR CLK ratio, and CPU_CLK to CPU L2 clock ratio are listed in Table 30, Supported Clock Combinations, on page 61.

Table 32: Reset Configuration (Continued)

Pin	Configuration Function
GE_TXD[2:0]	Boot Device
	0x0 = Reserved 0x1 = Reserved 0x2 = Boot from SPI flash (SPI_CSn on MPP[7]) 0x3 = Reserved 0x4 = Boot from SPI flash (SPI_CSn on MPP[0]) 0x5 = Boot from NAND flash 0x6 = Boot from SATA 0x7 = Boot from the PCI Express port **NOTE:** • Internally pulled to 0x4. • Only SPI signals configured on pins MPP[3:0] or on pins MPP[7] and MPP[3:1] can be used for booting from SPI. SPI signals that are multiplexed on other MPPs can only be used after booting (see Section 4.1, Multi-Purpose Pins Functional Summary, on page 51). • When GE_TXD[2:0] is set to 0x4, MPP[3:0] wake up as SPI signals. • When GE_TXD[2:0] is set to 0x2, MPP[7] and MPP[3:1] wake up as SPI signals. • When GE_TXD[2:0] is set to 0x5, MPP[5:0] and MPP[19:18] wake up as NAND Flash signals. • For a more detailed description of the bootROM, see the BootROM section in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*. • For a more detailed description of the boot from SPI flash or NAND flash, see the SPI Interface and NAND Flash Interface sections in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*. • There is an option to boot from UART when GE_TXD[2:0] = 0x2–0x7. For a more detailed description of the boot from UART, see the BootROM section in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*.
GE_TXD[3]	SSCG Disable
	0 = Enable 1 = Disable **NOTE:** Internally pulled to 0x1.
GE_MDC	PCI Express Clock (100 MHz Differential Clock) Configuration
	0x0 = The device use external source for PCI Express clock. Pins PEX_CLK_P/PEX_CLK_N are inputs. 0x1 = The device uses internal generated clock for PCI Express clock. Pins PEX_CLK_P/PEX_CLK_N pins are outputs, driving out the PCI Express differential clock. **NOTE:** Internally pulled to 0x1.
GE_TXCTL	Used for internal testing
	Must be 0x0 during reset. Either leave the signal floating (internally pulled down to 0x0) or pull the signal to 0x0 during reset.
MPP[7]	Reserved
	Must be 0x1 during reset. Either leave the signal floating (internally pulled up to 0x1) or pull the signal to 0x1 during reset.

Table 32: Reset Configuration (Continued)

Pin	Configuration Function
MPP[18]	Reserved
	NOTE: MUST be externally pulled down to 0x0 during reset.

6.6 Serial ROM Initialization

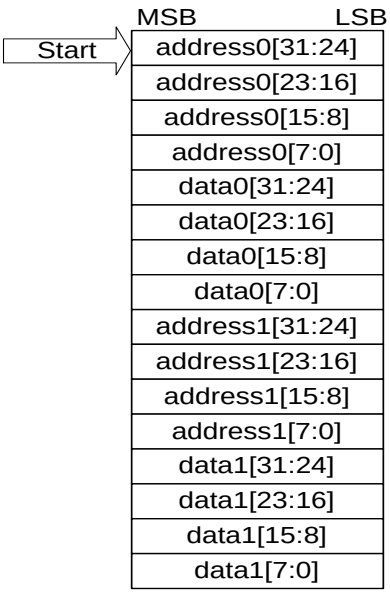
The device supports initialization of ALL of its internal and configuration registers through the TWSI master interface. If serial ROM initialization is enabled, the device TWSI master starts reading initialization data from serial ROM and writes it to the appropriate registers, upon de-assertion of SYSRSTn.

When using Serial ROM Initialization, the MPP[9:8] pins must be configured to as TW_SCK (MPP[9]) and TW_SDA (MPP[8]).

6.6.1 Serial ROM Data Structure

Serial ROM data structure consists of a sequence of 32-bit address and 32-bit data pairs, as shown in Figure 3.

Figure 3: Serial ROM Data Structure



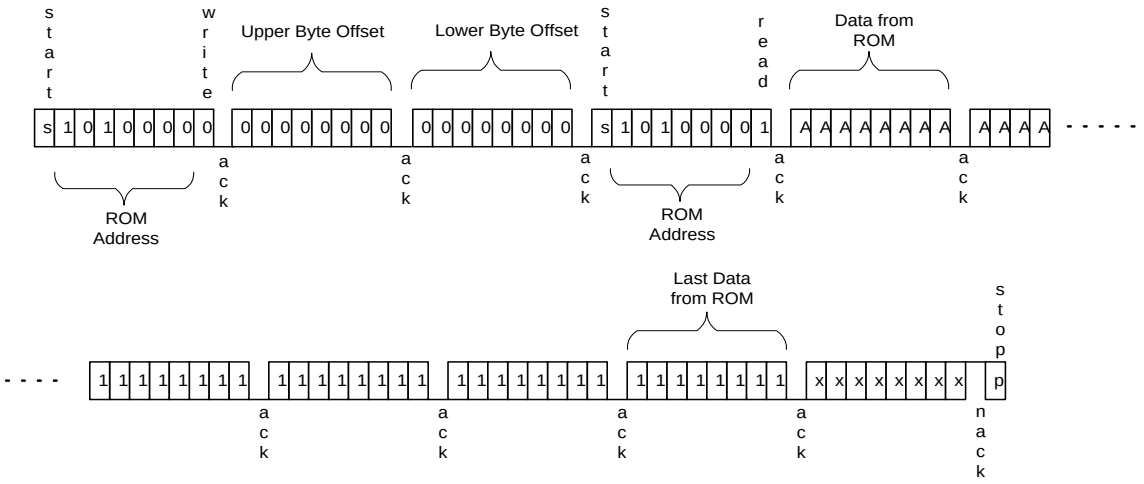
The serial ROM initialization logic reads eight bytes at a time. It performs address decoding on the 32-bit address being read, and based on address decoding result, writes the next four bytes to the required target.

The Serial Initialization Last Data Register contains the expected value of last serial data item (default value is 0xFFFFFFFF). When the device reaches last data, it stops the initialization sequence.

6.6.2 Serial ROM Initialization Operation

On SYSRSTn de-assertion, the device starts the initialization process. It first performs a dummy write access to the serial ROM, with data byte(s) of 0x0, to set the ROM byte offset to 0x0. Then, it performs the sequence of reads, until it reaches last data item, as shown in Figure 4.

Figure 4: Serial ROM Read Example



For a detailed description of TWSI implementation, see the Two-Wire Serial Interface section in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*.

- Initialization data must be programmed in the serial ROM starting at offset 0x0.
- The device assumes 7-bit serial ROM address of ‘b1010000.
- After receiving the last data identifier (default value is 0xFFFFFFFF), the device receives an additional byte of dummy data. It responds with no-ack and then asserts the stop bit.
- The serial EEPROM must contain two address offset bytes (It must not be less than a 256 byte ROM.).

6.7 Boot Sequence

The device requires that SYSRSTn stay asserted for at least 300 µs after power and clocks are stable. The following procedure describes the boot sequence starting with the reset assertion:

1. While SYSRSTn is asserted, the CPU PLL and the core PLL are locked.
2. Upon SYSRSTn de-assertion, the pad drive auto-calibration process starts. It takes 512 TCLK cycles.
3. If Serial ROM initialization is enabled, an initialization sequence is started.
4. If configured to boot from NAND flash (and BootROM is disabled), the device also performs a NAND Flash boot sequence to prepare page 0 in the NAND flash device for read.

Upon completing the above sequence, the internal CPU reset is de-asserted, and the CPU starts executing boot code from the boot device (SPI flash, NAND flash, or internal Boot ROM), according to sample at reset setting, see Table 32, Reset Configuration, on page 67.

For bootROM details, see the BootROM section in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*.

As part of the CPU boot code, the CPU typically performs the following:

- Configures the PCI Express address map.
- Configures the proper SDRAM controller parameters, and then triggers SDRAM initialization (sets <InitEn> bit [0] to 1 in the SDRAM Initialization Control register).
- Sets the <PEXEn> bits in the CPU Control and Status register to wake up the PCI Express link.

7 JTAG Interface

To enable board testing, the device supports a test mode operation through its JTAG boundary scan interface.

The JTAG interface is IEEE 1149.1 standard compliant. It supports mandatory and optional boundary scan instructions.

7.1 TAP Controller

The Test Access Port (TAP) is constructed with a 5-pin interface and a 16-state Finite State Machine (FSM), as defined by IEEE JTAG standard 1149.1.

To place the device in a functional mode, reset the JTAG state machine to disable the JTAG interface.

According to the IEEE 1149.1 standard, the JTAG state machine is not reset when the 88F6281 SYSRSTn is asserted. The JTAG state machine can only be reset by one of the following methods:

- Asserting JT_RSTn.
- Setting JT_TMS_CORE for at least five JT_CLK cycles.

To place the device in one of the boundary scan test mode, the JTAG state machine must be moved to its control states. JT_TMS_CORE and JT_TDI inputs control the state transitions of the JTAG state machine, as specified in the IEEE 1149.1 standard. The JTAG state machine will shift instructions into the Instruction register while in *SHIFT-IR* state and shift data into and from the various data registers when in *SHIFT-DR* state.

7.2 Instruction Register

The Instruction register (IR) is a 4-bit, two-stage register. It contains the command that is shifted in when the TAP FSM is in the *Shift-IR* state. When the TAP FSM is in the *Capture-IR* state, the IR outputs all four bits in parallel.

Table 33 lists the instructions supported by the device.

Table 33: Supported JTAG Instructions

Instruction	Code	Description
HIGHZ	0011	Select the single bit Bypass register between TDI and TDO. Sets the device output pins to high-impedance state.
IDCODE	0010	Selects the Identification register between TDI and TDO. This 32-bit register is used to identify the device.
EXTEST	0000	Selects the Boundary Scan register between TDI and TDO. Outputs the boundary scan register cells to drive the output pins of the device. Inputs the boundary scan register cell to sample the input pin of the device.
SAMPLE/PRELOAD	0001	Selects the Boundary Scan register between TDI and TDO. Samples input pins of the device to input boundary scan register cells. Preloads the output boundary scan register cells with the Boundary Scan register value.
BYPASS	1111	Selects the single bit Bypass register between TDI and TDO. This allows for rapid data movement through an untested device.

7.3 Bypass Register

The Bypass register (BR) is a single bit serial shift register that connects TDI to TDO, when the IR holds the Bypass command, and the TAP FSM is in *Shift-DR* state. Data that is driven on the TDI input pin is shifted out one cycle later on the TDO output pin. The Bypass register is loaded with 0 when the TAP FSM is in the *Capture-DR* state.

7.4 JTAG Scan Chain

The JTAG Scan Chain is a serial shift register used to sample and drive all of the device pins during the JTAG tests. It is a 2-bit per pin shift register in the device, thereby allowing the shift register to sequentially access all of the data pins both for driving and strobing data. For further details, refer to the BSDL Description file for the device.

7.5 ID Register

The ID register is a 32-bit deep serial shift register. The ID register is loaded with vendor and device information when the TAP FSM is in the *Capture-DR* state. The Identification code format of the ID register is shown in Table 34, which describes the various ID Code fields.

Table 34: IDCODE Register Map

Bits	Value	Description
31:28	0x0	Version (4'b0010 for version A0, 4'b0011 for A1, etc.)
27:12	0x6281	Part number
11:1	0x1AB	Manufacturer ID
0	1	Mandatory

8 Electrical Specifications (Preliminary)

Note The numbers specified in this section are PRELIMINARY and SUBJECT TO CHANGE.

8.1 Absolute Maximum Ratings

Table 35: Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
VDD	-0.5	1.2	V	Core voltage
VDD_CPU	-0.5	1.32	V	CPU interface
CPU_PLL_AVDD CORE_PLL_AVDD	-0.5	2.2	V	Analog supply for the internal PLL
SSCG_AVDD	-0.5	2.2	V	Analog supply for: Internal Spread Spectrum Clock Generator
VDD_GE_A VDD_GE_B	-0.5	4.0	V	I/O voltage for: RGMII/GMII/MII/MMII/SMI interface
VDD_M	-0.5	2.2	V	I/O voltage for: SDRAM interface
VDDO	-0.5	4.0	V	I/O voltage for: MPP, TWSI, JTAG, SDIO, I^2S, SPI, TS, and TDM interfaces
VHV	-0.5	3.0	V	I/O voltage for eFuse burning
PEX_AVDD	-0.5	2.2	V	Analog supply for: PCI Express interface
USB_AVDD	-0.5	4.0	V	Analog supply for: USB interface
SATA0_AVDD SATA1_AVDD	-0.5	4.0	V	Analog supply for: SATA interface
XTAL_AVDD	-0.5	2.2	V	Analog supply for internal clock inverter for crystal support and current source for SATA and USB PHYs

Table 35: Absolute Maximum Ratings (Continued)

Parameter	Min	Max	Units	Comments
RTC_AVDD	-0.5	2.2	V	Analog supply for: RTC interface
T_C	-40	125	° C	Case temperature
T_{STG}	-40	125	° C	Storage temperature

Caution

- Exposure to conditions at or beyond the maximum rating may damage the device.
- Operation beyond the recommended operating conditions (Table 36) is neither recommended nor guaranteed.

8.2 Recommended Operating Conditions

Table 36: Recommended Operating Conditions

Parameter	Min	Typ	Max	Units	Comments
VDD	0.95	1.0	1.05	V	Core voltage
VDD_CPU	1.05	1.1	1.15	V	CPU interface
CPU_PLL_AVDD CORE_PLL_AVDD	1.7	1.8	1.9	V	Analog supply for the internal PLL
SSCG_AVDD	1.7	1.8	1.9	V	Analog supply for: Internal Spread Spectrum Clock Generator
VDD_GE_A VDD_GE_B	3.15	3.3	3.45	V	I/O voltage for: RGMII(10/100 RGMII only)/ GMII/MII/MMII/SMI interfaces
	1.7	1.8	1.9	V	I/O voltage for: RGMII/SMI interfaces
VDD_M	1.7	1.8	1.9	V	I/O voltage for: SDRAM interface
VDDO	3.15	3.3	3.45	V	I/O voltage for: MPP, TWSI, JTAG, SDIO, I^2S, SPI, TS, and TDM interfaces
VHV (during eFuse Burning mode)	2.375	2.5	2.625	V	I/O voltage for eFuse burning **NOTE:** If the VHV voltage is higher than VDD voltage (burning mode), VDD must be powered before VHV, to prevent the fuse from being accidentally burned.
VHV (during eFuse Reading mode)	0.95	1.0	1.05	V	I/O voltage for eFuse reading **NOTE:** It is recommended that if only a read operation is required, VHV would be connected to the device VDD power.
PEX_AVDD	1.7	1.8	1.9	V	Analog supply for: PCI Express interface
USB_AVDD	3.15	3.3	3.45	V	Analog supply for: USB interface
SATA0_AVDD SATA1_AVDD	3.15	3.3	3.45	V	Analog supply for: SATA interface

Table 36: Recommended Operating Conditions (Continued)

Parameter	Min	Typ	Max	Units	Comments
XTAL_AVDD	1.7	1.8	1.9	V	Analog supply for: Internal clock inverter for crystal support and current source for SATA and USB PHYs
RTC_AVDD	1.7	1.8	1.9	V	Analog supply for RTC in Regular mode
	1.3	1.5	1.7	V	Analog supply for RTC in Battery Back-up mode
TJ	0		105	° C	Junction Temperature

Caution Operation beyond the recommended operating conditions is neither recommended nor guaranteed.

8.3 Thermal Power Dissipation

Note

Before designing a system, Marvell recommends reading application note *AN-63: Thermal Management for Marvell Technology Products*. This application note presents basic concepts of thermal management for integrated circuits (ICs) and includes guidelines to ensure optimal operating conditions for Marvell Technology's products.

The purpose of the Thermal Power Dissipation table is to support system engineering in thermal design.

Table 37: Thermal Power Dissipation

Interface	Symbol	Test Conditions	Typ	Units
Core (VDD 1.0V)	P_{VDD}	TCLK @ 200 MHz	280	mW
Embedded CPU (VDD_CPU 1.1V)	P_{VDD_CPU}	CPU @ 1000 MHz, L2 @ 333 MHz	790	mW
		CPU @ 1200 MHz, L2 @ 400 MHz	870	mW
		CPU @ 1500 MHz, L2 @ 500 MHz	1050	mW
RGMII 1.8V interface	P_{RGMII}		30	mW
RGMII (10/100 RGMII only) 3.3V interface	P_{RGMII}		50	mW
GMII 3.3V interface	P_{GMII}		50	mW
MII/MMII 3.3V interface	P_{MII}		10	mW
Miscellaneous interfaces (JTAG, TWSI, UART, NAND flash, Audio, SDIO, TDM, TS, and SPI)	P_{MISC}		50	mW
DDR2 SDRAM interface (On-board, 16-bit, 400 MHz)	P_{DDR2}	Four on board devices, 75 ohm ODT termination	250	mW
eFuse during Burning mode **NOTE:** Since the eFuse burn is performed only once, there is no thermal effect after the burn has finished.	P_{FUSE}		50	mW
eFuse during Reading mode	P_{FUSE}		25	mW
PCI Express interface	P_{PEX}		100	mW
USB interface	P_{USB}		120	mW
SATA interface	P_{SATA}	Both SATA ports	410	mW

Notes:

1. The values are for nominal voltage.
2. Power in mW is calculated using the typical recommended VDDIO specification for each power rail.

8.4 Current Consumption

The purpose of the Current Consumption table is to support board power design and power module selection.

Table 38: Current Consumption

Interface	Symbol	Test Conditions	Max	Units
Core (VDD 1.0V)	I_{VDD}	TCLK @ 200 MHz	600	mA
Embedded CPU (VDD_CPU 1.1V)	I_{VDD_CPU}	CPU @ 1000 MHz, L2 @ 333 MHz	1920	mA
		CPU @ 1200 MHz, L2 @ 400 MHz	2010	mA
		CPU @ 1500 MHz, L2 @ 500 MHz	2100	mA
RGMII 1.8V or 3.3V interface	I_{RGMII}		25	mA
GMII 3.3V interface	I_{GMII}		25	mA
MII/MMII 3.3V interface	I_{MII_MMII}		25	mA
Miscellaneous interfaces (JTAG, TWSI, UART, NAND flash, Audio, SDIO, TDM, TS, and SPI)	I_{MISC}		25	mA
DDR2 SDRAM interface (16-bit 400 MHz)	I_{DDR2}	Four on board devices, 75 ohm ODT termination	550	mA
eFuse during Burning mode	I_{FUSE}		20	mA
eFuse during Reading mode	I_{FUSE}		25	mA
PCI Express interface	I_{PEX}		50	mA
USB interface	I_{USB}		40	mA
SATA interface	I_{SATA}	Both SATA ports	130	mA

Notes:

1. Current in mA is calculated using maximum recommended VDDIO specification for each power rail.
2. All output clocks toggling at their specified rate.
3. Maximum drawn current from the power supply.

8.5 DC Electrical Specifications

Note See Section 1.3, Internal Pull-up and Pull-down Pins, on page 48 for internal pullup/pulldown information.

8.5.1 General 3.3V (CMOS) DC Electrical Specifications

The DC electrical specifications in Table 39 are applicable for the following interfaces and signals:

- JTAG
- RGMII (10/100 Mbps)/GMII/MII/MMII
- Secure Digital Input/Output (SDIO)
- S/PDIF / I^2S (Audio)
- Transport Stream (TS)
- NAND flash
- UART
- MPP
- PTP
- SYSRSTn

In the following table, for the JTAG, SDIO, S/PDIF / I^2S, TS, NAND flash, UART, PTP, and MPP interfaces, VDDIO means the VDDO power rail. For the RGMII/GMII/MII/MMII interface, VDDIO means the VDD_GE_A and VDD_GE_B power rails.

Table 39: General 3.3V Interface (CMOS) DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.8	V	-
Input high level	VIH		2.0		VDDIO+0.3	V	-
Output low level	VOL	IOL = 2 mA	-		0.4	V	-
Output high level	VOH	IOH = -2 mA	2.4		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

8.5.2 RGMII, SMI and REF_CLK_XIN 1.8V (CMOS) DC Electrical Specifications

In the following table, for the RGMII interface, VDDIO means the VDD_GE_A power rail.

In the following table, for the REF_CLK_XIN pin, VDDIO means the XTAL_AVDD power rail.

Table 40: RGMII 1.8V Interface (CMOS) DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.35*VDDIO	V	-
Input high level	VIH		0.65*VDDIO		VDDIO+0.3	V	-
Output low level	VOL	IOL = 2 mA	-		0.45	V	-
Output high level	VOH	IOH = -2 mA	VDDIO-0.45		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.

2. This current does not include the current flowing through the pullup/pulldown resistor.

8.5.3 SDRAM DDR2 Interface DC Electrical Specifications

In the following table, VREF is VDD_M/2 and VDDIO means the VDD_M power rail.

Table 41: SDRAM DDR2 Interface DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL	-	-0.3		VREF - 0.125	V	-
Input high level	VIH	-	VREF + 0.125		VDDIO + 0.3	V	-
Output low level	VOL	IOL = 13.4 mA			0.28	V	-
Output high level	VOH	IOH = -13.4 mA	1.42			V	-
Rtt effective impedance value	RTT	See note 2	120	150	180	ohm	1 , 2
			60	75	90	ohm	1 , 2
			40	50	60	ohm	1 , 2
Deviation of VM with respect to VDDQ/2	dVm	See note 3	-6		6	%	3
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	4, 5
Pin capacitance	Cpin	-		5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. See SDRAM functional description section for ODT configuration.
2. Measurement definition for RTT: Apply VREF +/- 0.25 to input pin separately,
   then measure current I(*VREF* +0.25) and I(*VREF* -0.25) respectively.

$$RTT = \frac{0.5}{I_{(VREF+0.25)} - I_{(VREF-0.25)}}$$

3. Measurement definition for VM: Measured voltage (VM) at input pin (midpoint) with no load.

$$dVM = \left(\frac{2 \times Vm}{VDDIO} - 1 \right) \times 100\%$$

4. While I/O is in High-Z.
5. This current does not include the current flowing through the pullup/pulldown resistor.

8.5.4 Two-Wire Serial Interface (TWSI) 3.3V DC Electrical Specifications

In the following table, VDDIO means the VDDO power rail.

Table 42: TWSI Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.5		0.3*VDDIO	V	-
Input high level	VIH		0.7*VDDIO		VDDIO+0.5	V	-
Output low level	VOL	IOL = 3 mA	-		0.4	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.

2. This current does not include the current flowing through the pullup/pulldown resistor.

8.5.5 Serial Peripheral Interface (SPI) 3.3V DC Electrical Specifications

In the following table VDDIO means the VDDO power rail.

Table 43: SPI Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.5		0.3*VDDIO	V	-
Input high level	VIH		0.7*VDDIO		VDDIO+0.5	V	-
Output low level	VOL	IOL = 4 mA	-		0.4	V	-
Output high level	VOH	IOH = -4 mA	VDDIO-0.6		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.

2. This current does not include the current flowing through the pullup/pulldown resistor.

8.5.6 Time Division Multiplexing (TDM) 3.3V DC Electrical Specifications

In the following table VDDIO means the either the VDDO or the VDD_GE_B power rail, depending on which MPP pins are configured for the TDM interface.

Table 44: TDM Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.5		0.3*VDDIO	V	-
Input high level	VIH		0.7*VDDIO		VDDIO+0.5	V	-
Output low level	VOL	IOL = 4 mA	-		0.4	V	-
Output high level	VOH	IOH = -4 mA	VDDIO-0.6		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.

2. This current does not include the current flowing through the pullup/pulldown resistor.

8.6 AC Electrical Specifications

See Section 8.7, Differential Interface Electrical Characteristics, on page 118 for differential interface specifications.

8.6.1 Reference Clock AC Timing Specifications

Table 45: Reference Clock AC Timing Specifications

Description	Symbol	Min	Max	Units	Notes
CPU and Core Reference Clock					
Frequency	$F_{REF\_CLK\_XIN}$	25 - 50 ppm	25 + 50 ppm	MHz	
Clock duty cycle	$DC_{REF\_CLK\_XIN}$	40	60	%	
Slew rate	$SR_{REF\_CLK\_XIN}$	0.7		V/ns	1
Pk-Pk jitter	$JR_{REF\_CLK\_XIN}$		200	ps	
Ethernet Reference Clock					
Frequency in MII/MMII-MAC mode	$F_{GE\_TXCLK\_OUT}$ F_{GE_RXCLK}	2.5 - 100 ppm	50 + 100 ppm	MHz	7
MII/MMII-MAC mode clock duty cycle	$DC_{GE\_TXCLK\_OUT}$ DC_{GE_RXCLK}	35	65	%	7
Slew rate	$SR_{GE\_TXCLK\_OUT}$ SR_{GE_RXCLK}	0.7		V/ns	1, 7
Audio External Reference Clock					
Audio external reference clock	F_{AU_EXTCLK}	256 X F_s		kHz	3
S/PDIF Recovered Master Clock					
S/PDIF recovered master clock	$F_{AU\_SPDFRMCLK}$	256 X F_s		kHz	3
I^2S Reference Clock					
I^2S clock	F_{I2S_BCLK}	64 X F_s		kHz	3
SPI Output Clock					
SPI output clock	F_{SPI_SCK}	TCLK/30	TCLK/4	MHz	2
RTC Reference Clock					
RTC_XIN crystal frequency	F_{RTC_XIN}	32.768		kHz	4
Transport Stream (TS) Output Mode Reference Clock					
TS output clock in parallel mode	F_{TS0_CLK}, F_{TS1_CLK}	9.61	12.5	MHz	5
TS output clock in serial mode	F_{TS0_CLK}, F_{TS1_CLK}	9.61	83	MHz	5
Transport Stream Input Mode Reference Clock					
TS input clock in parallel mode	F_{TS0_CLK}, F_{TS1_CLK}		13.5	MHz	
TS input clock in serial mode	F_{TS0_CLK}, F_{TS1_CLK}		83	MHz	
Transport Stream External Reference Clock					
TS external clock in parallel mode	F_{EXT_CLK}	9.61	12.5	MHz	5
TS external clock in serial mode	F_{EXT_CLK}	9.61	83	MHz	5

Table 45: Reference Clock AC Timing Specifications (Continued)

Description	Symbol	Min	Max	Units	Notes
TDM_SPI Output Clock					
TDM_SPI output clock	$F_{TDM\_SPI\_SCK}$		8.192	MHz	
SMI Master Mode Reference Clock					
SMI output MDC clock	F_{GE_MDC}	TCLK/128		MHz	
TWSI Master Mode Reference Clock					
SCK output clock	F_{TW_SCK}		TCLK/ 1600	kHz	6
PTP Reference Clock					
Frequency	F_{PTP_CLK}	125 - 100 ppm	125 + 100 ppm	MHz	
Clock duty cycle	DC_{PTP_CLK}	40	60	%	
Slew rate	SR_{PTP_CLK}	0.7		V/ns	1
Pk-Pk jitter	JR_{PTP_CLK}		100	ps	

Notes:

1. Slew rate is defined from 20% to 80% of the reference clock signal.
2. For additional information regarding configuring this clock, see the Serial Memory Interface Control Register in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*.
3. F_S is the audio sample rate, which can be configured to 44.1 kHz, 48 kHz, or 96 kHz (see the Audio (I^2S / S/PDIF) Interface section in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications).*
4. The RTC design was optimized for a standard CL = 12.5 pF crystal. No passive components are provided internally. Connect the crystal and the passive network as recommended by the crystal manufacturer.
5. The frequency can be set using the TS Interface Configuration register (see the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*).
6. For the minimum value refer to the Baud Rate Register section of the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications.*
7. The Ethernet Reference Clock parameters refer both to the reference clock for an Ethernet port configured using the dedicated port pins and for an Ethernet port configured using the multiplexed port pins.

8.6.2 SDRAM DDR2 Interface AC Timing

8.6.2.1 SDRAM DDR2 Interface AC Timing Table

Table 46: SDRAM DDR2 Interface AC Timing Table

Description	Symbol	400 MHz @ 1.8V		Units	Notes
		Min	Max		
Clock frequency	fCK	400.0		MHz	-
DQ and DM valid output time before DQS transition	tDOVB	0.40	-	ns	-
DQ and DM valid output time after DQS transition	tDOVA	0.40	-	ns	-
DQ and DM output pulse width	tDIPW	0.35	-	tCK(avg)	-
DQS output high pulse width	tDQSH	0.35	-	tCK(avg)	-
DQS output low pulse width	tDQSL	0.35	-	tCK(avg)	-
DQS falling edge to CLK-CLKn rising edge	tDSS	0.34	-	tCK(avg)	1
DQS falling edge from CLK-CLKn rising edge	tDSH	0.34	-	tCK(avg)	1
DQS latching rising transitions to associated clock edges	tDQSS	-0.11	0.11	tCK(avg)	-
DQS write preamble	tWPRE	0.35	-	tCK(avg)	-
DQS write postamble	tWPST	0.40	-	tCK(avg)	-
Average CLK-CLKn high-level width	tCH(avg)	0.48	0.52	tCK(avg)	1, 2, 3
Average CLK-CLKn low-level width	tCL(avg)	0.48	0.52	tCK(avg)	1, 2, 4
DQ input setup time relative to DQS in transition	tDSI	-0.42	-	ns	-
DQ input hold time relative to DQS in transition	tDHI	0.70	-	ns	-
Address and control output pulse width	tIPW	0.60	-	tCK(avg)	-

Notes:

General comment: All timing values are defined from Vref to Vref, unless otherwise specified.

General comment: All input timing values assume minimum slew rate of 1 V/ns (slew rate defined from Vref +/-125 mV).

General comment: tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window.

General comment: All timing parameters with DQS signal are defined on DQS-DQSn crossing point.

General comment: For Address and Control output timing parameters, refer to the Address Timing table.

General comment: For all signals, the load is CL = 14 pF.

1. This timing value is defined on CLK / CLKn crossing point.
2. Refer to SDRAM DDR2 clock specifications table for more information.
3. tCH(avg) is defined as the average HIGH pulse width, as calculated across any consecutive 200 HIGH pulses.
4. tCL(avg) is defined as the average LOW pulse width, as calculated across any consecutive 200 LOW pulses.

Table 47: SDRAM DDR2 Interface Address Timing Table

Description	Symbol	400 MHz @ 1.8V		Units	Notes
		Min	Max		
Address and Control valid output time before CLK-CLkn rising edge	tAOVB	0.65	-	ns	1, 2
Address and Control valid output time after CLK-CLKn rising edge	tAOVA	0.65	-	ns	1, 2
Address and Control valid output time before CLK-CLkn rising edge	tAOVB	2.95	-	ns	1, 3
Address and Control valid output time after CLK-CLKn rising edge	tAOVA	0.65	-	ns	1, 3

Notes:

General comment: All timing values were measured from vref to vref, unless otherwise specified.

General comment: For all signals, the load is CL = 14 pF.

1. This timing value is defined on CLK / CLKn crossing point.
2. This timing value is defined when Address and Control signals are output on CLK-CLKn falling edge.
   For more information, see register settings.
3. This timing value is defined when Address and Control signals are output on CLK-CLKn falling edge.
   and 2T mode is enabled. For more information, see register settings.
   Except for ODT, CKE and CS signals.

8.6.2.2 SDRAM DDR2 Clock Specifications

Table 48: SDRAM DDR2 Clock Specifications

Description	Symbol	Min	Max	Units	Notes
Clock period jitter	tJIT(per)	-100	100	ps	1
Clock perior jitter during DLL locking period	tJIT(per,lck)	-80	80	ps	2
Cycle to cycle clock period jitter	tJIT(cc)	-200	200	ps	3
Cycle to cycle clock period jitter during DLL locking period	tJIT(cc,lck)	-160	160	ps	4
Cumulative error across 2 cycles	tERR(2per)	-150	150	ps	5
Cumulative error across 3 cycles	tERR(3per)	-175	175	ps	5
Cumulative error across 4 cycles	tERR(4per)	-200	200	ps	5
Cumulative error across 5 cycles	tERR(5per)	-200	200	ps	5
Cumulative error across n cycles, n=6...10, inclusive	tERR(6-10per)	-300	300	ps	5
Cumulative error across n cycles, n=11…50, inclusive	tERR(11-50per)	-450	450	ps	5
Duty cycle jitter	tJIT(duty)	-100	100	ps	6
Absolute clock period	tCK(abs)	See note 7		ps	7
Absolute clock high pulse width	tCH(abs)	See note 8		ps	8
Absolute clock low pulse width	tCL(abs)	See note 9		ps	9

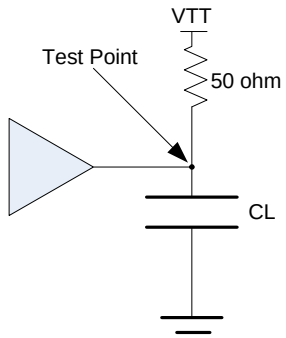
Notes:

General comment: All timing values are defined on CLK / CLKn crossing point, unless otherwise specified.

1. tJIT(per) is defined as the largest deviation of any single tCK from tCK(avg).
   tJIT(per) = Min/max of {tCKi- tCK(avg) where i=1 to 200}.
   tJIT(per) defines the single period jitter when the DLL is already locked.
2. tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.
3. tJIT(cc) is defined as the difference in clock period between two consecutive clock cycles: tJIT(cc) = Max of |tCKi+1 – tCKi|.
   tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.
4. tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.
5. tERR is defined as the cumulative error across multiple consecutive cycles from tCK(avg).
   Please refer to JEDEC Standard No. 79-2C (DDR2 SDRAM Specification), Chapter 5 (page 100) for more information.
6. tJIT(duty) is defined as the cumulative set of tCH jitter and tCL jitter. tCH jitter is the largest deviation of
   any single tCH from tCH(avg). tCL jitter is the largest deviation of any single tCL from tCL(avg).
   tJIT(duty) = Min/max of {tJIT(CH), tJIT(CL)} where,
   tJIT(CH) = {tCHi- tCH(avg) where i=1 to 200}; tJIT(CL) = {tCLi- tCL(avg) where i=1 to 200}.
7. tCK(abs),min = tCK(avg),min + tJIT(per),min; tCK(abs),max = tCK(avg),max + tJIT(per),max.
8. tCH(abs),min = tCH(avg),min x tCK(avg),min + tJIT(duty),min; tCH(abs),max = tCH(avg),max x tCK(avg),max + tJIT(duty),max.
9. tCL(abs),min = tCL(avg),min x tCK(avg),min + tJIT(duty),min; tCL(abs),max = tCL(avg),max x tCK(avg),max + tJIT(duty),max.

8.6.2.3 SDRAM DDR2 Interface Test Circuit

Figure 5: SDRAM DDR2 Interface Test Circuit



8.6.2.4 SDRAM DDR2 Interface AC Timing Diagrams

Figure 6: SDRAM DDR2 Interface Write AC Timing Diagram

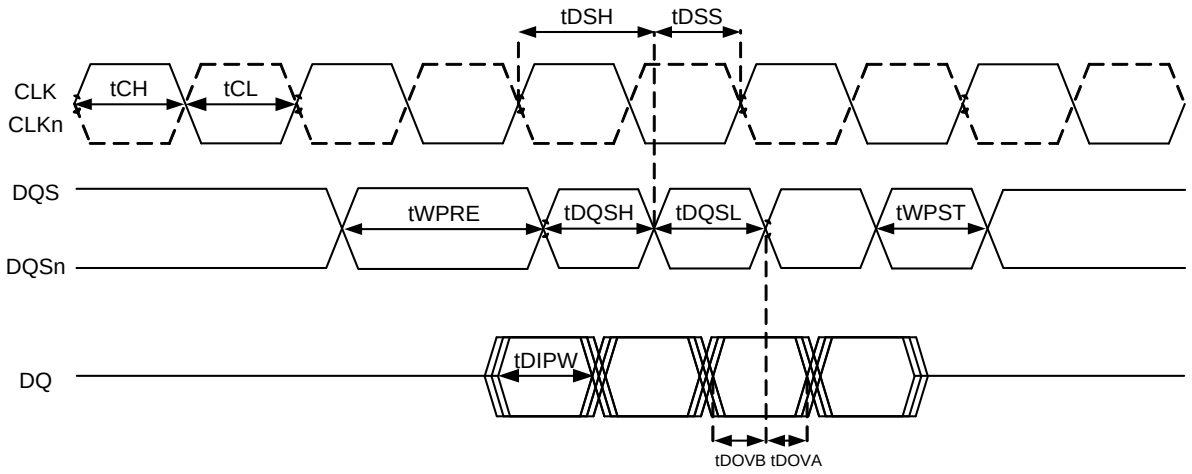


Figure 7: SDRAM DDR2 Interface Address and Control AC Timing Diagram

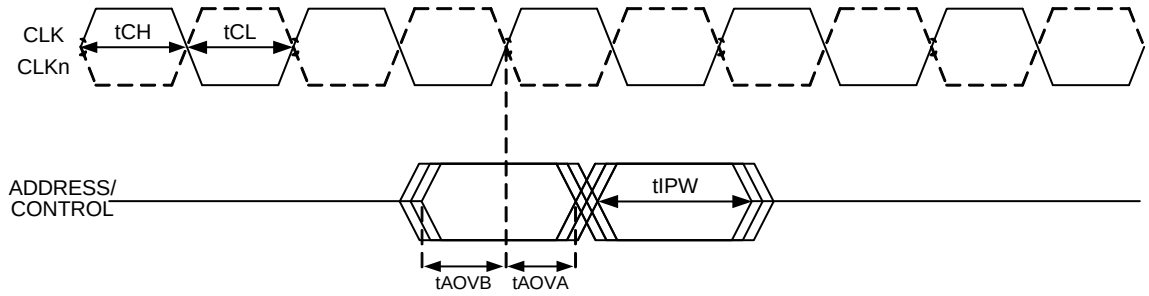
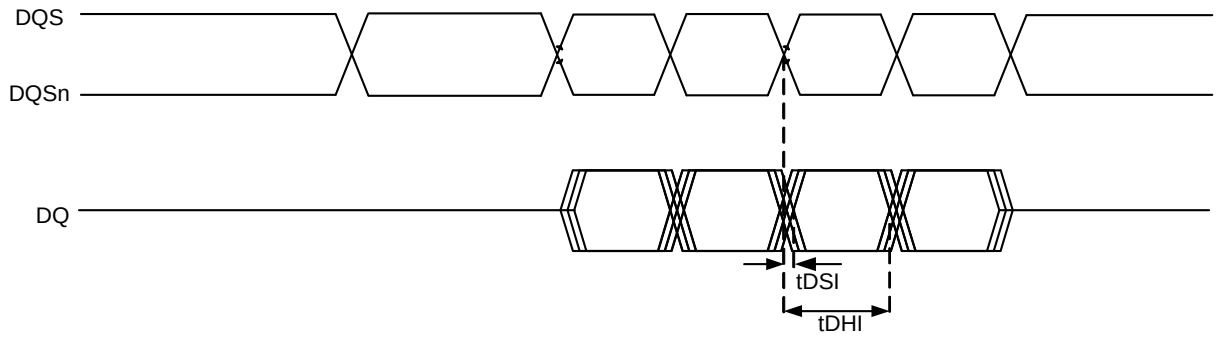


Figure 8: SDRAM DDR2 Interface Read AC Timing Diagram



8.6.3 Reduced Gigabit Media Independent Interface (RGMII) AC Timing

8.6.3.1 RGMII AC Timing Table

Table 49: RGMII 10/100/1000 AC Timing Table at 1.8V

Description	Symbol	Min	Max	Units	Notes
Clock frequency	fCK	125.0		MHz	-
Data to Clock output skew	TskewT	-0.50	0.50	ns	2
Data to Clock input skew	TskewR	1.00	2.60	ns	-
Clock cycle duration	Tcyc	7.20	8.80	ns	1 , 2
Duty cycle for Gigabit	Duty_G	0.45	0.55	tCK	2
Duty cycle for 10/100 Megabit	Duty_T	0.40	0.60	tCK	2

Notes:

General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

General comment: tCK = 1/fCK.

General comment: If the PHY does not support internal-delay mode, the PC board design requires routing clocks so that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal.
For 10/100 Mbps RGMII, the Max value is unspecified.

1. For RGMII at 10 Mbps and 100 Mbps, Tcyc will scale to 400 ns +/-40 ns and 40 ns +/-4 ns, respectively.
2. For all signals, the load is CL = 5 pF.

Table 50: RGMII 10/100 AC Timing Table at 3.3V

Description	Symbol	Min	Max	Units	Notes
Clock frequency	fCK	25.0		MHz	-
Data to Clock output skew	TskewT	-0.50	0.50	ns	2
Data to Clock input skew	TskewR	1.00	2.60	ns	-
Clock cycle duration	Tcyc	7.20	8.80	ns	1 , 2
Duty cycle for Gigabit	Duty_G	0.45	0.55	tCK	2
Duty cycle for 10/100 Megabit	Duty_T	0.40	0.60	tCK	2

Notes:

General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

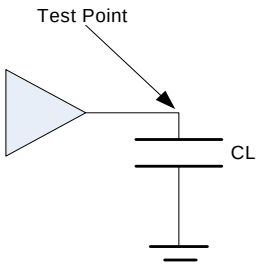
General comment: tCK = 1/fCK.

General comment: If the PHY does not support internal-delay mode, the PC board design requires routing clocks so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
For 10/100 Mbps RGMII, the Max value is unspecified.

1. For RGMII at 10 Mbps and 100 Mbps, Tcyc will scale to 400 ns +/-40 ns and 40 ns +/-4 ns, respectively.
2. For all signals, the load is CL = 5 pF.

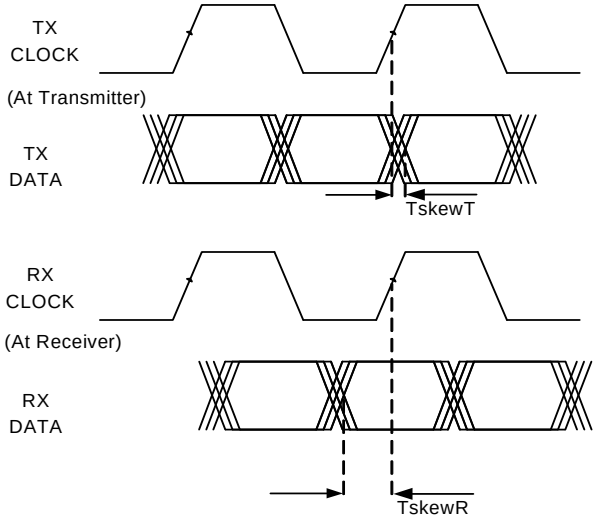
8.6.3.2 RGMII Test Circuit

Figure 9: RGMII Test Circuit



8.6.3.3 RGMII AC Timing Diagram

Figure 10: RGMII AC Timing Diagram



8.6.4 Gigabit Media Independent Interface (GMII) AC Timing

8.6.4.1 GMII AC Timing Table

Table 51: GMII AC Timing Table

Description	Symbol	125 MHz		Units	Notes
		Min	Max		
GTX_CLK cycle time	tCK	7.5	8.5	ns	-
RX_CLK cycle time	tCKrx	7.5	-	ns	-
GTX_CLK and RX_CLK high level width	tHIGH	2.5	-	ns	1
GTX_CLK and RX_CLK low level width	tLOW	2.5	-	ns	1
GTX_CLK and RX_CLK rise time	tR	-	1.0	ns	1, 2
GTX_CLK and RX_CLK fall time	tF	-	1.0	ns	1, 2
Data input setup time relative to RX_CLK rising edge	tSETUP	2.0	-	ns	-
Data input hold time relative to RX_CLK rising edge	tHOLD	0.0	-	ns	-
Data output valid before GTX_CLK rising edge	tOVB	2.5	-	ns	1
Data output valid after GTX_CLK rising edge	tOVA	0.5	-	ns	1

Notes:

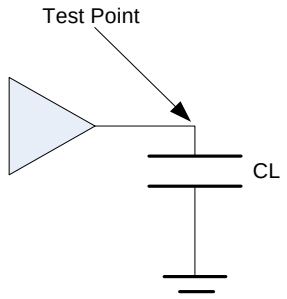
General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

1. For all signals, the load is CL = 5 pF.

2. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max).

8.6.4.2 GMII Test Circuit

Figure 11: GMII Test Circuit



8.6.4.3 GMII AC Timing Diagrams

Figure 12: GMII Output AC Timing Diagram

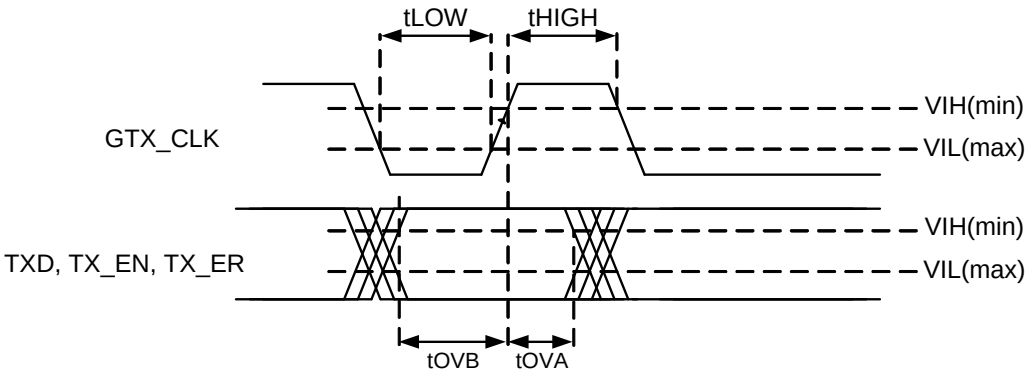
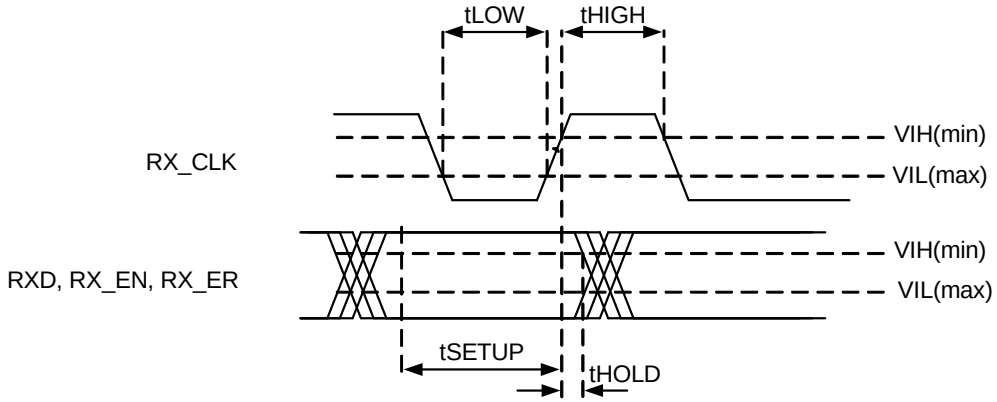


Figure 13: GMII Input AC Timing Diagram



8.6.5 Media Independent Interface/Marvell Media Independent Interface (MII/MMII) AC Timing

8.6.5.1 MII/MMII MAC Mode AC Timing Table

Table 52: MII/MMII MAC Mode AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Data input setup relative to RX_CLK rising edge	tSU	3.5	-	ns	-
Data input hold relative to RX_CLK rising edge	tHD	2.0	-	ns	-
Data output delay relative to MII_TX_CLK rising edge	tOV	0.0	10.0	ns	1

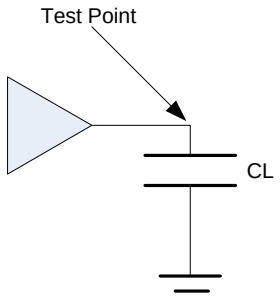
Notes:

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

1. For all signals, the load is CL = 5 pF.

8.6.5.2 MII/MMII MAC Mode Test Circuit

Figure 14: MII/MMII MAC Mode Test Circuit



8.6.5.3 MII/MMII MAC Mode AC Timing Diagrams

Figure 15: MII/MMII MAC Mode Output Delay AC Timing Diagram

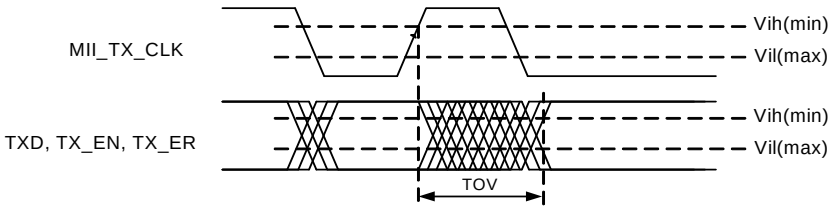
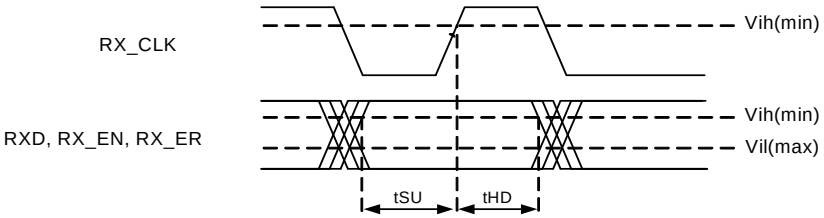


Figure 16: MII/MMII MAC Mode Input AC Timing Diagram



8.6.6 Serial Management Interface (SMI) AC Timing

8.6.6.1 SMI Master Mode AC Timing Table

Table 53: SMI Master Mode AC Timing Table

Description	Symbol	Min	Max	Units	Notes
MDC clock frequency	fCK	See note 2		MHz	2
MDC clock duty cycle	tDC	0.4	0.6	tCK	-
MDIO input setup time relative to MDC rise time	tSU	40.0	-	ns	-
MDIO input hold time relative to MDC rise time	tHO	0.0	-	ns	-
MDIO output valid before MDC rise time	tOVB	15.0	-	ns	1
MDIO output valid after MDC rise time	tOVA	15.0	-	ns	1

Notes:

General comment: All timing values were measured from VIL(max) and VIH(min) levels, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For MDC signal, the load is CL = 390 pF, and for MDIO signal, the load is CL = 470 pF.

2. See "Reference Clocks" table for more details.

8.6.6.2 SMI Master Mode Test Circuit

Figure 17: MDIO Master Mode Test Circuit

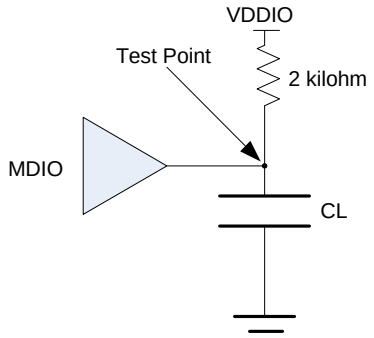
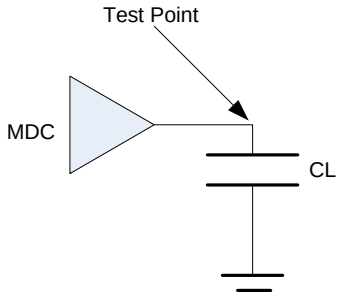


Figure 18: MDC Master Mode Test Circuit



8.6.6.3 SMI Master Mode AC Timing Diagrams

Figure 19: SMI Master Mode Output AC Timing Diagram

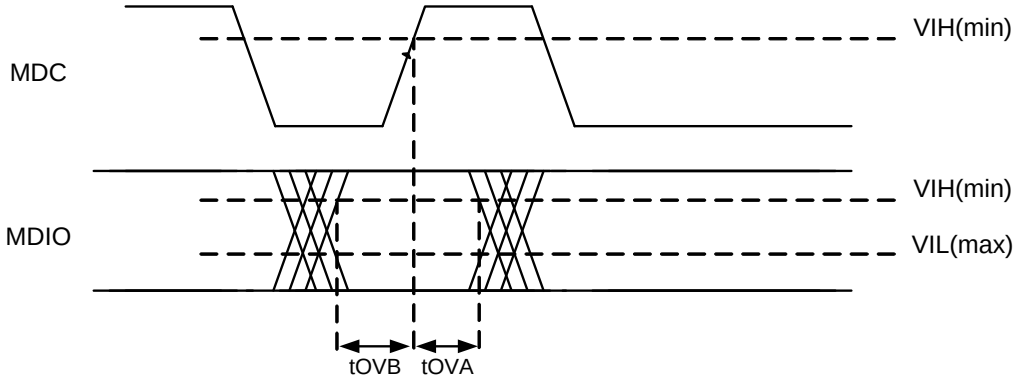
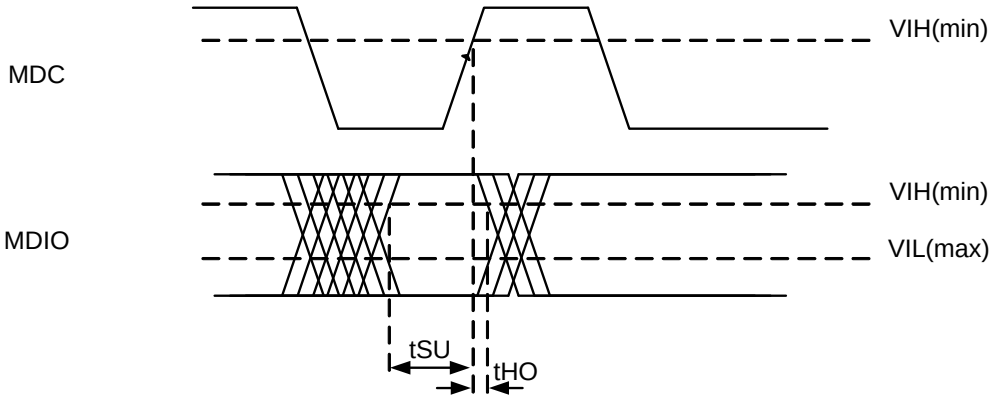


Figure 20: SMI Master Mode Input AC Timing Diagram



8.6.7 JTAG Interface AC Timing

8.6.7.1 JTAG Interface AC Timing Table

Table 54: JTAG Interface AC Timing Table

Description	Symbol	30 MHz		Units	Notes
		Min	Max		
JTClk frequency	fCK	30.0		MHz	-
JTClk minimum pulse width	Tpw	0.45	0.55	tCK	-
JTClk rise/fall slew rate	Sr/Sf	0.50	-	V/ns	2
JTRSTn active time	Trst	1.0	-	ms	-
TMS, TDI input setup relative to JTClk rising edge	Tsetup	6.67	-	ns	-
TMS, TDI input hold relative to JTClk rising edge	Thold	13.0	-	ns	-
JTClk falling edge to TDO output delay	Tprop	1.0	8.33	ns	1

Notes:

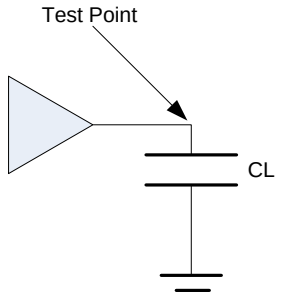
General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For TDO signal, the load is CL = 10 pF.
2. Defined from VIL to VIH for rise time, and from VIH to VIL for fall time.

8.6.7.2 JTAG Interface Test Circuit

Figure 21: JTAG Interface Test Circuit



8.6.7.3 JTAG Interface AC Timing Diagrams

Figure 22: JTAG Interface Output Delay AC Timing Diagram

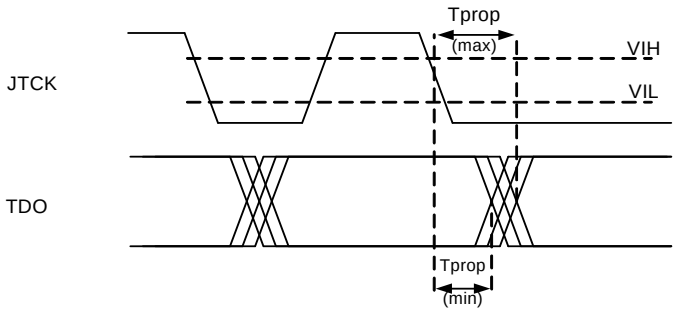
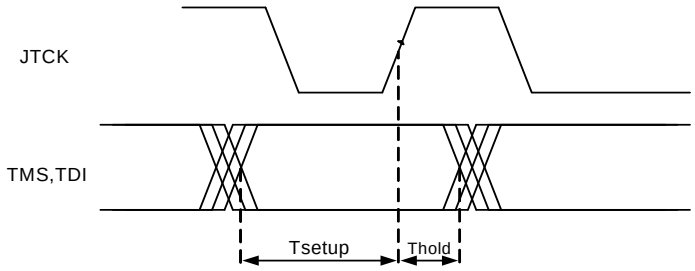


Figure 23: JTAG Interface Input AC Timing Diagram



8.6.8 Two-Wire Serial Interface (TWSI) AC Timing

8.6.8.1 TWSI AC Timing Table

Table 55: TWSI Master AC Timing Table

Description	Symbol	Min	Max	Units	Notes
SCK clock frequency	fCK	See note 1		kHz	1
SCK minimum low level width	tLOW	0.47	-	tCK	2
SCK minimum high level width	tHIGH	0.40	-	tCK	2
SDA input setup time relative to SCK rising edge	tSU	250.0	-	ns	-
SDA input hold time relative to SCK falling edge	tHD	0.0	-	ns	-
SDA and SCK rise time	tr	-	1000.0	ns	2, 3
SDA and SCK fall time	tf	-	300.0	ns	2, 3
SDA output delay relative to SCK falling edge	tOV	0.0	0.4	tCK	2

Notes:

General comment: All values referred to VIH(min) and VIL(max) levels, unless otherwise specified.

General comment: tCK = 1/fCK.

1. See "Reference Clocks" table for more details.
2. For all signals, the load is CL = 100 pF, and RL value can be 500 ohm to 8 kilohm.
3. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max).

Table 56: TWSI Slave AC Timing Table

Description	Symbol	100 kHz		Units	Notes
		Min	Max		
SCK minimum low level width	tLOW	4.7	-	us	1
SCK minimum high level width	tHIGH	4.0	-	us	1
SDA input setup time relative to SCK rising edge	tSU	250.0	-	ns	-
SDA input hold time relative to SCK falling edge	tHD	0.0	-	ns	-
SDA and SCK rise time	tr	-	1000.0	ns	1, 2
SDA and SCK fall time	tf	-	300.0	ns	1, 2
SDA output delay relative to SCK falling edge	tOV	0.0	4.0	us	1

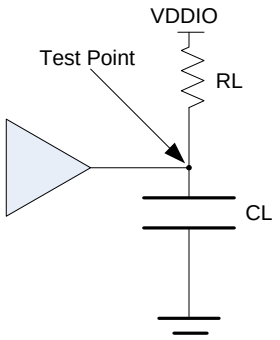
Notes:

General comment: All values referred to VIH(min) and VIL(max) levels, unless otherwise specified.

1. For all signals, the load is CL = 100 pF, and RL value can be 500 ohm to 8 kilohm.
2. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max).

8.6.8.2 TWSI Test Circuit

Figure 24: TWSI Test Circuit



8.6.8.3 TWSI AC Timing Diagrams

Figure 25: TWSI Output Delay AC Timing Diagram

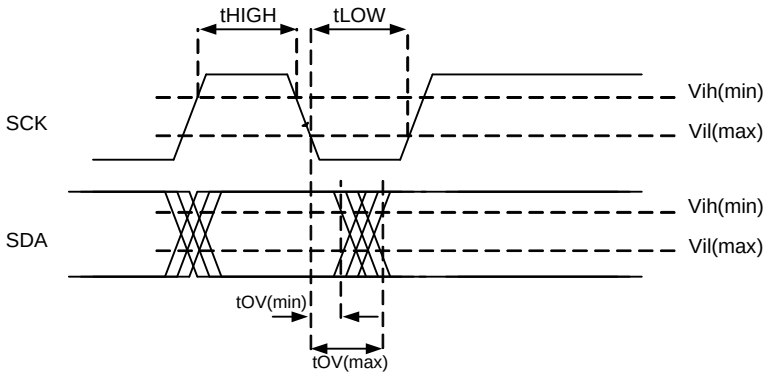
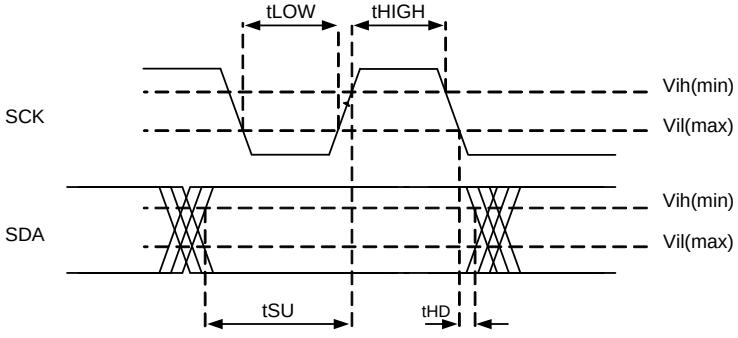


Figure 26: TWSI Input AC Timing Diagram



8.6.9 Sony/Philips Digital Interconnect Format (S/PDIF) AC Timing

8.6.9.1 S/PDIF AC Timing Table

Table 57: S/PDIF AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Output frequency accuracy	Ftxtol	-50.0	50.0	ppm	1
Input frequency accuracy	Frxtol	-100.0	100.0	ppm	-
Output jitter - total peak-to-peak	Txjit	-	0.05	UI	1, 2
Jitter transfer gain	Txjitgain	-	3.0	dB	3
Input jitter - total peak-to-peak	Rxjit	-	10.0	UI	4
		-	0.25	UI	5
		-	0.2	UI	6

Notes:

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

General comment: For more information, refer to the Digital Audio Interface - Part 3: Consumer Applications, IEC 60958-3:2003(E), Chapter 7.3, January 2003.

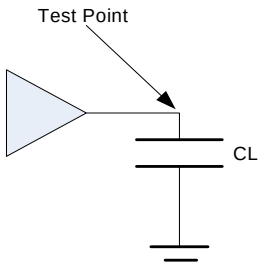
1. For all signals, the load is CL = 10 pF.
2. Using inristic jitter filter.
3. Refer to Figure-8 in IEC 60958-3:2003(E), Chapter 7.3, January 2003.
4. Defined for up to 5 Hz.
5. Defined from 200 Hz to 400 kHz.
6. Defined for above 400 kHz.

Note

For additional information about working with a coax connection, see the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide*.

8.6.9.2 S/PDIF Test Circuit

Figure 27: S/PDIF Test Circuit



8.6.10 Inter-IC Sound Interface (I^2S) AC Timing

8.6.10.1 Inter-IC Sound (I^2S) AC Timing Table

Table 58: Inter-IC Sound (I^2S) AC Timing Table

Description	Symbol	Min	Max	Units	Notes
I2SBCLK clock frequency	fCK	See note 2		MHz	2
I2SBCLK clock high/low level pulse width	tCH/tCL	0.37	-	tCK	1
I2SDI input setup time relative to I2SBCLK rise time	tSU	0.10	-	tCK	-
I2SDI input hold time relative to I2SBCLK rise time	tHO	0.00	-	ns	-
I2SDO, I2SLRCLK output delay relative to I2SBCLK rise time	tOD	0.10	0.70	tCK	1

Notes:

General comment: All timing values were measured from VIL(max) and VIH(min) levels, unless otherwise specified.

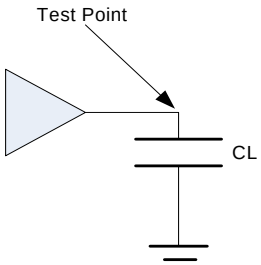
General comment: tCK = 1/fCK.

1. For all signals, the load is CL = 15 pF.

2. See "Reference Clocks" table for more details.

8.6.10.2 Inter-IC Sound (I^2S) Test Circuit

Figure 28: Inter-IC Sound (I^2S) Test Circuit



8.6.10.3 Inter-IC Sound (I^2S) AC Timing Diagrams

Figure 29: Inter-IC Sound (I^2S) Output Delay AC Timing Diagram

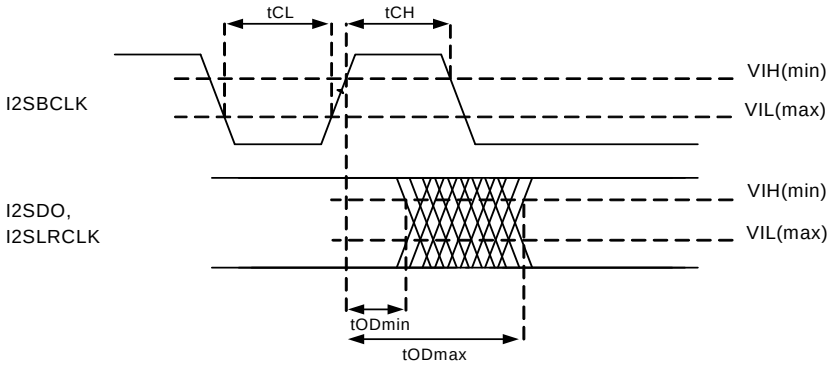
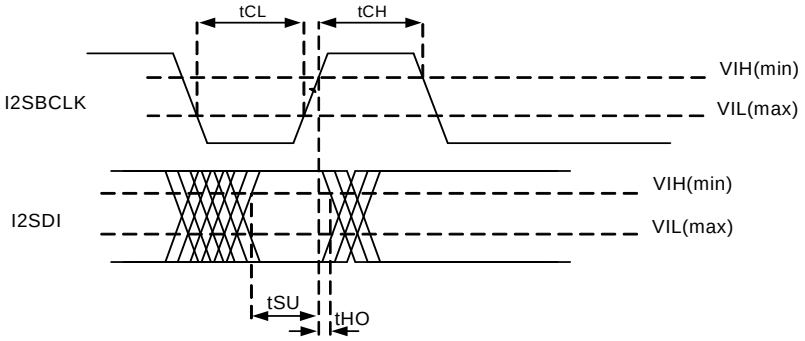


Figure 30: Inter-IC Sound (I^2S) Input AC Timing Diagram



8.6.11 Time Division Multiplexing (TDM) Interface AC Timing

8.6.11.1 TDM Interface AC Timing Table

Table 59: TDM Interface AC Timing Table

Description	Symbol	8.192 MHz		Units	Notes
		Min	Max		
PCLK cycle time	1/tC	0.256	8.192	MHz	1, 3
PCLK duty cycle	tDTY	0.4	0.6	tC	1
PCLK rise/fall time	tR/tF	-	3.0	ns	1, 2, 8
DTX and FSYNC valid after PCLK rising edge	tD	0.0	20.0	ns	1, 4, 6
DRX and FSYNC setup time relative to PCLK falling edge	tSU	10.0	-	ns	5, 7
DRX and FSYNC hold time relative to PCLK falling edge	tHD	10.0	-	ns	5, 7

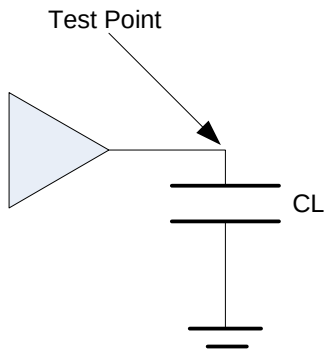
Notes:

General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

1. For all signals, the load is CL = 20 pF.
2. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.
3. PCLK can be configured to 0.256, 0.512, 0.768, 1.024, 1.536, 2.048, 4.096, 8.192 MHz frequencies only.
4. This parameter is relevant to FSYNC signal in master-mode only.
5. This parameter is relevant to FSYNC signal in slave-mode only.
6. In negative-mode, the DTX signal is relative to PCLK falling edge.
7. In negative-mode, the DRX signal is relative to PCLK rising edge.
8. This parameter is relevant when the PCLK pin is output.

8.6.11.2 TDM Interface Test Circuit

Figure 31: TDM Interface Test Circuit



8.6.11.3 TDM Interface Timing Diagrams

Figure 32: TDM Interface Output Delay AC Timing Diagram

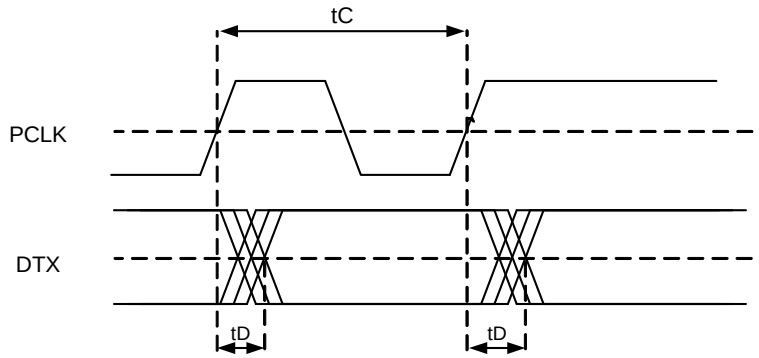
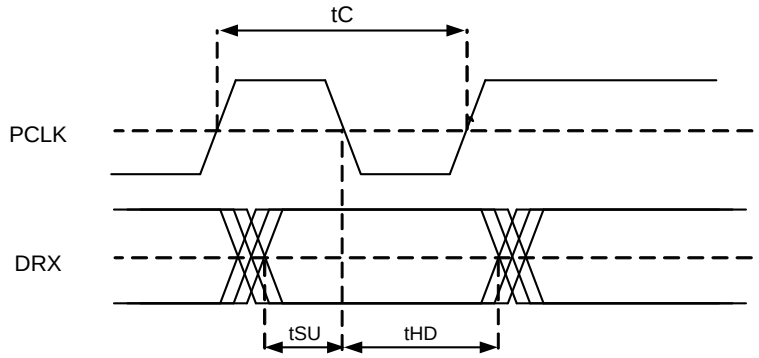


Figure 33: TDM Interface Input Delay AC Timing Diagram



8.6.12 Serial Peripheral Interface (SPI) AC Timing

8.6.12.1 SPI (Master Mode) AC Timing Table

Table 60: SPI (Master Mode) AC Timing Table

Description	Symbol	SPI		Units	Notes
		Min	Max		
SCLK clock frequency	fCK	See Note 3		MHz	3
SCLK high time	tCH	0.46	-	tCK	1
SCLK low time	tCL	0.46	-	tCK	1
SCLK slew rate	tSR	0.5	-	V/ns	1
Data out valid relative to SCLK falling edge	tDOV	-2.5	2.5	ns	1
CS active before SCLK rising edge	tCSB	8.0	-	ns	1
CS not active after SCLK rising edge	tCSA	8.0	-	ns	1
Data in setup time relative to SCLK rising edge	tSU	0.2	-	tCK	2
Data in hold time relative to SCLK rising edge	tHD	5.0	-	ns	2

Notes:

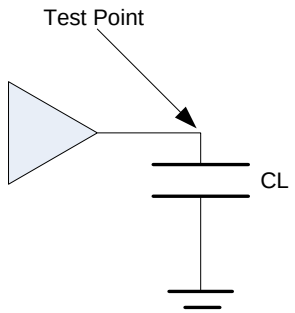
General comment: All values were measured from 0.3*vddio to 0.7*vddio, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For all signals, the load is CL = 10 pF.
2. Defined from vddio/2 to vddio/2.
3. See "Reference Clocks" table for more details.

8.6.12.2 SPI (Master Mode) Test Circuit

Figure 34: SPI (Master Mode) Test Circuit



8.6.12.3 SPI (Master Mode) Timing Diagrams

Figure 35: SPI (Master Mode) Output AC Timing Diagram

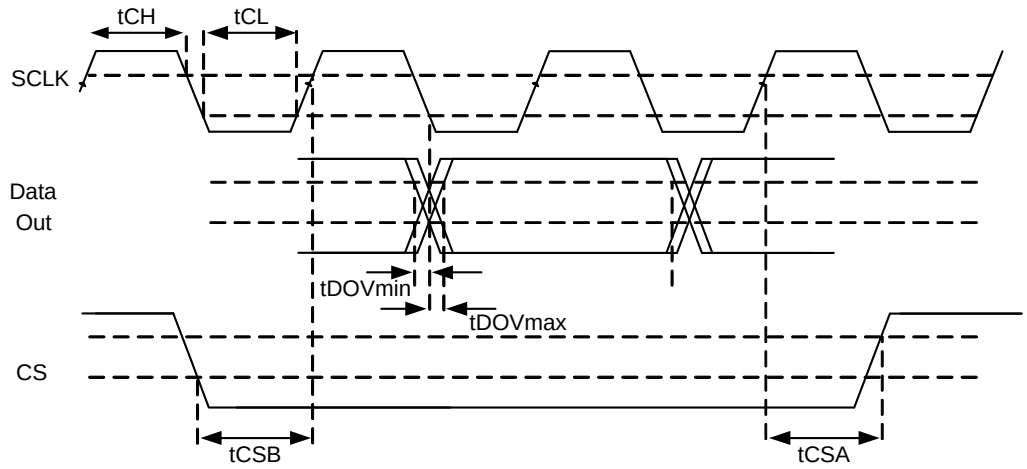
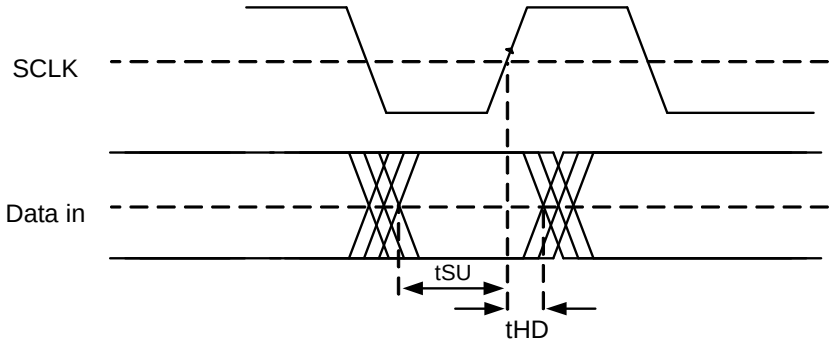


Figure 36: SPI (Master Mode) Input AC Timing Diagram



8.6.13 Secure Digital Input/Output (SDIO) Interface AC Timing

8.6.13.1 Secure Digital Input/Output (SDIO) AC Timing Table

Table 61: SDIO Host in High Speed Mode AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Clock frequency in Data Transfer Mode	fCK	0	50	MHz	-
Clock high/low level pulse width	tWL/tWH	0.35	-	tCK	1, 3
Clock rise/fall time	tTLH/tTHL	-	3.0	ns	1, 3
CMD, DAT output valid before CLK rising edge	tDOVB	6.5	-	ns	2, 3
CMD, DAT output valid after CLK rising edge	tDOVA	2.5	-	ns	2, 3
CMD, DAT input setup relative to CLK rising edge	tISU	7.0	-	ns	2
CMD, DAT input hold relative to CLK rising edge	tIHD	0.0	-	ns	2

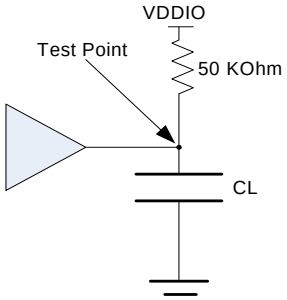
Notes:

General comment: tCK = 1/fCK.

1. Defined on VIL(max) and VIH(min) levels.
2. Defined on VDDIO/2 for Clock signal, and VIL(max) / VIH(min) for CMD & DAT signals.
3. For all signals, the load is CL = 10 pF.

8.6.13.2 Secure Digital Input/Output (SDIO) Test Circuit

Figure 37: Secure Digital Input/Output (SDIO) Test Circuit



8.6.13.3 Secure Digital Input/Output (SDIO) AC Timing Diagrams

Figure 38: SDIO Host in High Speed Mode Output AC Timing Diagram

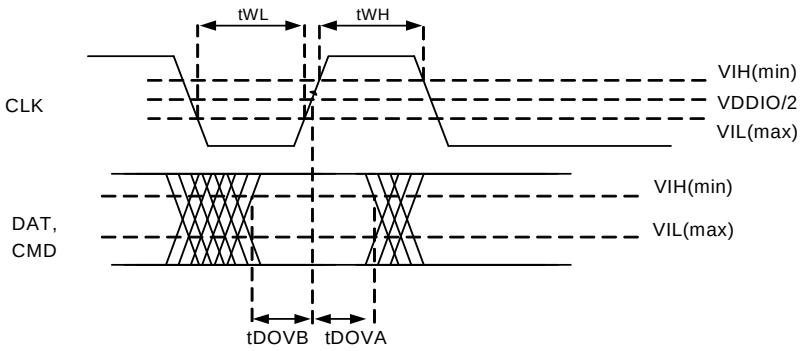
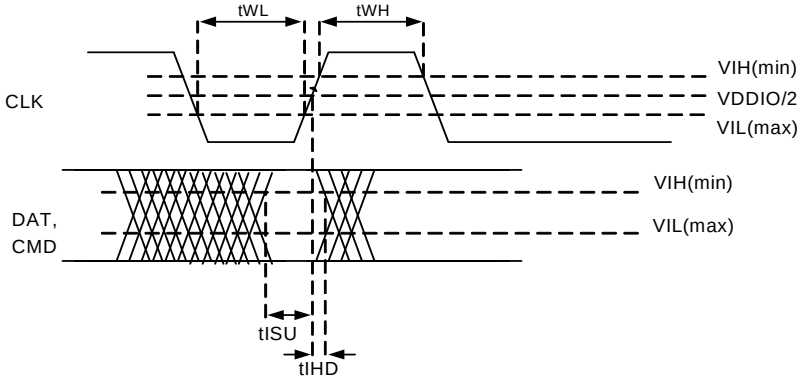


Figure 39: SDIO Host in High Speed Mode Input AC Timing Diagram



8.6.14 Transport Stream (TS) Interface AC Timing

8.6.14.1 Transport Stream Interface AC Timing Table

Table 62: Transport Stream Output Interface AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Clock frequency	fCK	See note 1		MHz	1
Clock minimum low level width	tLOW	0.4	0.6	tCK	2
Clock minimum high level width	tHIGH	0.4	0.6	tCK	2
Data output valid after Clock rising edge	tOV	0.4	0.6	tCK	2, 3

Notes:

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

General comment: tCK = 1/fCK.

1. See "Reference Clocks" table for more details.
2. For all signals, the load is CL = 5 pF.
3. When configured to falling edge, the tOV parameter is relative to Clock falling edge.

Table 63: Transport Stream Input Interface AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Clock frequency	fCK	See note 1		MHz	1
Clock minimum low level width	tLOW	0.35	0.65	tCK	-
Clock minimum high level width	tHIGH	0.35	0.65	tCK	-
Data input setup time relative to Clock rising edge	tSU	0.30	-	tCK	2
Data input setup time relative to Clock rising edge	tHD	0.30	-	tCK	2

Notes:

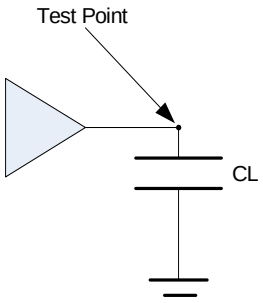
General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

General comment: tCK = 1/fCK.

1. See "Reference Clocks" table for more details.
2. When configured to falling edge, the tSU/tHD parameters are relative to Clock falling edge.

8.6.14.2 Transport Stream Interface Test Circuit

Figure 40: Transport Stream Interface Test Circuit



8.6.14.3 Transport Stream Interface Timing Diagrams

Figure 41: Transport Stream Output Interface AC Timing Diagram

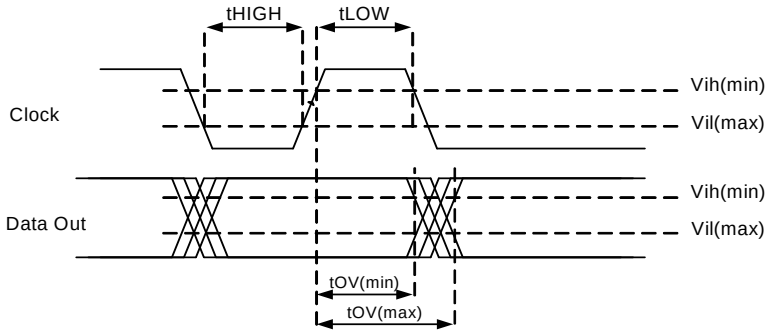
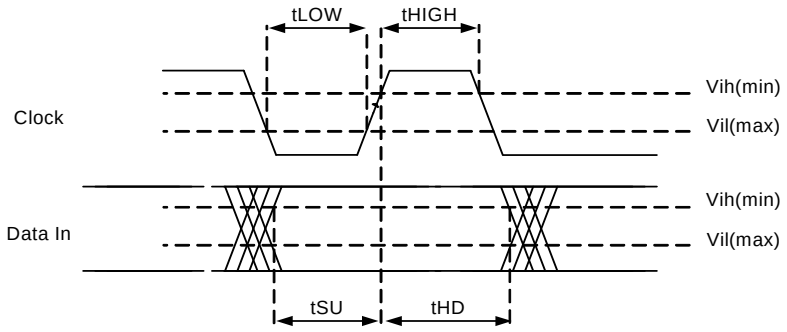


Figure 42: Transport Stream Input Interface AC Timing Diagram



8.7 Differential Interface Electrical Characteristics

This section provides the reference clock, AC, and DC characteristics for the following differential interfaces:

- PCI Express Interface Electrical Characteristics
- SATA Interface Electrical Characteristics
- USB Electrical Characteristics

8.7.1 Differential Interface Reference Clock Characteristics

8.7.1.1 PCI Express Interface Differential Reference Clock Characteristics

Table 64: PCI Express Interface Differential Reference Clock Characteristics

Description	Symbol	Min	Max	Units	Notes
Clock frequency	fCK	100.0		MHz	-
Clock duty cycle	DCrefclk	0.4	0.6	tCK	-
Differential rising/falling slew rate	SRrefclk	0.6	4.0	V/nS	3
Differential high voltage	VIHrefclk	150.0	-	mV	-
Differential low voltage	VILrefclk	-	-150.0	mV	-
Absolute crossing point voltage	Vcross	250.0	550.0	mV	1
Variation of Vcross over all rising clock edges	Vcrs_dlta	-	140.0	mV	1
Average differential clock period accuracy	Tperavg	-300.0	2800.0	ppm	-
Absolute differential clock period	Tperabs	9.8	10.2	nS	2
Differential clock cycle-to-cycle jitter	Tccjit	-	150.0	pS	-

Notes:

General Comment: The reference clock timings are based on 100 ohm test circuit.

General Comment: Refer to the PCI Express Card Electromechanical Specification, Revision 1.1, March 2005, section 2.1.3 for more information.

1. Defined on a single-ended signal.
2. Including jitter and spread spectrum.
3. Defined from -150 mV to +150 mV on the differential waveform.

PCI Express Interface Spread Spectrum Requirements

Table 65: PCI Express Interface Spread Spectrum Requirements

Symbol	Min	Max	Units	Notes
Fmod	0.0	33.0	kHz	1
Fspread	-0.5	0.0	%	1

Notes:
1. Defined on linear sweep or “Hershey’s Kiss” (US Patent 5,631,920) modulations.

8.7.2 PCI Express Interface Electrical Characteristics

8.7.2.1 PCI Express Interface Driver and Receiver Characteristics

Table 66: PCI Express Interface Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud rate	BR	2.5		Gbps	-
Unit interval	UI	400.0		ps	-
Baud rate tolerance	Bppm	-300.0	300.0	ppm	2
Driver parameters					
Differential peak to peak output voltage	VTXpp	0.8	1.2	V	-
Minimum TX eye width	TTXeye	0.75	-	UI	-
Differential return loss	TRLdiff	10.0	-	dB	1
Common mode return loss	TRLcm	6.0	-	dB	1
DC differential TX impedance	ZTXdiff	80.0	120.0	Ohm	-
Receiver parameters					
Differential input peak to peak voltage	VRXpp	0.175	1.2	V	-
Minimum receiver eye width	TRXeye	0.4	-	UI	-
Differential return loss	RRLdiff	10.0	-	dB	1
Common mode return loss	RRLcm	6.0	-	dB	1
DC differential RX impedance	ZRXdiff	80.0	120.0	Ohm	-
DC common input impedance	ZRXcm	40.0	60.0	Ohm	-

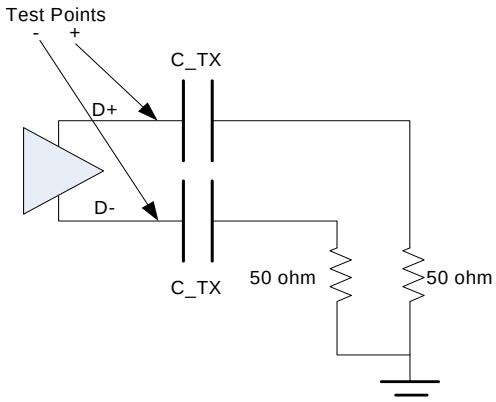
Notes:

General Comment: For more information, refer to the PCI Express Base Specification, Revision 1.1, March, 2005.

1. Defined from 50 MHz to 1.25 GHz.
2. Does not account for SSC dictated variations.

8.7.2.2 PCI Express Interface Test Circuit

Figure 43: PCI Express Interface Test Circuit



When measuring Transmitter output parameters, C_TX is an optional portion of the Test/Measurement load. When used, the value of C_TX must be in the range of 75 nF to 200 nF. C_TX must not be used when the Test/Measurement load is placed in the Receiver package reference plane.

8.7.3 SATA Interface Electrical Characteristics

The driver and receiver characteristics for the SATA-I Interface Gen1i Mode and the SATA-II Interface Gen2i Mode are provided in the following sections.

8.7.3.1 SATA-I Interface Gen1i Mode Driver and Receiver Characteristics

Table 67: SATA-I Interface Gen1i Mode Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud Rate	BR	1.5		Gbps	-
Baud rate tolerance	Bppm	-350.0	350.0	ppm	-
Spread spectrum modulation frequency	Fssc	30.0	33.0	kHz	-
Spread spectrum modulation Deviation	SSCtol	-5000.0	0.0	ppm	-
Unit Interval	UI	666.67		ps	-
Driver Parameters					
Differential impedance	Zdifftx	85.0	115.0	Ohm	-
Single ended impedance	Zsetx	40.0	-	Ohm	-
Differential return loss (75 MHz-150 MHz)	RLOD	14.0	-	dB	-
Differential return loss (150 MHz-300 MHz)	RLOD	8.0	-	dB	-
Differential return loss (300 MHz-1.2 GHz)	RLOD	6.0	-	dB	-
Differential return loss (1.2 GHz-2.4 GHz)	RLOD	3.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLOD	1.0	-	dB	-
Output differential voltage	Vdifftx	400.0	600.0	mV	2
Total jitter at connector data-data, 5UI	TJ5	-	0.355	UI	1
Deterministic jitter at connector data-data, 5UI	DJ5	-	0.175	UI	-
Total jitter at connector data-data, 250UI	TJ250	-	0.470	UI	1
Deterministic jitter at connector data-data, 250UI	DJ250	-	0.220	UI	-
Receiver Parameters					
Differential impedance	Zdiffrx	85.0	115.0	Ohm	-
Single ended impedance	Zsetx	40.0	-	Ohm	-
Differential return loss (75 MHz-150 MHz)	RLID	18.0	-	dB	-
Differential return loss (150 MHz-300 MHz)	RLID	14.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLID	10.0	-	dB	-
Differential return loss (600 MHz-1.2 GHz)	RLID	8.0	-	dB	-
Differential return loss (1.2 GHz-2.4 GHz)	RLID	3.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLID	1.0	-	dB	-
Input differential voltage	Vdiffrx	325.0	600.0	mV	-
Total jitter at connector data-data, 5UI	TJ5	-	0.430	UI	1
Deterministic jitter at connector data-data, 5UI	DJ5	-	0.250	UI	-
Total jitter at connector data-data, 250UI	TJ250	-	0.600	UI	1
Deterministic jitter at connector data-data, 250UI	DJ250	-	0.350	UI	-

Notes:

General Comment: For more information, refer to SATA II Revision 2.6 Specification, February, 2007.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Total jitter is defined as TJ = (14 * RJσ) + DJ where Rjσ is random jitter.
2. Output Differential Amplitude and Pre-Emphasis are configurabile. See functional register description for more details.

8.7.3.2 SATA-II Interface Gen2i Mode Driver and Receiver Characteristics

Table 68: SATA-II Interface Gen2i Mode Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud Rate	BR	3.0		Gbps	-
Baud rate tolerance	Bppm	-350.0	350.0	ppm	-
Spread spectrum modulation frequency	Fssc	30.0	33.0	kHz	-
Spread spectrum modulation Deviation	SSCtol	-5000.0	0.0	ppm	-
Unit Interval	UI	333.33		ps	-
Driver Parameters					
Output differential voltage	Vdifftx	400.0	700.0	mV	1 , 2
Differential return loss (150 MHz-300 MHz)	RLOD	14.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLOD	8.0	-	dB	-
Differential return loss (600 MHz-2.4 GHz)	RLOD	6.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLOD	3.0	-	dB	-
Differential return loss (3.0 GHz-5.0 GHz)	RLOD	1.0	-	dB	-
Total jitter at connector clock-data	TJ10	-	0.30	UI	3
Deterministic jitter at connector clock-data	DJ10	-	0.17	UI	3
Total jitter at connector clock-data	TJ500	-	0.37	UI	4
Deterministic jitter at connector clock-data	DJ500	-	0.19	UI	4
Receiver Parameters					
Input differential voltage	Vdiffrx	275.0	750.0	mV	5
Differential return loss (150 MHz-300 MHz)	RLID	18.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLID	14.0	-	dB	-
Differential return loss (600 MHz-1.2 GHz)	RLID	10.0	-	dB	-
Differential return loss (1.2 GHz-2.4 GHz)	RLID	8.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLID	3.0	-	dB	-
Differential return loss (3.0 GHz-5.0 GHz)	RLID	1.0	-	dB	-
Total jitter at connector clock-data	TJ10	-	0.46	UI	3
Deterministic jitter at connector clock-data	DJ10	-	0.35	UI	3
Total jitter at connector clock-data	TJ500	-	0.60	UI	4
Deterministic jitter at connector clock-data	DJ500	-	0.42	UI	4

Notes:

General Comment: For more information, refer to SATA II Revision 2.6 Specification, February, 2007.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. 0.45-0.55 UI is the range where the signal meets the minimum level.
2. Output Differential Amplitude and Pre-Emphasis are configurabile. See functional register description for more details.
3. Defined for BR/10.
4. Defined for BR/500.
5. 0.5 UI is the point where the signal meets the minimum level.

8.7.4 USB Electrical Characteristics

8.7.4.1 USB Driver and Receiver Characteristics

Table 69: USB Low Speed Driver and Receiver Characteristics

Description	Symbol	Low Speed		Units	Notes
		Min	Max		
Baud Rate	BR	1.5		Mbps	-
Baud rate tolerance	Bppm	-15000.0	15000.0	ppm	-
Driver Parameters					
Ouput single ended high	VOH	2.8	3.6	V	1
Ouput single ended low	VOL	0.0	0.3	V	2
Output signal crossover voltage	VCRS	1.3	2.0	V	3
Data fall time	TLR	75.0	300.0	ns	3, 4
Data rise time	TLF	75.0	300.0	ns	3, 4
Rise and fall time matching	TLRFM	80.0	125.0	%	-
Source jitter total: to next transition	TUDJ1	-95.0	95.0	ns	5
Source jitter total: for paired transitions	TUDJ2	-150.0	150.0	ns	5
Receiver Parameters					
Input single ended high	VIH	2.0	-	V	-
Input single ended low	VIL	-	0.8	V	-
Differential input sensitivity	VDI	0.2	-	V	-

Notes:

General Comment: For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Defined with 1.425 kilohm pull-up resistor to 3.6V.
2. Defined with 14.25 kilohm pull-down resistor to ground.
3. See "Data Signal Rise and Fall Time" waveform.
4. Defined from 10% to 90% for rise time and 90% to 10% for fall time.
5. Including frequency tolerance. Timing difference between the differential data signals.

   Defined at crossover point of differential data signals.

Table 70: USB Full Speed Driver and Receiver Characteristics

Description	Symbol	Full Speed		Units	Notes
		Min	Max		
Baud Rate	BR	12.0		Mbps	-
Baud rate tolerance	Bppm	-2500.0	2500.0	ppm	-
Driver Parameters					
Ouput single ended high	VOH	2.8	3.6	V	1
Ouput single ended low	VOL	0.0	0.3	V	2
Output signal crossover voltage	VCRS	1.3	2.0	V	4
Output rise time	TFR	4.0	20.0	ns	3, 4
Output fall time	TFL	4.0	20.0	ns	3, 4
Source jitter total: to next transition	TDJ1	-3.5	3.5	ns	5, 6
Source jitter total: for paired transitions	TDJ2	-4.0	4.0	ns	5, 6
Source jitter for differential transition to SE0 transition	TFDEOP	-2.0	5.0	ns	6
Receiver Parameters					
Input single ended high	VIH	2.0	-	V	-
Input single ended low	VIL	-	0.8	V	-
Differential input sensitivity	VDI	0.2	-	V	-
Receiver jitter : to next transition	tJR1	-18.5	18.5	ns	6
Receiver jitter: for paired transitions	tJR2	-9.0	9.0	ns	6

Notes:

General Comment: For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1.. Defined with 1.425 kilohm pull-up resistor to 3.6V.

2.. Defined with 14.25 kilohm pull-down resistor to ground.

3. Defined from 10% to 90% for rise time and 90% to 10% for fall time.

4. See "Data Signal Rise and Fall Time" waveform.

5. Including frequency tolerance. Timing difference between the differential data signals.

6. Defined at crossover point of differential data signals.

Table 71: USB High Speed Driver and Receiver Characteristics

Description	Symbol	High Speed		Units	Notes
		Min	Max		
Baud Rate	BR	480.0		Mbps	-
Baud rate tolerance	Bppm	-500.0	500.0	ppm	-
Driver Parameters					
Data signaling high	VHSOH	360.0	440.0	mV	-
Data signaling low	VHSOL	-10.0	10.0	mV	-
Data rise time	THSR	500.0	-	ps	1
Data fall time	THSF	500.0	-	ps	1
Data source jitter		See note 2			2
Receiver Parameters					
Differential input signaling levels		See note 3			3
Data signaling common mode voltage range	VHSCM	-50.0	500.0	mV	-
Receiver jitter tolerance		See note 3			3

Notes:

General Comment: For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Defined from 10% to 90% for rise time and 90% to 10% for fall time.
2. Source jitter specified by the "TX eye diagram pattern template" figure.
3. Receiver jitter specified by the "RX eye diagram pattern template" figure.

8.7.4.2 USB Interface Driver Waveforms

Figure 44: Low/Full Speed Data Signal Rise and Fall Time

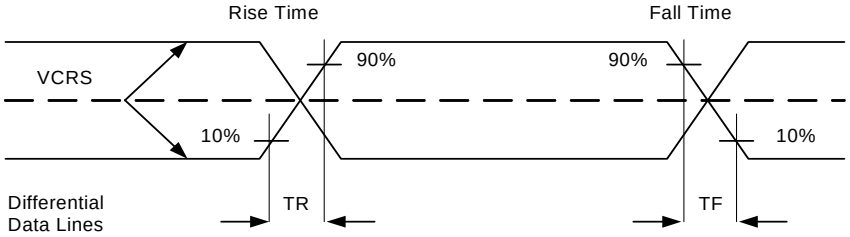


Figure 45: High Speed TX Eye Diagram Pattern Template

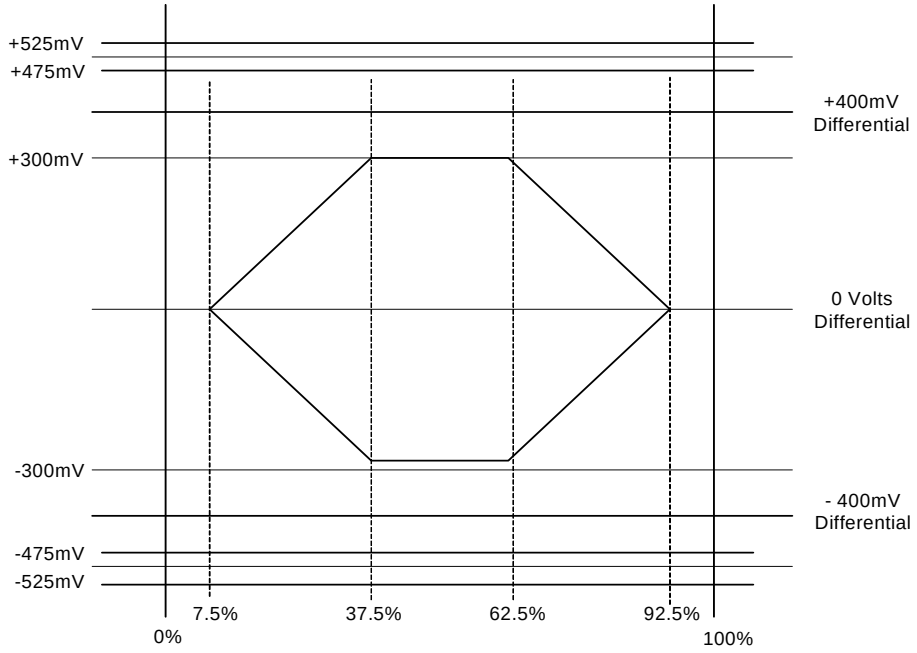
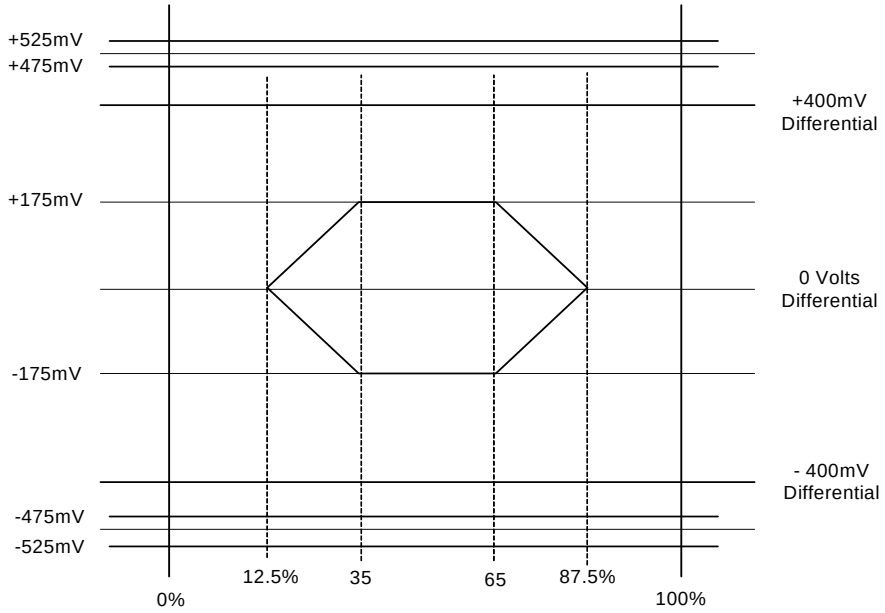


Figure 46: High Speed RX Eye Diagram Pattern Template



9 Thermal Data (Preliminary)

Table 72 provides the package thermal data for the device. This data is derived from simulations that were run according to the JEDEC standard.

Note The thermal parameters are preliminary and subject to change.

The documents listed below provide a basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell products. Before designing a system it is recommended to refer to these documents:

- Application Note, *AN-63 Thermal Management for Selected Marvell® Products,* Document Number MV-S300281-00
- White Paper, *ThetaJC, ThetaJA, and Temperature Calculations,* Document Number MV-S700019-00.

Table 72: Thermal Data for the 88F6281 in the BGA 19 x 19 mm Package (Preliminary)

Symbol	Definition	Airflow Value (C/W)		
		0[m/s]	1[m/s]	2[m/s]
θ_{JA}	Thermal resistance: junction to ambient.	20.2	18.7	18.1
Ψ_{JT}	Thermal characterization parameter: junction to case center.	7.0	7.0	7.1
θ_{JC}	Thermal resistance: junction to case (not air-flow dependent)	8.4		
Ψ_{JB}	Thermal characterization parameter: junction to the bottom of the package.	10.7	10.6	10.6
θ_{JB}	Thermal resistance: junction to the bottom of the package (not air-flow dependent)	10.9		

10 Package

This section provides the 88F6281 package drawing and dimensions.

Figure 47: HSBGA 288-pin Package and Dimensions

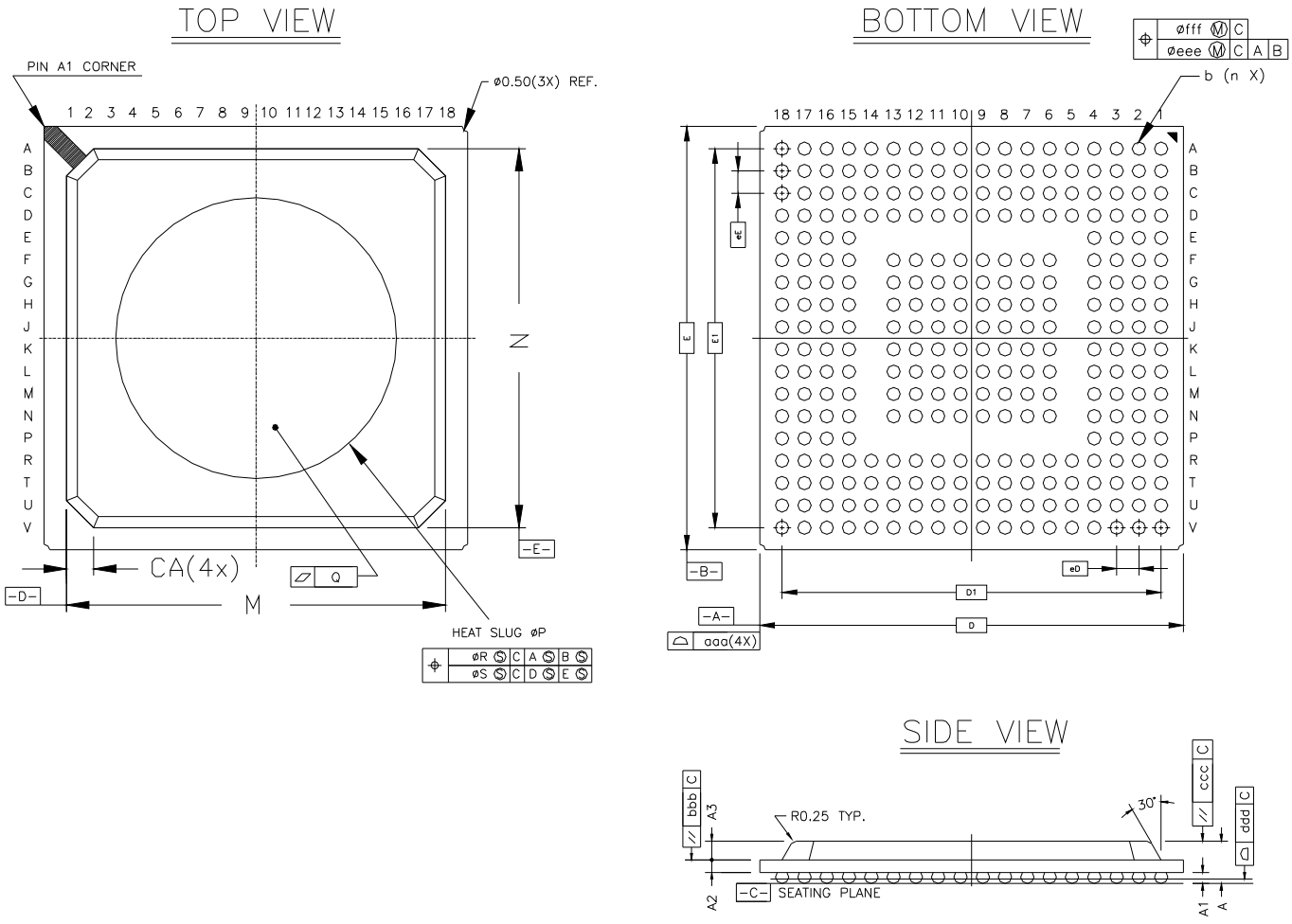


Table 73: HSBGA 288-pin Package Dimensions

		Symbol	Common Dimension (in millimeters)
Package			HSBGA
Body size	X	D	19.000
	Y	E	19.000
Ball pitch	X	eD	1.000
	Y	eE	1.000
Total thickness		A	1.910 ± 0.190
Mold thickness		A3	0.850 ref
Substrate thickness		A2	0.560 ref
Ball diameter			0.600
Standoff		A1	0.400 ~ 0.600
Ball width		b	0.500 ~ 0.700
Mold area	X	M	17.000
	Y	N	17.000
H/S exposed size		P	12.000 ~ 13.200
H/S flatness		Q	0.100
H/S shift with substrate edge		R	0.300
H/S shift with mold area		S	0.500
Chamfer		CA	1.215 ref
Package edge tolerance		aaa	0.200
Substrate flatness		bbb	0.250
Mold flatness		ccc	0.350
Copolarity		ddd	0.200
Ball offset (package)		eee	0.250
Ball offset (ball)		fff	0.100
Ball count		n	288
Edge ball center-to-center	X	D1	17.000
	Y	E1	17.000

11 Part Order Numbering/Package Marking

11.1 Part Order Numbering

Figure 48 shows the part order numbering scheme for the 88F6281. Refer to Marvell Field Application Engineers (FAEs) or representatives for further information when ordering parts.

Figure 48: Sample Part Number

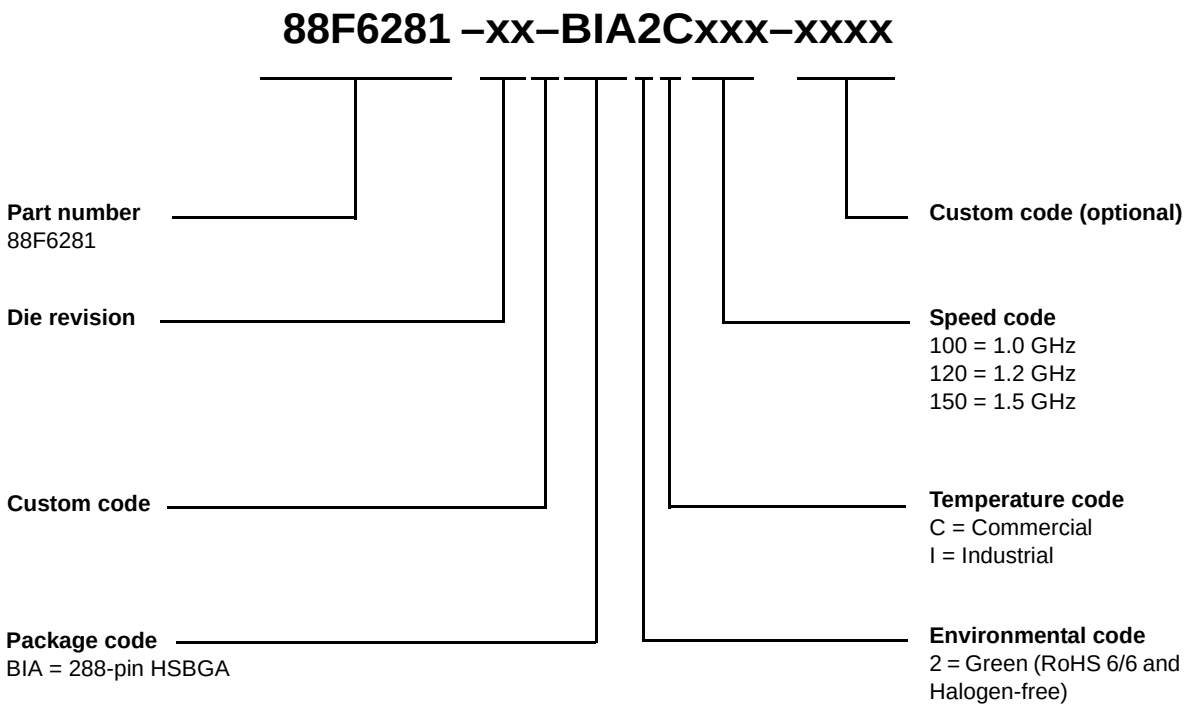


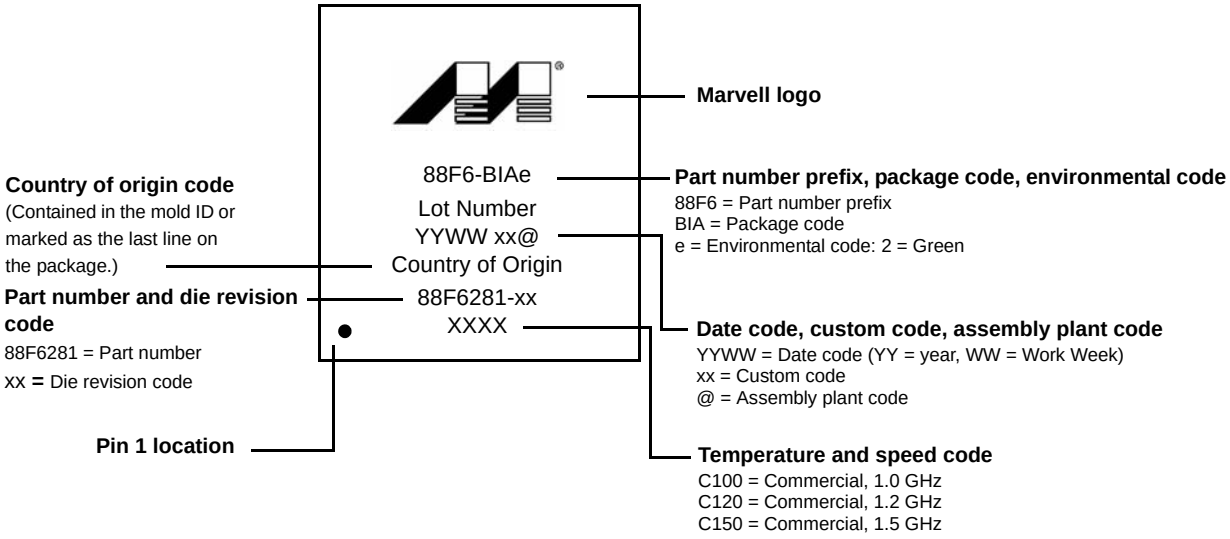
Table 74: 88F6281 Part Order Options

Package Type	Part Order Number
288-pin BGA	88F6281-xx-BIA2C100 (Green, RoHS 6/6 and Halogen-free package), 1.0 GHz
288-pin BGA	88F6281-xx-BIA2C120 (Green, RoHS 6/6 and Halogen-free package), 1.2 GHz
288-pin BGA	88F6281-xx-BIA2C150 (Green, RoHS 6/6 and Halogen-free package), 1.5 GHz

11.2 Package Marking

Figure 49 shows a sample Commercial package marking and pin 1 location for the 88F6281.

Figure 49: Commercial Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

A Revision History

Table 75: Revision History

Revision	Date	Comments
E	December 2, 2008	Revision
1. In Figure 1, 88F6281 Pin Logic Diagram, on page 18, changed the GE_TXCLKOUT pin to input/output and added a note under the figure, stating that the pin is an input when used the MII/MMII Transmit Clock.		
2. In Table 6, PCI Express Interface Pin Assignments, on page 26, revised the description of the PEX_CLK_P/N pins to state that they can be configured as input or output according to the reset strap.		
3. In Table 8, Gigabit Ethernet Port0/1 Interface Pin Assignments, on page 28, indicated that: • When the GE_TXCLKOUT pin is used as an MII/MMII Transmit Clock, it is an input pin. • When the MPP[29]/GE1[9] pin is used as a GMII Transmit Clock, it is a Tri-State output pin.		
4. In Table 12, RTC Interface Pin Assignments, on page 35, changed the type for RTC_XOUT to analog.		
5. In the description of signal AU_SPDFRMCLK in Table 17, Audio (S/PDIF / I^2S) Interface Signal Assignment, on page 40, added a reference to the new AU_SPDFRMCLK information in the Reference Clock AC Timing Specifications table.		
6. In Table 24, Unused Interface Strapping, on page 49, revise the description for configuring the PCI Express clock signals.		
7. At the end of Section 4.2, Gigabit Ethernet (GbE) Pins Multiplexing on MPP, on page 57, added a note stating that all relevant Gigabit Ethernet signals must be implemented.		
8. In the Table 32, Reset Configuration, on page 67, revised the configuration function for parameter CPU_CLK to DDR CLK Ratio.		
9. In Table 36, Recommended Operating Conditions, on page 77, for parameter RTC_AVDD Analog supply for RTC in Battery Back-up mode, revised the values for the minimum to 1.3V from 1.4V and for the maximum to 1.7V from 1.6V.		
10. In Table 37, Thermal Power Dissipation, on page 79: • For the Embedded CPU (VDD_CPU 1.1V) parameter changed the L2 cache frequency to 333 MHz. • for the eFuse during Burning mode parameter added a note: The eFuse burn is done once, and there should be no thermal effect, after it has been burned.		
11. In Table 38, Current Consumption, on page 80, for the Embedded CPU (VDD_CPU 1.1V) parameter changed the L2 cache frequency to 333 MHz.		
12. In Table 45, Reference Clock AC Timing Specifications, on page 86: • Revised the names of the Ethernet transmit symbols to $F_{GE\_TXCLK\_OUT}$, $DC_{GE\_TXCLK\_OUT}$, and $SR_{GE\_TXCLK\_OUT}$. • Added the S/PDIF Recovered Master Clock. • Added the Transport Stream External Reference Clock. • For the PTP Reference Clock, revised the values for the Frequency, Duty Cycle, and Pk-Pk jitter parameters.		
13. In Table 46, SDRAM DDR2 Interface AC Timing Table, on page 88, revised the minimum value for symbol tDHI to 0.70 ns from 0.72 ns.		
D	October 5, 2008	Revision
14. In Table 6, PCI Express Interface Pin Assignments, on page 26, revised the note in the description of the PEX_CLK_P/N pins.		
15. In Table 24, Unused Interface Strapping, on page 49, added the eFuse strapping.		
16. In Section 6.1.1, Power-Up Sequence Requirements, on page 63 and Section 6.1.2, Power-Down Sequence Requirements, on page 64, added a power up/down requirements for when VHV is in eFuse Burning mode.		

Table 75: Revision History (Continued)

Revision	Date	Comments
17. In Table 36, Recommended Operating Conditions, on page 77: • For VHV, revised the two parameters to *VHV (during eFuse Burning mode)* and *VHV (during eFuse Reading mode)* and added notes in the comments column for both VHV voltages. • For VDD_M, PEX_AVDD, and USB_AVDD, revised the comments column. • for RTC_AVDD, revised the values for minimum to 1.4V from 1.3V and for maximum to 1.6V from 1.7V.		
18. In Table 37, Thermal Power Dissipation, on page 79, revised the row for the SDRAM and added a row for the eFuse.		
19. In Table 38, Current Consumption, on page 80, revised the row for the SDRAM and added a row for the eFuse.		
20. In Table 45, Reference Clock AC Timing Specifications, on page 86: • For the CPU and Core Reference Clock frequency, revised the values. • For the PTP Reference Clock, added the Slew rate and Pk-Pk jitter parameters.		
C	August 18, 2008	Revision
1. Added the XOR engine to the block diagram in the Product Overview on page 3.		
2. Added *AN-249: Configuring the Marvell® SATA PHY to Transmit Predefined Test Patterns* to the list of Related Documentation on page 15.		
3. In Figure 1, 88F6281 Pin Logic Diagram, on page 18, added VHV, and MRn and changed PEX_CLK_P/N for input to input/output (I/O).		
4. In the pin map and pin list, revised pins F04 to MRn and G04 to VHV.		
5. In Table 3, Power Pin Assignments, on page 21: • Added VHV. • Changed the voltage for XTAL_AVDD from 2.5V to 1.8V. • Changed the voltage for SATA0_AVDD/SATA1_AVDD from 2.5V to 3.3V. • Revised the description of VDD_GE_A and VDD_GE_B to add additional information about RGMII.		
6. In Table 4, Miscellaneous Pin Assignments, on page 23, added the signal MRn.		
7. In Table 5, DDR SDRAM Interface Pin Assignments, on page 24, revised the description of M_NCASL and M_PCAL to indicate the range of the resistor.		
8. In Table 6, PCI Express Interface Pin Assignments, on page 26, changed PEX_CLK_P/N for input to input/output (I/O).		
9. Added present and active pins to Table 7, SATA Port Interface Pin Assignment, on page 27.		
10. In Section 1.2.6, Gigabit Ethernet Port Interface Pin Assignments, on page 28: • Added a note: For the TXCLK, use the GE_RXCLK pin. Also indicated which pins are for port0 and which for port1. • In Table 8, Gigabit Ethernet Port0/1 Interface Pin Assignments, on page 28, added a description for MII/MMII to the GE_TXD[3:0], GE_TXCTL, GE_RXCTL, GE_RXCLK, GE_RXD[3:0] rows. Also for pin MPP[30]/GE1[10] added a description for MII/MMII Receive Data Valid.		
11. In Table 17, Audio (S/PDIF / I^2S) Interface Signal Assignment, on page 40, revised the power rail to VDDO/VDD_GE_B.		
12. Revised Table 19, Secure Digital Input/Output (SDIO) Interface Signal Assignment, on page 42 to indicate the pins requiring pull up.		
13. Added Table 21, Transport Stream (TS) Interface Signal Assignment, on page 45.		
14. Added Section 1.2.20, Precise Timing Protocol (PTP) Interface, on page 47.		
15. In Table 23, Internal Pull-up and Pull-down Pins, on page 48, revised the pin numbers and changed pins GE_MDC, MPP[7] and MPP[18] from pull down to pull up and removed MPP[13], MPP[15], and MPP[17] from the table, since they do not require a pull up/down.		
16. In Table 2, Unused Interface Strapping, on page 49, revised the description of the strapping for the SATA0_AVDD/SATA1_AVDD pins.		

Table 75: Revision History (Continued)

Revision	Date	Comments
17. In Section 4.1, Multi-Purpose Pins Functional Summary, on page 51: • Changed all references to MPP[0] and MPP[11] from GPI to GPIO. • Changed the MPP[6] row in the table to remove the 0x0 option. • Added the following bullet at the end of the section, after the tables: When TWSI serial ROM initialization is enabled, MPP[8] and MPP[9] wake up as TWSI data and clock pins, respectively. • Revised the description of SYSRST_OUTn. • Added a bullet: Pin MPP[6] wakes up after reset in 0x1 mode (SYSRST_OUTn).		
18. In Table 27, Ethernet Ports Pins Multiplexing, on page 57, added a new configuration option for the Gigabit Ethernet ports: Port 0 MII/MMII, port 1 RGMII.		
19. In Section 4.3, TSMP (TS Multiplexing Pins) on MPP, on page 59, added to the description of the TSMP pins.		
20. Revised Table 29, 88F6281Clocks, on page 60 and Table 30, Supported Clock Combinations, on page 61.		
21. Revised Section 5.1, Spread Spectrum Clock Generator (SSCG), on page 62.		
22. In Section 6.2, Hardware Reset, on page 64, added SYSRST_OUTn to the list of pins that are still active during SYSRSTn assertion.		
23. Revised Section 6.2.1, Reset Out Signal, on page 65 and Section 6.2.3, SYSRSTn Duration Counter, on page 65 and added Section 6.2.2, Power On Reset (POR), on page 65.		
24. In Section 6.3.2, PCI Express Endpoint Reset, on page 66 revised the bulleted items.		
25. Revised Section 6.5, Pins Sample Configuration, on page 66.		
26. Made major revisions to Table 32, Reset Configuration, on page 67.		
27. Revised the first two paragraphs in Section 6.6, Serial ROM Initialization, on page 70.		
28. In Section 6.7, Boot Sequence, on page 71 revised the paragraph following step 4.		
29. Revised Table 45, Reference Clock AC Timing Specifications, on page 86.		
30. In Table 34, IDCODE Register Map, on page 74, revised the description of bits [31:28].		
31. In Table 35, Absolute Maximum Ratings, on page 75: • Added VHV. • Revised the voltage for the SATA and XTAL AVDD parameters.		
32. In the Table 36, Recommended Operating Conditions, on page 77: • Added values for VDD_CPU. • Added VHV and revised the voltage for the SATA and XTAL AVDD parameters. • For the 3.3V interfaces, revised the minimum value to 3.15V and the maximum value to 3.45V (+/-5%). • Revised the description of the VDD_GE_A/VDD_GE_B row, to show that RGMII can also operate with a voltage of 3.3V. • Revised the values for PEX_AVDD to minimum 1.7V, typical 1.8V, and maximum 1.9V.		
33. In Table 37, Thermal Power Dissipation, on page 79 • Revised values for Core, Embedded CPU, PCI Express, USB and SATA parameters. • Changed all occurrences of VDD_CPU to VDD. • Added the row RGMII 3.3V interface. • Revised the notes following the table, to remove reference to the trace length or resistance.		
34. In Table 38, Current Consumption, on page 80 • Revised values for Core, Embedded CPU, SATA, PCI Express and USB parameters. • Changed all occurrences of VDD_CPU to VDD. • Revised the interface *RGMII 1.8V interface* to *RGMII 1.8V or 3.3V interface.* • Revised the notes following the table to remove reference to the trace length or resistance.		
35. Deleted Section 8.5.2 REF_CLK_XIN 2.5V (CMOS) DC Electrical Specifications and added pin REF_CLK_XIN to Section 8.5.2, RGMII, SMI and REF_CLK_XIN 1.8V (CMOS) DC Electrical Specifications, on page 82, since the power rail for the REF_CLK_XIN pin was changed from 2.5V to 1.8V.		
36. In Section 8.5.1, General 3.3V (CMOS) DC Electrical Specifications, on page 81, added reference to PTP and RGMII.		
37. Revised Table 64, PCI Express Interface Differential Reference Clock Characteristics, on page 118 and Table 65, PCI Express Interface Spread Spectrum Requirements, on page 119.		

Table 75: Revision History (Continued)

Revision	Date	Comments
		38. Revised Figure 25, TWSI Output Delay AC Timing Diagram, on page 104 so that it shows SDA t_{OV} relative to the SCK falling edge, as shown in the two tables that proceed the figure. 39. In Table 73, HSBGA 288-pin Package Dimensions, on page 131, changed the maximum value for the parameter *H/S exposed size* to 13.200 mm. 40. Revised all of Section 11, Part Order Numbering/Package Marking, on page 132.
B	April 8, 2008	Revision
		1. In the features list: • Added the bullets Precise Timing Protocol (PTP) and Audio Video Bridging networks. • Added the functional block diagram and the usage model diagram. 2. Throughout this specification, LVCMOS and LVTTL were changed to CMOS. 3. In Figure 1, 88F6281 Pin Logic Diagram, on page 18 revised the power pins and removed the interfaces that are multiplexed on the MPP pins. 4. Revised Table 1, Pin Functions and Assignments Table Key, on page 19 to show only terms relevant for this device. 5. In Table 3, Power Pin Assignments, on page 21, added pins SSCG_AVDD and SSCG_AVSS and added the SMI interface at 1.8V and the MII/MMII interface at 3.3V to the description of the interfaces supported by pin VDD_GE_A. 6. In Table 8, Gigabit Ethernet Port0/1 Interface Pin Assignments, on page 28, removed pins GE_MDC and GE_MDIO. 7. Added Section 1.2.7, Serial Management Interface (SMI) Interface Pin Assignments, on page 32, with a description of the GE_MDC and GE_MDIO pins. 8. In Table 12, RTC Interface Pin Assignments, on page 35, changed the pin type for RTC_XIN to analog from CMOS. 9. In Table 15, Two-Wire Serial Interface (TWSI) Interface Pin Assignment, on page 38, changed the note to: Requires a pull-up resistor to VDDO. 10. Added Section 2, Unused Interface Strapping, on page 49. 11. In Table 29, 88F6281Clocks, on page 60, revised the description of CPU PLL to mention SSCG. 12. Added Section 5.1, Spread Spectrum Clock Generator (SSCG), on page 62. 13. Added Section 6.1, Power-Up/Down Sequence Requirements, on page 63 and revised the title of Section 6 to reflect this change. 14. In Section 6.4, Sheeva™ CPU TAP Controller Reset, on page 66, revised the note referring to sample at reset and added the note: If a signal is pulled up on the board, it must be pulled to the proper voltage level. Certain reset configuration pins are powered by VDD_GE_A and VDD_GE_B. Those pins have multiple voltage options (see Table 36, Recommended Operating Conditions, on page 77). 15. In Table 35, Absolute Maximum Ratings, on page 75 and Table 36, Recommended Operating Conditions, on page 77, added the parameter SSCG_VDD. 16. In Table 37, Thermal Power Dissipation, on page 79 added the following: The purpose of the Thermal Power Dissipation table is to support system engineering in thermal design. 17. In Table 38, Current Consumption, on page 80 added the following: The purpose of the Current Consumption table is to support board power design and power module selection. 18. In Table 45, Reference Clock AC Timing Specifications, on page 86: • Revised the symbols for the Transport Stream (TS) output and input mode reference clocks. • Revised the symbols for the SMI master mode reference clock. • Revised the symbols for the TWSI master mode reference clock. • Revised the description for symbol F_{RTC_XIN}. • Removed the RGMII, GMII, MII 100 Mbps, and MII 10 Mbps rows, since they are not relevant to this device. 19. In Table 67, SATA-I Interface Gen1i Mode Driver and Receiver Characteristics, on page 123, added driver and receiver return loss parameters, according to updated standard.
A	January 28, 2008	Initial release

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