Reconfigurable I/O

NI 781*x*R User Manual

Reconfigurable I/O Devices for PCI and PXI/CompactPCI Bus Computers

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Depending on where it is operated, this Class A product could be subject to restrictions in the FCC rules. (In Canada, the Department of Communications (DOC), of Industry Canada, regulates wireless interference in much the same way.) Digital electronics emit weak signals during normal operation that can affect radio, television, or other wireless products.

All Class A products display a simple warning statement of one paragraph in length regarding interference and undesired operation. The FCC rules have restrictions regarding the locations where FCC Class A products can be operated.

Consult the FCC Web site at `www.fcc.gov` for more information.

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This equipment generates and uses radio frequency energy and, if not installed and used in strict accordance with the instructions in this manual and the CE marking Declaration of Conformity*, may cause interference to radio and television reception. Classification requirements are the same for the Federal Communications Commission (FCC) and the Canadian Department of Communications (DOC).

Changes or modifications not expressly approved by NI could void the user's authority to operate the equipment under the FCC Rules.

Class A

Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user is required to correct the interference at their own expense.

Canadian Department of Communications

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe A respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

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* The CE marking Declaration of Conformity contains important supplementary information and instructions for the user or installer.

Contents

About This Manual

This manual describes the electrical and mechanical aspects of the National Instruments 781*x*R devices, and contains information about programming and using the devices.

Conventions

The following conventions appear in this manual:

<> — Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, AO <3..0>.

» — The » symbol leads you through nested menu items and dialog box options to a final action. The sequence **File»Page Setup»Options** directs you to pull down the **File** menu, select the **Page Setup** item, and select **Options** from the last dialog box.

 — This icon denotes a note, which alerts you to important information.

 — This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on the device, refer to the *Safety Information* section of Chapter 1, *Introduction*, for precautions to take.

bold — Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names and hardware labels.

italic — Italic text denotes variables, emphasis, a cross-reference, or an introduction to a key concept. Italic text also denotes text that is a placeholder for a word or value that you must supply.

`monospace`	Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames, and extensions.
NI 781*x*R	NI 781*x*R refers to all R Series devices with digital I/O.

Reconfigurable I/O Documentation

The *NI 781xR User Manual* is one piece of the documentation set for your reconfigurable I/O system and application. Depending on the hardware and software you use for your application, you could have any of several types of documentation. The documentation set includes the following documents:

- *Getting Started with the NI 781xR*—This document lists what you need to get started, describes how to unpack and install the software and hardware, and contains information about connecting I/O signals to the NI 781*x*R.
- *LabVIEW FPGA Module Release and Upgrade Notes*—This document contains information about installing and getting started with the LabVIEW FPGA Module. Select **Start»Program Files» National Instruments»<LabVIEW>»LabVIEW Manuals** to view the LabVIEW Manuals directory that contains this document.
- *LabVIEW Help*—Select **Help»Search the LabVIEW Help** in LabVIEW to view the *LabVIEW Help*. This help file contains information about using VIs with the NI 781*x*R and using the LabVIEW FPGA Module and the LabVIEW Real-Time Module.
  - Browse the **FPGA Module** book in the **Contents** tab for information about how to use the FPGA Module to create VIs that run on the NI 781*x*R device.
  - Browse the **Real-Time Module** book in the **Contents** tab for information about how to build deterministic applications using the LabVIEW Real-Time Module.

Related Documentation

The following documents contain information you may find helpful:

- *PICMG CompactPCI 2.0 R3.0*
- *PXI Hardware Specification Revision 2.1*
- *PXI Software Specification Revision 2.1*
- *PCI Specification Revision 3.0*

1 Introduction

This chapter describes the NI 781*x*R, the concept of the Reconfigurable I/O (RIO) device, optional software and equipment for using the NI 781*x*R, and safety information about the NI 781*x*R.

About the Reconfigurable I/O Devices

The NI 781*x*R devices are R Series RIO devices with 160 digital I/O (DIO) lines and four DIO connectors.

- The NI 7811R has a one million gate Field-Programmable Gate Array (FPGA).
- The NI 7813R has a three million gate FPGA.

A user-reconfigurable FPGA controls the digital I/O lines on the NI 781*x*R. The FPGA on the R Series device allows you to define the functionality and timing of the device. You can change the functionality of the FPGA on the R Series device in LabVIEW using the LabVIEW FPGA Module to create and download a custom virtual instrument (VI) to the FPGA. Using the FPGA Module, you can graphically design the timing and functionality of the R Series device. If you have LabVIEW but not the FPGA Module, you cannot create new FPGA VIs, but you can create VIs that run on Windows or on a LabVIEW Real-Time (RT) target to control existing FPGA VIs.

Some applications require tasks such as real-time, floating-point processing, or datalogging while performing I/O and logic on the R Series device. You can use the LabVIEW Real-Time Module to perform these additional applications while communicating with and controlling the R Series device.

The R Series device contains flash memory to store a startup VI for automatic loading of the FPGA when the system is powered on.

The NI 781*x*R uses the Real-Time System Integration (RTSI) bus to easily synchronize several measurement functions to a common trigger or timing event. The NI 781*x*R accesses the RTSI bus through the PXI trigger lines implemented on the PXI backplane. The RTSI bus can route timing and trigger signals between as many as seven PXI devices in your system.

You can add additional I/O channels and signal conditioning using the CompactRIO R Series Expansion Chassis and CompactRIO I/O modules.

Refer to Appendix A, *Specifications*, for detailed NI 781*x*R specifications.

Using PXI with CompactPCI

Using PXI-compatible products with standard CompactPCI products is an important feature provided by *PXI Hardware Specification Revision 2.1* and *PXI Software Specification Revision 2.1*. If you use a PXI-compatible plug-in card in a standard CompactPCI chassis, you cannot use PXI-specific functions, but you still can use the basic plug-in card functions. For example, the RTSI bus on the R Series device is available in a PXI chassis, but not in a CompactPCI chassis.

The CompactPCI specification permits vendors to develop sub-buses that coexist with the basic PCI interface on the CompactPCI bus. Compatible operation is not guaranteed between CompactPCI devices with different sub-buses nor between CompactPCI devices with sub-buses and PXI. The standard implementation for CompactPCI does not include these sub-buses. The R Series device works in any standard CompactPCI chassis adhering to the *PICMG CompactPCI 2.0 R3.0* core specification.

PXI-specific features are implemented on the J2 connector of the CompactPCI bus. Table 1-1 lists the J2 pins used by the NI PXI-781*x*R. The NI PXI-781*x*R is compatible with any CompactPCI chassis with a sub-bus that does not drive these lines. Even if the sub-bus is capable of driving these lines, the R Series device is still compatible as long as those pins on the sub-bus are disabled by default and are never enabled.

Caution Damage can result if the J2 lines are driven by the sub-bus.

Table 1-1. Pins Used by the NI PXI-781*x*R

NI PXI-781*x*R Signal	PXI Pin Name	PXI J2 Pin Number
PXI Trigger<0..7>	PXI Trigger<0..7>	A16, A17, A18, B16, B18, C18, E16, E18
PXI Clock 10 MHz	PXI Clock 10 MHz	E17
PXI Star Trigger	PXI Star Trigger	D17
LBLSTAR<0..12>	LBL<0..12>	A1, A19, C1, C19, C20, D1, D2, D15, D19, E1, E2, E19, E20
LBR<0..12>	LBR<0..12>	A2, A3, A20, A21, B2, B20, C3, C21, D3, D21, E3, E15, E21

Overview of Reconfigurable I/O

This section explains reconfigurable I/O and describes how to use the LabVIEW FPGA Module to build high-level functions in hardware.

Refer to Chapter 2, *Hardware Overview of the NI 781xR*, for descriptions of the I/O resources on the NI 781*x*R.

Reconfigurable I/O Concept

The NI 781*x*R is based on a reconfigurable FPGA core surrounded by fixed digital input and output resources. You can configure the behavior of the FPGA to meet the requirements of your measurement and control system. You can implement this user-defined behavior as an FPGA VI to create an application-specific I/O device.

Flexible Functionality

Flexible functionality allows the NI 781*x*R to match individual application requirements and to mimic the functionality of fixed I/O devices. For example, you can configure an R Series device in one application for three 32-bit quadrature encoders and then reconfigure the R Series device in another application for eight 16-bit event counters.

You also can use the R Series device with the LabVIEW Real-Time Module in timing and triggering applications, such as control and hardware-in-the-loop (HIL) simulations. For example, you can configure the R Series device for a single timed loop in one application and then reconfigure the device in another application for four independent timed loops with separate I/O resources.

User-Defined I/O Resources

You can create your own custom measurements using the fixed I/O resources. For example, one application might require an event counter that increments when a rising edge appears on any of three digital input lines. You can implement these behaviors in the hardware for fast, deterministic performance.

Device-Embedded Logic and Processing

You can implement LabVIEW logic and processing on the FPGA of the R Series device. Typical logic functions include Boolean operations, comparisons, and basic mathematical operations. You can implement multiple functions efficiently in the same design, operating sequentially or in parallel. You also can implement more complex algorithms such as control loops. You are limited only by the size of the FPGA.

Reconfigurable I/O Architecture

Figure 1-1 shows an FPGA connected to fixed I/O resources and a bus interface.

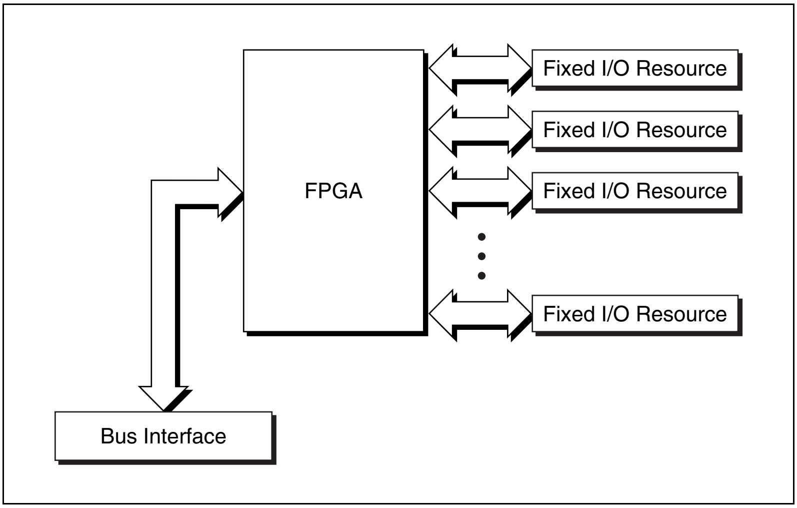

Figure 1-1. High-Level FPGA Functional Overview

Software accesses the R Series device through the bus interface. The FPGA connects the bus interface and the fixed I/O to make possible timing, triggering, processing, and custom I/O measurements using the LabVIEW FPGA Module.

The FPGA logic provides timing, triggering, processing, and custom I/O measurements. Each fixed I/O resource used by the application uses a small portion of the FPGA logic that controls the fixed I/O resource. The bus interface also uses a small portion of the FPGA logic to provide software access to the device.

The remaining FPGA logic is available for higher-level functions such as timing, triggering, and counting. The functions use varied amounts of logic.

You can place useful applications in the FPGA. How much FPGA space your application requires depends on your need for I/O recovery, I/O, and logic algorithms.

The FPGA does not retain the VI when the R Series device is powered off, so you must reload the VI every time you power on the device. You can load the VI from onboard flash memory or from software over the bus interface. One advantage to using flash memory is that the VI can start executing almost immediately after power-up instead of waiting for the computer to completely boot and load the FPGA VI. Refer to the *LabVIEW Help* for more information about how to store your VI in flash memory.

Reconfigurable I/O Applications

You can use the LabVIEW FPGA Module to create or acquire new VIs for your application. The FPGA Module allows you to define custom functionality for the R Series device using a subset of LabVIEW functionality. Refer to the R Series examples, located in the `<LabVIEW>\examples\R Series` directory, for examples of FPGA VIs.

Software Development

You can use LabVIEW with the LabVIEW FPGA Module to program the NI 781*x*R. To develop real-time applications that control the NI 781*x*R, use LabVIEW with the LabVIEW Real-Time Module.

LabVIEW FPGA Module

The LabVIEW FPGA Module enables you to use LabVIEW to create VIs that run on the FPGA of the R Series device. Use the FPGA Module VIs and functions to control the I/O, timing, and logic of the R Series device and generate interrupts for synchronization. Select **Help»Search the LabVIEW Help** to view the *LabVIEW Help*. In the *LabVIEW Help*, use the **Contents** tab to browse to the **FPGA Interface** book for more information about the FPGA Interface functions.

You can use Interactive Front Panel Communication to communicate directly with the FPGA VI running on the FPGA target. You can use Programmatic FPGA Interface Communication to programmatically monitor and control an FPGA VI with a separate host VI.

Use the FPGA Interface functions when you target LabVIEW for Windows or an RT target to create host VIs that wait for interrupts and control the FPGA by reading and writing to the FPGA VI running on the R Series device.

Note If you use the R Series device without the FPGA Module, you can use the RIO Device Setup utility, available by selecting **Start»Program Files»National Instruments» NI-RIO»RIO Device Setup**, to download precompiled FPGA VIs to the flash memory of the R Series device. This utility is installed by the NI-RIO CD. You also can use the utility to synchronize the clock R Series device to the PXI clock, and to configure when the VI loads from flash memory.

LabVIEW Real-Time Module

The LabVIEW Real-Time Module extends the LabVIEW development environment to deliver deterministic, real-time performance.

You can write host VIs that run in Windows or on RT targets to communicate with FPGA VIs that run on the NI 781*x*R.You can develop real-time VIs with LabVIEW and the LabVIEW Real-Time Module and then download the Real-Time VIs to run on a hardware target with a real-time operating system. The LabVIEW Real-Time Module allows you to use the NI 781*x*R in RT Series PXI systems being controlled in real time by a VI.

The NI 781*x*R is designed as a single-point DIO complement to the LabVIEW Real-Time Module. Refer to the *LabVIEW Help*, available by selecting **Help»Search the LabVIEW Help**, for more information about the LabVIEW Real-Time Module.

Cables and Optional Equipment

National Instruments offers a variety of products you can use with R Series devices, including cables, connector blocks, and other accessories listed in Table 1-2.

Table 1-2. Cables and Accessories

Cable	Cable Description	Accessories
SH68-C68-S	Shielded 68-pin VHDCI male connector to female 0.050 series D-type connector. The cable is constructed with 34 twisted wire pairs plus an overall shield.	Connects to the following standard 68-pin screw-terminal blocks: • SCB-68 • CB-68LP • CB-68LPR • TBX-68 • cRIO-9151—passive backplane
NSC68-5050	Unshielded cable connects from 68-pin VHDCI male connector to two 50-pin female headers. The pinout of these headers allows for direct connection to SSR backplanes for digital signal conditioning.	50-pin headers can connect to the following SSR backplanes for digital signal conditioning: • 8-channel backplane • 16-channel backplane • 32-channel backplane

Refer to Appendix B, *Connecting I/O Signals*, for more information about using these cables and accessories to connect I/O signals to the NI 781*x*R. Refer to `ni.com/products` or contact the sales office nearest to you for the most current cabling options.

Custom Cabling

NI offers a variety of cables for connecting signals to the NI 781*x*R. If you need to develop a custom cable, a generic unterminated shielded cable is available from NI. The SHC68-NT-S connects to the NI 781*x*R VHDCI connectors on one end of the cable. The other end of the cable is not terminated. This cable ships with a wire list identifying which wire corresponds to each NI 781*x*R pin. Using this cable, you can quickly connect the NI 781*x*R signals that you need to the connector of your choice. Refer to Appendix B, *Connecting I/O Signals*, for the NI 781*x*R connector pinouts.

Safety Information

The following section contains important safety information that you *must* follow when installing and using the NI 781*x*R.

Do *not* operate the NI 781*x*R in a manner not specified in this document. Misuse of the NI 781*x*R can result in a hazard. You can compromise the safety protection built into the NI 781*x*R if the NI 781*x*R is damaged in any way. If the NI 781*x*R is damaged, return it to NI for repair.

Do *not* substitute parts or modify the NI 781*x*R except as described in this document. Use the NI 781*x*R only with the chassis, modules, accessories, and cables specified in the installation instructions. You *must* have all covers and filler panels installed during operation of the NI 781*x*R.

Do *not* operate the NI 781*x*R in an explosive atmosphere or where there might be flammable gases or fumes. If you must operate the NI 781*x*R in such an environment, it must be in a suitably rated enclosure.

If you need to clean the NI 781*x*R, use a soft, nonmetallic brush. Make sure that the NI 781*x*R is completely dry and free from contaminants before returning it to service.

Operate the NI 781*x*R only at or below Pollution Degree 2. Pollution is foreign matter in a solid, liquid, or gaseous state that can reduce dielectric strength or surface resistivity. The following list describes pollution degrees:

- **Pollution Degree 1**—No pollution or only dry, nonconductive pollution occurs. The pollution has no influence.
- **Pollution Degree 2**—Only nonconductive pollution occurs in most cases. Occasionally, however, a temporary conductivity caused by condensation must be expected.
- **Pollution Degree 3**—Conductive pollution occurs, or dry, nonconductive pollution occurs that becomes conductive due to condensation.

You *must* insulate signal connections for the maximum voltage for which the NI 781*x*R is rated. Do *not* exceed the maximum ratings for the NI 781*x*R. Do not install wiring while the NI 781*x*R is live with electrical signals. Do not remove or add connector blocks when power is connected to the system. Remove power from signal lines before connecting them to or disconnecting them from the NI 781*x*R.

Operate the NI 781*x*R at or below the *measurement category*[1] listed in the *Environmental* section of Appendix A, *Specifications*. Measurement circuits are subjected to *working voltages*[2] and transient stresses (overvoltage) from the circuit to which they are connected during measurement or test. Measurement categories establish standard impulse withstand voltage levels that commonly occur in electrical distribution systems. The following list describes installation categories:

- **Measurement Category I**—Measurements performed on circuits not directly connected to the electrical distribution system referred to as MAINS[3] voltage. This category is for measurements of voltages from specially protected secondary circuits. Such voltage measurements include signal levels, special equipment, limited-energy parts of equipment, circuits powered by regulated low-voltage sources, and electronics.
- **Measurement Category II**—Measurements performed on circuits directly connected to the electrical distribution system. This category refers to local-level electrical distribution, such as that provided by a standard wall outlet (for example, 115 V for U.S. or 230 V for Europe). Examples of Measurement Category II are measurements performed on household appliances, portable tools, and similar products.
- **Measurement Category III**—Measurements performed in the building installation at the distribution level. This category refers to measurements on hard-wired equipment such as equipment in fixed installations, distribution boards, and circuit breakers. Other examples are wiring, including cables, bus-bars, junction boxes, switches, socket-outlets in the fixed installation, and stationary motors with permanent connections to fixed installations.
- **Measurement Category IV**—Measurements performed at the primary electrical supply installation (<1,000 V). Examples include electricity meters and measurements on primary overcurrent protection devices and on ripple control units.

[1] Measurement categories, also referred to as *installation categories*, are defined in electrical safety standard IEC 61010-1.

[2] Working voltage is the highest rms value of an AC or DC voltage that can occur across any particular insulation.

[3] MAINS is defined as a hazardous live electrical supply system that powers equipment. Suitably rated measuring circuits may be connected to the MAINS for measuring purposes.

2

Hardware Overview of the NI 781*x*R

This chapter presents an overview of the hardware functions and I/O connectors on the NI 781*x*R.

Figure 2-1 shows a block diagram for the NI 781*x*R.

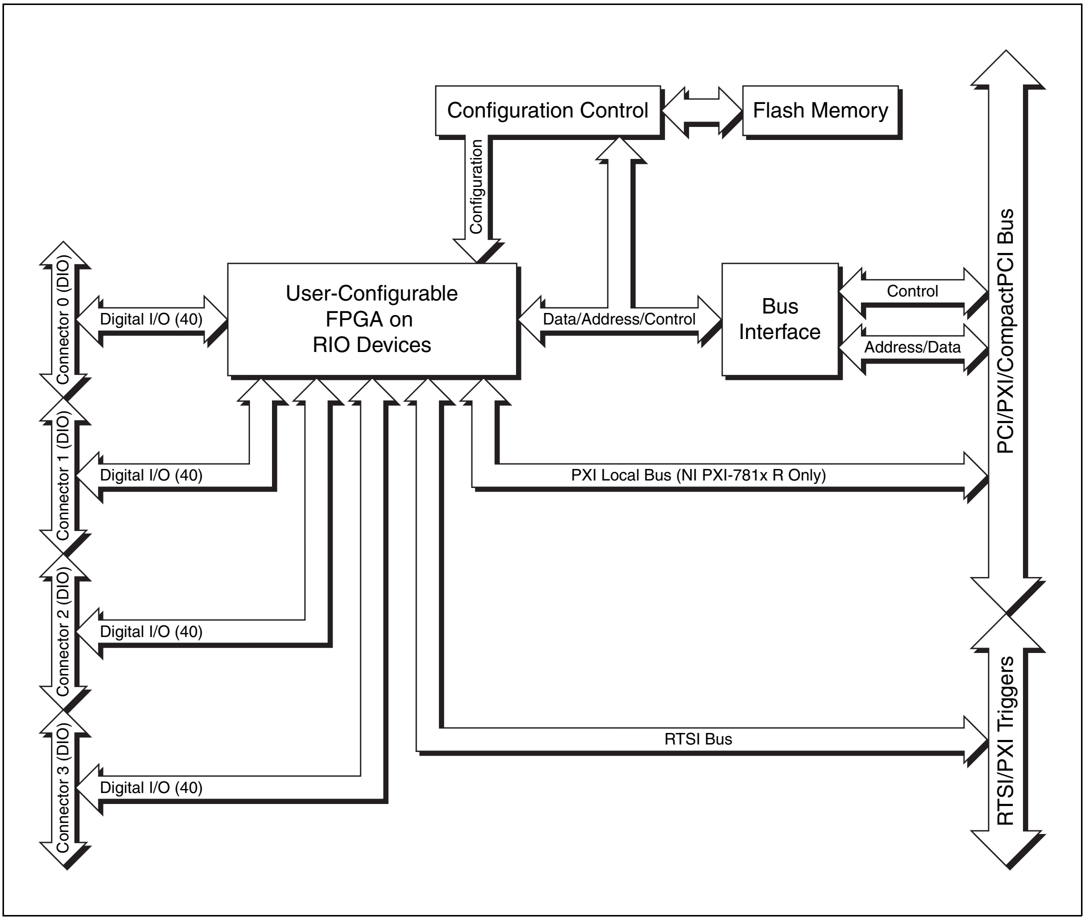

Figure 2-1. NI 781*x*R Block Diagram

NI 7811R Overview

The NI 7811R has 160 bidirectional DIO lines and a one million gate FPGA.

NI 7813R Overview

The NI 7813R has 160 bidirectional DIO lines and a three million gate FPGA.

Digital I/O

You can configure the NI 781*x*R DIO lines individually for either input or output. When the system powers on, the DIO lines are all high-impedance. To set another power-on state, you can configure the NI 781*x*R to load a VI when the system powers on. This VI then can then set the DIO lines to any power-on state.

Connecting Digital I/O Signals

The DIO signals on the NI 781*x*R connectors are DGND and DIO<0..39>. DIO<0..*n*> signals make up the DIO port, and DGND is the ground reference signal for the DIO port. The NI 781*x*R has four DIO connectors for a total of 160 DIO lines.

Refer to Figure B-1, *NI 781xR Connector Locations*, and Figure B-2, *NI 781xR I/O Connector Pin Assignments*, for the connector locations and the I/O connector pin assignments on the NI 781*x*R.

The DIO lines on the NI 781*x*R are TTL compatible. When configured as inputs, they can receive signals from 5 V TTL, 3.3 V LVTTL, 5 V CMOS, and 3.3 V LVCMOS devices. When configured as outputs, they can send signals to 5 V TTL, 3.3 V LVTTL, and 3.3 V LVCMOS devices. Because the digital outputs provide a nominal output swing of 0 to 3.3 V (3.3 V TTL), the DIO lines cannot drive 5 V CMOS logic levels. To interface to 5 V CMOS devices, you must provide an external pull-up resistor to 5 V. This resistor pulls up the 3.3 V digital output from the NI 781*x*R to 5 V CMOS logic levels. Refer to Appendix A, *Specifications*, for detailed DIO specifications.

Caution Exceeding the maximum input voltage ratings listed in Table B-2, *NI 781xR I/O Signal Summary*, can damage the NI 781*x*R and the computer. NI is *not* liable for any damage resulting from such signal connections.

Caution Do *not* short the DIO lines of the NI 781*x*R directly to power or to ground. Doing so can damage the NI 781*x*R by causing excessive current to flow through the DIO lines.

You can connect multiple NI 781*x*R digital output lines in parallel to provide higher current sourcing or sinking capability. If you connect multiple digital output lines in parallel, your application must drive all of these lines simultaneously to the same value. If you connect digital lines together and drive them to different values, excessive current can flow through the DIO lines and damage the NI 781*x*R. Refer to Appendix A, *Specifications*, for more information about DIO specifications. Figure 2-2 shows signal connections for three typical DIO applications.

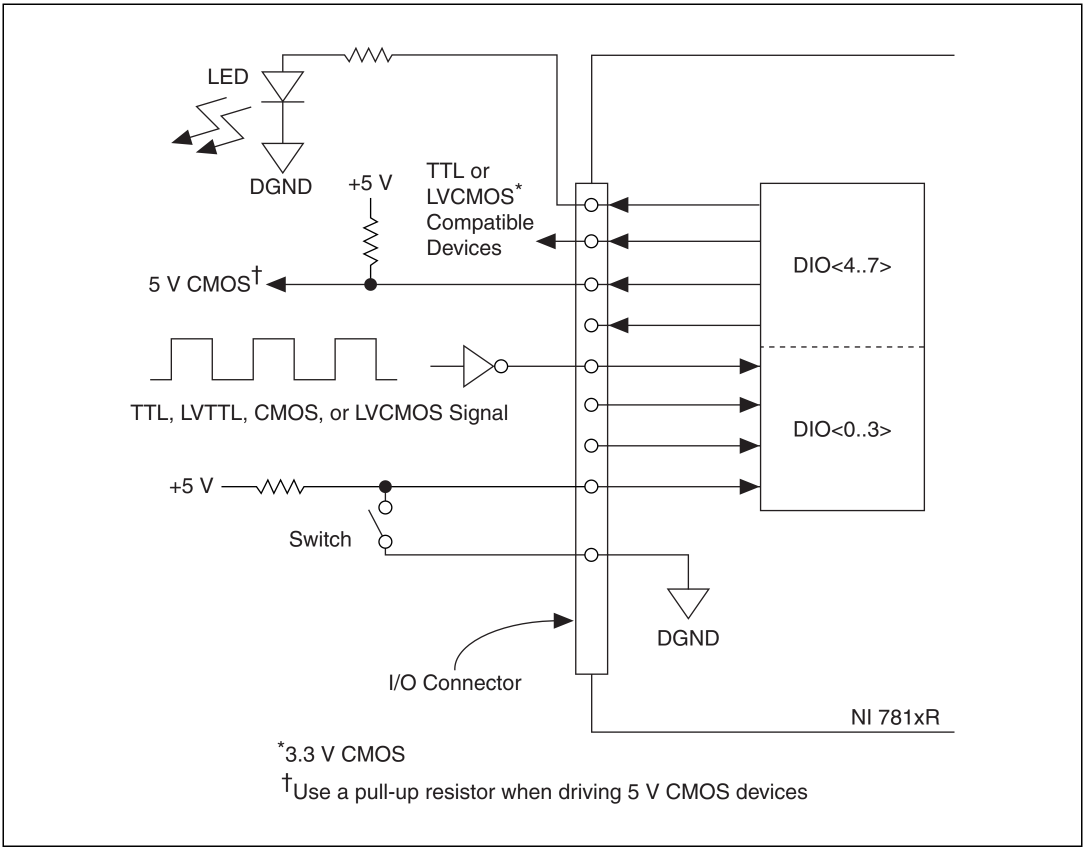

Figure 2-2. Example Digital I/O Connections

Figure 2-2 shows DIO<0..3> configured for digital input and DIO<4..7> configured for digital output. Digital input applications include receiving TTL, LVTTL, CMOS, or LVCMOS signals and sensing external device states, such as the state of the switch shown in Figure 2-2. Digital output applications include sending TTL or LVCMOS signals and driving external devices, such as the LED shown in Figure 2-2.

The NI 781*x*R SH68-C68-S shielded cable contains 34 twisted pairs of conductors. To maximize the digital I/O available on the NI 781*x*R, some of the DIO lines are twisted with power or ground, and some DIO lines are twisted with other DIO lines. To obtain maximum signal integrity, place edge-sensitive or high-frequency digital signals on the DIO lines that are paired with power or ground. Because the DIO lines that are twisted with other DIO lines can couple noise onto each other, use these lines for static signals or for non-edge-sensitive, low-frequency digital signals. Examples of high-frequency or edge-sensitive signals include clock, trigger, pulse-width modulation (PWM), encoder, and counter signals. Examples of static signals or non-edge-sensitive, low-frequency signals include LEDs, switches, and relays. Table 2-1 summarizes these guidelines.

Table 2-1. DIO Signal Guidelines for the NI PXI-781*x*R

Digital Lines	SH68-C68-S Shielded Cable Signal Pairing	Recommended Types of Digital Signals
DIO<0..27>	DIO line paired with power or ground	All types—high-frequency or low-frequency signals, edge-sensitive or non-edge-sensitive signals
DIO<28..39>	DIO line paired with another DIO line	Static signals or non-edge-sensitive, low-frequency signals

RTSI Trigger Bus

The NI 781*x*R can send and receive triggers through the RTSI trigger bus. The RTSI bus provides eight shared trigger lines that connect to all the devices on the bus. In PXI, the trigger lines are shared between all the PXI slots in a bus segment. In PCI, the RTSI bus is implemented through a ribbon cable connected to the RTSI connector on each device that needs to access the RTSI bus.

You can use the RTSI trigger lines to synchronize the NI 781*x*R to any other device that supports RTSI triggers. On the NI PCI-781*x*R, the RTSI trigger lines are labeled RTSI/TRIG<0..6> and RTSI/OSC. On the NI PXI-781*x*R, the RTSI trigger lines are labeled PXI/TRIG<0..7>. In addition, the NI PXI-781*x*R can use the PXI star trigger line to send or receive triggers from a device plugged into Slot 2 of the PXI chassis. The PXI star trigger line on the NI PXI-781*x*R is PXI/STAR.

The NI 781*x*R can configure each RTSI trigger line as either an input or an output signal. Because each trigger line on the RTSI bus is connected in parallel to all the other RTSI devices on the bus, only one device should drive a particular RTSI trigger line at a time. For example, if one NI PXI-781*x*R is configured to send out a trigger pulse on PXI/TRIG0, the remaining devices on that PXI bus segment must have PXI/TRIG0 configured as an input.

Caution Do *not* drive the same RTSI trigger bus line with the NI 781*x*R and another device simultaneously. Such signal driving can damage both devices. NI is *not* liable for any damage resulting from such signal driving.

For more information on using and configuring triggers, select **Help»Search the LabVIEW Help** in LabVIEW to view the *LabVIEW Help*. Refer to the *PXI Hardware Specification Revision 2.1* and *PXI Software Specification Revision 2.1* at `www.pxisa.org` for more information about PXI triggers.

PXI Local Bus

The NI PXI-781*x*R can communicate with other PXI devices using the PXI local bus. The PXI local bus is a daisy-chained bus that connects each PXI peripheral slot with the adjacent peripheral slot on either side. For example, the right local bus lines from a given PXI peripheral slot connect to the left local bus lines of the adjacent slot on the right. Each local bus is 13 lines wide. All of these lines connect to the FPGA on the NI PXI-781*x*R, and you can use these lines as you use any of the other NI PXI-781*x*R DIO lines. The PXI local bus right lines on the NI PXI-781*x*R are PXI/LBR<0..12>. The PXI local bus left lines on the NI PXI-781*x*R are PXI/LBLSTAR<0..12>.

The NI PXI-781*x*R can configure each PXI local bus line as either an input or an output signal. Only one device can drive the same physical local bus line at a given time. For example, if an NI PXI-781*x*R is configured to drive a signal on PXI/LBR0, the device in the slot immediately to the right must have its PXI/LBLSTAR 0 line configured as an input.

Caution Do *not* drive the same PXI local bus line with the NI PXI-781*x*R and another device simultaneously. Such signal driving can damage both devices. NI is *not* liable for any damage resulting from such signal driving.

The NI PXI-781*x*R local bus lines are compatible only with 3.3 V signaling LVTTL and LVCMOS levels.

Caution Do *not* enable the local bus lines on an adjacent device if the device drives anything other than 0–3.3 V LVTTL signal levels on the NI PXI-781*x*R. Enabling the lines in this way can damage the NI PXI-781*x*R. NI is *not* liable for any damage resulting from enabling such lines.

The left local bus lines from the left peripheral slot of a PXI backplane (Slot 2) are routed to the star trigger lines of up to 13 other peripheral slots in a two-segment PXI system. This configuration provides a dedicated, delay-matched trigger signal between the first peripheral slot and the other peripheral slots and results in very precise trigger timing signals. For example, an NI PXI-781*x*R in Slot 2 can send an independent trigger signal to each device plugged into Slots <3..15> using the PXI/LBLSTAR<0..12>. Each device receives its trigger signal on its own dedicated star trigger line.

Caution Do *not* configure the NI PXI-781*x*R and another device to drive the same physical star trigger line simultaneously. Such signal driving can damage the NI PXI-781*x*R and the other device. NI is *not* liable for any damage resulting from such signal driving.

Refer to the *PXI Hardware Specification Revision 2.1* and *PXI Software Specification Revision 2.1* at `www.pxisa.org` for more information about PXI triggers.

Switch Settings

Refer to Figure 2-3 for the location of the switches on the NI 781*x*R. For normal operation, SW1 is in the OFF position. To prevent a VI stored in flash memory from loading to the FPGA at power up, move SW1 to the ON position, as shown in Figure 2-5.

Note SW2 and SW3 are not connected.

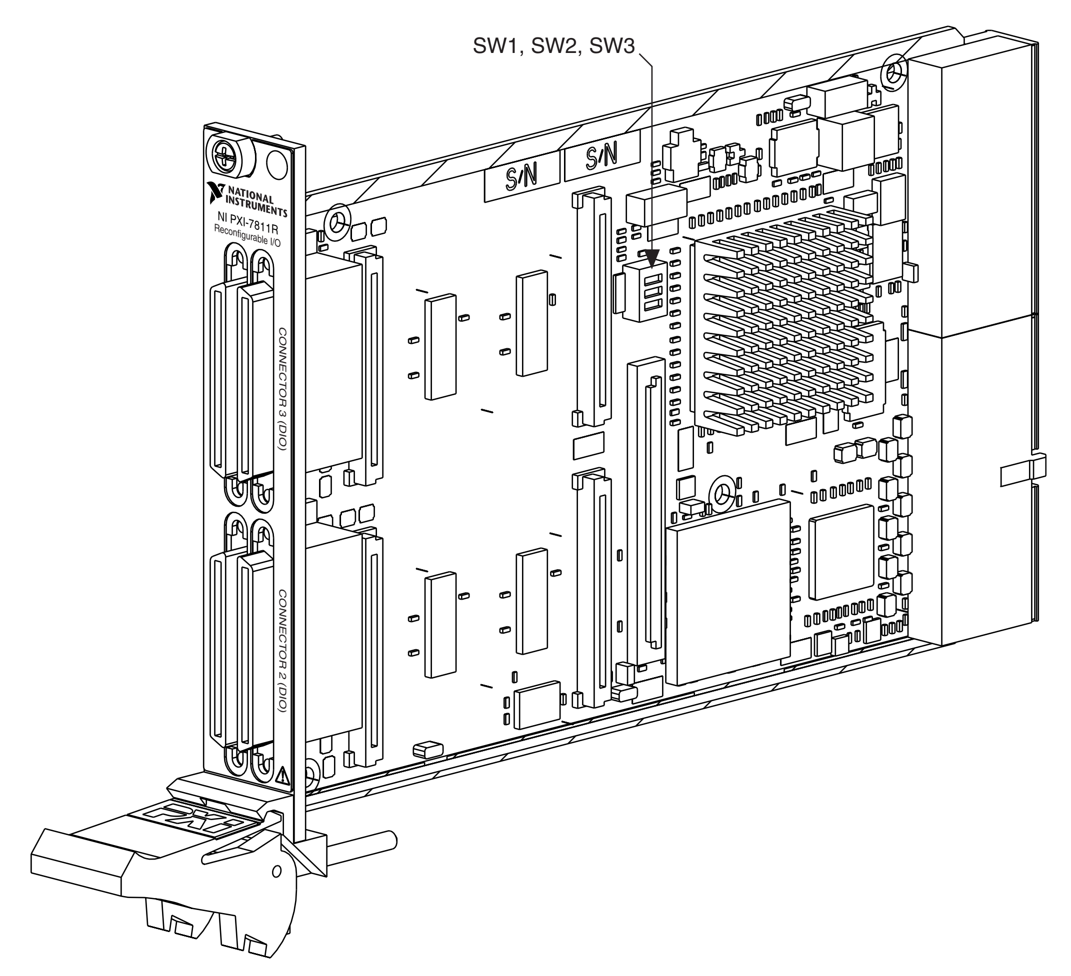

Figure 2-3. Switch Location on the NI PXI-781*x*R

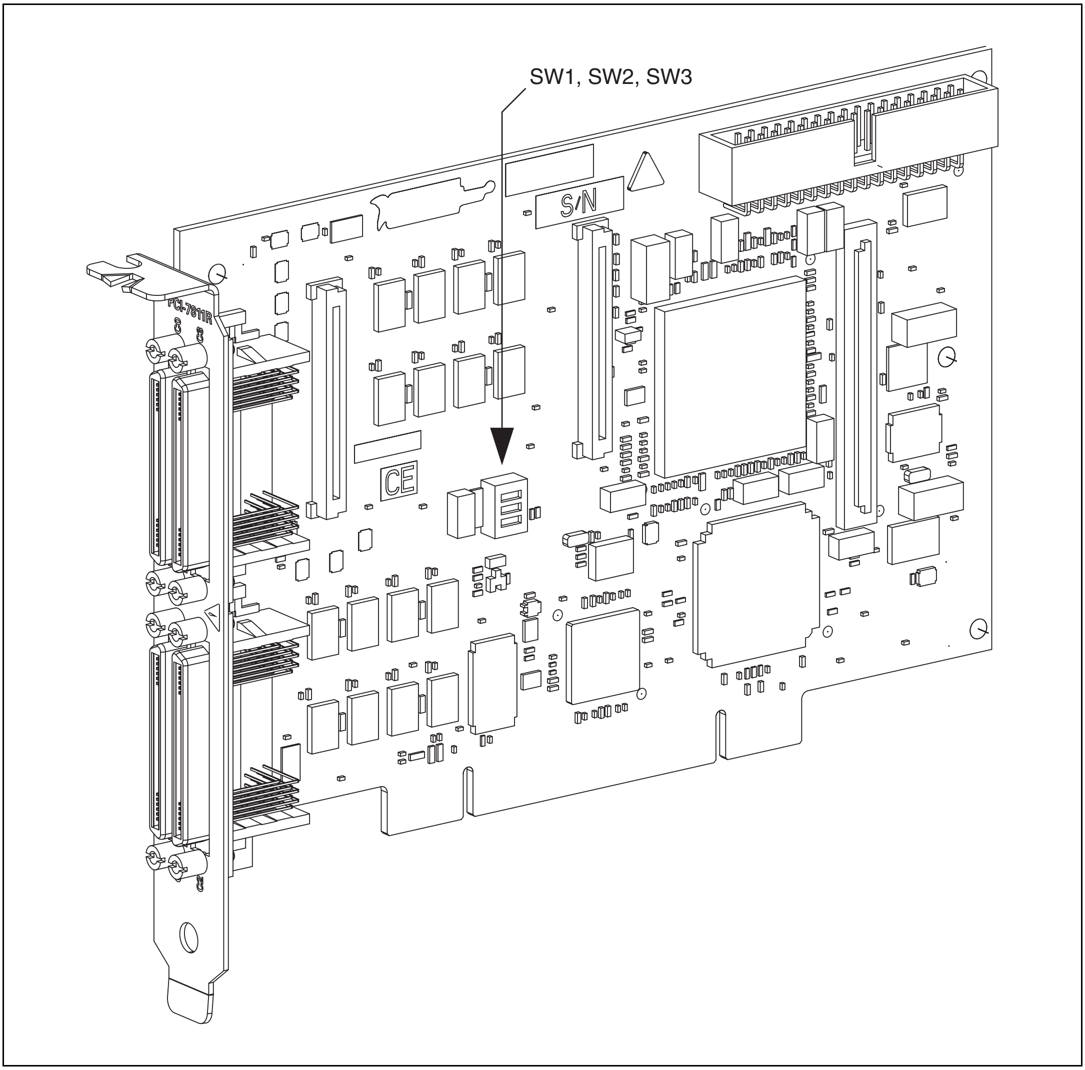

Figure 2-4. Switch Location on the NI PCI-781*x*R

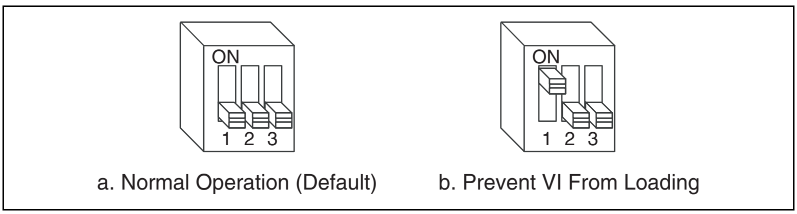

Figure 2-5. Switch Settings

Complete the following steps to prevent a VI stored in flash memory from loading to the FPGA:

1. Power off and unplug the PC or the PXI/CompactPCI chassis.
2. Remove the NI 781*x*R from the PCI or PXI/CompactPCI chassis.
3. Move SW1 to the ON position, as shown in Figure 2-5b.
4. Reinsert the NI PXI-781*x*R into the PC or PXI/CompactPCI chassis. Refer to the *Installing the Hardware* section of the *Getting Started with the NI 781xR* document for installation instructions.
5. Plug in and power on the PC or PXI/CompactPCI chassis.

After you complete this procedure, a VI stored in flash memory does not load to the FPGA at power up. You can use software to reconfigure the NI 781*x*R, if necessary. To return to the default setting so that VIs load from flash memory, repeat the previous procedure but return SW1 to the OFF position in step 3. You can use this switch to enable or disable the ability to load from flash memory. In addition to this switch, you must configure the NI 781*x*R with the software to autoload an FPGA VI.

Note When the NI 781*x*R is powered on with SW1 in the ON position, the analog circuitry does not return properly calibrated data. Move the switch to the ON position only while you are using software to reconfigure the NI 781*x*R for the desired power-up behavior. Afterward, return SW1 to the OFF position.

Power Connections

Two pins on each I/O connector supply 5 V from the computer power supply using a self-resetting fuse. The fuse resets automatically within a few seconds after the overcurrent condition is removed. The +5 V pins are referenced to DGND and power external digital circuitry. The NI 781*x*R has the following power rating:

+4.50 to +5.25 VDC (250 mA max per 5 V pin)

Caution Do *not* connect the +5 V power pins directly to digital ground or to any other voltage source on the NI 781*x*R or on any other device under any circumstance. Doing so can damage the NI 781*x*R and the computer. NI is *not* liable for damage resulting from such a connection.

A

Specifications

This appendix lists the specifications of the NI 781*x*R. These specifications are typical at 25 °C unless otherwise noted.

Digital I/O

Number of channels .... 160 input/output

Compatibility .... TTL

Digital logic levels

Level	Min	Max
Input low voltage (V_{IL})	0.0 V	0.8 V
Input high voltage (V_{IH})	2.0 V	5.5 V
Output low voltage (V_{OL}), where $I_{OUT} = -I_{max}$ (sink)	—	0.4 V
Output high voltage (V_{OH}), where $I_{OUT} = I_{max}$ (source)	2.4 V	—

Maximum output current

I_{max} (sink) .... 5.0 mA

I_{max} (source) .... 5.0 mA

Input leakage current.............................. ±10 µA

Power-on state.. Programmable by line

Data transfers .... Interrupts, programmed I/O

Protection

Input .... –0.5 to 7.0 V

Output .... Short-circuit (up to eight lines can be shorted at a time)

Reconfigurable FPGA

Number of logic slices

NI 7811R 5,120

NI 7813R 14,336

Equivalent number of logic cells

NI 7811R 11,520

NI 7813R 32,256

Available embedded RAM

NI 7811R ....81,920 bytes

NI 7813R ....196,608 bytes

Timebase..40, 80, 120, 160, or 200 MHz

Timebase reference sources....................Onboard clock, phase-locked to PXI 10 MHz clock

Timebase accuracy

Onboard clock ....±100 ppm, 450 ps jitter

Phase locked to PXI 10 MHz clock...........................Adds 350 ps jitter, 300 ps skew

Additional frequency-dependent jitter

40 MHz...None

80 MHz...400 ps

120 MHz...720 ps

160 MHz...710 ps

200 MHz...700 ps

Bus Interface

NI 781*x*R..Master, slave

Power Requirement

+5 VDC (±5%)

NI 7811R.. 9 mA (typ), 50 mA (max)[1]

NI 7813R.. 9 mA (typ), 50 mA (max)[1]

+3.3 VDC (±5%)

NI 7811R.. 650 mA (typ), 1,000 mA (max)[2]

NI 7813R.. 850 mA (typ), 1,350 mA (max)[2]

To calculate the total current sourced by the digital outputs, use the following equation:

$$\sum_{i=1}^{j} \text{current sourced on channel } i$$

where j is the number of digital outputs being used to source current.

Power available at I/O connectors .... +4.50 to +5.25 VDC, 250 mA per I/O connector pin

Physical

Dimensions (not including connectors)

NI PXI-781*x*R .... 16.0 cm × 10.0 cm (6.3 in. × 3.9 in.)

NI PCI-781*x*R .... 15.5 cm × 10.6 cm (6.105 in. × 4.162 in.)

Weight

PCI-781*x*R .... 112 g

PXI-781*x*R .... 162 g

I/O connectors .... Four 68-pin female high-density VHDCI type

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[1] Does not include current drawn form the +5 V line on the I/O connectors.

[2] Does not include current sourced by the digital outputs.

Environmental

Operating Environment

The NI 781*x*R is intended for indoor use only.

Ambient temperature range ....0 °C to 55 °C, tested in accordance with IEC-60068-2-1 and IEC-60068-2-2

Relative humidity range..........................10% to 90%, noncondensing, tested in accordance with IEC-60068-2-56

Altitude ....2,000 m at 25 °C ambient temperature

Storage Environment

Ambient temperature range ....–20 °C to 70 °C, tested in accordance with IEC-60068-2-1 and IEC-60068-2-2

Relative humidity range..........................5% to 95%, noncondensing, tested in accordance with IEC-60068-2-56

Note Clean the device with a soft, non-metallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

Shock and Vibration (NI PXI-781*x*R Only)

Operational shock ....30 g peak, half-sine, 11 ms pulse Tested in accordance with IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.

Random vibration

Operating ....5 Hz to 500 Hz, 0.3 g_{rms}

Nonoperating ....5 Hz to 500 Hz, 2.4 g_{rms} Tested in accordance with IEC-60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.

Safety

The NI 781*x*R is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CAN/CSA-C22.2 No. 61010-1

Note Refer to the product label, or visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column for UL and other safety certifications.

Electromagnetic Compatibility

The NI 781*x*R is designed to meet the requirements of the following standards of EMC for electrical equipment for measurement, control, and laboratory use:

- EN 61326 EMC requirements; Minimum Immunity
- EN 55011 Emissions; Group 1, Class A
- CE, C-Tick, ICES, and FCC Part 15 Emissions; Class A

Note For EMC compliance, operate this device with shielded cabling.

CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

- 73/23/EEC; Low-Voltage Directive (safety)
- 89/336/EEC; Electromagnetic Compatibility Directive (EMC)

Note Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of their life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers and National Instruments WEEE initiatives, visit `ni.com/environment/weee.htm`.

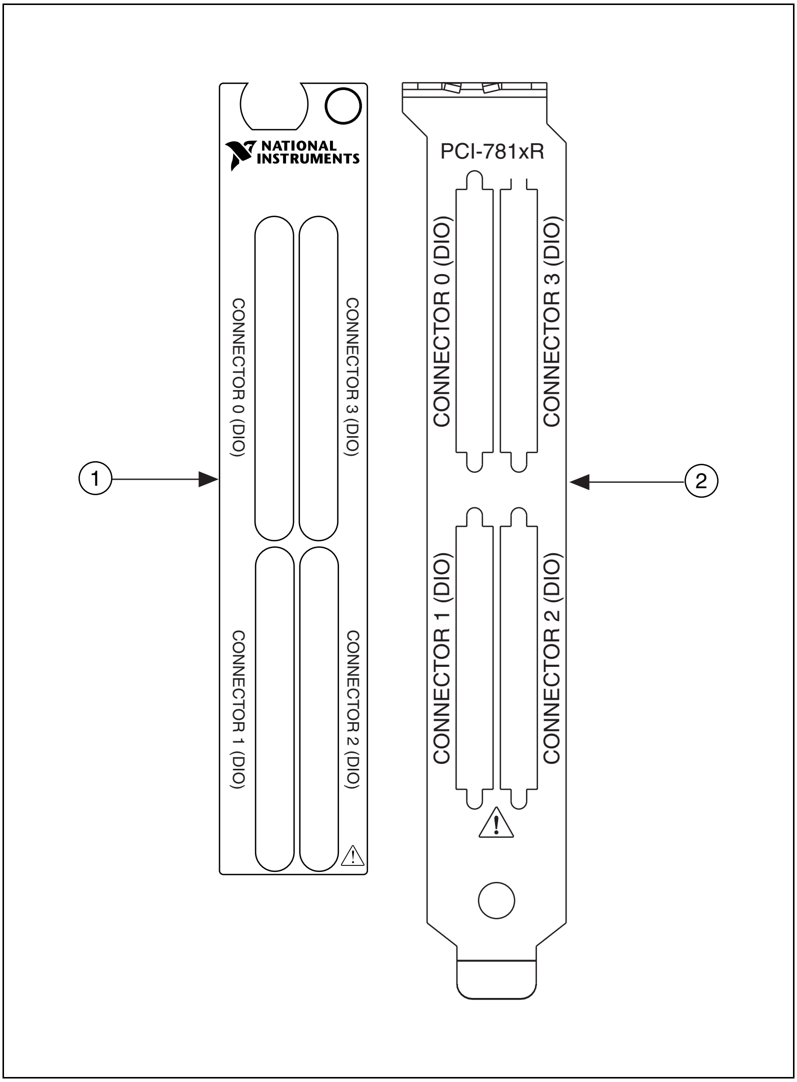
B

Connecting I/O Signals

This appendix describes how to make input and output signal connections to the NI 781*x*R I/O connectors.

The NI 781*x*R has four DIO connectors with 40 DIO lines per connector.

Figure B-1 shows the I/O connector locations for the NI 781*x*R. The I/O connectors are numbered starting at zero.



1 Connector Overlay for the NI PXI-781*x*	2 Connector Overlay for the NI PCI-781*x*

Figure B-1. NI 781*x*R Connector Locations

Figure B-2 shows the I/O connector pin assignments for the I/O connectors on the NI 781*x*R.

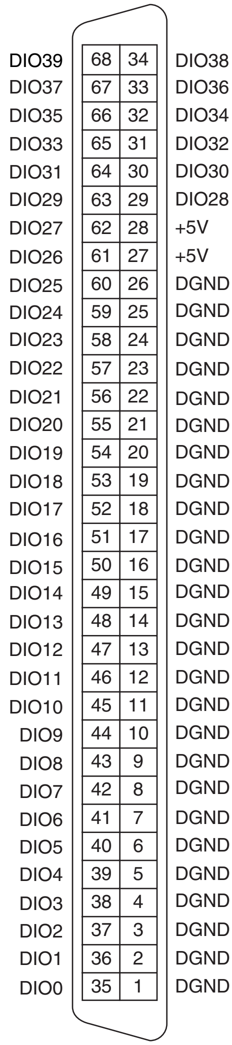


Figure B-2. NI 781*x*R I/O Connector Pin Assignments

To access the signals on the I/O connectors, you must connect a cable from the I/O connector to a signal accessory. Plug the small VHDCI connector end of the cable into the appropriate I/O connector and connect the other end of the cable to the appropriate signal accessory.

Table B-1. I/O Connector Signal Descriptions

Signal Name	Reference	Direction	Description
+5V	DGND	Output	+5 VDC Source—These pins supply 5 V from the computer power supply using a self-resetting 1 A fuse. No more than 250 mA should be pulled from a single pin.
DGND	—	—	Digital Ground—These pins supply the reference for the digital signals at the I/O connector as well as the 5 V supply.
DIO<0..39>	DGND	Input or Output	Digital I/O signals.

Caution Connections that exceed any of the maximum ratings of input or output signals on the NI 781*x*R can damage the NI 781*x*R and the computer. Maximum input ratings for each signal are given in the *Protection (Volts) On/Off* column of Table B-2. NI is *not* liable for any damage resulting from such signal connections.

Table B-2. NI 781*x*R I/O Signal Summary

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time	Bias
+5V	DO	—	—	—	—	—	—
DGND	DO	—	—	—	—	—	—
DIO<0..39> Connector<0..3>	DIO	—	–0.5 to +7.0	5.0 at 2.4	5.0 at 0.4	12 ns	—
DIO = Digital Input/Output DO = Digital Output							

Connecting to CompactRIO Extension I/O Chassis

You can use the CompactRIO R Series Expansion chassis and CompactRIO I/O modules with the NI 781*x*R. Refer to the *CompactRIO R Series Expansion System Installation Instructions* for information about connecting the chassis to the NI 781*x*R.

Connecting to SSR Signal Conditioning

NI provides cables that allow you to connect signals from the NI 781*x*R directly to SSR backplanes for digital signal conditioning.

The NSC68-5050 cable is designed to connect the signals on the NI 781*x*R DIO connectors directly to SSR backplanes for digital signal conditioning. This cable has a 68-pin male VHDCI connector on one end that plugs into the NI 781*x*R DIO connectors. The other end of this cable provides two 50-pin female headers.

Each of these 50-pin headers can be plugged directly into an eight-, 16-, 24-, or 32-channel SSR backplane for digital signal conditioning. One of the 50-pin headers contains DIO lines <0..23> from the NI 781*x*R DIO connector. These lines are mapped to slots <0..23> on an SSR backplane in sequential order. The other 50-pin header contains DIO lines <24..39> from the NI 781*x*R DIO connector. These lines are mapped to slots <0..15> on an SSR backplane in sequential order. You can connect to an SSR backplane containing a number channels that does not equal the number of lines on the NSC68-5050 cable header. In this case, you have access only to the channels that exist on both the SSR backplane and the NSC68-5050 cable header you are using.

Figure B-3 shows the connector pinouts when using the NSC68-5050 cable.

Signal	Pin	Pin	Signal
DIO23	1	2	NC
DIO22	3	4	NC
DIO21	5	6	NC
DIO20	7	8	NC
DIO19	9	10	NC
DIO18	11	12	NC
DIO17	13	14	NC
DIO16	15	16	NC
DIO15	17	18	NC
DIO14	19	20	DGND
DIO13	21	22	DGND
DIO12	23	24	DGND
DIO11	25	26	DGND
DIO10	27	28	DGND
DIO9	29	30	DGND
DIO8	31	32	DGND
DIO7	33	34	DGND
DIO6	35	36	DGND
DIO5	37	38	DGND
DIO4	39	40	DGND
DIO3	41	42	DGND
DIO2	43	44	DGND
DIO1	45	46	DGND
DIO0	47	48	DGND
+5V	49	50	DGND

DIO 0–23 Connector
Pin Assignment

Signal	Pin	Pin	Signal
NC	1	2	NC
NC	3	4	NC
NC	5	6	NC
NC	7	8	NC
NC	9	10	NC
NC	11	12	NC
NC	13	14	NC
NC	15	16	NC
DIO39	17	18	NC
DIO38	19	20	NC
DIO37	21	22	NC
DIO36	23	24	NC
DIO35	25	26	NC
DIO34	27	28	NC
DIO33	29	30	NC
DIO32	31	32	DGND
DIO31	33	34	DGND
DIO30	35	36	DGND
DIO29	37	38	DGND
DIO28	39	40	DGND
DIO27	41	42	DGND
DIO26	43	44	DGND
DIO25	45	46	DGND
DIO24	47	48	DGND
+5V	49	50	DGND

DIO 24–39 Connector
Pin Assignment

Figure B-3. Connector Pinouts for Use with the NSC68-5050 Cable

C

Using the SCB-68 Shielded Connector Block

This appendix describes how to connect input and output signals to the NI 781*x*R with the SCB-68 shielded connector block.

The SCB-68 has 68 screw terminals for I/O signal connections. To use the SCB-68 with the NI 781*x*R, you must configure the SCB-68 as a general-purpose connector block. Figure C-1 illustrates the general-purpose switch configuration.

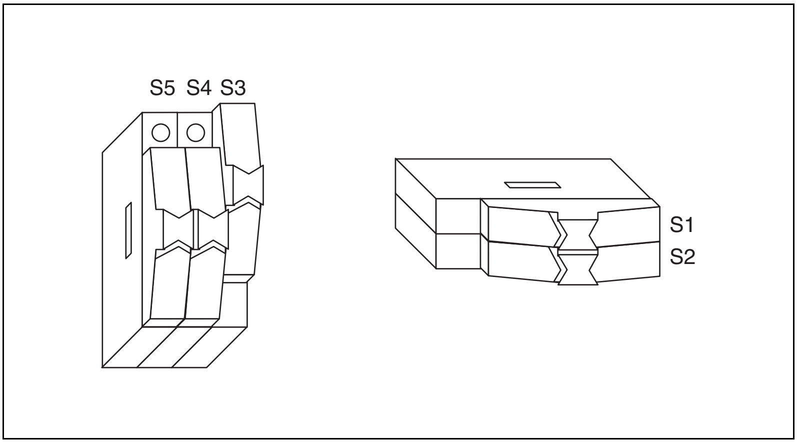


Figure C-1. General-Purpose Switch Configuration for the SCB-68 Terminal Block

After configuring the SCB-68 switches, you can connect the I/O signals to the SCB-68 screw terminals. Refer to Appendix B, *Connecting I/O Signals*, for the connector pin assignments for the NI 781*x*R. After connecting I/O signals to the SCB-68 screw terminals, you can connect the SCB-68 to the NI 781*x*R with the SH68-C68-S shielded cable.

D

Technical Support and Professional Services

Visit the following sections of the National Instruments Web site at `ni.com` for technical support and professional services:

- **Support**—Online technical support resources at `ni.com/support` include the following:
  - **Self-Help Resources**—For answers and solutions, visit the award-winning National Instruments Web site for software drivers and updates, a searchable KnowledgeBase, product manuals, step-by-step troubleshooting wizards, thousands of example programs, tutorials, application notes, instrument drivers, and so on.
  - **Free Technical Support**—All registered users receive free Basic Service, which includes access to hundreds of Application Engineers worldwide in the NI Developer Exchange at `ni.com/exchange`. National Instruments Application Engineers make sure every question receives an answer.

    For information about other technical support options in your area, visit `ni.com/services` or contact your local office at `ni.com/contact`.
- **Training and Certification**—Visit `ni.com/training` for self-paced training, eLearning virtual classrooms, interactive CDs, and Certification program information. You also can register for instructor-led, hands-on courses at locations around the world.
- **System Integration**—If you have time constraints, limited in-house technical resources, or other project challenges, National Instruments Alliance Partner members can help. To learn more, call your local NI office or visit `ni.com/alliance`.
- **Declaration of Conformity (DoC)**—A DoC is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electronic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting `ni.com/certification`.

- **Calibration Certificate**—If your product supports calibration, you can obtain the calibration certificate for your product at `ni.com/calibration`.

If you searched `ni.com` and could not find the answers you need, contact your local office or NI corporate headquarters. Phone numbers for our worldwide offices are listed at the front of this manual. You also can visit the Worldwide Offices section of `ni.com/niglobal` to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

Glossary

Symbol	Prefix	Value
p	pico	10^{-12}
μ	micro	10^{-6}
m	milli	10^{-3}
M	mega	10^{6}

A

A	Amperes.
ASIC	Application-Specific Integrated Circuit—A proprietary semiconductor component designed and manufactured to perform a set of specific functions.

B

bipolar	A signal range that includes both positive and negative values (for example, –5 to +5 V).

C

C	Celsius.
CalDAC	Calibration DAC.
CH	Channel—Pin or wire lead to which you apply or from which you read the analog or digital signal. Analog signals can be single-ended or differential. For digital signals, you group channels to form ports. Ports usually consist of either four or eight digital channels.
cm	Centimeter.
CMOS	Complementary metal-oxide semiconductor.

CMRR	Common-mode rejection ratio—A measure of an instrument's ability to reject interference from a common-mode signal, usually expressed in decibels (dB).
common-mode voltage	Any voltage present at the instrumentation amplifier inputs with respect to amplifier ground.
CompactPCI	Refers to the core specification defined by the PCI Industrial Computer Manufacturer's Group (PICMG).

D

D/A	Digital-to-analog.
DAC	Digital-to-analog converter—An electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current.
DAQ	Data acquisition—A system that uses the computer to collect, receive, and generate electrical signals.
dB	Decibel—The unit for expressing a logarithmic measure of the ratio of two signal levels: dB = 20log10 V1/V2, for signals in volts.
DC	Direct current.
DGND	Digital ground signal.
DIFF	Differential mode.
DIO	Digital input/output.
DIO<*i*>	Digital input/output channel signal.
DMA	Direct memory access—A method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.
DNL	Differential nonlinearity—A measure in LSB of the worst-case deviation of code widths from their ideal value of 1 LSB.
DO	Digital output.

E

EEPROM	Electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed.

F

FPGA	Field-Programmable Gate Array.
FPGA VI	A configuration that is downloaded to the FPGA and that determines the functionality of the hardware.

G

glitch	An unwanted signal excursion of short duration that is usually unavoidable.

H

h	Hour.
HIL	Hardware-in-the-loop.
Hz	Hertz.

I

I/O	Input/output—The transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces.
INL	Relative accuracy.

L

LabVIEW	Laboratory Virtual Instrument Engineering Workbench. LabVIEW is a graphical programming language that uses icons instead of lines of text to create programs.
LSB	Least significant bit.

M

m	Meter.
max	Maximum.
MIMO	Multiple input, multiple output.
min	Minimum.
MIO	Multifunction I/O.
monotonicity	A characteristic of a DAC in which the analog output always increases as the values of the digital code input to it increase.
mux	Multiplexer—A switching device with multiple inputs that sequentially connects each of its inputs to its output, typically at high speeds, in order to measure several signals with a single analog input channel.

N

noise	An undesirable electrical signal—Noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.
NRSE	Nonreferenced single-ended mode—All measurements are made with respect to a common (NRSE) measurement system reference, but the voltage at this reference can vary with respect to the measurement system ground.

O

OUT	Output pin—A counter output pin where the counter can generate various TTL pulse waveforms.

P

PCI	Peripheral Component Interconnect—A high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and workstations. PCI offers a theoretical maximum transfer rate of 132 MB/s.
port	(1) A communications connection on a computer or a remote controller. (2) A digital port, consisting of four or eight lines of digital input and/or output.
ppm	Parts per million.
pu	Pull-up.
PWM	Pulse-width modulation.
PXI	PCI eXtensions for Instrumentation—An open specification that builds off the CompactPCI specification by adding instrumentation-specific features.

R

RAM	Random-access memory—The generic term for the read/write memory that is used in computers. RAM allows bits and bytes to be written to it as well as read from. Various types of RAM are DRAM, EDO RAM, SRAM, and VRAM.
resolution	The smallest signal increment that can be detected by a measurement system. Resolution can be expressed in bits, in proportions, or in percent of full scale. For example, a system has 12-bit resolution, one part in 4,096 resolution, and 0.0244% of full scale.
RIO	Reconfigurable I/O.
rms	Root mean square.
RSE	Referenced single-ended mode—All measurements are made with respect to a common reference measurement system or a ground. Also called a grounded measurement system.

S

s	Seconds.
S	Samples.
S/s	Samples per second—Used to express the rate at which a DAQ board samples an analog signal.
signal conditioning	The manipulation of signals to prepare them for digitizing.
slew rate	The voltage rate of change as a function of time. The maximum slew rate of an amplifier is often a key specification to its performance. Slew rate limitations are first seen as distortion at higher signal frequencies.

T

THD	Total harmonic distortion—The ratio of the total rms signal due to harmonic distortion to the overall rms signal, in decibel or a percentage.
thermocouple	A temperature sensor created by joining two dissimilar metals. The junction produces a small voltage as a function of the temperature.
TTL	Transistor-transistor logic.
two's complement	Given a number x expressed in base 2 with n digits to the left of the radix point, the (base 2) number $2n - x$.

V

V	Volts.
VDC	Volts direct current.
VHDCI	Very high density cabled interconnect.
VI	Virtual Instrument—Program in LabVIEW that models the appearance and function of a physical instrument.
V_{IH}	Volts, input high.
V_{IL}	Volts, input low.

V_{OH}	Volts, output high.
V_{OL}	Volts, output low.
V_{rms}	Volts, root mean square.

W

waveform	Multiple voltage readings taken at a specific sampling rate.