Reconfigurable I/O

NI PXI-7831R User Manual

Reconfigurable I/O Devices for PXI/CompactPCI Bus Computers

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All Class A products display a simple warning statement of one paragraph in length regarding interference and undesired operation. The FCC rules have restrictions regarding the locations where FCC Class A products can be operated.

Consult the FCC Web site at `www.fcc.gov` for more information.

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Changes or modifications not expressly approved by NI could void the user's authority to operate the equipment under the FCC Rules.

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Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user is required to correct the interference at their own expense.

Canadian Department of Communications

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Cet appareil numérique de la classe A respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

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Readers in the European Union (EU) must refer to the manufacturer's Declaration of Conformity (DoC) for information* pertaining to the CE marking compliance scheme. The manufacturer includes a DoC for most hardware products except for those bought from OEMs. In addition, DoCs are usually not provided if compliance is not required, for example electrically benign apparatus or cables.

To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by your product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.

* The CE marking Declaration of Conformity contains important supplementary information and instructions for the user or installer.

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About This Manual

This manual describes the electrical and mechanical aspects of the National Instruments PXI-7831R device and contains information concerning its operation and programming.

The NI PXI-7831R device is a Reconfigurable I/O (RIO) device. The NI PXI-7831R contains eight independent, 16-bit analog input (AI) channels, eight independent, 16-bit analog output (AO) channels, and 96 digital I/O (DIO) lines.

Conventions

The following conventions appear in this manual:

<> — Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, DIO<3..0>.

» — The » symbol leads you through nested menu items and dialog box options to a final action. The sequence **File»Page Setup»Options** directs you to pull down the **File** menu, select the **Page Setup** item, and select **Options** from the last dialog box.

 This icon denotes a note, which alerts you to important information.

 This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on the device, refer to the *Safety Information* section of Chapter 1, *Introduction*, for precautions to take.

bold — Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names and hardware labels.

italic — Italic text denotes variables, emphasis, a cross reference, or an introduction to a key concept. This font also denotes text that is a placeholder for a word or value that you must supply.

`monospace` — Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories,

programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and code excerpts.

Reconfigurable I/O Documentation

The *NI PXI-7831R User Manual* is one piece of the documentation set for your RIO system and application. Depending on the hardware and software you use for your application, you could have any of several types of documentation. Use the documentation you have as follows:

- *Where to Start with the NI PXI-7831R*—This document lists what you need to get started, describes how to unpack and install the hardware, and contains information about connecting signals to the NI PXI-7831R.
- *NI PXI-7831R User Manual*—This manual contains detailed information about the NI PXI-7831R hardware.
- *LabVIEW FPGA Module Release Notes*—This document contains information about installing and getting started with the FPGA Module.
- *LabVIEW FPGA Module User Manual*—This manual describes how to use the FPGA Module.
- *LabVIEW Help*—This help contains information about using various virtual instruments (VIs) with the NI PXI-7831R and using the FPGA Module and the LabVIEW Real-Time (RT) Module.
- *LabVIEW Real-Time Module User Manual*—This manual contains information about how to install and use the RT Module.

Related Documentation

The following documents contain information you might find helpful:

- NI Developer Zone tutorial, *Field Wiring and Noise Considerations for Analog Signals*, at `ni.com/zone`
- *PICMG CompactPCI 2.0 R3.0*
- *PXI Hardware Specification Revision 2.1*
- *PXI Software Specification Revision 2.1*

1

Introduction

This chapter describes the NI PXI-7831R, describes the concept of the Reconfigurable I/O (RIO) device, lists what you need to get started, describes the optional software and optional equipment, explains how to unpack the hardware, and contains safety information about the NI PXI-7831R.

About the Reconfigurable I/O Devices

Thank you for purchasing the NI PXI-7831R. This RIO device has 96 digital I/O (DIO) lines, 8 independent, 16-bit analog output (AO) channels, and 8 independent, 16-bit analog input (AI) channels.

A user-reconfigurable field-programmable gate array (FPGA) controls the digital and analog I/O on the NI PXI-7831R. The FPGA on the RIO device allows you to define the functionality and timing of the device, whereas traditional multifunction I/O (MIO) devices have a fixed functionality provided by an application-specific integrated circuit (ASIC). You can change the functionality of the FPGA on the RIO device by using LabVIEW, a graphical programming environment, and the LabVIEW FPGA Module to create and download a custom virtual instrument (VI) to the FPGA. You can reconfigure the RIO device with a new VI at any time. Using LabVIEW, you can graphically design the timing and functionality of the RIO device without having to learn the low-level programming language or hardware description language (HDL) that is traditionally used for FPGA design. If you only have LabVIEW and do not have the FPGA Module, you cannot create new FPGA VIs but you can create VIs that run in LabVIEW to control existing FPGA VIs.

Some applications require tasks such as real-time, floating-point processing or data logging while performing I/O and logic on the RIO device. You can use the LabVIEW Real-Time (RT) Module to perform these additional applications while also communicating with and controlling the RIO device.

The RIO device contains flash memory to store VIs for instant loading of the FPGA when the system is powered on.

The PXI chassis has the Real-Time System Integration (RTSI) bus to easily synchronize several measurement functions to a common trigger or timing event. The RTSI bus is implemented on the PXI trigger bus on the PXI backplane. The RTSI bus can route timing and trigger signals between as many as seven PXI devices in your system.

Refer to Appendix A, *Specifications*, for detailed specifications of the RIO device.

Using PXI with CompactPCI

Using PXI compatible products with standard CompactPCI products is an important feature provided by *PXI Hardware Specification Revision 2.1* and *PXI Software Specification Revision 2.1*. If you use a PXI-compatible plug-in card in a standard CompactPCI chassis, you cannot use PXI-specific functions, but you can still use the basic plug-in card functions. For example, the RTSI bus on the RIO device is available in a PXI chassis, but not in a CompactPCI chassis.

The CompactPCI specification permits vendors to develop sub-buses that coexist with the basic PCI interface on the CompactPCI bus. Compatible operation is not guaranteed between CompactPCI devices with different sub-buses nor between CompactPCI devices with sub-buses and PXI. The standard implementation for CompactPCI does not include these sub-buses. The RIO device works in any standard CompactPCI chassis adhering to *PICMG CompactPCI 2.0 R3.0*.

PXI-specific features are implemented on the J2 connector of the CompactPCI bus. Table 1-1 lists the J2 pins used by the NI PXI-7831R. The NI PXI-7831R is compatible with any CompactPCI chassis with a sub-bus that does not drive these lines. Even if the sub-bus is capable of driving these lines, the RIO device is still compatible as long as those pins on the sub-bus are disabled by default and are never enabled.

Caution Damage can result if the J2 lines are driven by the sub-bus.

Table 1-1. Pins Used by the NI PXI-7831R

NI PXI-7831R Signal	PXI Pin Name	PXI J2 Pin Number
PXI Trigger<0..7>	PXI Trigger<0..7>	A16, A17, A18, B15, B18, C18, E16, E18
PXI Clock 10 MHz	PXI Clock 10 MHz	E17
PXI Star Trigger	PXI Star Trigger	D17
LBLSTAR<0..12>	LBL<0..12>	A1, A19, C1, C19, C20, D1, D2, D15, D19, E1, E2, E19, E20
LBR<0..12>	LBR<0..12>	A2, A3, A20, A21, B2, B20, C3, C21, D3, D21, E3, E15, E21

What You Need to Get Started

This section contains two lists that detail what you need to get started using the NI PXI-7831R with Windows 2000/XP or the RT Module.

Getting Started with Windows 2000/XP

To set up and use the NI PXI-7831R with Windows 2000/XP, you need the following items:

- ❑ NI PXI-7831R
- ❑ The following software packages:
  - LabVIEW version 7.0 or later
  - NI Device Drivers CD
  - FPGA Module version 7.0 or later (required to develop custom FPGA VIs for the RIO device)
- ❑ PXI/CompactPCI chassis and a PXI/CompactPCI embedded controller, running Windows 2000/XP (or any computer running Windows 2000/XP and an MXI-3 link to a PXI/CompactPCI chassis)
- ❑ At least one cable and terminal block for connecting signals to the NI PXI-7831R

- ❑ The following documents are included on the NI Device Drivers CD and are also available at `ni.com/manuals` (optional):
  - *LabVIEW FPGA Module Release Notes*
  - *LabVIEW FPGA Module User Manual*
  - *Where to Start with the NI PXI-7831R*
- ❑ The *LabVIEW Help*, which is available by selecting **Help»VI, Function, & How-To Help** from LabVIEW.

Getting Started with the RT Module

To set up and use the NI PXI-7831R with the FPGA Module and the RT Module, you need the following items:

- ❑ NI PXI-7831R
- ❑ The following software packages:
  - LabVIEW version 7.0 or later
  - NI Device Drivers CD
  - FPGA Module version 7.0 or later (required to develop custom FPGA VIs for the RIO device)
  - RT Module version 7.0 or later
- ❑ PXI/CompactPCI chassis and real-time PXI controller
- ❑ One of the following host computers, depending upon your application, running Windows 2000/XP:
  - PC
  - Laptop computer
  - PXI/CompactPCI embedded controller
- ❑ At least one cable and terminal block for connecting signals to the NI PXI-7831R
- ❑ Category 5 (Cat-5) crossover cable (if the real-time PXI system is not configured on a network). You need a regular network cable if you are configured on a network.

- The following documents are included on the NI Device Drivers CD and are also available at `ni.com/manuals` (optional):
  - *LabVIEW FPGA Module Release Notes*
  - *LabVIEW FPGA Module User Manual*
  - *LabVIEW Real-Time Module User Manual*
  - *Where to Start with the NI PXI-7831R*
- The *LabVIEW Help*, which is available by selecting **Help»VI, Function, & How-To Help** from LabVIEW.

Overview of Reconfigurable I/O

This section introduces the concept of RIO and describes how to use the reconfigurable FPGA to build high-level functions in hardware.

Refer to Chapter 2, *Hardware Overview of the NI PXI-7831R*, for descriptions of the physical I/O resources available on the NI PXI-7831R.

Reconfigurable I/O Concept

The NI PXI-7831R device is based on a reconfigurable FPGA core surrounded by fixed I/O resources. The behavior of the reconfigurable core can be configured to better match the requirements of the measurement and control system. The behavior can be fully user defined and implemented as a VI, creating an application-specific I/O device. In contrast, a traditional data acquisition (DAQ) device uses a fixed core with predetermined functionality.

Flexible Functionality

Flexible functionality allows the RIO device to match individual application requirements and to mimic the functionality of fixed I/O devices, including I/O combinations not available in standard products. For example, you can configure a RIO device in one application for three 32-bit quadrature decoders and then reconfigure the RIO device in another application for eight 16-bit event counters.

In timing and triggering applications, the flexible functionality of the RIO device makes it an ideal complement to applications based on the RT module, such as control and hardware-in-the-loop (HIL) simulations. For example, you can configure the RIO device for a single timed loop in one application and then reconfigure the device in another application for four independent timed loops with separate I/O resources.

User-Defined I/O Resources

With the RIO device, you can define both the combination of I/O resources and the I/O resources themselves. You can also create new building blocks on top of fixed I/O resources. For example, one application might require an event counter that increments when a rising edge appears on any of three digital input lines. Another application might require a digital line to be asserted once an analog input exceeds a programmable threshold. You can implement these user-defined behaviors in the hardware for fast, deterministic performance.

Device-Embedded Logic and Processing

You can embed logic and processing in the FPGA of the RIO device. Typical logic functions include Boolean operations, comparisons, and basic mathematical operations. You can implement multiple functions efficiently in the same design, operating sequentially or in parallel. It is possible to implement more complex algorithms such as control loops, but the size of the FPGA limits the scope of these algorithms.

Reconfigurable I/O Architecture

Figure 1-1, which illustrates a generic representation of RIO device, shows an FPGA connected to fixed I/O resources and a bus interface.

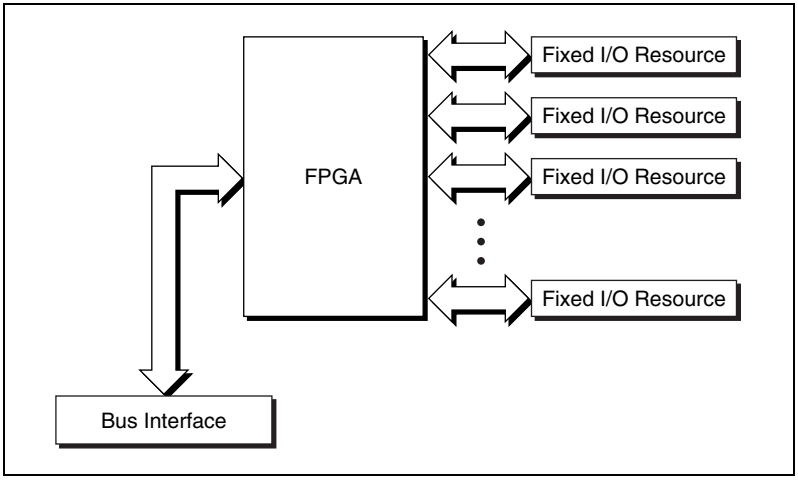


Figure 1-1. High-Level FPGA Functional Overview

The fixed I/O resources include A/D converters (ADCs), D/A converters (DACs), digital input or output lines, or other I/O resources. Software accesses the RIO device through the bus interface, and the FPGA provides

the connectivity between the bus interface and the fixed I/O, including any timing, triggering, processing, and custom I/O required by the application.

Timing, triggering, processing, and custom I/O is provided by consuming logic in the FPGA. Each fixed I/O resource used by the application consumes a small portion of the FPGA logic, which is used to perform basic control of the fixed I/O resource. The bus interface also consumes a small portion of the FPGA logic to provide software access to the device.

The remaining FPGA logic is available for higher-level functions such as timing, triggering, and counting. Each of these functions consumes varying amounts of logic. For example, a typical 32-bit counter consumes 20 times more logic than a DIO resource, while an 8-bit counter consumes five times more logic than a DIO resource. Figures 1-2 and 1-3 illustrate the logic used by the FPGA in two different applications. The application shown in Figure 1-2 requires many fixed I/O resources, leaving little logic left over for higher-level functions. The application in Figure 1-3 uses relatively few I/O resources and has enough logic left over for several large functions.

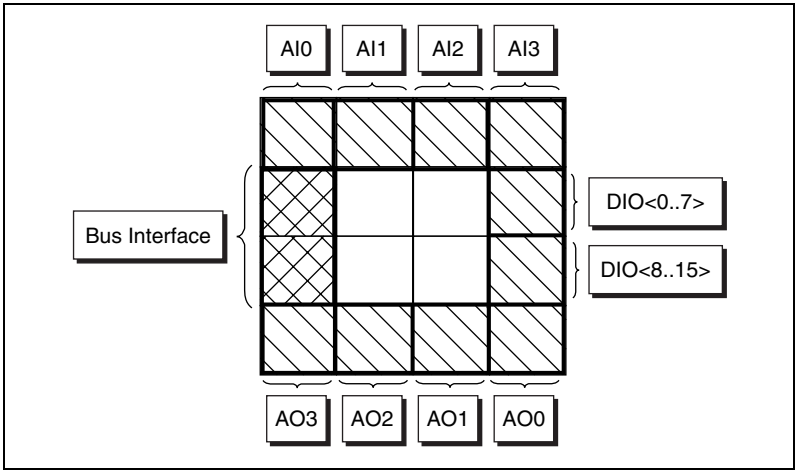


Figure 1-2. FPGA Logic Use in an Application with Many Fixed I/O Resources

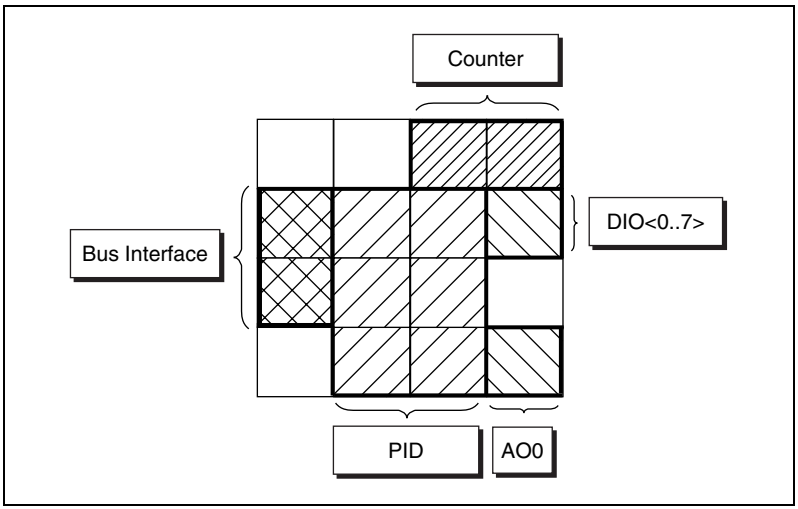


Figure 1-3. FPGA Logic Use in an Application with Higher-Level Functions

The FPGA is volatile and does not retain the VI when it is powered off. Therefore, the VI must be reloaded every time power is turned on. The VI comes from onboard flash memory or from the software over the bus interface. One advantage to using flash memory is that the VI can start executing almost immediately after power up, instead of waiting for the computer to completely boot and load the FPGA. Refer to the *LabVIEW FPGA User Manual* for more information about how to store your VI in flash memory.

Reconfigurable I/O Applications

To create or obtain new VIs for your application, you can use the FPGA Module, which allows the application to be specified using a subset of LabVIEW. Arbitrary functionality can be defined for the RIO device. If you are using the FPGA Module, refer to the FPGA Module examples located in `LabVIEW 7.0\examples\FPGA`.

Software Development

You can use LabVIEW with the FPGA Module to program the NI PXI-7831R. To develop real-time applications that control the NI PXI-7831R, you can use the RT Module with LabVIEW and the FPGA Module.

FPGA Module

The FPGA Module enables you to use LabVIEW to create VIs that run on the RIO device, which contains a reconfigurable FPGA. The FPGA Module includes a new function palette, which contains functions that run on the FPGA on the RIO device. These functions can control the I/O, timing, and logic of the RIO device and can generate interrupts for synchronization. The FPGA Module synthesizes a VI into a form that can be downloaded to the FPGA on the RIO device. The Interactive Front Panel Communication with the FPGA Module allows you to interact with the VI running on the FPGA. The FPGA Module also includes a palette of functions for use in LabVIEW for Windows, or when targeting an RT Module device, that create applications that wait for interrupts and that control the FPGA by programmatically reading and writing to the device.

Note A software utility installed with the NI-RIO Device Drivers CD allows users without the FPGA module to configure the NI PXI-7831R analog input mode, synchronize to the PXI clock, and configure the device to automatically load FPGA VIs when powered on.

RT Module

The RT Module extends the LabVIEW development environment to deliver deterministic, real-time performance.

You can develop your RT Module application on a host computer with graphical programming and then download the program to run on an independent hardware target with a real-time operating system. The RT Module allows you to use the NI PXI-7831R in PXI systems being controlled in real time by a LabVIEW VI.

The NI PXI-7831R plug-in device is designed as a single-point AI, AO, and DIO complement to the RT Module. Refer to `ni.com/labviewrt` for more information about the RT Module.

Cables and Optional Equipment

NI offers a variety of products to use with your device, including cables, connector blocks, and other accessories as follows.

Table 1-2. Cables and Accessories

Cable	Cable Description	Accessories
SH68-C68-S	Shielded 68-pin VHDCI male connector to female 0.050 series D-type connector. The cable is constructed with 34 twisted wire pairs plus an overall shield.	Connects to the following standard 68-pin screw terminal blocks: • SCB-68 • CB-68LP • CB-68LPR • TBX-68
NSC68-262650	Non-shielded cable connects from 68-pin VHDCI male connector to two 26-pin female headers plus one 50-pin female header. The pinout of these headers allows for direct connection to 5B backplanes for analog signal conditioning and SSR backplanes for digital signal conditioning.	26-pin headers can connect to the following 5B backplanes for analog signal conditioning: • 5B08 (8-channel) • 5B01 (16-channel) 50-pin header can connect to the following SSR backplanes for digital signal conditioning: • 8-channel backplane • 16-channel backplane • 32-channel backplane
NSC68-5050	Non-shielded cable connects from 68-pin VHDCI male connector to two 50-pin female headers. The pinout of these headers allows for direct connection to SSR backplanes for digital signal conditioning.	50-pin headers can connect to the following SSR backplanes for digital signal conditioning: • 8-channel backplane • 16-channel backplane • 32-channel backplane

Refer to Appendix B, *Connecting I/O Signals*, for more information on using these cables and accessories to connect I/O signals to the PXI-7831R. For the most up-to-date cabling options, refer to `ni.com/catalog` or call the sales office nearest to you.

Custom Cabling

NI offers a variety of cables that you can use to connect signals to the NI PXI-7831R. If you need to develop a custom cable, NI provides a generic un-terminated shielded cable that makes this task easier. The

SHC68-NT-S (NI part #189041-02) connects to the NI PXI-7831R VHDCI connectors on one end of the cable. The other end of the cable is not terminated. This cable ships with a wire list identifying which wire corresponds to which NI PXI-7831R pin. Using this cable, you can quickly connect the NI PXI-7831R signals that you need to the connector of your choice without having to connect these signals to the VHDCI connector end of the cable. Refer to Appendix B, *Connecting I/O Signals* for the NI PXI-7831R connector pinouts.

Unpacking

The RIO device is shipped in an antistatic package to prevent electrostatic damage (ESD) to the device. ESD can damage several components on the device.

Caution *Never* touch the exposed pins of connectors.

To avoid such damage in handling the device, take the following precautions:

- Ground yourself using a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of the computer chassis before removing the device from the package.

Remove the device from the package and inspect the device for loose components or any sign of damage. Notify NI if the device appears damaged in any way. Do *not* install a damaged device into the computer.

Store the RIO device in the antistatic envelope when not in use.

Safety Information

The following section contains important safety information that you *must* follow when installing and using the NI PXI-7831R.

Do *not* operate the NI PXI-7831R in a manner not specified in this document. Misuse of the NI PXI-7831R can result in a hazard. You can compromise the safety protection built into the NI PXI-7831R if the NI PXI-7831R is damaged in any way. If the NI PXI-7831R is damaged, return it to NI for repair.

Do *not* substitute parts or modify the NI PXI-7831R except as described in this document. Use the NI PXI-7831R only with the chassis, modules, accessories, and cables specified in the installation instructions. You *must* have all covers and filler panels installed during operation of the NI PXI-7831R.

Do *not* operate the NI PXI-7831R in an explosive atmosphere or where there may be flammable gases or fumes. If you must operate the NI PXI-7831R in such an environment, it must be in a suitably rated enclosure.

If you need to clean the NI PXI-7831R, use a soft, nonmetallic brush. Make sure that the NI PXI-7831R is completely dry and free from contaminants before returning it to service.

Operate the NI PXI-7831R only at or below Pollution Degree 2. Pollution is foreign matter in a solid, liquid, or gaseous state that can reduce dielectric strength or surface resistivity. The following is a description of pollution degrees:

- Pollution Degree 1 means no pollution or only dry, nonconductive pollution occurs. The pollution has no influence.
- Pollution Degree 2 means that only nonconductive pollution occurs in most cases. Occasionally, however, a temporary conductivity caused by condensation must be expected.
- Pollution Degree 3 means that conductive pollution occurs, or dry, nonconductive pollution occurs that becomes conductive due to condensation.

You *must* insulate signal connections for the maximum voltage for which the NI PXI-7831R is rated. Do *not* exceed the maximum ratings for the NI PXI-7831R. Do not install wiring while the NI PXI-7831R is live with electrical signals. Do not remove or add connector blocks when power is connected to the system. Remove power from signal lines before connecting them to or disconnecting them from the NI PXI-7831R.

Operate the NI PXI-7831R at or below the *installation category*[1] marked on the hardware label. Measurement circuits are subjected to *working voltages*[2] and transient stresses (overvoltage) from the circuit to which they are connected during measurement or test. Installation categories establish

[1] Installation categories, also referred to as *measurement categories*, are defined in electrical safety standard IEC 61010-1.

[2] Working voltage is the highest rms value of an AC or DC voltage that can occur across any particular insulation.

standard impulse withstand voltage levels that commonly occur in electrical distribution systems. The following is a description of installation categories:

- Installation Category I is for measurements performed on circuits not directly connected to the electrical distribution system referred to as MAINS[1] voltage. This category is for measurements of voltages from specially protected secondary circuits. Such voltage measurements include signal levels, special equipment, limited-energy parts of equipment, circuits powered by regulated low-voltage sources, and electronics.
- Installation Category II is for measurements performed on circuits directly connected to the electrical distribution system. This category refers to local-level electrical distribution, such as that provided by a standard wall outlet (for example, 115 V for U.S. or 230 V for Europe). Examples of Installation Category II are measurements performed on household appliances, portable tools, and similar products.
- Installation Category III is for measurements performed in the building installation at the distribution level. This category refers to measurements on hard-wired equipment such as equipment in fixed installations, distribution boards, and circuit breakers. Other examples are wiring, including cables, bus-bars, junction boxes, switches, socket-outlets in the fixed installation, and stationary motors with permanent connections to fixed installations.
- Installation Category IV is for measurements performed at the primary electrical supply installation (<1,000V). Examples include electricity meters and measurements on primary overcurrent protection devices and on ripple control units.

[1] MAINS is defined as a hazardous live electrical supply system that powers equipment. Suitably rated measuring circuits may be connected to the MAINS for measuring purposes.

2

Hardware Overview of the NI PXI-7831R

This chapter presents an overview of the hardware functions and I/O connectors on the NI PXI-7831R.

Figure 2-1 shows a block diagram for the NI PXI-7831R, and Figure 2-2 shows the parts locator diagrams for the NI PXI-7831R.

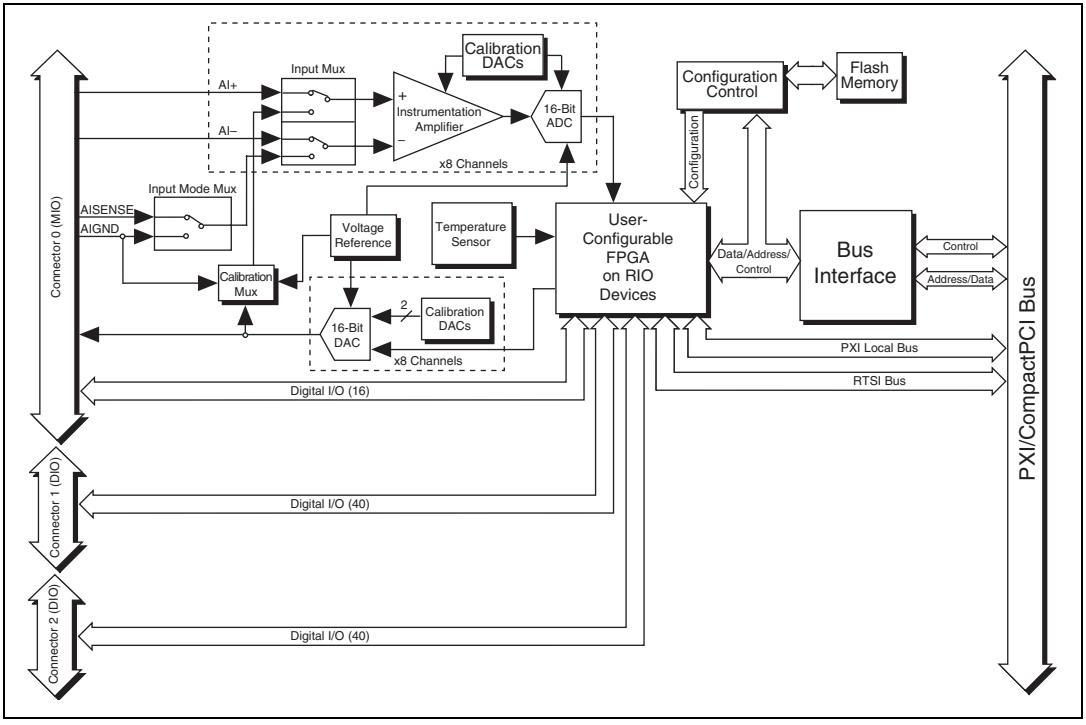


Figure 2-1. NI PXI-7831R Block Diagram

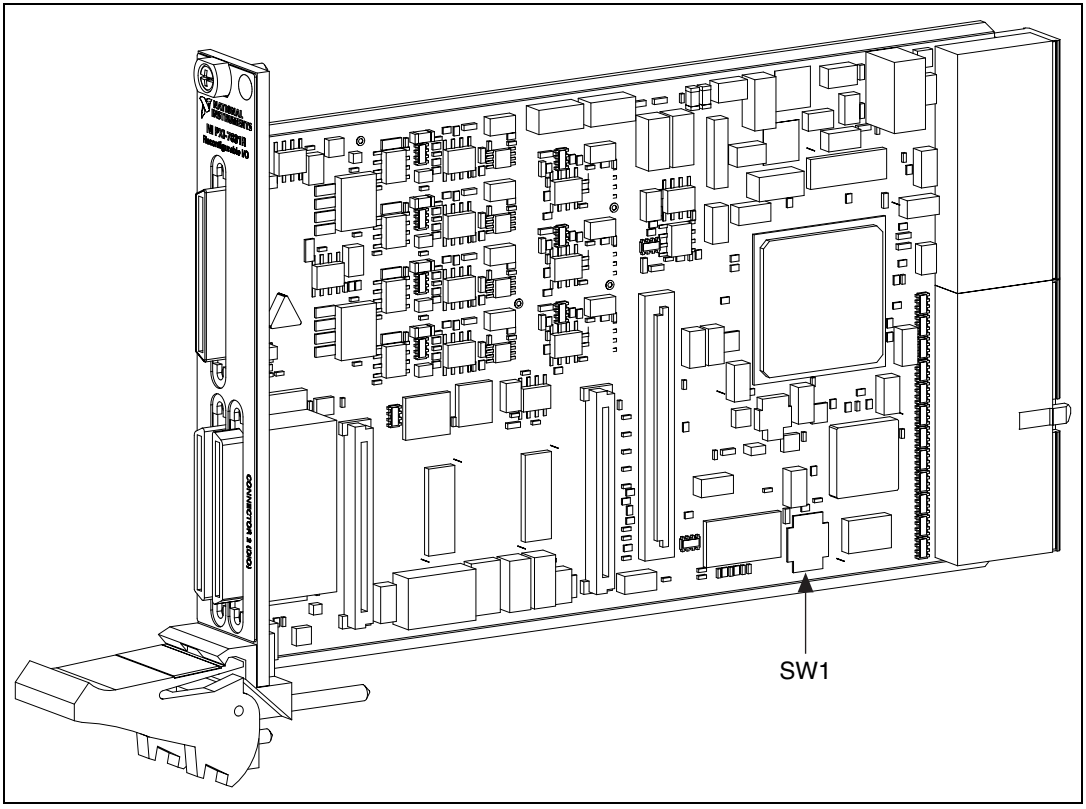


Figure 2-2. Parts Locator Diagram for the NI PXI-7831R

Analog Input

The NI PXI-7831R has eight independent, 16-bit AI channels that can be simultaneously sampled or sampled at different rates. The input mode is software configurable, and the input range is fixed at ±10 V. The converters return data in two's complement format. Table 2-1 shows the ideal output code returned for a given AI voltage.

Table 2-1. Ideal Output Code and AI Voltage Mapping

Input Description	AI Voltage	Output Code (Hex) (Two's Complement)
Full-scale range –1 LSB	9.999695	7FFF
Full-scale range –2 LSB	9.999390	7FFE

Table 2-1. Ideal Output Code and AI Voltage Mapping (Continued)

Input Description	AI Voltage	Output Code (Hex) (Two's Complement)
Midscale	0.000000	0000
Negative full-scale range +1 LSB	–9.999695	8001
Negative full-scale range	–10.000000	8000
Any input voltage	$\frac{Output\ Code}{32{,}768} \times 10.0\ \text{V}$	—

Input Modes

The NI PXI-7831R input mode is software configurable. The input channels support three input modes—differential (DIFF) input, referenced single-ended (RSE) input, and nonreferenced single-ended (NRSE) input. The selected input mode applies to all the input channels. Table 2-2 describes the three input modes.

Table 2-2. Available Input Modes for the NI PXI-7831R

Input Mode	Description
DIFF	When the NI PXI-7831R is configured in DIFF input mode, each channel uses two AI lines. The positive input pin connects to the positive terminal of the onboard instrumentation amplifier, and the negative input pin connects to the negative input of the instrumentation amplifier.
RSE	When the NI PXI-7831R is configured in RSE input mode, each channel uses only its positive AI pin. This pin connects to the positive terminal of the onboard instrumentation amplifier. The negative input of the instrumentation amplifier is internally tied to the AI ground (AIGND).
NRSE	When the NI PXI-7831R is configured in NRSE input mode, each channel uses only its positive AI pin. This pin connects to the positive terminal of the onboard instrumentation amplifier. The negative input of the instrumentation amplifier on each AI channel is internally connected to the AI sense (AISENSE) input pin.

Input Range

The NI PXI-7831R AI range is fixed at ±10 V.

Connecting Analog Input Signals

The AI signals for the NI PXI-7831R are AI<0..7>+, AI<0..7>–, AIGND, and AISENSE. The AI<0..7>+ and AI<0..7>– signals are tied to the eight AI channels of the NI PXI-7831R. For all input modes, the AI<0..7>+ signals are connected to the positive input of the instrumentation amplifier on each channel. The signal connected to the negative input of the instrumentation amplifier depends on the input mode for which the NI PXI-7831R is configured.

In differential input mode, signals connected to AI<0..7>– are routed to the negative input of the instrumentation amplifier for each channel. In RSE input mode, the negative input of the instrumentation amplifier for each channel is internally connected to AIGND. In NRSE input mode, the AISENSE signal is connected internally to the negative input of the instrumentation amplifier for each channel. In DIFF and RSE input modes, AISENSE is not used and can be left unconnected.

Caution Exceeding the differential and common-mode input ranges distorts the input signals. Exceeding the maximum input voltage rating can damage the NI PXI-7831R and the computer. NI is *not* liable for any damage resulting from such signal connections. The maximum input voltage ratings are listed in Table B-2, *NI PXI-7831R I/O Signal Summary*.

AIGND is a common AI signal that is routed directly to the ground tie point on the NI PXI-7831R. You can use this signal for a general analog ground tie point to the NI PXI-7831R, if necessary.

Connection of AI signals to the NI PXI-7831R depends on the input mode of the AI channels you are using and the type of input signal source. With different input modes, you can use the instrumentation amplifier in different ways. Figure 2-3 shows a diagram of the NI PXI-7831R instrumentation amplifier.

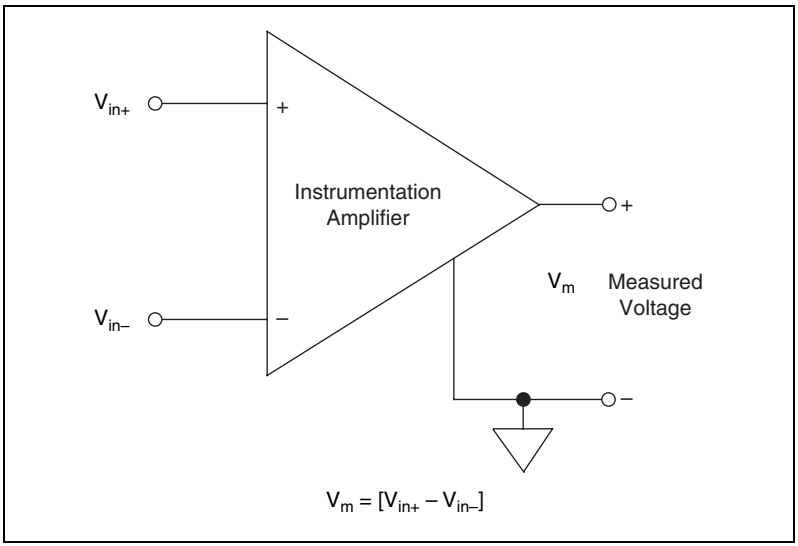


Figure 2-3. NI PXI-7831R Instrumentation Amplifier

The instrumentation amplifier applies common-mode voltage rejection and presents high input impedance to the AI signals connected to the NI PXI-7831R. Signals are routed to the positive and negative inputs of the instrumentation amplifier through input multiplexers on the device. The instrumentation amplifier converts two input signals to a signal that is the difference between the two input signals. The amplifier output voltage is referenced to the device ground. The NI PXI-7831R ADC measures this output voltage when it performs A/D conversions.

You must reference all signals to ground either at the source device or at the NI PXI-7831R. If you have a floating source, you should reference the signal to ground by using RSE input mode or the DIFF input mode with bias resistors. Refer to the *Differential Connections for Nonreferenced or Floating Signal Sources* section for more information about these input modes. If you have a grounded source, you should not reference the signal to AIGND. You can avoid this reference by using DIFF or NRSE input modes.

Types of Signal Sources

When configuring the input channels and making signal connections, you must first determine whether the signal sources are floating or ground referenced. The following sections describe these two signal types.

Floating Signal Sources

A floating signal source is in no way connected to the building ground system but instead has an isolated ground-reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolator outputs, and isolation amplifiers. An instrument or device that has an isolated output is a floating signal source. You must tie the ground reference of a floating signal to the NI PXI-7831R AIGND through a bias resistor to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies as the source floats out of the common-mode input range.

Ground-Referenced Signal Sources

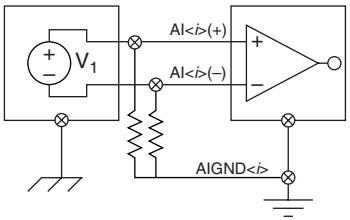
A ground-referenced signal source is connected in some way to the building system ground and is, therefore, already connected to a common ground point with respect to the NI PXI-7831R, assuming that the computer is plugged into the same power system. Nonisolated outputs of instruments and devices that plug into the building power system fall into this category.

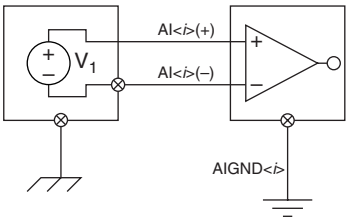
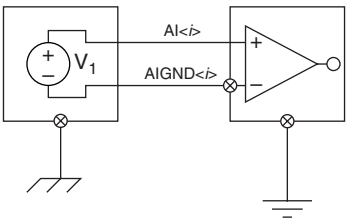
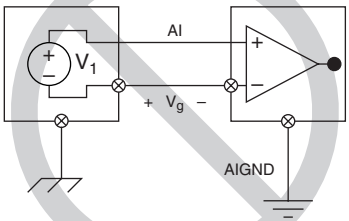
The difference in ground potential between two instruments connected to the same building power system is typically between 1 and 100 mV but can be much higher if power distribution circuits are improperly connected. If a grounded signal source is improperly measured, this difference may appear as a measurement error. The connection instructions for grounded signal sources are designed to eliminate this ground potential difference from the measured signal.

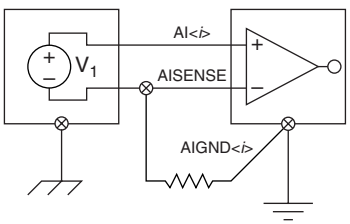
Input Modes

You can configure the NI PXI-7831R for one of three input modes—DIFF, RSE, or NRSE. The following sections discuss the use of single-ended and differential measurements and considerations for measuring both floating and ground-referenced signal sources.

Figure 2-4 summarizes the recommended input mode for both types of signal sources.

<table>
<tr><th rowspan="2">Input</th><th colspan="2">Signal Source Type</th></tr>
<tr><th>Floating Signal Source
(Not Connected to Building Ground)</th><th>Grounded Signal Source</th></tr>
<tr><td></td><td>Examples
• Ungrounded Thermocouples
• Signal Conditioning with Isolated Outputs
• Battery Devices</td><td>Examples
• Plug-in Instruments with Nonisolated Outputs</td></tr>
<tr><td>Differential
(DIFF)</td><td> 

See text for information on bias resistors.</td><td> 
</td></tr>
<tr><td>Single-Ended —
Ground
Referenced
(RSE)</td><td> 
</td><td>NOT RECOMMENDED
 

Ground-loop losses, V_g, are added to measured signal.</td></tr>
<tr><td>Single-Ended —
Nonreferenced
(NRSE)</td><td> 

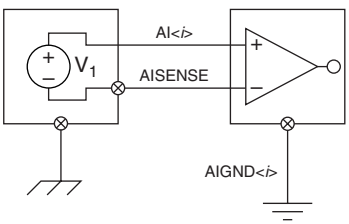
See text for information on bias resistors.</td><td> 
</td></tr>
</table>

Figure 2-4. Summary of Analog Input Connections

Differential Connection Considerations (DIFF Input Mode)

In DIFF input mode, the NI PXI-7831R measures the difference between the positive and negative inputs. DIFF input mode is ideal for measuring ground-referenced signals from other devices. When using DIFF input mode, the input signal is tied to the positive input of the instrumentation amplifier, and its reference signal, or return, is tied to the negative input of the instrumentation amplifier.

Use differential input connections for any channel that meets any of the following conditions:

- The input signal is low-level (less than 1 V).
- The leads connecting the signal to the NI PXI-7831R are greater than 3 m (10 ft).
- The input signal requires a separate ground-reference point or return signal.
- The signal leads travel through noisy environments.

Differential signal connections reduce noise pickup and increase common-mode noise rejection. Differential signal connections also allow input signals to float within the common-mode limits of the instrumentation amplifier.

Differential Connections for Ground-Referenced Signal Sources

Figure 2-5 shows how to connect a ground-referenced signal source to a channel on the NI PXI-7831R configured in DIFF input mode.

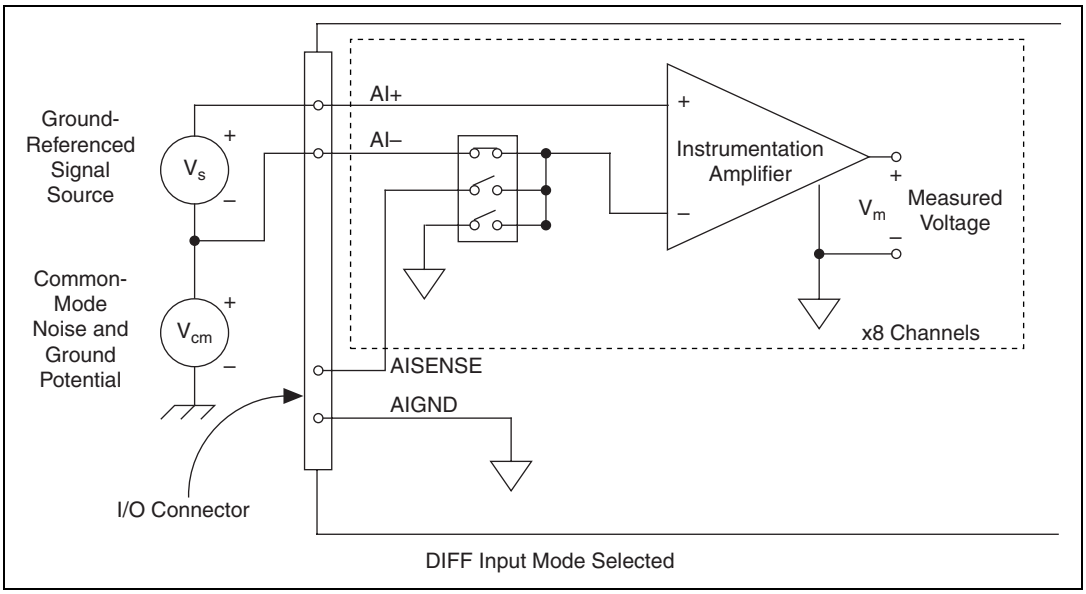


Figure 2-5. Differential Input Connections for Ground-Referenced Signals

With this connection type, the instrumentation amplifier rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the NI PXI-7831R ground, shown as V_{cm} in Figure 2-5. In addition, the instrumentation amplifier can reject common-mode noise pickup in the leads connecting the signal sources to the device. The instrumentation amplifier can reject common-mode signals as long as $V+_{in}$ and $V-_{in}$ (input signals) are both within their specified input ranges. Refer to Appendix A, *Specifications*, for more information about input ranges.

Differential Connections for Nonreferenced or Floating Signal Sources

Figure 2-6 shows how to connect a floating signal source to a channel on the NI PXI-7831R configured in DIFF input mode.

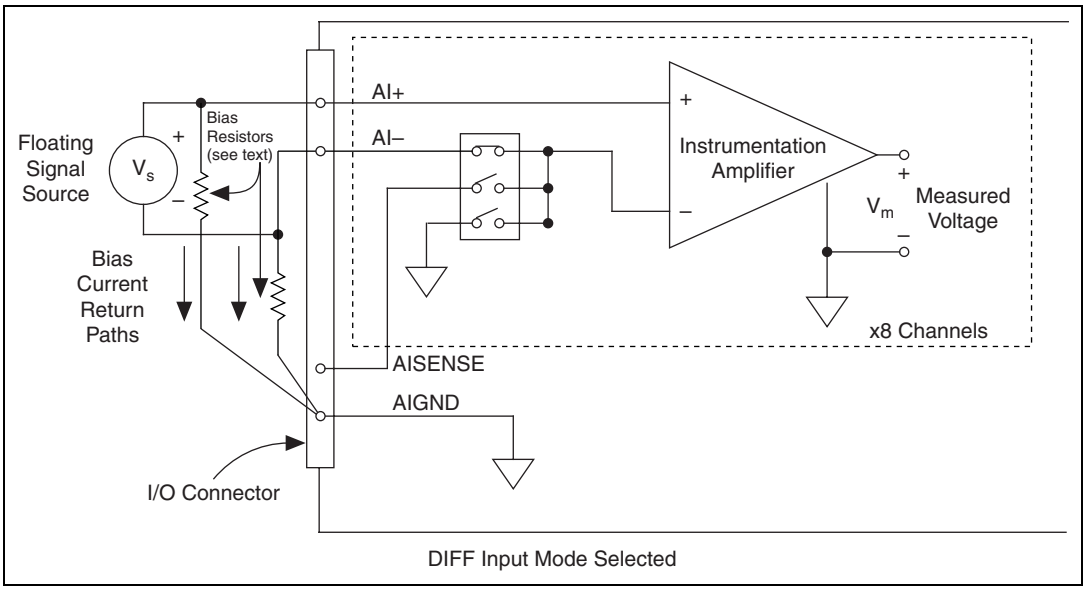


Figure 2-6. Differential Input Connections for Nonreferenced Signals

Figure 2-6 shows two bias resistors connected in parallel with the signal leads of a floating signal source. If you do not use the resistors and the source is truly floating, the source is not likely to remain within the common-mode signal range of the instrumentation amplifier, and the instrumentation amplifier will saturate, causing erroneous readings. You must reference the source to AIGND, which you can do by connecting the positive side of the signal to the positive input of the instrumentation amplifier and connecting the negative side of the signal to AIGND and to the negative input of the instrumentation amplifier, without any resistors at all. This connection works well for DC-coupled sources with low source impedance (less than 100 Ω).

However, for larger source impedances, this connection leaves the differential signal path significantly out of balance. Noise that couples electrostatically onto the positive line does not couple onto the negative line because it is connected to ground. Hence, this noise appears as a differential-mode signal instead of a common-mode signal, and the instrumentation amplifier does not reject it. In this case, instead of directly connecting the negative line to AIGND, connect it to AIGND through a resistor that is about 100 times the equivalent source impedance. The resistor puts the signal path nearly in balance, so about the same amount of noise couples onto both connections, which yields better rejection of electrostatically coupled noise. Also, this input mode does not load down

the source, other than the very high-input impedance of the instrumentation amplifier.

You can fully balance the signal path by connecting another resistor of the same value between the positive input and AIGND, as shown in Figure 2-6. This fully balanced input mode offers slightly better noise rejection but has the disadvantage of loading the source down with the series combination (sum) of the two resistors. If, for example, the source impedance is 2 kΩ and each of the two resistors is 100 kΩ, the resistors load down the source with 200 kΩ and produce a –1% gain error.

Both inputs of the instrumentation amplifier require a DC path to ground in order for the instrumentation amplifier to work. If the source is AC coupled (capacitively coupled), the instrumentation amplifier needs a resistor between the positive input and AIGND. If the source has low-impedance, choose a resistor that is large enough not to significantly load the source but small enough not to produce significant input offset voltage as a result of input bias current (typically 100 kΩ to 1 MΩ). In this case, you can tie the negative input directly to AIGND. If the source has high output impedance, you should balance the signal path as previously described using the same value resistor on both the positive and negative inputs; you should be aware that there is some gain error from loading down the source.

Single-Ended Connection Considerations

A single-ended connection is one in which the NI PXI-7831R AI signal is referenced to a ground that can be shared with other input signals. The input signal is tied to the positive input of the instrumentation amplifier, and the ground is tied to the negative input of the instrumentation amplifier.

You can use single-ended input connections for any input signal that meets the following conditions:

- The input signal is high-level (>1 V).
- The leads connecting the signal to the NI PXI-7831R are less than 3 m (10 ft).
- The input signal can share a common reference point with other signals.

DIFF input connections are recommended for greater signal integrity for any input signal that does not meet the preceding conditions.

You can configure in software the NI PXI-7831R channels for two different types of single-ended connections—RSE input mode and NRSE input mode. The RSE input mode is used for floating signal sources; in this case,

the NI PXI-7831R provides the reference ground point for the external signal. The NRSE input mode is used for ground-referenced signal sources; in this case, the external signal supplies its own reference ground point and the NI PXI-7831R should not supply one.

In single-ended input modes, more electrostatic and magnetic noise couples into the signal connections than in differential input modes. The coupling is the result of differences in the signal path. Magnetic coupling is proportional to the area between the two signal conductors. Electrical coupling is a function of how much the electric field differs between the two conductors.

Single-Ended Connections for Floating Signal Sources (RSE Input Mode)

Figure 2-7 shows how to connect a floating signal source to a channel on the NI PXI-7831R configured for RSE input mode.

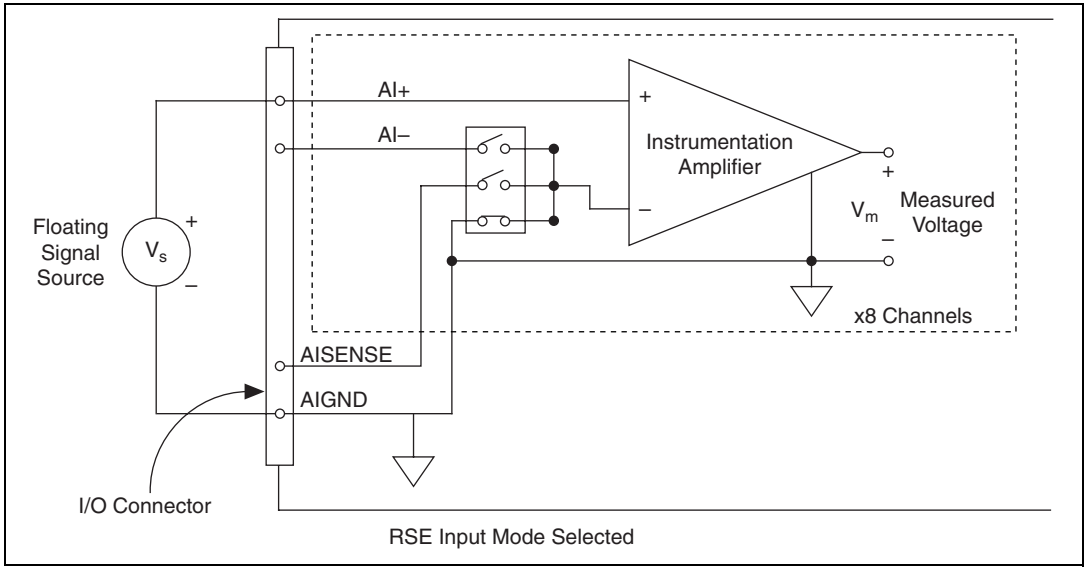


Figure 2-7. Single-Ended Input Connections for Nonreferenced or Floating Signals

Single-Ended Connections for Grounded Signal Sources (NRSE Input Mode)

To measure a grounded signal source with a single-ended input mode, you must configure the NI PXI-7831R in the NRSE input mode. The signal is then connected to the positive input of the NI PXI-7831R instrumentation

amplifier, and the signal local ground reference is connected to the negative input of the instrumentation amplifier. The ground point of the signal should, therefore, be connected to AISENSE. Any potential difference between the NI PXI-7831R ground and the signal ground appears as a common-mode signal at both the positive and negative inputs of the instrumentation amplifier, and this difference is rejected by the amplifier. If the input circuitry of a NI PXI-7831R were referenced to ground, in this situation as in RSE input mode, this difference in ground potentials would appear as an error in the measured voltage.

Figure 2-8 shows how to connect a grounded signal source to a channel on the NI PXI-7831R configured for NRSE input mode.

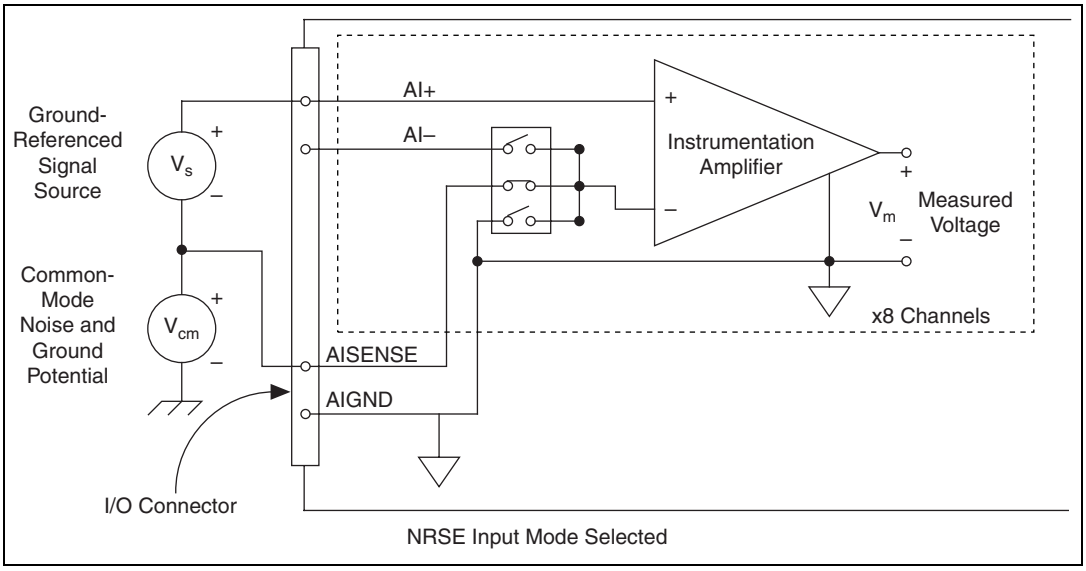


Figure 2-8. Single-Ended Input Connections for Ground-Referenced Signals

Common-Mode Signal Rejection Considerations

Figures 2-5 and 2-8 show connections for signal sources that are already referenced to some ground point with respect to the NI PXI-7831R. In these cases, the instrumentation amplifier can reject any voltage caused by ground potential differences between the signal source and the device. In addition, with differential input connections, the instrumentation amplifier can reject common-mode noise pickup in the leads connecting the signal sources to the device. The instrumentation amplifier can reject

common-mode signals as long as $V+_{in}$ and $V-_{in}$ (input signals) are both within their specified input ranges. Refer to Appendix A, *Specifications*, for more information about input ranges.

Analog Output

The NI PXI-7831R has eight 16-bit AO channels. The bipolar output range is fixed at ±10 V. Some applications require that the AO channels power-on to known voltage levels. To set the power-on levels, you can configure the NI PXI-7831R to automatically load and run your VI when the system powers on. This VI can then set the AO channels to the desired voltage levels. Data written to the DAC is interpreted in two's complement format. Table 2-3 shows the ideal AO voltage generated for a given input code.

Table 2-3. Ideal Output Voltage and Input Code Mapping

Output Description	AO Voltage	Input Code (Hex) (Two's Complement)
Full-scale range –1 LSB	9.999695	7FFF
Full-scale range –2 LSB	9.999390	7FFE
Midscale	0.000000	0000
Negative full-scale range, +1 LSB	–9.999695	8001
Negative full-scale range	–10.000000	8000
Any output voltage	—	$\frac{AO\ Voltage}{10.0\ V} \times 32{,}768$

Note If the output value for an AO channel is not specifically set by your VI then the AO channel voltage output will be undefined.

Connecting Analog Output Signals

The AO signals are AO<0..7> and AOGND.

AO<0..7> are the eight available AO channels. AOGND is the ground reference signal for the AO channels.

Figure 2-9 shows how to make AO connections to the NI PXI-7831R.

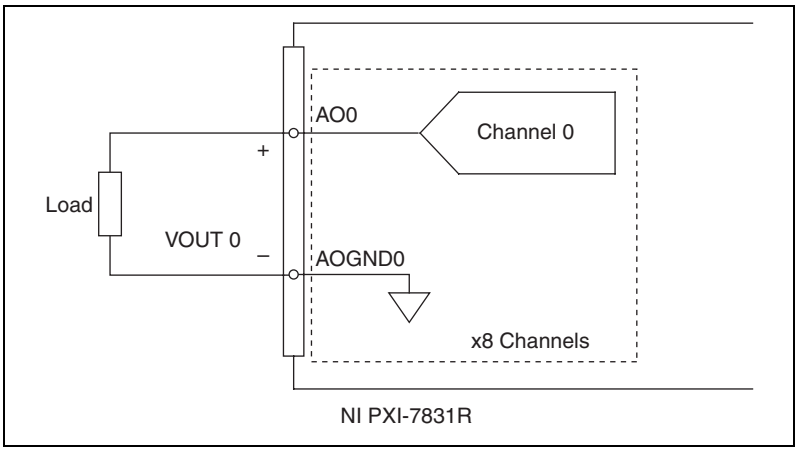


Figure 2-9. Analog Output Connections

Digital I/O

The NI PXI-7831R has 96 bidirectional DIO lines that can be individually configured for either input or output. When the system powers on, the DIO lines are all high-impedance. To set another power-on state, you can configure the NI PXI-7831R to automatically load a VI when the system powers on. This VI can then set the DIO lines to any desired power-on state.

Connecting Digital I/O Signals

The DIO signals on the NI PXI-7831R MIO connector are DGND and DIO<0..15>. The DIO signals on the NI PXI-7831R DIO connector are DGND and DIO<0..39>. DIO<0..*n*> are the signals making up the DIO port, and DGND is the ground reference signal for the DIO port. The NI PXI-7831R has one MIO and two DIO connectors for a total of 96 DIO lines.

Refer to Figure B-1, *NI PXI-7831R Connector Locations*, and Figure B-2, *NI PXI-7831R I/O Connector Pin Assignments*, for the connector locations and the I/O connector pin assignments on the NI PXI-7831R.

The DIO lines on the NI PXI-7831R are TTL compatible. When configured as inputs, they can receive signals from 5 V TTL, 3.3 V LVTTL, 5 V CMOS, and 3.3 V LVCMOS devices. When configured as outputs, they can send signals to 5 V TTL, 3.3 V LVTTL, and 3.3 V LVCMOS

devices. Because the NI PXI-7831R digital outputs provide a nominal output swing of 0 to 3.3 V (3.3 V TTL), the NI PXI-7831R DIO lines cannot drive 5 V CMOS logic levels. To interface to 5 V CMOS devices, you must provide an external pull-up resistor to 5 V. This resistor pulls up the 3.3 V digital output from the NI PXI-7831R to 5 V CMOS logic levels. For detailed DIO specifications, refer to Appendix A, *Specifications*.

Cautions Exceeding the maximum input voltage ratings, which are listed in Table B-2, *NI PXI-7831R I/O Signal Summary*, can damage the NI PXI-7831R and the computer. NI is *not* liable for any damage resulting from such signal connections.

Do *not* short the DIO lines of the NI PXI-7831R directly to power or to ground. Doing so can damage the NI PXI-7831R by causing excessive current to flow through the DIO lines. Refer to Appendix A, *Specifications*, for more information. NI is *not* liable for any damage resulting from such signal connections.

If required by your application, you can connect multiple NI PXI-7831R digital output lines in parallel to provide higher current sourcing or sinking capability. If you connect multiple digital output lines in parallel, your application must drive all of these lines simultaneously to the same value. If you connect digital lines together and drive them to different values, excessive current may flow through the DIO lines and damage the NI PXI-7831R. Refer to Appendix A, *Specifications*, for more information. NI is *not* liable for any damage resulting from such signal connections.

Figure 2-10 shows signal connections for three typical DIO applications.

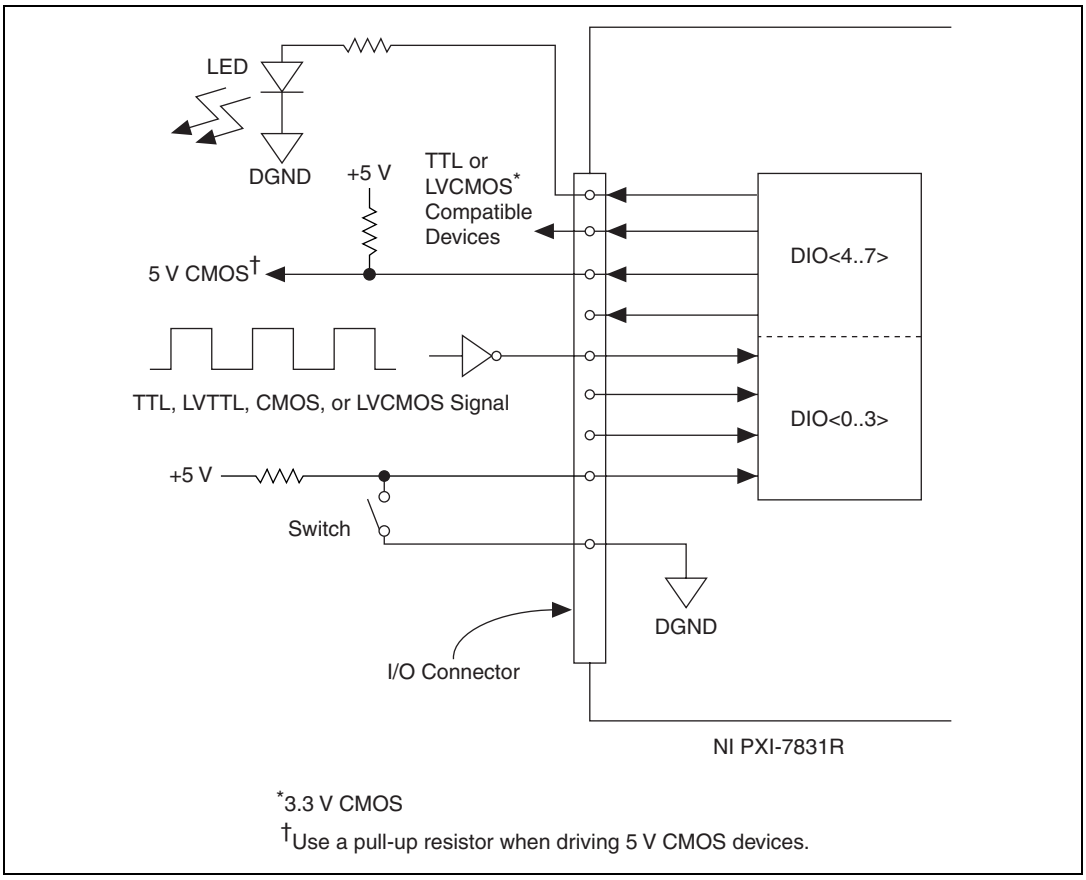


Figure 2-10. Example Digital I/O Connections

Figure 2-10 shows DIO<0..3> configured for digital input and DIO<4..7> configured for digital output. Digital input applications include receiving TTL, LVTTL, CMOS, or LVCMOS signals and sensing external device states, such as the state of the switch shown in the figure. Digital output applications include sending TTL or LVCMOS signals and driving external devices, such as the LED shown in the figure.

The NI PXI-7831R SH68-C68-S shielded cable contains 34 twisted pairs of conductors. To maximize the digital I/O available on the NI PXI-7831R, some of the DIO lines are twisted with power or ground as they are run through the cable, and some DIO lines are twisted with other DIO lines as they are run through the cable. To obtain maximum signal integrity, place

edge-sensitive or high-frequency digital signals on the DIO lines that are paired with power or ground. Because the DIO lines that are twisted with other DIO lines can couple noise onto each other, these lines should be used for static signals or for non-edge-sensitive, low-frequency digital signals. Examples of high-frequency or edge-sensitive signals include clock, trigger, pulse-width modulation (PWM), encoder, and counter signals. Examples of static signals or non-edge-sensitive, low-frequency signals include LEDs, switches, and relays. Table 2-4 summarizes these guidelines.

Table 2-4. DIO Signal Guidelines for the NI PXI-7831R

Digital Lines	SH68-C68-S Shielded Cable Signal Pairing	Recommended Types of Digital Signals
Connector 0, DIO<0..7>; Connector 1, DIO<0..27>; Connector 2, DIO<0..27>	DIO line paired with power or ground	All types (high frequency or low frequency signals, edge-sensitive or non-edge-sensitive signals)
Connector 0, DIO<8..15>; Connector 1, DIO<28..39>; Connector 2, DIO<28..39>	DIO line paired with another DIO line	Static signals or non-edge-sensitive, low-frequency signals

PXI Trigger Bus

The NI PXI-7831R can send and receive triggers through the PXI trigger bus, which provides eight trigger lines that link all PXI slots in a bus segment. These trigger lines connect to the FPGA on the NI PXI-7831R and can be used just like any of the other NI PXI-7831R DIO lines. The PXI trigger lines can be used to synchronize an NI PXI-7831R to any other device that supports PXI triggers. The PXI trigger lines on the NI PXI-7831R are PXI/TRIG<0..7>. In addition, the NI PXI-7831R can use the PXI star trigger line to send or receive triggers from a device plugged into slot 2 of the PXI chassis. The PXI star trigger line on the NI PXI-7831R is PXI/STAR.

The PXI-7831R can configure each PXI trigger line either as an input or an output signal. Since each PXI trigger line in the PXI trigger bus is connected in parallel to all the PXI slots in a bus segment, only one PXI device can drive a particular PXI trigger line at a time. For example, if one NI PXI-7831R is configured to send out a trigger pulse on PXI/TRIG<0>, the remaining devices on that PXI bus segment must have PXI/TRIG<0> configured as an input.

Caution Do *not* drive the same PXI trigger bus line on the same PXI bus segment with the NI PXI-7831R and another device simultaneously. Such signal driving can damage both devices. NI is *not* liable for any damage resulting from such signal driving.

Refer to the *PXI Hardware Specification Revision 2.1* and *PXI Software Specification Revision 2.1* at `www.pxisa.org` for more information about PXI triggers.

PXI Local Bus

The NI PXI-7831R can communicate with other PXI devices using the PXI local bus. The PXI local bus is a daisy-chained bus that connects each PXI peripheral slot with its adjacent peripheral slot on either side. For example, the right local bus lines from a given PXI peripheral slot connect to the left local bus lines of the adjacent slot. Each local bus is 13 lines wide. All of these lines connect to the FPGA on the NI PXI-7831R and can be used like any of the other NI PXI-7831R DIO lines. The PXI local bus right lines on the NI PXI-7831R are PXI/LBR<0..12>. The PXI local bus left lines on the NI PXI-7831R are PXI/LBLSTAR<0..12>.

The NI PXI-7831R can configure each PXI local bus line either as an input or an output signal. Only one device can drive the same physical local bus line at a given time. For example, if an NI PXI-7831R is configured to drive a signal on PXI/LBR<0>, the device in the slot immediately to the right must have its PXI/LBLSTAR<0> line configured as an input.

Caution Do *not* drive the same PXI local bus line with the NI PXI-7831R and another device simultaneously. Such signal driving can damage both devices. NI is *not* liable for any damage resulting from such signal driving.

The NI PXI-7831R local bus lines are only compatible with 3.3 V signaling LVTTL and LVCMOS levels.

Caution Do *not* enable the local bus lines on an adjacent device if the device drives anything other than 0–3.3V LVTTL signal levels on the NI PXI-7831R. Enabling the lines in this way can damage the NI PXI-7831R. NI is *not* liable for any damage resulting from enabling such lines.

The left local bus lines from the left peripheral slot of a PXI backplane (slot 2) are routed to the star trigger lines of up to 13 other peripheral slots in a two-segment PXI system. This configuration provides a dedicated, delay-matched trigger signal between the first peripheral slot and the

other peripheral slots and results in very precise trigger timing signals. For example, an NI PXI-7831R in slot 2 can send out an independent trigger signal to each device plugged into slots <3..15> using the PXI/LBLSTAR<0..12>. Each device receives its trigger signal on its own dedicated star trigger line.

Caution Do *not* configure the NI PXI-7831R and another device to drive the same physical star trigger line simultaneously. Such signal driving can damage the NI PXI-7831R and the other device. NI is *not* liable for any damage resulting from such signal driving.

Refer to the *PXI Hardware Specification Revision 2.1* and *PXI Software Specification Revision 2.1* at `www.pxisa.org` for more information about PXI triggers.

Switch Settings

Refer to Figure 2-2 for the location of switch SW1. For normal operation, switch 1 is in the OFF position. To prevent a VI stored in flash memory from loading to the FPGA upon power up, you can move switch 1 to the ON position, as shown in Figure 2-11.

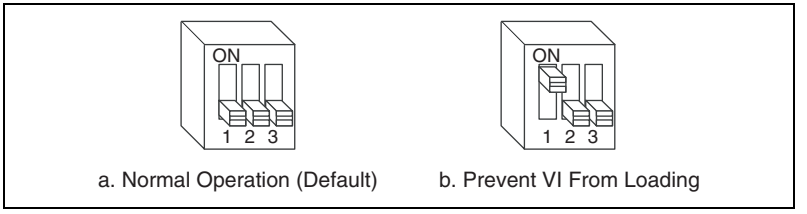


Figure 2-11. Switch Settings on Switch SW1

To move switch 1 to the ON position, complete the following steps:

1. Power off and unplug the PXI/CompactPCI chassis.
2. Remove the NI PXI-7831R.
3. Move switch 1 to the ON position, as shown in Figure 2-11.
4. Refer to the *Installing the Hardware* section of the *Where to Start with the NI PXI-7831R* document for installation instructions for reinserting the NI PXI-7831R into the PXI/CompactPCI chassis.
5. Plug in and power on the PXI/CompactPCI chassis.

After completing this procedure, a VI stored in flash memory does not load to the FPGA on power up. You can use software to reconfigure the NI PXI-7831R if necessary. To return to the default mode of loading from

flash memory, repeat the procedure above but return switch 1 to the OFF position in step 3.

Note When the NI PXI-7831R is powered on with switch 1 in the ON position, the analog circuitry does not return properly calibrated data. For this reason, the switch should only be switched to the ON position while you are using software to reconfigure the NI PXI-7831R for the desired power-up behavior. Afterwards, you should return switch 1 to the OFF position.

Power Connections

Two pins on each I/O connector supply +5 V from the computer power supply using a self-resetting fuse. The fuse resets automatically within a few seconds after the overcurrent condition is removed. The +5 V pins are referenced to DGND and can be used to power external digital circuitry.

Power rating ..... +4.65 to +5.25 VDC at 1 A
(250 mA max per 5 V pin,
1 A max total for all +5 V lines
on the device)

Caution Do *not* connect the +5 V power pins directly to analog or digital ground or to any other voltage source on the NI PXI-7831R or any other device under any circumstance. Doing so can damage the NI PXI-7831R and the computer. NI is *not* liable for damage resulting from such a connection.

Field Wiring Considerations

Environmental noise can seriously affect the accuracy of measurements made with the NI PXI-7831R if you do not take proper care when running signal wires between signal sources and the device. The following recommendations mainly apply to AI signal routing to the device, although they also apply to signal routing in general.

Minimize noise pickup and maximize measurement accuracy by taking the following precautions:

- Use differential AI connections to reject common-mode noise.
- Use individually shielded, twisted-pair wires to connect AI signals to the device. With this type of wire, the signals attached to the AI+ and AI– inputs are twisted together and then covered with a shield. You then connect this shield only at one point to the signal source ground. This kind of connection is required for signals traveling

through areas with large magnetic fields or high electromagnetic interference.

- Route signals to the device carefully. Keep cabling away from noise sources. The most common noise source in a PXI DAQ system is the video monitor. Separate the monitor from the analog signals as much as possible.

The following recommendations apply for all signal connections to the NI PXI-7831R:

- Separate NI PXI-7831R signal lines from high-current or high-voltage lines. These lines can induce currents in or voltages on the NI PXI-7831R signal lines if they run in parallel paths at a close distance. To reduce the magnetic coupling between lines, separate them by a reasonable distance if they run in parallel, or run the lines at right angles to each other.
- Do *not* run signal lines through conduits that also contain power lines.
- Protect signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running them through special metal conduits.

Refer to the NI Developer Zone tutorial, *Field Wiring and Noise Considerations for Analog Signals*, at `ni.com/zone` for more information.

3

Calibration

Calibration refers to the process of minimizing measurement and output voltage errors. On the NI PXI-7831R, these errors are corrected in the analog circuitry by onboard calibration DACs (CalDACs). Because calibration is handled by the analog circuitry, the data read from the AI channels or written to the AO channels in the FPGA VI is already calibrated.

Three levels of calibration are available for the NI PXI-7831R to ensure the accuracy of its analog circuitry. The first level, loading calibration constants, is the fastest, easiest, and least accurate. The intermediate level, internal calibration, is the preferred method of assuring accuracy in your application. The last level, external calibration, is the slowest, most difficult, and most accurate.

Loading Calibration Constants

The NI PXI-7831R is factory calibrated before shipment at approximately 25 °C to the levels indicated in Appendix A, *Specifications*. The associated calibration constants (the values that were written to the CalDACs to achieve calibration in the factory) are stored in the onboard nonvolatile flash memory. These constants are automatically read from the flash memory and loaded into the CalDACs by the NI PXI-7831R hardware on power-up. This occurs before a VI is loaded into the FPGA.

Internal Calibration

The NI PXI-7831R can measure and correct for almost all of its calibration-related errors without any external signal connections. This calibration method is referred to as internal calibration. NI provides software to perform an internal calibration. This internal calibration process, which generally takes less than two minutes, is the preferred method of assuring accuracy in your application. Initiate an internal calibration to minimize the effects of any offset and gain drifts, particularly those due to changes in temperature. During the internal calibration process, the AI and AO channels are compared to the NI PXI-7831R

onboard voltage reference. The offset and gain errors in the analog circuitry are calibrated out by adjusting the CalDACs to minimize these errors.

Immediately after internal calibration, the only significant residual calibration error should be gain error due to time and temperature drift of the onboard voltage reference. This error is addressed by external calibration, which is discussed in the *External Calibration* section. If you are interested primarily in relative measurements, you can ignore a small amount of gain error, and self-calibration should be sufficient.

The results of an internal calibration can be stored in the flash memory on the NI PXI-7831R so that the CalDACs are automatically loaded with the newly calculated calibration constants the next time the NI PXI-7831R is powered on.

External Calibration

The NI PXI-7831R has an onboard calibration reference to ensure the accuracy of self-calibration. Its specifications are listed in Appendix A, *Specifications*. The reference voltage is measured at the factory and stored in the flash memory for subsequent internal calibrations. This voltage is stable enough for most applications, but if you are using your device at an extreme temperature or if the onboard reference has not been measured for a year or more, you may want to externally calibrate your device.

An external calibration refers to calibrating your device with a known external reference rather than relying on the onboard reference. During the external calibration process, the onboard reference value is re-calculated. This compensates for any time or temperature drift related errors in the onboard reference, which may have resulted since the last calibration. You can save the results of the external calibration process to flash memory so that the new calibration constants are automatically loaded the next time the NI PXI-7831R is powered on and so that the newly measured onboard reference level is used for subsequent internal calibrations.

To externally calibrate your device, be sure to use a very accurate external reference. The reference should be several times more accurate than the device itself.

For a detailed calibration procedure for the NI PXI-7831R, refer to the *NI PXI-7831R Calibration Procedure* by clicking **Manual Calibration Procedures** at `ni.com/calibration`.

A

Specifications

This appendix lists the specifications of the NI PXI-7831R. These specifications are typical at 25 °C unless otherwise noted.

Analog Input

Input Characteristics

Number of channels 8

Input modes ..... DIFF, RSE, NRSE (software-selectable; selection applies to all 8 channels)

Type of ADC ..... Successive approximation

Resolution ..... 16 bits, 1 in 65,536

Conversion time ..... 4 µs

Maximum sampling rate ..... 200 kS/s (per channel)

Input impedance

- Powered on ..... 10 GΩ in parallel with 100 pF
- Powered off ..... 4 kΩ min
- Overload ..... 4 kΩ min

Input signal range ..... ±10 V

Input bias current ..... ±2 nA

Input offset current ..... ±1 nA

Input coupling ..... DC

Maximum working voltage (signal + common mode) ..... Inputs should remain within ±12 V of ground

Overvoltage protection .....±42 V

Data transfers .....Interrupts, programmed I/O

Accuracy Information

Nominal Range (V)		Absolute Accuracy							Relative Accuracy	
		% of Reading			Noise + Quantization (µV)			Absolute Accuracy at Full Scale (±mV)	Resolution (µV)	
Positive Full Scale	Negative Full Scale	24 Hours	1 Year	Offset (µV)	Single Pt.	Averaged	Temp Drift (%/ °C)		Single Pt.	Averaged
10.0	–10.0	0.0496	0.0507	2542	1779	165	0.0005	7.78	2170	217

Note: Accuracies are valid for measurements following an internal calibration. Measurement accuracies are listed for operational temperatures within ±1 °C of internal calibration temperature and ±10 °C of external or factory-calibration temperature. Temp drift applies only if ambient is greater than ±10 °C of previous external calibration.

DC Transfer Characteristics

INL.....±3 LSB typ, ±6 LSB max

DNL .....–1.0 to +2.0 LSB max

No missing codes resolution.....16 bits typ, 15 bits min

CMRR, DC to 60 Hz .....86 dB

Dynamic Characteristics

Bandwidth

Small signal (–3 dB).....820 kHz

Large signal (1% THD).....55 kHz

System noise .....1.8 LSB_{rms} (including quantization)

Settling time

Step Size	Accuracy		
	16 LSB	4 LSB	2 LSB
±20.0 V	7.5 µs	10.3 µs	40 µs
±2.0 V	2.7 µs	4.1 µs	5.1 µs
±0.2 V	1.7 µs	2.9 µs	3.6 µs

Crosstalk..... –80 dB, DC to 100 kHz

Analog Output

Output Characteristics

Number of channels ..... 8 single-ended, voltage output

Resolution ..... 16 bits, 1 in 65,536

Update time ..... 1.0 µs

Max update rate..... 1 MS/s

Type of DAC..... Enhanced R-2R

Data transfers ..... Interrupts, programmed I/O

Accuracy Information

Nominal Range (V)		Absolute Accuracy				Absolute Accuracy at Full Scale (mV)
		% of Reading				
Positive Full Scale	Negative Full Scale	24 Hours	1 Year	Offset (µV)	Temp Drift (%/ °C)	
10.0	–10.0	0.0335	0.0351	2366	0.0005	5.88

Note: Accuracies are valid for analog output following an internal calibration. Analog output accuracies are listed for operation temperatures within ±1 °C of internal calibration temperature and ±10 °C of external or factory calibration temperature. Temp Drift applies only if ambient is greater than ±10 °C of previous external calibration.

DC Transfer Characteristics

INL.....±0.5 LSB typ, ±4.0 LSB max

DNL.....±0.5 LSB typ, ±1 LSB max

Monotonicity .....16 bits, guaranteed

Voltage Output

Range.....±10 V

Output coupling .....DC

Output impedance.....1.25 Ω max

Current drive.....±5 mA

Protection .....Short-circuit to ground

Power-on state .....User configurable

Dynamic Characteristics

Settling time

Step Size	Accuracy		
	16 LSB	4 LSB	2 LSB
±20.0 V	6.0 µs	6.2 µs	7.2 µs
±2.0 V	2.2 µs	2.9 µs	3.8 µs
±0.2 V	1.5 µs	2.6 µs	3.6 µs

Slew rate .....10 V/µs

Noise.....150 μV_{rms}, DC to 1 MHz

Glitch energy
at midscale transition .....±100 mV for 3 µs

Digital I/O

Number of channels

NI PXI-7831R ..... 96 input/output

Compatibility ..... TTL

Digital logic levels

Level	Min	Max
Input low voltage (V_{IL})	0.0 V	0.8 V
Input high voltage (V_{IH})	2.0 V	5.5 V
Output low voltage (V_{OL}), where $I_{OUT} = -I_{max}$ (sink)	—	0.4 V
Output high voltage (V_{OH}), where $I_{OUT} = I_{max}$ (source)	2.4 V	—

Maximum output current

Driver Type (Software Selectable)	I_{max} (Source)	I_{max} (Sink)
Default	5.4 mA	5.0 mA
Slow	1.9 mA	1.9 mA
Fast	16 mA	14 mA

Power-on state ..... Programmable, by line

Data transfers ..... Interrupts, programmed I/O

Protection

Input ..... –0.5 to 7.0 V

Output ..... Short-circuit (up to eight lines may be shorted at a time)

Reconfigurable FPGA

Number of logic slices 5, 120

Equivalent number of logic cells 11, 520

Available embedded RAM..... 16, 384 KB

Timebase ..... 40 MHz

Timebase accuracy

With onboard base clock .....±100 ppm

Phase locked
to PXI 10 MHz clock.....±350 ps jitter, 300 ps skew (max)

Calibration

Recommended warm-up time.....15 minutes

Calibration interval .....1 year

Onboard calibration reference

DC level.....5.000 V (±3.5 mV)
(actual value stored
in flash memory)

Temperature coefficient.....±5 ppm/°C max

Long-term stability .....±20 ppm/$\sqrt{1{,}000\ \text{h}}$

Note To generate a calibration certificate for the NI PXI-7831R, click **On-line Calibration Certificates** at `ni.com/calibration`.

Bus Interface

PXI.....Master, slave

Power Requirement

+5 VDC (±5%)

NI PXI-7831R .....450 mA (typ), 700 mA (max)
(does not include current drawn
from the +5 V line on the
I/O connectors)

+3.3 VDC (±5%)

NI PXI-7831R .....335 mA (typ), 730 mA (max)

Power available at I/O connectors .....+4.65 to +5.25 VDC at 1 A total,
250 mA per I/O connector pin

Physical

Dimensions
(not including connectors) ..... 16.0 by 10.0 cm (6.3 by 3.9 in.)

I/O connectors

NI PXI-7831R ..... Three 68-pin female high-density VHDCI type

Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Channel-to-earth..... ±12 V, Installation Category I

Channel-to-channel ..... ±24 V, Installation Category I

Environmental

Operating temperature..... –40 to 70 °C

Storage temperature ..... –55 to 85 °C

Humidity ..... 10 to 90% RH, noncondensing

Maximum altitude ..... 2,000 meters

Pollution Degree (indoor use only)..... 2

Safety

The NI PXI-7831R devices meet the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 3111-1
- CAN/CSA C22.2 No. 1010.1

Note For UL and other safety certifications, refer to the product label or to `ni.com`.

Electromagnetic Compatibility

Emissions.....EN 55011 Class A at 10 m
FCC Part 15A above 1 GHz

Immunity .....EN 61326-1:1997 + A2:2001, Table 1

EMC/EMI .....CE, C-Tick, and FCC Part 15 (Class A) Compliant

Note For EMC compliance, you *must* operate this device with shielded cabling.

CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

Low-Voltage Directive (safety).....73/23/EEC

Electromagnetic Compatibility Directive (EMC).....89/336/EEC

Note Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, click **Declaration of Conformity Information** at `ni.com/hardref.nsf/`.

B

Connecting I/O Signals

This appendix describes how to make input and output signal connections to the NI PXI-7831R I/O connectors.

The NI PXI-7831R has two DIO connectors with 40 DIO lines per connector, and one MIO connector with eight AI lines, eight AO lines, and 16 DIO lines.

Figure B-1 shows the I/O connector locations for the NI PXI-7831R. The I/O connectors are numbered starting at zero. The text in parentheses indicates whether each I/O connector is an MIO connector or a DIO connector.

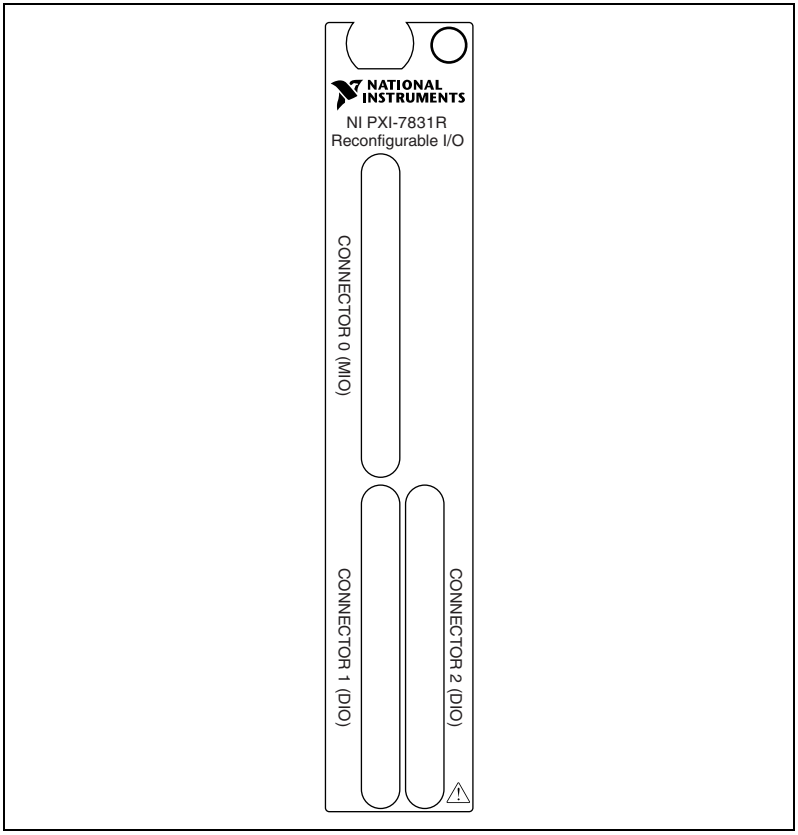


Figure B-1. NI PXI-7831R Connector Locations

Figure B-2 shows the I/O connector pin assignments for the I/O connectors on the NI PXI-7831R. The DIO connector pin assignment applies to connectors<1..2> on the NI PXI-7831R. The MIO connector pin assignment applies to connector 0 on the NI PXI-7831R.

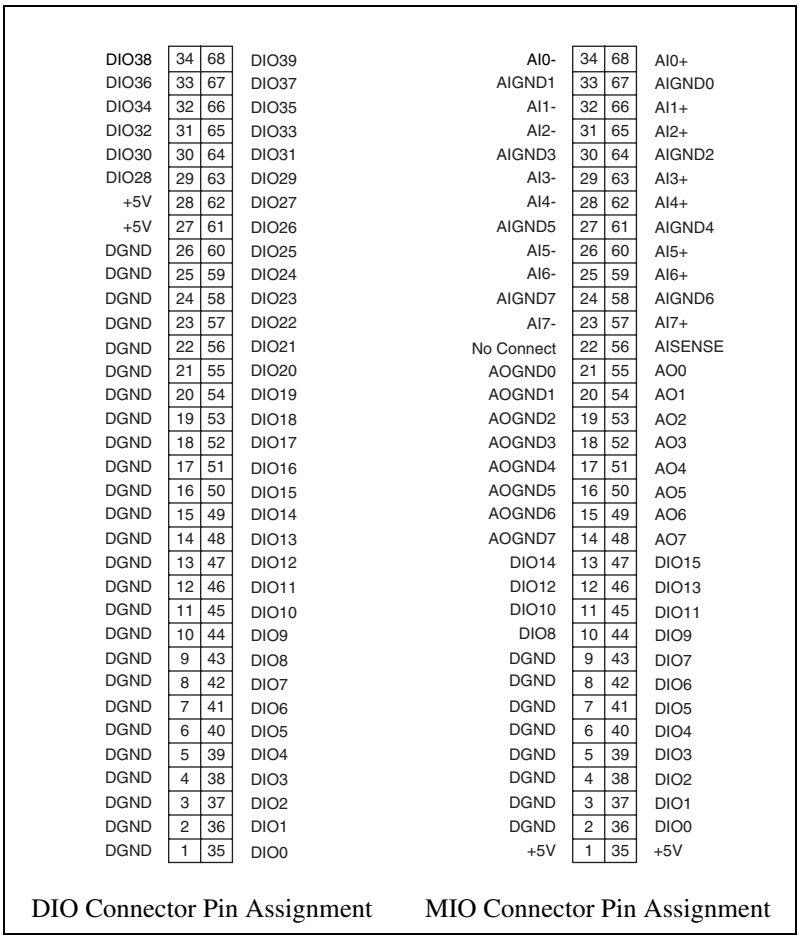


Figure B-2. NI PXI-7831R I/O Connector Pin Assignments

To access the signals on the I/O connectors, you must connect a cable from the I/O connector to a signal accessory. Plug the small VHDCI connector end of the cable into the appropriate I/O connector, and connect the other end of the cable to the appropriate signal accessory.

Table B-1. I/O Connector Signal Descriptions

Signal Name	Reference	Direction	Description
+5V	DGND	Output	+5 VDC Source—These pins supply +5 V from the computer power supply using a self-resetting 1 A fuse. No more than 250 mA should be pulled from a single pin.
AI<0..7>+	AIGND	Input	Positive Input for Analog Channels 0 through 7.
AI<0..7>–	AIGND	Input	Negative Input for Analog Channels 0 through 7.
AIGND	—	—	Analog Input Ground—These pins are the reference point for single-ended measurements in RSE configuration and the bias current return point for differential measurements. All three ground references—AIGND, AOGND, and DGND—are connected together on the NI PXI-7831R.
AISENSE	AIGND	Input	Analog Input Sense—This pin serves as the reference node for channels AI<0..7> when the device is configured for NRSE mode.
AO<0..7>	AOGND	Output	Analog Output Channels 0 through 7. Each channel can source or sink up to 5 mA.
AOGND	—	—	Analog Output Ground—The analog output voltages are referenced to this node. All three ground references—AIGND, AOGND, and DGND—are connected together on the NI PXI-7831R.
DGND	—	—	Digital Ground—These pins supply the reference for the digital signals at the I/O connector as well as the +5 V supply. All three ground references—AIGND, AOGND, and DGND—are connected together on the NI PXI-7831R.
DIO<0..15> Connector 0 DIO<0..39> Connector<1..2>	DGND	Input or Output	Digital I/O signals.

Caution Connections that exceed any of the maximum ratings of input or output signals on the NI PXI-7831R can damage the NI PXI-7831R and the computer. Maximum input ratings for each signal are given in the *Protection* column of Table B-2. NI is *not* liable for any damage resulting from such signal connections

Table B-2. NI PXI-7831R I/O Signal Summary

Signal Name	Driver Type	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time	Bias
+5V	—	DO	—	—	—	—	—	—
AI<0..7>+	—	AI	10 GΩ in parallel with 100 pF	42/35	—	—	—	±2 nA
AI<0..7>–	—	AI	10 GΩ in parallel with 100 pF	42/35	—	—	—	±2 nA
AIGND	—	AO	—	—	—	—	—	—
AISENSE	—	AI	10 GΩ in parallel with 100 pF	42/35	—	—	—	±2 nA
AO<0..7>	—	AO	1.25 Ω	Short-circuit to ground	5 at 10	5 at –10	10 V/µs	—
AOGND	—	AO	—	—	—	—	—	—
DGND	—	DO	—	—	—	—	—	—
DIO<0..15> Connector 0 DIO<0..39> Connector<1..2>	Default	DIO	—	–0.5 to +7.0	5.4 at 2.4	5.0 at 0.4	12 ns	—
	Slow	DIO	—	–0.5 to +7.0	1.9 at 0.4	1.9 at 0.4	75 ns	—
	Fast	DIO	—	–0.5 to +7.0	16 at 2.4	14 at 0.4	6 ns	—

AI = Analog Input AO = Analog Output DIO = Digital Input/Output DO = Digital Output

Connecting to 5B and SSR Signal Conditioning

NI provides cables that allow you to connect signals from the NI PXI-7831R directly to 5B backplanes for analog signal conditioning and SSR backplanes for digital signal conditioning.

The NSC68-262650 cable is designed to connect the signals on the NI PXI-7831R MIO connector directly to 5B and SSR backplanes. This cable has a 68-pin male VHDCI connector on one end that plugs into the NI PXI-7831R MIO connector. The other end of this cable provides two 26-pin female headers plus one 50-pin female header.

One of the 26-pin headers contains all the NI PXI-7831R analog input signals. This connector can be plugged directly into a 5B backplane for analog input signal conditioning. The NI PXI-7831R AI channels <0..7> are mapped to the 5B backplane channels <0..7> in sequential order. The AI channels should be configured to use the NRSE input mode when using 5B signal conditioning.

The other 26-pin header contains all the NI PXI-7831R analog output signals. This connector can be plugged directly into a 5B backplane for AO signal conditioning. The NI PXI-7831R AO channels <0..7> are mapped to the 5B backplane channels <0..7> in sequential order.

The 50-pin header contains the 16 DIO lines available on the NI PXI-7831R MIO connector. This header can be plugged directly into an SSR backplane for digital signal conditioning. DIO lines <0..15> are mapped to the 5B backplane slots <0..15> in sequential order.

The 5B connector pinouts are compatible with 8-channel 5B08 backplanes and 16-channel 5B01 backplanes, but since the NI PXI-7831R only provides 8 AI channels, you only have access to the first 8 channels in a 16-channel backplane. The SSR connector pinout is compatible with 8, 16, 24, and 32-channel SSR backplanes. You can connect to an SSR backplane containing a number of channels that does not equal the 16 DIO lines available on the 50-pin header. In this case, you only have access to the channels that exist on both the SSR backplane and the NSC68-262650 cable 50-pin header.

Figure B-3 shows the connector pinouts when using the NSC68-262650 cable.

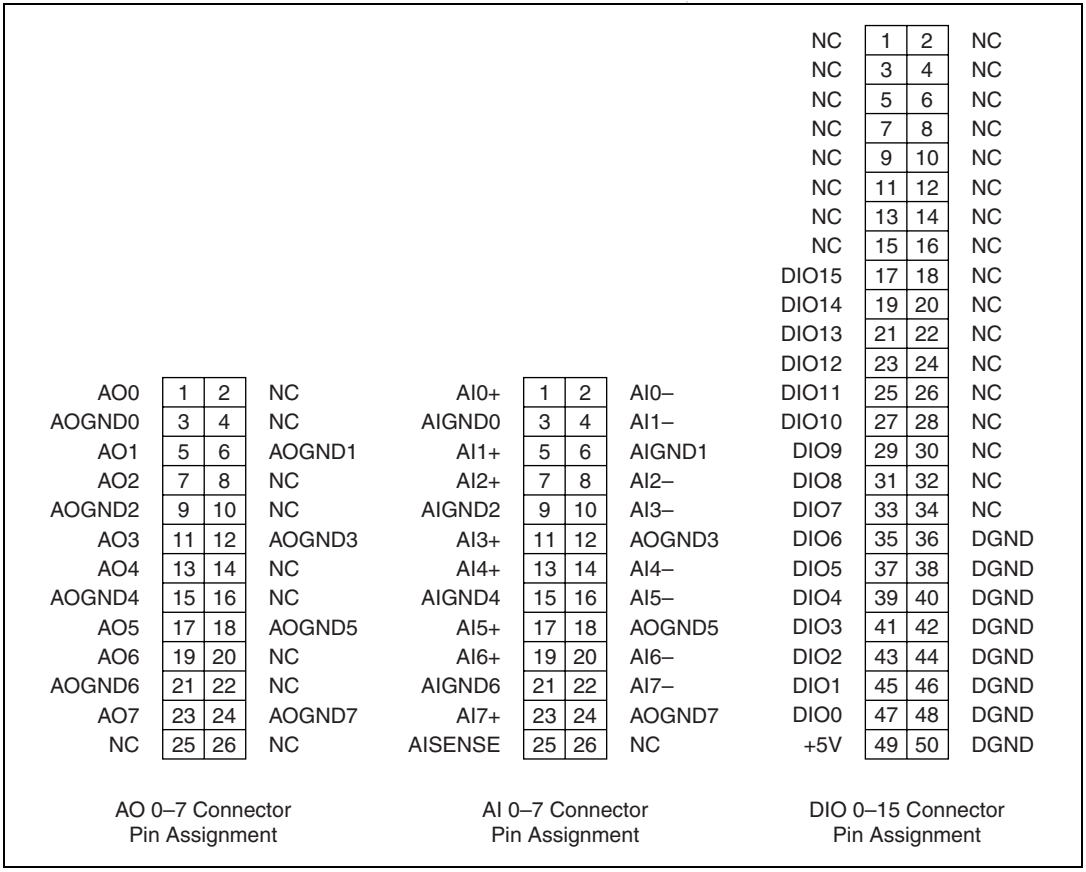


Figure B-3. Connector Pinouts When Using NSC68-262650 Cable

The NSC68-5050 cable is designed to connect the signals on the NI PXI-7831R DIO connectors directly to SSR backplanes for digital signal conditioning. This cable has a 68-pin male VHDCI connector on one end that plugs into the NI PXI-7831R DIO connectors. The other end of this cable provides two 50-pin female headers.

Each of these 50-pin headers can be plugged directly into an 8-, 16-, 24-, or 32-channel SSR backplane for digital signal conditioning. One of the 50-pin headers contains DIO lines 0–23 from the NI PXI-7831R DIO connector. These lines are mapped to slots 0–23 on an SSR backplane in sequential order. The other 50-pin header contains DIO lines 24–39 from the NI PXI-7831R DIO connector. These lines are mapped to slots 0–15 on an SSR backplane in sequential order. You can connect to an SSR backplane containing a number channels that does not equal the number of

lines on the NSC68-5050 cable header. In this case, you only have access to the channels that exist on both the SSR backplane and the NSC68-5050 cable header you are using.

Figure B-4 shows the connector pinouts when using the NSC68-5050 cable.

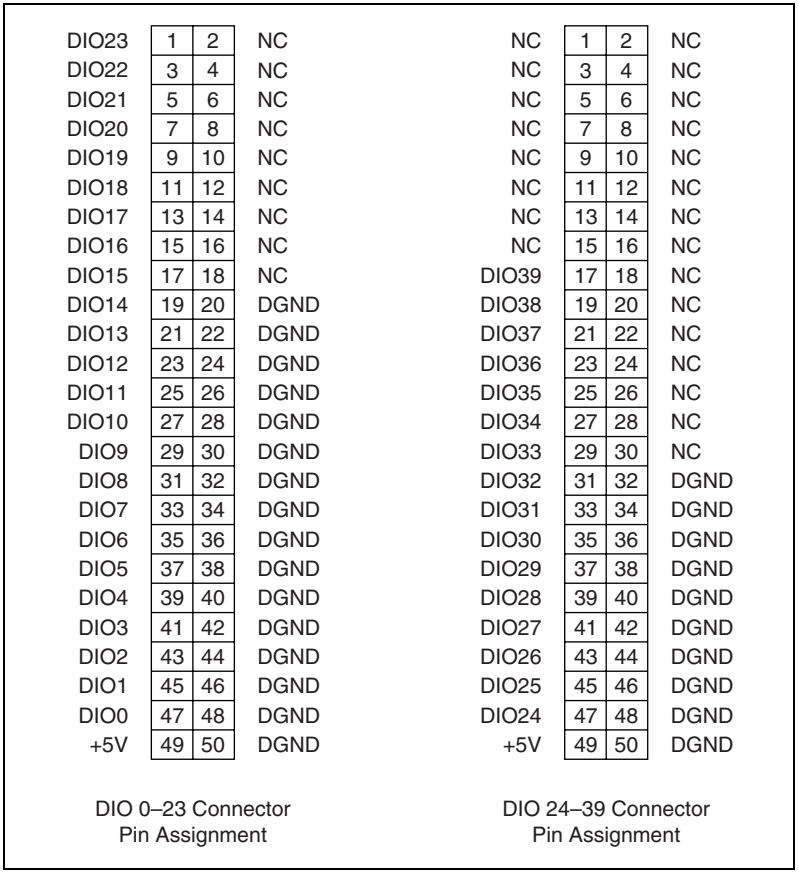


Figure B-4. Connector Pinouts When Using the NSC68-5050 Cable

C

Using the SCB-68 Shielded Connector Block

This appendix describes how to connect input and output signals to the NI PXI-7831R with the SCB-68 shielded connector block.

The SCB-68 has 68 screw terminals for I/O signal connections. To use the SCB-68 with the NI PXI-7831R, you must configure the SCB-68 as a general-purpose connector block. Refer to Figure C-1 for the general-purpose switch configuration.

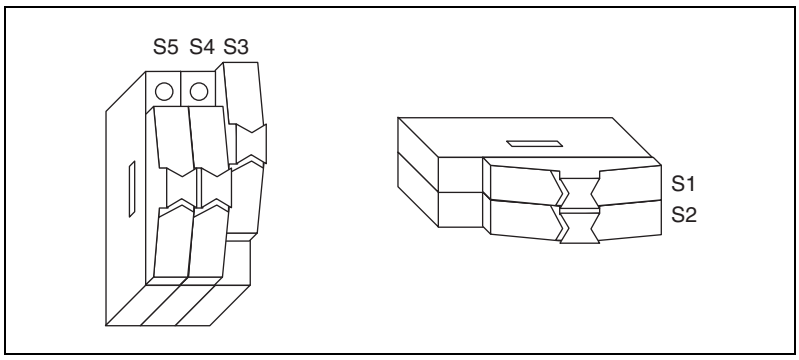


Figure C-1. General-Purpose Switch Configuration for the SCB-68 Terminal Block

After configuring the SCB-68 switches, you can connect the I/O signals to the SCB-68 screw terminals. Refer to Appendix B, *Connecting I/O Signals*, for the connector pin assignments for the NI PXI-7831R. After connecting I/O signals to the SCB-68 screw terminals, you can connect the SCB-68 to the NI PXI-7831R with the SH68-C68-S shielded cable.

Quick Reference Label

Figure C-2 shows the pinout that appears on the SCB-68 quick reference label that ships with the NI PXI-7831R.

SCB-68 Quick Reference Label

NATIONAL INSTRUMENTS

NI 7811R/7831R DEVICES[1]

PIN#	MIO	DIO	PIN#	MIO	DIO	PIN#	MIO	DIO
68	AI0+	DIO39						
34	AI0-	DIO38	12	DIO12	DGND	1	+5V	DGND
67	AIGND0	DIO37	46	DIO13	DIO11	35	+5V	DIO0
33	AIGND1	DIO36	13	DIO14	DGND	2	DGND	DGND
66	AI1+	DIO35	47	DIO15	DIO12	36	DIO0	DIO1
32	AI1-	DIO34	14	AOGND7	DGND	3	DGND	DGND
65	AI2+	DIO33	48	AO7	DIO13	37	DIO1	DIO2
31	AI2-	DIO32	15	AOGND6	DGND	4	DGND	DGND
64	AIGND2	DIO31	49	AO6	DIO14	38	DIO2	DIO3
30	AIGND3	DIO30	16	AOGND5	DGND	5	DGND	DGND
63	AI3+	DIO29	50	AO5	DIO15	39	DIO3	DIO4
29	AI3-	DIO28	17	AOGND4	DGND	6	DGND	DGND
62	AI4+	DIO27	51	AO4	DIO16	40	DIO4	DIO5
28	AI4-	+5V	18	AOGND3	DGND	7	DGND	DGND
61	AIGND4	DIO26	52	AO3	DIO17	41	DIO5	DIO6
27	AIGND5	+5V	19	AOGND2	DGND	8	DGND	DGND
60	AI5+	DIO25	53	AO2	DIO18	42	DIO6	DIO7
26	AI5-	DGND	20	AOGND0	DGND	9	DGND	DGND
59	AI6+	DIO24	54	AO1	DIO19	43	DIO7	DIO8
25	AI6-	DGND	21	AOGND0	DGND	10	DIO8	DGND
58	AIGND6	DIO23	55	AO0	DIO20	44	DIO9	DIO9
24	AIGND7	DGND	22	NC	DGND	11	DIO10	DGND
57	AI7+	DIO22	56	AISENSE	DIO21	45	DIO11	DIO10
23	AI7-	DGND						

[1] THE MIO COLUMN CORRESPONDS TO THE MIO CONNECTOR ON THE NI 7831R, AND THE DIO COLUMN CORRESPONDS TO THE DIO CONNECTORS ON THE NI 7811R / 7831R.

NC = No Connect

SET SWITCHES IN THIS CONFIGURATION TO USE THE SCB-68 WITH THE NI 7811R/7831R

Figure C-2. SCB-68 Quick Reference Label for the NI PXI-7831R

D

Technical Support and Professional Services

Visit the following sections of the National Instruments Web site at ni.com for technical support and professional services:

- **Support**—Online technical support resources include the following:
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  - **Assisted Support Options**—Contact NI engineers and other measurement and automation professionals by visiting ni.com/support. Our online system helps you define your question and connects you to the experts by phone, discussion forum, or email.
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Glossary

Symbol	Prefix	Value
p	pico	10^{-12}
n	nano	10^{-9}
µ	micro	10^{-6}
m	milli	10^{-3}
k	kilo	10^{3}
M	mega	10^{6}
G	giga	10^{9}

Numbers/Symbols

°	Degrees.
>	Greater than.
≥	Greater than or equal to.
<	Less than.
≤	Less than or equal to.
–	Negative of, or minus.
Ω	Ohms.
/	Per.
%	Percent.
±	Plus or minus.
+	Positive of, or plus.

$\sqrt{\ }$	Square root of.
+5V	+5 VDC source signal.

A

A	Amperes.
A/D	Analog-to-digital.
AC	Alternating current.
ADC	Analog-to-digital converter—an electronic device, often an integrated circuit, that converts an analog voltage to a digital number.
AI	Analog input.
AI<*i*>	Analog input channel signal.
AIGND	Analog input ground signal.
AISENSE	Analog input sense signal.
AO	Analog output.
AO<*i*>	Analog output channel signal.
AOGND	Analog output ground signal.
ASIC	Application-Specific Integrated Circuit—a proprietary semiconductor component designed and manufactured to perform a set of specific functions.

B

bipolar	A signal range that includes both positive and negative values (for example, –5 to +5 V).

C

C	Celsius.
CalDAC	Calibration DAC.
CH	Channel—pin or wire lead to which you apply or from which you read the analog or digital signal. Analog signals can be single-ended or differential. For digital signals, you group channels to form ports. Ports usually consist of either four or eight digital channels.
cm	Centimeter.
CMOS	Complementary metal-oxide semiconductor.
CMRR	Common-mode rejection ratio—a measure of an instrument's ability to reject interference from a common-mode signal, usually expressed in decibels (dB).
common-mode voltage	Any voltage present at the instrumentation amplifier inputs with respect to amplifier ground.
CompactPCI	Refers to the core specification defined by the PCI Industrial Computer Manufacturer's Group (PICMG).

D

D/A	Digital-to-analog.
DAC	Digital-to-analog converter—an electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current.
DAQ	Data acquisition—a system that uses the computer to collect, receive, and generate electrical signals.
dB	Decibel—the unit for expressing a logarithmic measure of the ratio of two signal levels: dB = 20log10 V1/V2, for signals in volts.
DC	Direct current.
DGND	Digital ground signal.
DIFF	Differential mode.

DIO	Digital input/output.
DIO<*i*>	Digital input/output channel signal.
DMA	Direct memory access—a method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.
DNL	Differential nonlinearity—a measure in LSB of the worst-case deviation of code widths from their ideal value of 1 LSB.
DO	Digital output.

E

EEPROM	Electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed.

F

FPGA	Field-programmable gate array.
FPGA VI	A configuration that is downloaded to the FPGA and that determines the functionality of the hardware.

G

glitch	An unwanted signal excursion of short duration that is usually unavoidable.

H

h	Hour.
HIL	Hardware-in-the-loop.
Hz	Hertz.

I

I/O	Input/output—the transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces.
INL	Relative accuracy.

L

LabVIEW	Laboratory Virtual Instrument Engineering Workbench. LabVIEW is a graphical programming language that uses icons instead of lines of text to create programs.
LSB	Least significant bit.

M

m	Meter.
max	Maximum.
MIMO	Multiple input, multiple output.
min	Minimum.
MIO	Multifunction I/O.
monotonicity	A characteristic of a DAC in which the analog output always increases as the values of the digital code input to it increase.
mux	Multiplexer—a switching device with multiple inputs that sequentially connects each of its inputs to its output, typically at high speeds, in order to measure several signals with a single analog input channel.

N

noise	An undesirable electrical signal—noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.
NRSE	Nonreferenced single-ended mode—all measurements are made with respect to a common (NRSE) measurement system reference, but the voltage at this reference can vary with respect to the measurement system ground.

O

OUT	Output pin—a counter output pin where the counter can generate various TTL pulse waveforms.

P

PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations; it offers a theoretical maximum transfer rate of 132 MB/s.
port	(1) A communications connection on a computer or a remote controller. (2) A digital port, consisting of four or eight lines of digital input and/or output.
ppm	Parts per million.
pu	Pull-up.
PWM	Pulse-width modulation.
PXI	Stands for PCI eXtensions for Instrumentation. PXI is an open specification that builds off the CompactPCI specification by adding instrumentation-specific features.

R

RAM	Random-access memory—the generic term for the read/write memory that is used in computers. RAM allows bits and bytes to be written to it as well as read from. Various types of RAM are DRAM, EDO RAM, SRAM, and VRAM.
resolution	The smallest signal increment that can be detected by a measurement system. Resolution can be expressed in bits, in proportions, or in percent of full scale. For example, a system has 12-bit resolution, one part in 4,096 resolution, and 0.0244% of full scale.
RIO	Reconfigurable I/O.
rms	Root mean square.
RSE	Referenced single-ended mode—all measurements are made with respect to a common reference measurement system or a ground. Also called a grounded measurement system.

S

s	Seconds.
S	Samples.
S/s	Samples per second—used to express the rate at which a DAQ board samples an analog signal.
signal conditioning	The manipulation of signals to prepare them for digitizing.
slew rate	The voltage rate of change as a function of time. The maximum slew rate of an amplifier is often a key specification to its performance. Slew rate limitations are first seen as distortion at higher signal frequencies.

T

THD	Total harmonic distortion—the ratio of the total rms signal due to harmonic distortion to the overall rms signal, in decibel or a percentage.
thermocouple	A temperature sensor created by joining two dissimilar metals. The junction produces a small voltage as a function of the temperature.
TTL	Transistor-transistor logic.
two's complement	Given a number x expressed in base 2 with n digits to the left of the radix point, the (base 2) number $2n - x$.

V

V	Volts.
VDC	Volts direct current.
VHDCI	Very high density cabled interconnect.
VI	Virtual instrument—program in LabVIEW that models the appearance and function of a physical instrument.
V_{IH}	Volts, input high.
V_{IL}	Volts, input low.
V_{OH}	Volts, output high.
V_{OL}	Volts, output low.
V_{rms}	Volts, root mean square.

W

waveform	Multiple voltage readings taken at a specific sampling rate.