NI 5412 Specifications

NI PXI/PCI-5412 14-Bit 100 MS/s Arbitrary Waveform Generator

Unless otherwise noted, the following conditions were used for each specification:

- Interpolation set to maximum allowed factor for a given sample rate.
- Signals terminated with 50 Ω.
- Low-Gain Amplifier Path set to 2 V_{pk-pk}, and High-Gain Amplifier Path set to 12 V_{pk-pk}.
- Sample clock set to 100 MS/s.

Typical values are representative of an average unit operating at room temperature. Specifications are subject to change without notice. For the most recent NI 5412 specifications, visit `ni.com/manuals`.

To access all the NI 5412 documentation, including the *NI Signal Generators Getting Started Guide*, which contains functional descriptions of the NI 5412 signals, navigate to **Start»Programs»National Instruments»NI-FGEN»Documentation**.

Caution Hot Surface Allow the NI 5412 to cool before removing it from the chassis to reduce risk of burns. Use caution when handling because recently used NI 5412 devices may exceed safe handling temperatures.

Contents

CH 0
(Channel 0 Analog Output, Front Panel Connector)

Table 1.

Specification	Value				Comments
Number of Channels	1				—
Connector	SMB (jack)				—
Output Voltage Characteristics					
Output Paths	The software-selectable Main Output Path setting provides full-scale voltages from 12.00 V_{pk-pk} to 5.64 mV_{pk-pk} into a 50 Ω load. NI-FGEN uses either the Low-Gain Amplifier or the High-Gain Amplifier when the Main Output Path is selected, depending on the Gain attribute.				—
DAC Resolution	14 bits				—
Amplitude and Offset					
Amplitude Range	Path	Load	Amplitude (V_{pk-pk})		1. Amplitude values assume the full scale of the DAC is utilized. If an amplitude smaller than the minimum value is desired, then waveforms less than full scale of the DAC can be used.
			Minimum Value	Maximum Value	
	Low-Gain Amplifier	50 Ω	0.00564	2.00	
		1 kΩ	0.0107	3.81	
		Open	0.0113	4.00	
	High-Gain Amplifier	50 Ω	0.0338	12.0	
		1 kΩ	0.0644	22.9	
		Open	0.0676	24.0	
Amplitude Resolution	3 digits				—
Offset Range	Span of ±25% of Amplitude Range with increments <0.0014% of Amplitude Range.				—

Table 1. (Continued)

Specification	Value			Comments
Maximum Output Voltage				
Maximum Output Voltage	Path	Load	Maximum Output Voltage (V_{pk-pk})	The Maximum Output Voltage of the NI 5412 is determined by the Amplitude Range and the Offset Range.
	Low-Gain Amplifier	50 Ω	±1.000	
		1 kΩ	±1.905	
		Open	±2.000	
	High-Gain Amplifier	50 Ω	±6.000	
		1 kΩ	±11.43	
		Open	±12.00	
Accuracy				
DC Accuracy	±0.2% of Amplitude ± 0.05% of Offset ± 500 µV (within ±10 °C of self-calibration temperature) ±0.4% of Amplitude ± 0.05% of Offset ± 1 mV (0 °C to 55 °C)			Calibrated for high impedance load.
AC Amplitude Accuracy	±1.0% of desired Amplitude ± 1 mV			50 kHz sine wave.
Output Characteristics				
Output Impedance	50 Ω or 75 Ω nominal, software-selectable.			—
Output Coupling	DC			—
Output Enable	Software-selectable. When the Output Path is disabled, the CH 0 Output is terminated to ground with a 1 W resistor equal to the selected output impedance.			—
Maximum Output Overload	The CH 0 output can be connected to a 50 Ω, ±12 V source without sustaining any damage. No damage occurs if the CH 0 output is shorted to ground indefinitely.			—
Waveform Summing	The CH 0 output supports waveform summing among similar paths—specifically, the outputs of multiple NI 5412 signal generators can be connected directly together.			—

Table 1. (Continued)

Specification	Value		Comments
Frequency and Transient Response			
Bandwidth	20 MHz		–3 dB
Digital Interpolation Filter	Software-selectable Finite Impulse Response (FIR) filter. Available interpolation factors are 2, 4, or 8.		—
Passband Flatness	Low-Gain and High-Gain Amplifiers Path		—
	±1.0 dB from DC to 6 MHz		
Pulse Response	Path		All values are typical. Measured with a 1 m RG-223 cable.
	Low-Gain Amplifier	High-Gain Amplifier	
Rise/Fall Time	<20 ns	<20 ns	
Aberration	<5%	<5%	

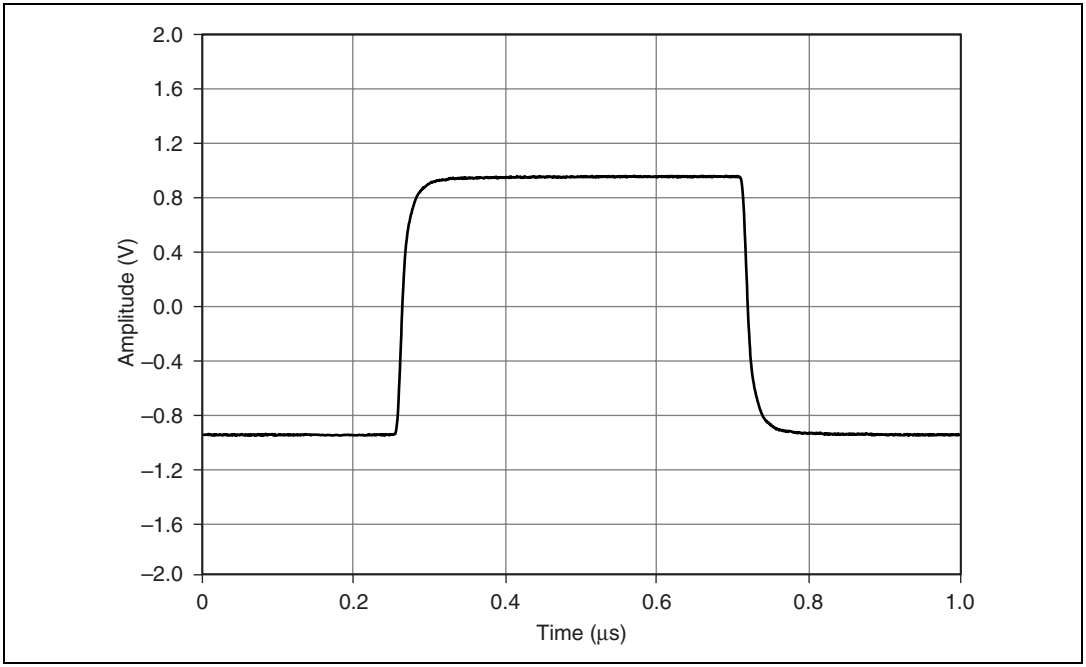

Figure 1. Pulse Response, Low-Gain Amplifier Path 50 Ω Load

Table 1. (Continued)

Specification	Value		Comments
Suggested Maximum Frequencies for Common Functions			
Function	Path		—
	Low-Gain Amplifier	High-Gain Amplifier	
Sine	20 MHz	20 MHz	
Square	5 MHz	5 MHz	
Ramp	1 MHz	1 MHz	
Triangle	1 MHz	1 MHz	
Spectral Characteristics			
Spurious-Free Dynamic Range (SFDR) without Harmonics	Path		Amplitude –1 dBFS. Measured from DC to 50 MHz. SFDR without harmonics at low amplitudes is limited by a –148 dBm/Hz noise floor. All values are typical.
	Low-Gain Amplifier	High-Gain Amplifier	
1 MHz	–70 dBc	–70 dBc	
10 MHz	–65 dBc	–65 dBc	
20 MHz	–60 dBc	–60 dBc	
0 °C to 40 °C Total Harmonic Distortion (THD)	Path		Amplitude –1 dBFS. Includes the 2nd through the 6th harmonic. All values are typical.
	Low-Gain Amplifier	High-Gain Amplifier	
1 MHz	–59 dBc	–51 dBc	
10 MHz	–52 dBc	–40 dBc	
20 MHz	–45 dBc	–37 dBc	

Table 1. (Continued)

Specification	Value					Comments
Spectral Characteristics (Continued)						
Average Noise Density	Path	Amplitude Range		Average Noise Density			Average Noise Density at small amplitudes is limited by a –148 dBm/Hz noise floor.
		V_{pk-pk}	dBm	$\frac{nV}{\sqrt{Hz}}$	dBm/Hz	dBFS/Hz	
	Low-Gain	2	10	45	–134	–144	
	High-Gain	12	25.6	251	–119	–145	

Sample Clock

Table 2.

Specification	Value	Comments
Sources	1. Internal, Divide-by-*N* (*N* ≥ 1) 2. Internal, DDS-based, High-Resolution 3. External, CLK IN (SMB front panel connector) 4. **NI PXI-5412**: External, PXI Star trigger (backplane connector) 5. **NI PXI-5412**: External, PXI_Trig<0..7> (backplane connector) **NI PCI-5412**: External, RTSI<0..7>	Refer to the *Onboard Clock* section for more information about Internal Clock Sources.

Table 2. (Continued)

Specification	Value		Comments
Sample Rate Range and Resolution			
Sample Clock Source	Sample Rate Range	Sample Rate Resolution	—
Divide-by-*N*	23.84 S/s to 100 MS/s	Settable to (100 MS/s) / *N* ($1 \le N \le 4{,}194{,}304$)	
High-Resolution	10 S/s to 100 MS/s	1.06 µHz	
CLK IN	200 kS/s to 105 MS/s	Resolution determined by external clock source. External Sample Clock duty cycle tolerance 40% to 60%.	
NI PXI-5412 PXI Star Trigger	10 S/s to 105 MS/s		
NI PXI-5412 PXI_Trig<0..7>	10 S/s to 20 MS/s		
NI PCI-5412 RTSI<0..7>	10 S/s to 20 MS/s		
Effective Sample Rate			
	Sample Rate (MS/s)	Interpolation Factor	Effective Sample Rate	Effective Sample Rate = (Interpolation Factor) * (Sample Rate)
	10 S/s to 105 MS/s	1 (Off)	10 S/s to 105 MS/s	
	12.5 MS/s to 105 MS/s	2	25 MS/s to 210 MS/s	
	10 MS/s to 100 MS/s	4	40 MS/s to 400 MS/s	
	10 MS/s to 50 MS/s	8	80 MS/s to 400 MS/s	
Sample Clock Delay Range and Resolution			
Sample Clock Source	Delay Adjustment Range	Delay Adjustment Resolution	—
Divide-by-*N*	±1 sample clock period	<10 ps	
High-Resolution	±1 sample clock period	Sample Clock Period/16,384	

Table 2. (Continued)

<table>
<tr><th>Specification</th><th colspan="4">Value</th><th>Comments</th></tr>
<tr><td colspan="6">System Phase Noise and Jitter (10 MHz Carrier)</td></tr>
<tr><td rowspan="2">Sample Clock Source</td><td colspan="3">System Phase Noise Density (dBc/Hz) Offset</td><td rowspan="2">System Output Jitter (Integrated from 100 Hz to 100 kHz)</td><td rowspan="3">1. High-Resolution specifications vary with Sample Rate.
2. All values are typical.</td></tr>
<tr><td>100 Hz</td><td>1 kHz</td><td>10 kHz</td></tr>
<tr><td>NI PXI-5412</td><td>–100</td><td>–118</td><td>–120</td><td><6 ps rms</td></tr>
<tr><td>NI PCI-5412</td><td>–90</td><td>–110</td><td>–120</td><td><7 ps rms</td><td></td></tr>
<tr><td>External Sample Clock Input Jitter Tolerance</td><td colspan="4">Cycle-Cycle Jitter ±300 ps
Period Jitter ±1 ns</td><td>—</td></tr>
<tr><td colspan="6">Sample Clock Exporting</td></tr>
<tr><td>Exported Sample Clock Destinations</td><td colspan="4">1. PFI<0..1> (SMB front panel connectors)
2. NI PXI-5412: PXI_Trig<0..6> (backplane connector)
NI PCI-5412: RTSI<0..6></td><td>Exported Sample Clocks can be divided by integer K (1 ≤ K ≤ 4,194,304).</td></tr>
<tr><td>Exported Sample Clock Destinations</td><td colspan="2">Maximum Frequency</td><td colspan="2">Duty Cycle</td><td>—</td></tr>
<tr><td>PFI<0..1></td><td colspan="2">105 MHz</td><td colspan="2">25% to 65%</td></tr>
<tr><td>NI PXI-5412
PXI_Trig<0..6></td><td colspan="2">20 MHz</td><td colspan="2">—</td></tr>
<tr><td>NI PCI-5412
RTSI<0..6></td><td colspan="2">20 MHz</td><td colspan="2">—</td></tr>
</table>

Onboard Clock
(Internal VCXO)

Table 3.

Specification	Value	Comments
Clock Source	Internal sample clocks can either be locked to a Reference Clock using a phase-locked loop or be derived from the onboard VCXO frequency reference.	—
Frequency Accuracy	±25 ppm	—

Phase-Locked Loop (PLL) Reference Clock

Table 4.

Specification	Value	Comments
Sources	1. **NI PXI-5412**—PXI_CLK10 (backplane connector) **NI PCI-5412**—RTSI_7 (RTSI_CLK) 2. CLK IN (SMB front panel connector)	The PLL Reference Clock provides the reference frequency for the phase-locked loop.
Frequency Accuracy	When using the PLL, the Frequency Accuracy of the NI 5412 is solely dependent on the Frequency Accuracy of the PLL Reference Clock Source.	—
Lock Time	≤ 200 ms.	—
Frequency Range	5 MHz to 20 MHz in increments of 1 MHz. Default of 10 MHz. The PLL Reference Clock Frequency has to be accurate to ±50 ppm.	—
Duty Cycle Range	40% to 60%	—
Exported PLL Reference Clock Destinations	1. PFI<0..1> (SMB front panel connectors) 2. **NI PXI-5412**—PXI_Trig<0..6> (backplane connector) **NI PCI-5412**—RTSI<0..6>	—

CLK IN
(Sample Clock and Reference Clock Input, Front Panel Connector)

Table 5.

Specification	Value	Comments
Connector	SMB (jack)	—
Direction	Input	—
Destinations	1. Sample Clock 2. PLL Reference Clock	—
Frequency Range	1 MHz to 105 MHz (Sample Clock destination and sine waves) 200 kHz to 105 MHz (Sample Clock destination and square waves) 5 MHz to 20 MHz (PLL Reference Clock destination)	—
Input Voltage Range	Sine wave: 0.65 V_{pk-pk} to 2.8 V_{pk-pk} into 50 Ω (0 dBm to +13 dBm) Square wave: 0.2 V_{pk-pk} to 2.8 V_{pk-pk} into 50 Ω	—
Maximum Input Overload	±10 V	—
Input Impedance	50 Ω	—
Input Coupling	AC	—

PFI 0 and PFI 1
(Programmable Function Interface, Front Panel Connectors)

Table 6.

Specification	Value	Comments
Connectors	Two SMB (jack)	—
Direction	Bi-directional	—
Frequency Range	DC to 105 MHz	—
As an Input (Trigger)		
Destinations	Start Trigger	—
Maximum Input Overload	–2 V to +7 V	—
V_{IH}	2.0 V	
V_{IL}	0.8 V	
Input Impedance	1 kΩ	
As an Output (Event)		
Sources	1. Sample Clock divided by integer K ($1 \le K \le 4{,}194{,}304$) 2. Sample Clock Timebase (100 MHz) divided by integer M ($2 \le M \le 4{,}194{,}304$) 3. PLL Reference Clock 4. Marker 5. Exported Start Trigger (Out Start Trigger)	—
Output Impedance	50 Ω	—
Maximum Output Overload	–2 V to +7 V	—

Table 6. (Continued)

Specification	Value	Comments
V_{OH}	Minimum: 2.9 V (open load), 1.4 V (50 Ω load)	Output drivers are +3.3 V TTL compatible. Measured with a 1 m cable.
V_{OL}	Maximum: 0.2 V (open load), 0.2 V (50 Ω load)	
Rise/Fall Time (20% to 80%)	≤2.0 ns	Load of 10 pF.

Start Trigger

Table 7.

Specification	Value	Comments
Sources	1. PFI<0..1> (SMB front panel connectors) 2. **NI PXI-5412**—PXI_Trig<0..7> (backplane connector) **NI PCI-5412**—RTSI<0..7> 3. **NI PXI-5412**—PXI Star trigger (backplane connector) 4. Software (use function call) 5. Immediate (does not wait for a trigger). Default.	—
Modes	1. Single 2. Continuous 3. Stepped 4. Burst	—
Edge Detection	Rising	—
Minimum Pulse Width	25 ns. Refer to t_{s1} at **NI Signal Generators Help»Devices» NI 5412»NI <bus>-5412»Triggering»Trigger Timing**.	—

Table 7. (Continued)

Specification	Value		Comments
Delay from Start Trigger to CH 0 Analog Output	Interpolation Factor	Typical Delay	Refer to t_{s2} at **NI Signal Generators Help»Devices» NI 5412» NI <bus>-5412» Triggering» Trigger Timing**.
	Digital Interpolation Filter disabled.	43 Sample Clock Periods + 110 ns	
	2	57 Sample Clock Periods + 110 ns	
	4	63 Sample Clock Periods + 110 ns	
	8	64 Sample Clock Periods + 110 ns	
Trigger Exporting			
Exported Trigger Destinations	A signal used as a trigger can be routed out to any destination listed in the *Destinations* specification of Table 8.		—
Exported Trigger Delay	65 ns (typical). Refer to t_{s3} at **NI Signal Generators Help» Devices»NI 5412»NI <bus>-5412»Triggering»Trigger Timing**.		—
Exported Trigger Pulse Width	>150 ns. Refer to t_{s4} at **NI Signal Generators Help» Devices»NI 5412»NI <bus>-5412»Triggering»Trigger Timing**.		—

Markers

Table 8.

<table>
<tr><th>Specification</th><th colspan="2">Value</th><th>Comments</th></tr>
<tr><td>Destinations</td><td colspan="2">1. PFI<0..1> (SMB front panel connectors)
2. NI PXI-5412—PXI_Trig<0..6> (backplane connector)
NI PCI-5412—RTSI<0..6></td><td>—</td></tr>
<tr><td>Quantity</td><td colspan="2">One Marker per Segment.</td><td>—</td></tr>
<tr><td>Quantum</td><td colspan="2">Marker position must be placed at an integer multiple of four samples.</td><td>—</td></tr>
<tr><td>Width</td><td colspan="2">>150 ns. Refer to t_{m2} at NI Signal Generators Help» Devices»NI 5412»NI <bus>-5412»Waveform Generation»Marker Events.</td><td>—</td></tr>
<tr><td rowspan="3">Skew</td><td>Destination</td><td>With Respect to Analog Output</td><td rowspan="3">Refer to t_{m1} at NI Signal Generators Help»Devices» NI 5412» NI <bus>-5412» Waveform Generation» Marker Events.</td></tr>
<tr><td>PFI<0..1></td><td>±2 Sample Clock Periods</td></tr>
<tr><td>NI PXI-5412 PXI_Trig<0..6>
NI PCI-5412 RTSI<0..6></td><td>±2 Sample Clock Periods</td></tr>
</table>

Waveform and Instruction Memory Utilization

Table 9.

Specification	Value			Comments
Memory Usage	The NI 5412 uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters, such as number of segments in sequence list, maximum number of waveforms in memory, and number of samples available for waveform storage, are flexible and user defined.			—
Onboard Memory Size	8 MB standard: 8,388,608 bytes	32 MB option: 33,554,432 bytes	256 MB option: 268,435,456 bytes	—
Output Modes	Arbitrary Waveform mode and Arbitrary Sequence mode			—
Arbitrary Waveform Mode	In Arbitrary Waveform mode, a single waveform is selected from the set of waveforms stored in onboard memory and generated.			—
Arbitrary Sequence Mode	In Arbitrary Sequence mode, a sequence directs the NI 5412 to generate a set of waveforms in a specific order. Elements of the sequence are referred to as segments. Each segment is associated with a set of instructions. The instructions identify which waveform is selected from the set of waveforms in memory, how many loops (iterations) of the waveform are generated, and at which sample in the waveform a marker output signal is sent.			—
Minimum Waveform Size (Samples)	Trigger Mode	Arbitrary Waveform Mode	Arbitrary Sequence Mode	The Minimum Waveform Size is sample rate dependent in Arbitrary Sequence Mode.
	Single	16	16	
	Continuous	16	96 @ >50 MS/s	
			32 @ ≤50 MS/s	
	Stepped	32	96 @ >50 MS/s	
			32 @ ≤50 MS/s	
	Burst	16	512 @ >50 MS/s	
			256 @ ≤50 MS/s	

Table 9. (Continued)

Specification	Value			Comments
Loop Count	1 to 16,777,215. Burst trigger: Unlimited			—
Quantum	Waveform size must be an integer multiple of four samples.			—
Memory Limits				
	8 MB Standard	32 MB Option	256 MB Option	All trigger modes except where noted.
Arbitrary Waveform Mode, Maximum Waveform Memory	4,194,176 Samples	16,777,088 Samples	134,217,600 Samples	
Arbitrary Sequence Mode, Maximum Waveform Memory	4,194,120 Samples	16,777,008 Samples	134,217,520 Samples	Condition: One or two segments in a sequence.
Arbitrary Sequence Mode, Maximum Waveforms	65,000 Burst trigger: 8,000	262,000 Burst trigger: 32,000	2,097,000 Burst trigger: 262,000	Condition: One or two segments in a sequence.
Arbitrary Sequence Mode, Maximum Segments in a Sequence	104,000 Burst trigger: 65,000	418,000 Burst trigger: 262,000	3,354,000 Burst trigger: 2,090,000	Condition: Waveform memory is <4,000 samples.

Calibration

Table 10.

Specification	Value	Comments
Self-Calibration	An onboard, 24-bit ADC and precision voltage reference are used to calibrate the DC gain and offset. The self-calibration is initiated by the user through the software and takes approximately 75 seconds to complete.	—
External Calibration	The External Calibration calibrates the VCXO, voltage reference, DC gain, and offset. Appropriate constants are stored in nonvolatile memory.	—
Calibration Interval	Specifications valid within 2 years of External Calibration.	—
Warm-up Time	15 minutes	—

Power

Table 11.

Specification	Normal Operation	Overload Operation	Comments
Total Power	22 W	26 W	Typical. Overload operation occurs when CH 0 is shorted to ground.

Table 12.

Specification	Value	Comments
Driver Software	NI-FGEN 2.3 or later version. NI-FGEN is an IVI-compliant driver that allows you to configure, control, and calibrate the NI 5412. NI-FGEN provides application programming interfaces for many development environments.	—
Application Software	NI-FGEN provides programming interfaces for the following application development environments: • LabVIEW • LabWindows™/CVI™ • Measurement Studio • Microsoft Visual C++ .NET • Microsoft Visual C/C++ • Microsoft Visual Basic	—
Soft Front Panel/ Interactive Configuration	The FGEN Soft Front Panel 2.3 or later supports interactive control of the NI 5412. The FGEN Soft Front Panel is included on the NI-FGEN driver CD. Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the NI 5412. MAX is also included on the NI-FGEN CD.	—

Environment

NI PXI-5412 Environment

Note To ensure that the NI PXI-5412 cools effectively, follow the guidelines in the *Maintain Forced-Air Cooling Note to Users* included in the NI 5412 kit. The NI PXI-5412 is intended for indoor use only.

Table 13.

Specifications	Value	Comments
Operating Temperature	0 ºC to +55 ºC in all NI PXI chassis except the following: 0 ºC to +45 ºC when installed in an NI PXI-101*x* or NI PXI-1000B chassis. Meets IEC-60068-2-1 and IEC-60068-2-2.	—
Storage Temperature	–25 ºC to +85 ºC. Meets IEC-60068-2-1 and IEC-60068-2-2.	—
Operating Relative Humidity	10% to 90%, noncondensing. Meets IEC-60068-2-56.	—
Storage Relative Humidity	5% to 95%, noncondensing. Meets IEC-60068-2-56.	—
Operating Shock	30 g, half-sine, 11 ms pulse. Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	Spectral and jitter specifications could degrade.
Storage Shock	50 g, half-sine, 11 ms pulse. Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	—
Operating Vibration	5 Hz to 500 Hz, 0.31 g_{rms}. Meets IEC-60068-2-64.	Spectral and jitter specifications could degrade.
Storage Vibration	5 Hz to 500 Hz, 2.46 g_{rms}. Meets IEC-60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B.	—
Altitude	2,000 m maximum (at 25 °C ambient temperature)	—
Pollution Degree	2	—

NI PCI-5412 Environment

Note To ensure that the NI PCI-5412 cools effectively, follow the guidelines in the *Maintain Forced-Air Cooling Note to Users* included in the NI 5412 kit. Also, to maximize airflow and extend the life of the device, leave any adjacent PCI slots empty. The NI PCI-5412 is intended for indoor use only.

Table 14.

Specifications	Value	Comments
Operating Temperature	0 ºC to +45 ºC. Meets IEC-60068-2-1 and IEC-60068-2-2.	—
Storage Temperature	–25 ºC to +85 ºC. Meets IEC-60068-2-1 and IEC-60068-2-2.	—
Operating Relative Humidity	10% to 90%, noncondensing. Meets IEC-60068-2-56.	—
Storage Relative Humidity	5% to 95%, noncondensing. Meets IEC-60068-2-56.	—
Storage Shock	50 g, half-sine, 11 ms pulse. Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	—
Storage Vibration	5 Hz to 500 Hz, 2.46 g_{rms}. Meets IEC-60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B.	—
Altitude	2,000 m maximum (at 25 °C ambient temperature)	—
Pollution Degree	2	—

Table 15.

Specification	Value	Comments
Safety	The NI 5412 meets the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use: • IEC 61010-1, EN 61010-1 • UL 61010-1 • CAN/CSA C22.2 No. 61010-1	For UL and other safety certifications, refer to the product label or to `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.
Emissions	EN 55011 Class A at 10 m FCC Part 15A above 1 GHz	—
Immunity	EN 61326:1997 + A2:2001, Table 1 Up to 4 mVpp noise (about –44 dBm) may be present on the output during the conducted immunity test. Use of the product at levels below –44 dBm will result in self-recoverable errors. Good screening (shielding) techniques must be employed throughout the user's data acquisition system.	—

Table 15. (Continued)

Specification	Value	Comments
EMC/EMI	CE, C-Tick, and FCC Part 15 (Class A) Compliant **Notes**: 1. This device is not intended for, and is restricted from, use in residential areas. 2. For EMC compliance, operate this device with shielded cabling. 3. When connected to other test objects, this product may cause radio interference. If this occurs, you may be required to take adequate measures to reduce the interference.	—
This product meets the essential requirements of applicable European Directives as amended for CE marking, as follows:		
Low-Voltage Directive (safety)	73/23/EEC	—
Electromagnetic Compatibility Directive (EMC)	89/336/EEC	—
Note: Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.		

Physical

Table 16.

Specification	Value		Comments
Dimensions	NI PXI-5412	NI PCI-5412	—
	Single 3U PXI slot. CompactPCI compatible. 2.0 × 13.0 × 21.6 cm (0.8 × 5.1 × 8.5 inches)	34.07 × 10.67 × 2.03 cm (13.4 × 4.20 × 0.8 inches)	
Weight	340 g (11 oz)	480 g (17 oz)	—
Front Panel Connectors			
Label	Function(s)	Connector Type	—
CH 0	Analog Output	SMB (jack)	
CLK IN	Sample clock input and PLL reference clock input.	SMB (jack)	
PFI 0	Marker output, trigger input, sample clock output, exported trigger output, and PLL reference clock output.	SMB (jack)	
PFI 1	Marker output, trigger input, sample clock output, exported trigger output, and PLL reference clock output.	SMB (jack)	
NI PXI-5412 Only—Front Panel LED Indicators			
Label	Function		For more information, refer to the *NI Signal Generators Help.*
ACCESS LED	The ACCESS LED indicates the status of the PCI bus and the interface from the NI 5412 to the controller.		
ACTIVE LED	The ACTIVE LED indicates the status of the onboard generation hardware of the NI 5412.		
Included Cable			
	1 (NI part number 763541-01), 50 Ω, BNC Male to SMB Plug, RG223/U, Double Shielded, 1 m cable.		—

Where to Go for Support

The National Instruments Web site is your complete resource for technical support. At `ni.com/support` you have access to everything from troubleshooting and application development self-help resources to email and phone assistance from NI Application Engineers.

A Declaration of Conformity (DoC) is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electronic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting `ni.com/certification`. If your product supports calibration, you can obtain the calibration certificate for your product at `ni.com/calibration`.

National Instruments corporate headquarters is located at 11500 North Mopac Expressway, Austin, Texas, 78759-3504. National Instruments also has offices located around the world to help address your support needs. For telephone support in the United States, create your service request at `ni.com/support` and follow the calling instructions or dial 512 795 8248. For telephone support outside the United States, contact your local branch office:

Australia 1800 300 800, Austria 43 0 662 45 79 90 0,
Belgium 32 0 2 757 00 20, Brazil 55 11 3262 3599,
Canada (Calgary) 403 274 9391, Canada (Ottawa) 613 233 5949,
Canada (Québec) 450 510 3055, Canada (Toronto) 905 785 0085,
Canada (Vancouver) 604 685 7530, China 86 21 6555 7838,
Czech Republic 420 224 235 774, Denmark 45 45 76 26 00,
Finland 385 0 9 725 725 11, France 33 0 1 48 14 24 24,
Germany 49 0 89 741 31 30, India 91 80 51190000,
Israel 972 0 3 6393737, Italy 39 02 413091, Japan 81 3 5472 2970,
Korea 82 02 3451 3400, Malaysia 603 9131 0918,
Mexico 01 800 010 0793, Netherlands 31 0 348 433 466,
New Zealand 0800 553 322, Norway 47 0 66 90 76 60,
Poland 48 22 3390150, Portugal 351 210 311 210,
Russia 7 095 783 68 51, Singapore 65 6226 5886,
Slovenia 386 3 425 4200, South Africa 27 0 11 805 8197,
Spain 34 91 640 0085, Sweden 46 0 8 587 895 00,
Switzerland 41 56 200 51 51, Taiwan 886 2 2528 7227,
Thailand 662 992 7519, United Kingdom 44 0 1635 523545

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