DAQ

NI 6115/6120 User Manual

Multifunction I/O Devices for PCI/PXI/CompactPCI Bus Computers

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Compliance

FCC/Canada Radio Frequency Interference Compliance

Determining FCC Class

The Federal Communications Commission (FCC) has rules to protect wireless communications from interference. The FCC places digital electronics into two classes. These classes are known as Class A (for use in industrial-commercial locations only) or Class B (for use in residential or commercial locations). Depending on where it is operated, this product could be subject to restrictions in the FCC rules. (In Canada, the Department of Communications (DOC), of Industry Canada, regulates wireless interference in much the same way.)

Digital electronics emit weak signals during normal operation that can affect radio, television, or other wireless products. By examining the product you purchased, you can determine the FCC Class and therefore which of the two FCC/DOC Warnings apply in the following sections. (Some products may not be labeled at all for FCC; if so, the reader should then assume these are Class A devices.)

FCC Class A products only display a simple warning statement of one paragraph in length regarding interference and undesired operation. Most of our products are FCC Class A. The FCC rules have restrictions regarding the locations where FCC Class A products can be operated.

FCC Class B products display either a FCC ID code, starting with the letters **EXN**, or the FCC Class B compliance mark that appears as shown here on the right.

Consult the FCC Web site at `http://www.fcc.gov` for more information.

FCC/DOC Warnings

This equipment generates and uses radio frequency energy and, if not installed and used in strict accordance with the instructions in this manual and the CE Marking Declaration of Conformity*, may cause interference to radio and television reception. Classification requirements are the same for the Federal Communications Commission (FCC) and the Canadian Department of Communications (DOC).

Changes or modifications not expressly approved by National Instruments could void the user's authority to operate the equipment under the FCC Rules.

Class A

Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Canadian Department of Communications

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe A respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

Class B

Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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Canadian Department of Communications

This Class B digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe B respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

Compliance to EU Directives

Readers in the European Union (EU) must refer to the Manufacturer's Declaration of Conformity (DoC) for information* pertaining to the CE Marking compliance scheme. The Manufacturer includes a DoC for most every hardware product except for those bought for OEMs, if also available from an original manufacturer that also markets in the EU, or where compliance is not required as for electrically benign apparatus or cables.

To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by your product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.

* The CE Marking Declaration of Conformity will contain important supplementary information and instructions for the user or installer.

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About This Manual

This manual describes the electrical and mechanical aspects of the NI 6115/6120 and contains information concerning its operation and programming.

The NI 6115/6120 family includes the following devices:

- NI PCI-6115
- NI PXI-6115
- NI PCI-6120
- NI PXI-6120

The NI 6115/6120 is a high-performance multifunction analog, digital, and timing I/O data acquisition (DAQ) device for PXI and PCI bus computers. Supported functions include analog input (AI), analog output (AO), digital I/O (DIO), and timing I/O (TIO).

Conventions

The following conventions appear in this manual:

<> Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, DIO<3..0>.

» The » symbol leads you through nested menu items and dialog box options to a final action. The sequence **File»Page Setup»Options** directs you to pull down the **File** menu, select the **Page Setup** item, and select **Options** from the last dialog box.

♦ The ♦ symbol indicates that the following text applies only to a specific product, a specific operating system, or a specific software version.

This icon denotes a note, which alerts you to important information.

This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on the product, refer to the *Safety Information* section of Chapter 1, *Introduction*, for precautions to take.

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bold	Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names and hardware labels.
CompactPCI	CompactPCI refers to the core specification defined by the PCI Industrial Computer Manufacturer's Group (PICMG).
italic	Italic text denotes variables, emphasis, a cross reference, or an introduction to a key concept. This font also denotes text that is a placeholder for a word or value that you must supply.
`monospace`	Monospace text denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and code excerpts.
NI 6115/6120	This phrase refers to any device in the NI 6115/6120 family.
PCI	Peripheral Component Interconnect—PCI is a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA.
PXI	A rugged, open system for modular instrumentation based on CompactPCI, with special mechanical, electrical, and software features. The PXI bus standard was originally developed by National Instruments in 1997, and is now managed by the PXI bus Systems Alliance.

National Instruments Documentation

The *NI 6115/6120 User Manual* is one piece of the documentation set for the DAQ system. You could have any of several types of documentation depending on the hardware and software in the system. Use the documentation you have as follows:

- *DAQ Quick Start Guide*—This guide describes how to install the DAQ software and hardware, and confirm that the DAQ device is operating properly. When using this guide, refer to the pinout diagram for the NI 6110/6111. The pinouts for the NI 6110/6111 and the NI 6115/6120 are identical.
- DAQ hardware documentation—This documentation has detailed information about the DAQ hardware that plugs into or is connected to the computer. Use this documentation for hardware installation and

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configuration instructions, specification information about the DAQ hardware, and application hints.

- Software documentation—You may have both application software and NI-DAQ documentation. NI application software includes LabVIEW and Measurement Studio. After you set up the hardware system, use either your application software documentation or the NI-DAQ documentation to help you write your application. If you have a large, complicated system, it is worthwhile to look through the software documentation before you configure the hardware.
- Accessory installation guides or manuals—If you are using accessory products, read the terminal block and cable assembly installation guides. They explain how to physically connect the relevant pieces of the system. Consult these guides when you are making the connections.

Related Documentation

The following documents contain information you may find helpful:

- *DAQ Quick Start Guide*, located at `ni.com/manuals`
- *DAQ-STC Technical Reference Manual*, located at `ni.com/manuals`
- NI Developer Zone tutorial, *Field Wiring and Noise Considerations for Analog Signals*, located at `ni.com/zone`
- *NI-DAQ User Manual for PC Compatibles*, located at `ni.com/manuals`
- *NI-DAQ Function Reference Help*. You can access this help file by clicking **Start»Programs»National Instruments»NI-DAQ» NI-DAQ Help**.
- *PCI Local Bus Specification Revision 2.2*
- *PICMG 2.0 R3.0, CompactPCI Core Specification*
- *PXI Specification Revision 2.0*, available from `www.pxisa.org`

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1

Introduction

This chapter describes the NI 6115/6120, lists what you need to get started, describes the optional software and optional equipment, and explains how to unpack the device.

About the NI 6115/6120

Thank you for buying an NI 6115/6120. The NI 6115/6120 is a Plug and Play multifunction analog, digital, and timing I/O device for PXI and PCI bus computers. The NI 6115 features a 12-bit A/D converter (ADC) per channel with four simultaneously sampling analog inputs, and two 12-bit D/A converters (DACs) with voltage outputs. The NI 6120 features a 16-bit ADC per input channel and 16-bit DACs for output. Each device features eight lines of TTL-compatible correlated DIO, and two 24-bit counter/timers for TIO.

The NI 6115/6120 is a DAQ device for PXI or the PCI bus. The device is software configured and calibrated, and completely switchless and jumperless. This feature is made possible by the NI MITE bus interface chip that connects the device to the PXI or PCI I/O bus. The MITE implements the PCI Local Bus Specification so that you can configure all the interrupts and base memory addresses with software.

The NI 6115/6120 uses the NI data acquisition system timing controller (DAQ-STC) for time-related functions. The DAQ-STC consists of three timing groups that control AI, AO, and general-purpose counter/timer functions. These groups include a total of seven 24-bit and three 16-bit counters and a maximum timing resolution of 50 ns. The DAQ-STC makes possible such applications as buffered pulse generation and equivalent time sampling.

The NI 6115/6120 uses the Real-Time System Integration (RTSI) bus to easily synchronize several measurement devices to a common trigger or timing event. The RTSI bus allows synchronization of the measurements. The RTSI bus consists of the RTSI bus interface and a ribbon cable to route timing and trigger signals between as many as five DAQ devices in the computer. If you are using the NI PXI-6115/6120 in a PXI chassis, RTSI lines, known as the PXI trigger bus, are part of the backplane. Therefore,

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you do not need the RTSI cable for system triggering and timing on the PXI. In addition, a phase-locked loop (PLL) circuit accomplishes the synchronization of multiple NI PXI-6115/6120 devices or other PXI devices which support PLL synchronization by allowing these devices to all lock to the same reference clock present on the PXI backplane. Refer to the *Phase-Locked Loop Circuit* section of Chapter 3, *Hardware Overview*, for more information.

Detailed specifications of the NI 6115/6120 are in Appendix A, *Specifications*.

Using PXI with CompactPCI

The ability to use PXI-compatible products with standard CompactPCI products is an important feature of *PXI Specification Revision 2.0*. If you use a PXI-compatible plug-in device in a standard CompactPCI chassis, you are unable to use PXI-specific functions, but you can still use the basic plug-in device functions. For example, the RTSI interface on the NI PXI-6115/6120 is available in a PXI chassis, but not in a CompactPCI chassis.

The CompactPCI specification permits vendors to develop sub-buses that coexist with the basic PCI interface on the CompactPCI bus. Compatible operation is not guaranteed between CompactPCI devices with different sub-buses nor between CompactPCI devices with sub-buses and PXI devices. The standard implementation for CompactPCI does not include these sub-buses. The NI PXI-6115/6120 works in any standard CompactPCI chassis adhering to PICMG CompactPCI 2.0 R3.0.

PXI-specific features are implemented on the J2 connector of the CompactPCI bus. Table 1-1 lists the J2 pins used by the NI PXI-6115/6120. The PXI device is compatible with any CompactPCI chassis with a sub-bus that does not drive these lines. Even if the sub-bus is capable of driving these lines, the PXI device is still compatible as long as those pins on the sub-bus are disabled by default and are never enabled.

Caution Damage can result if these lines are driven by the sub-bus.

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Table 1-1. NI PXI-6115/6120 J2 Pin Assignment

NI PXI-6115/6120 Signal	PXI Pin Name	PXI J2 Pin Number
RTSI<0..5>	PXI Trigger<0..5>	B16, A16, A17, A18, B18, C18
RTSI 6	Star	D17
RTSI Clock	PXI Trigger 7	E16
Reserved	LBL<0..12>	C20, E20, A19, C19
Reserved	LBR<0..12>	A21, C21, D21, E21, A20, B20, E15, A3, C3, D3, E3, A2, B2

What You Need to Get Started

To set up and use the NI 6115/6120, you need the following:

- ❑ A computer or a PXI/CompactPCI chassis and controller (hereafter referred to as the computer)
- ❑ At least one of the following devices:
  - NI PCI-6115
  - NI PXI-6115
  - NI PCI-6120
  - NI PXI-6120
- ❑ *NI 6115/6120 User Manual*
- ❑ NI-DAQ for PC compatibles
- ❑ (Optional) One of the following software packages and documentation:
  - LabVIEW (Windows)
  - Measurement Studio (Windows)
  - VI Logger (Windows)

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Software Programming Choices

When programming National Instruments DAQ hardware, you can use an NI application development environment (ADE) or other ADEs. In either case, you use NI-DAQ.

NI-DAQ

NI-DAQ, which shipped with the NI 6115/6120, has an extensive library of functions that you can call from the ADE. These functions allow you to use all the features of the device.

NI-DAQ carries out many of the complex interactions, such as programming interrupts, between the computer and the DAQ hardware. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to the code. Whether you are using LabVIEW, LabWindows™/CVI™, Measurement Studio, VI Logger, or other ADEs, your application uses NI-DAQ, as illustrated in Figure 1-1.

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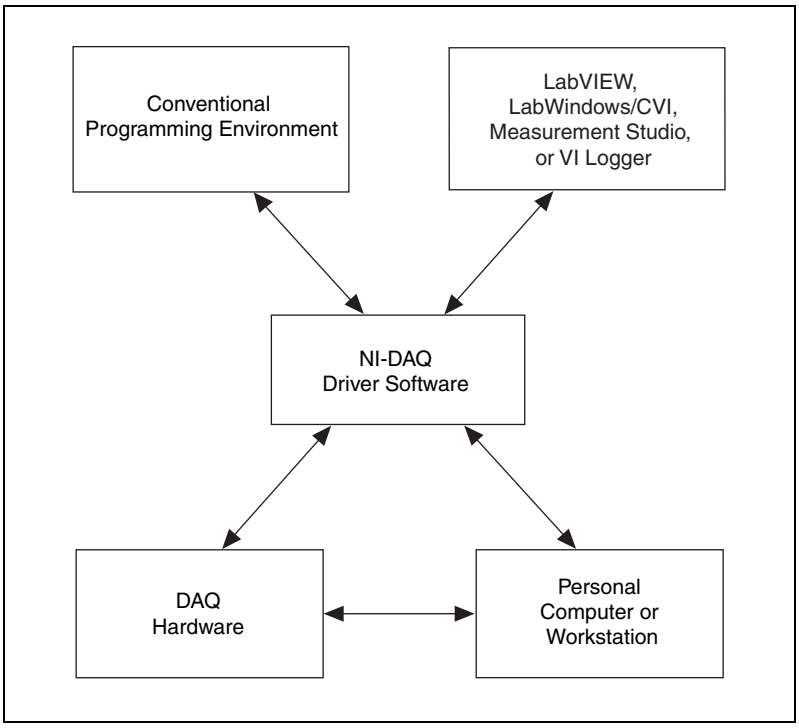

Figure 1-1. The Relationship Among the Programming Environment, NI-DAQ, and the Hardware

To download a free copy of the most recent version of NI-DAQ, click **Download Software** at `ni.com`.

National Instruments ADE Software

LabVIEW features interactive graphics, a state-of-the-art interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of virtual instruments for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW.

LabWindows/CVI is a complete ANSI C ADE that features an interactive user interface, code generation tools, and the LabWindows/CVI Data Acquisition and Easy I/O libraries.

Measurement Studio, which includes tools for Visual C++ and tools for Visual Basic, is a development suite that allows you to design test and measurement applications. For Visual Basic developers, Measurement Studio features a set of ActiveX controls for using National Instruments

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DAQ hardware. These ActiveX controls provide a high-level programming interface for building virtual instruments (VIs). For Visual C++ developers, Measurement Studio offers a set of Visual C++ classes and tools to integrate those classes into Visual C++ applications. The ActiveX controls and classes are available with Measurement Studio and the NI-DAQ software.

VI Logger is an easy-to-use yet flexible tool specifically designed for data logging applications. Using dialog windows, you can configure data logging tasks to easily acquire, log, view, and share your data. VI Logger does not require any programming; it is a stand-alone, configuration-based software program.

Using LabVIEW, LabWindows/CVI, Measurement Studio, or VI Logger greatly reduces the development time for your data acquisition and control application.

Optional Equipment

NI offers a variety of products to use with the NI 6115/6120, including cables, connector blocks, and other accessories, as follows:

- Shielded cables and cable assemblies
- Connector blocks, shielded 50- and 68-pin screw terminals
- RTSI bus cables (PCI only)
- Low channel-count signal conditioning modules, devices, and accessories, including conditioning for strain gauges, resistance temperature detectors, and relays

For more specific information about these products, refer to the NI catalog at `ni.com/catalog`.

Custom Cabling

NI offers cables and accessories to help you prototype your application or to use if you frequently change device interconnections.

If you want to develop your own cable, however, adhere to the following guidelines for best results:

- For AI signals, use shielded twisted-pair wires for each AI pair for differential inputs. Tie the shield for each signal pair to the ground reference at the source.

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- Route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

Mating connectors and a backshell kit for making custom 68-pin cables are available from NI.

The parts in the following list are recommended for connectors that mate to the I/O connector on the device:

- Honda 68-position, solder cup, female connector
- Honda backshell

Unpacking

The NI 6115/6120 is shipped in an antistatic package to prevent electrostatic damage to the device. Electrostatic discharge (ESD) can damage several components on the device.

Caution *Never* touch the exposed pins of connectors.

To avoid such damage when handling the device, take the following precautions:

- Ground yourself using a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of the computer chassis before removing the device from the package.

Remove the device from the package and inspect the device for loose components or any sign of damage. Notify NI if the device appears damaged in any way. Do *not* install a damaged device into the computer.

Store the NI 6115/6120 in the antistatic envelope when not in use.

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Safety Information

The following section contains important safety information that you *must* follow when installing and using the product.

Do *not* operate the product in a manner not specified in this document. Misuse of the product can result in a hazard. You can compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to National Instruments for repair.

Do *not* substitute parts or modify the product except as described in this document. Use the product only with the chassis, modules, accessories, and cables specified in the installation instructions. You *must* have all covers and filler panels installed during operation of the product.

Do *not* operate the product in an explosive atmosphere or where there may be flammable gases or fumes. If you must operate the product in such an environment, it must be in a suitably rated enclosure.

If you need to clean the product, use a soft, nonmetallic brush. The product *must* be completely dry and free from contaminants before you return it to service.

Operate the product only at or below Pollution Degree 2. Pollution is foreign matter in a solid, liquid, or gaseous state that can reduce dielectric strength or surface resistivity. The following is a description of pollution degrees:

- Pollution Degree 1 means no pollution or only dry, nonconductive pollution occurs. The pollution has no influence.
- Pollution Degree 2 means that only nonconductive pollution occurs in most cases. Occasionally, however, a temporary conductivity caused by condensation must be expected.
- Pollution Degree 3 means that conductive pollution occurs, or dry, nonconductive pollution occurs that becomes conductive due to condensation.

You *must* insulate signal connections for the maximum voltage for which the product is rated. Do *not* exceed the maximum ratings for the product. Do not install wiring while the product is live with electrical signals. Do not remove or add connector blocks when power is connected to the system. Avoid contact between your body and the connector block signal when hot swapping modules. Remove power from signal lines before connecting them to or disconnecting them from the product.

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Operate the product at or below the *installation category*[1] marked on the hardware label. Measurement circuits are subjected to *working voltages*[2] and transient stresses (overvoltage) from the circuit to which they are connected during measurement or test. Installation categories establish standard impulse withstand voltage levels that commonly occur in electrical distribution systems. The following is a description of installation categories:

- Installation Category I is for measurements performed on circuits not directly connected to the electrical distribution system referred to as MAINS[3] voltage. This category is for measurements of voltages from specially protected secondary circuits. Such voltage measurements include signal levels, special equipment, limited-energy parts of equipment, circuits powered by regulated low-voltage sources, and electronics.
- Installation Category II is for measurements performed on circuits directly connected to the electrical distribution system. This category refers to local-level electrical distribution, such as that provided by a standard wall outlet (for example, 115 V for U.S. or 230 V for Europe). Examples of Installation Category II are measurements performed on household appliances, portable tools, and similar products.
- Installation Category III is for measurements performed in the building installation at the distribution level. This category refers to measurements on hard-wired equipment such as equipment in fixed installations, distribution boards, and circuit breakers. Other examples are wiring, including cables, bus-bars, junction boxes, switches, socket-outlets in the fixed installation, and stationary motors with permanent connections to fixed installations.
- Installation Category IV is for measurements performed at the primary electrical supply installation (<1,000 V). Examples include electricity meters and measurements on primary overcurrent protection devices and on ripple control units.

[1] Installation categories, also referred to as *measurement categories*, are defined in electrical safety standard IEC 61010-1.

[2] Working voltage is the highest rms value of an AC or DC voltage that can occur across any particular insulation.

[3] MAINS is defined as a hazardous live electrical supply system that powers equipment. Suitably rated measuring circuits may be connected to the MAINS for measuring purposes.

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2

Installing and Configuring the NI 6115/6120

This chapter explains how to install and configure the NI 6115/6120.

Installing the Software

Before you install the NI 6115/6120, complete the following steps to install the software:

1. Install the ADE, such as LabVIEW or Measurement Studio, according to the instructions on the CD and the release notes.
2. Install NI-DAQ according to the instructions on the CD and the *DAQ Quick Start Guide* included with the device. When using the *DAQ Quick Start Guide,* refer to the pinout for the NI 6110/6111, which is identical to the pinout for the NI 6115/6120.

Note It is important to install NI-DAQ *before* installing the NI 6115/6120 to ensure that the device is properly detected.

Installing the Hardware

You can install the NI 6115/6120 in any available expansion slot in the computer. However, to achieve best noise performance, leave as much room as possible between the NI 6115/6120 and other devices and hardware.

The following are general installation instructions, so consult the computer user manual or technical reference manual for specific instructions and warnings.

- NI PXI-6115/6120
  1. Power off and unplug the computer.
  2. Choose an unused PXI slot in the system. For maximum performance, the NI PXI-6115/6120 has an onboard DMA controller that you can use only if the device is installed in a slot that supports bus arbitration,

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or bus master devices. NI recommends installing the NI PXI-6115/6120 in such a slot.

Note The PXI specification requires all slots to support bus master devices, but the CompactPCI specification does not. If you install in a CompactPCI non-master slot, you must disable the onboard DMA controller using software.

3. Make sure there are no lighted LEDs on the chassis. If any are lit, wait until they go out before continuing the installation.
4. Remove the filler panel for the slot you have chosen.
5. Ground yourself using a grounding strap or by touching a grounded object. Follow the ESD protection precautions described in the *Unpacking* section of Chapter 1, *Introduction*.
6. Remove the rubber front panel screw protectors.
7. Insert the NI PXI-6115/6120 into a 5 V PXI slot. Use the injector/ejector handle to fully insert the device into the chassis.
8. Screw the front panel of the NI PXI-6115/6120 to the front panel-mounting rail of the system.
9. Visually verify the installation. Make sure the device is not touching other devices or components and is fully inserted in the slot.
10. Plug in and power on the computer.

The NI PXI-6115/6120 is now installed. You are now ready to configure the hardware and software.

- NI PCI-6115/6120
  1. Power off and unplug the computer.
  2. Remove the cover.
  3. Make sure there are no lighted LEDs on the motherboard. If any are lit, wait until they go out before continuing the installation.
  4. Remove the expansion slot cover on the back panel of the computer.
  5. Ground yourself using a grounding strap or by touching a grounded object. Follow the ESD protection precautions described in the *Unpacking* section of Chapter 1, *Introduction*.
  6. Insert the NI PCI-6115/6120 into a PCI system slot. Gently rock the device to ease it into place. It may be a tight fit, but do *not* force the device into place.
  7. Screw the mounting bracket of the device to the back panel rail of the computer.

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8. Replace the cover.
9. Plug in and power on the computer.

The NI PCI-6115/6120 is now installed. You are now ready to configure the hardware and software.

Configuring the Device

Because of the NI standard architecture for data acquisition and the PCI bus specification, the NI 6115/6120 is completely software configurable. Two types of configuration are performed on the NI 6115/6120: bus-related and data acquisition-related configuration.

The NI PCI-6115/6120 is fully compatible with the industry-standard *PCI Local Bus Specification Revision 2.2*. This compatibility allows the PCI system to automatically perform all bus-related configurations with no user interaction. Bus-related configuration includes setting the device base memory address and interrupt channel.

The NI PXI-6115/6120 is fully compatible with the industry-standard *PXI Specification Revision 2.0*. This allows the PXI/CompactPCI system to automatically perform all bus-related configurations with no user interaction. Bus-related configuration includes setting the device base memory address and interrupt channel.

Data acquisition-related configuration, which you must perform, includes such settings as analog input coupling and range, and others. You can modify these settings using NI-DAQ or application-level software, such as LabVIEW and Measurement Studio.

To configure the device in Measurement & Automation Explorer (MAX), refer to either the *DAQ Quick Start Guide* or to the *NI-DAQ User Manual for PC Compatibles* at `ni.com/manuals`. For operating system-specific installation and troubleshooting instructions, refer to `ni.com/support/daq`.

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3

Hardware Overview

This chapter presents an overview of the hardware functions on the NI 6115/6120. Figures 3-1 and 3-2 provide block diagrams for the NI 6115 and NI 6120, respectively.

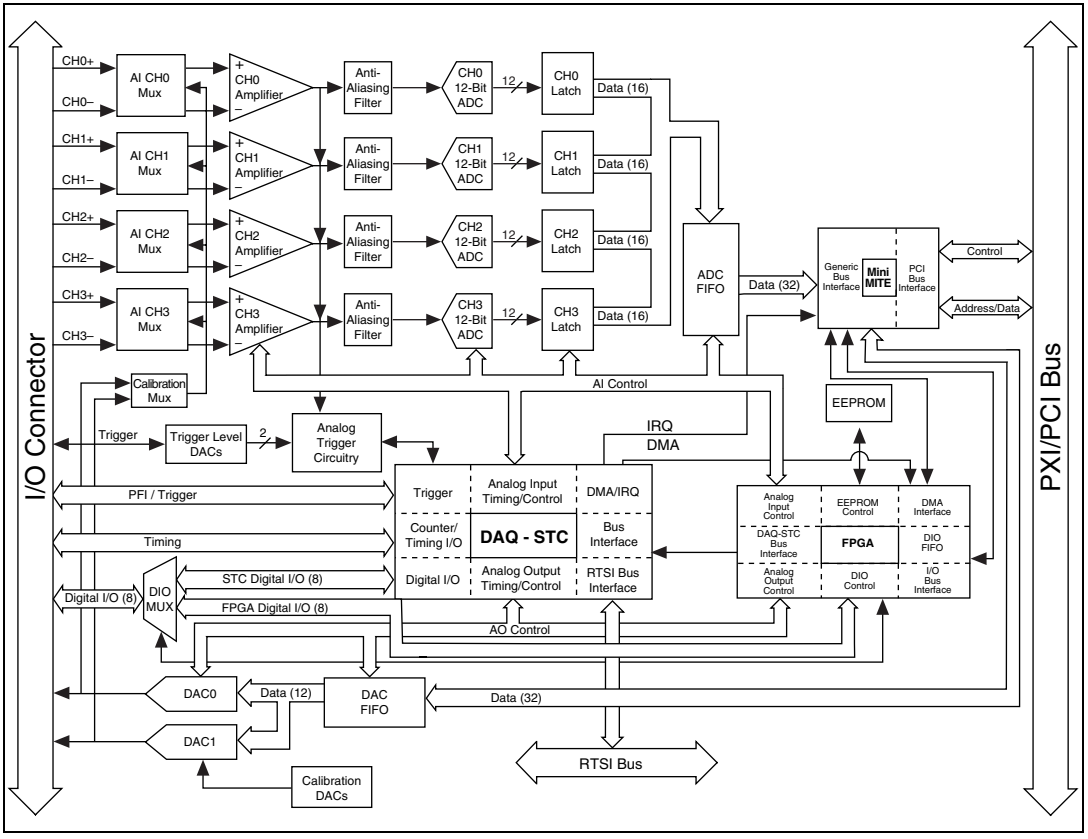

Figure 3-1. NI 6115 Block Diagram

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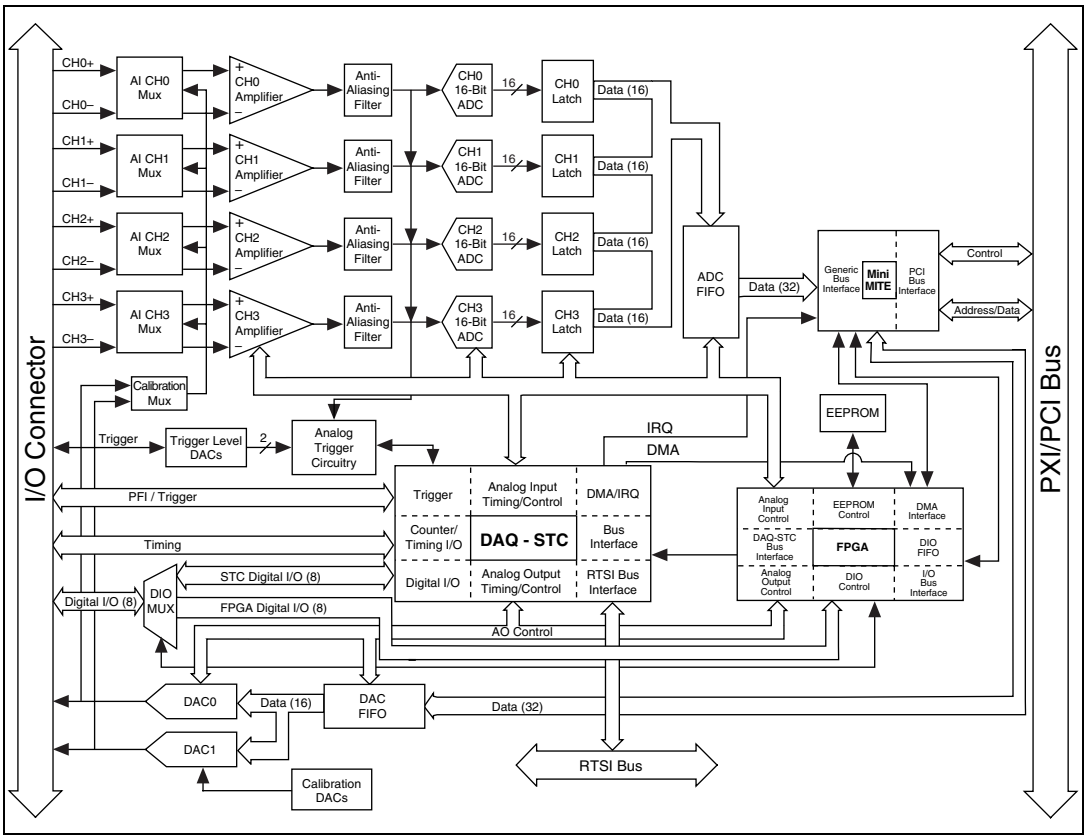

Figure 3-2. NI 6120 Block Diagram

Analog Input

The following sections describe in detail each AI category.

Input Mode

The NI 6115/6120 supports only differential (DIFF) input mode. For more information about DIFF input, refer to the *Connecting Analog Input Signals* section of Chapter 4, *Connecting Signals*, which contains diagrams showing the signal paths for DIFF input mode.

Note The inputs are differential only in the sense that the ground loops are broken. The negative input is not intended to carry signals of interest; rather it provides a DC reference point for the positive input, which may be different than ground.

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Input Polarity and Input Range

The NI 6115/6120 has bipolar inputs only. Bipolar input means that the midpoint of the input voltage range is centered at zero volts.

You can independently configure each channel for a different input voltage range.

The software-programmable gain on this device increases its overall flexibility by matching the input signal ranges to those that the ADC can accommodate. It has ranges of ±42 V, ±20 V, ±10 V, ±5 V, ±2 V, ±1 V, ±500 mV, and ±200 mV and is suited for a wide variety of signal levels. By choosing the optimal gain setting, you can maximize usage of the dynamic range of the ADC, which effectively increases input signal resolution. Table 3-1 shows the overall input range and precision according to the gain used.

Caution The NI 6115/6120 is not designed for input voltages greater than ±42 VDC. Input voltages greater than ±42 VDC can damage the NI 6115/6120, any device connected to it, and the host computer. Overvoltage can also cause an electric shock hazard for the operator. NI is *not* liable for damage or injury resulting from such misuse.

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Table 3-1. Input Range and Measurement Precision

Input Range	Precision[1]	
	6115 (12-Bit)	6120 (16-Bit)
–50 to +50 V[2]	24.4 mV	1.53 mV
–20 to +20 V	9.77 mV	610 µV
–10 to +10 V	4.88 mV	305 µV
–5 to +5 V	2.44 mV	153 µV
–2 to +2 V	977 µV	61.0 µV
–1 to +1V	488 µV	30.5 µV
–500 to +500 mV	244 µV	15.3 µV
–200 to +200 mV	97.7 µV	6.10 µV

[1] The value of 1 least significant bit (LSB) of the ADC; that is, the voltage increment corresponding to a change of one count in the ADC count.
[2] Do not exceed ±42 VDC maximum.

Note: Refer to Appendix A, *Specifications*, for absolute maximum ratings.

Considerations for Selecting Input Ranges

The range you select depends on the expected range of the incoming signal. A large input range can accommodate a large signal variation but reduces the voltage resolution. Choosing a smaller input range improves the voltage resolution but may result in the input signal going out of range. For best results, match the input range as closely as possible to the expected range of the input signal.

Input Coupling

You can configure the NI 6115/6120 for either AC or DC input coupling on a per channel basis. Use AC coupling when the AC signal contains a large DC component. If you enable AC coupling, you remove the large DC offset for the input amplifier and amplify only the AC component. This configuration effectively uses the dynamic range of the ADC.

The input impedance for the programmable gain instrumentation amplifier (PGIA) channels is 1 MΩ for ranges ≤ ±10 V and 10 kΩ for ranges > ±10 V. This configuration provides an AC-coupled corner frequency of 2.34 Hz for ranges ≤ ±10 V and 234 Hz for ranges > ±10 V.

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Analog Output

The NI 6115/6120 supplies two channels of AO voltage at the I/O connector. The range is fixed at bipolar ±10 V.

The AO channels on the NI 6115 contain 12-bit DACs that are capable of 4 MS/s for one channel or 2.5 MS/s for each of two channels. The NI 6120 DACs are 16-bit, and they have the same AO capabilities as the NI 6115. Refer to Appendix A, *Specifications*, for more detailed information about the AO capabilities of the NI 6115/6120.

Note The AO channels do *not* have analog or digital filtering hardware and do produce images in the frequency domain related to the update rate.

The NI 6115/6120 includes high-density memory modules allowing for long waveform generations.

Analog Trigger

In addition to supporting internal software triggering and external digital triggering to initiate a DAQ sequence, these devices also support analog hardware triggering. You can configure the analog trigger circuitry to accept either a direct analog input from the PFI0/TRIG1 pin on the I/O connector or a post-gain signal from the output of the PGIA on any of the channels, as shown in Figure 3-3. The trigger-level range for the direct analog channel is ±10 V with a resolution of 78 mV for the NI 6115 and 4.88 mV for the NI 6120. The input impedance for the direct analog channel is 10 kΩ. When this direct analog channel is configured for AC coupling, the corner frequency is 159 Hz.

The range for the post-PGIA trigger from a selected channel is the full-scale range of the selected channel with a resolution of that range divided by 256 for the NI 6115 and 4,096 for the NI 6120.

Two trigger reference signals, **lowValue** and **highValue**, can then be independently set to achieve advanced triggering modes. Refer to Figures 3-3 through 3-8 for illustrations of these modes.

Note The PFI0/TRIG1 pin is an analog input when configured as an analog trigger. Therefore, it is susceptible to crosstalk from adjacent pins, which can result in false triggering when the pin is left unconnected. To avoid false triggering, make sure the PFI0/TRIG1 pin is connected to a low-impedance signal source (less than 1 kΩ source impedance) if you plan to enable this input using software.

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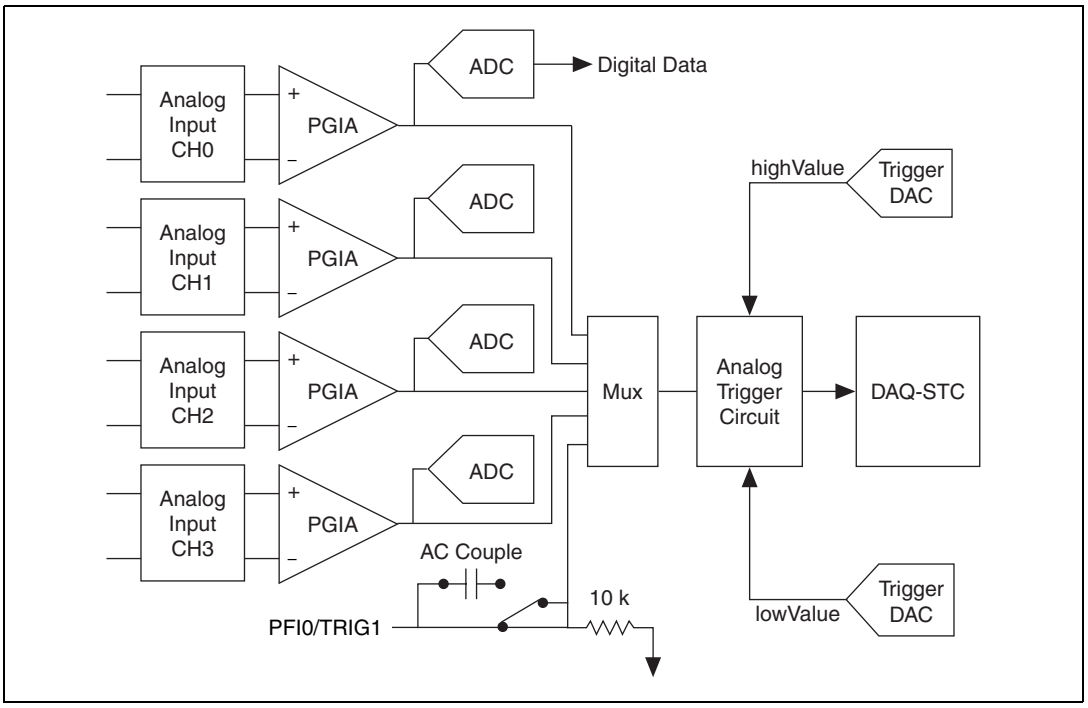

Figure 3-3. Analog Trigger Block Diagram for the NI 6115/6120

In below-low-level analog triggering mode, the trigger is generated when the signal value is less than **lowValue**, as shown in Figure 3-4. **HighValue** is unused.

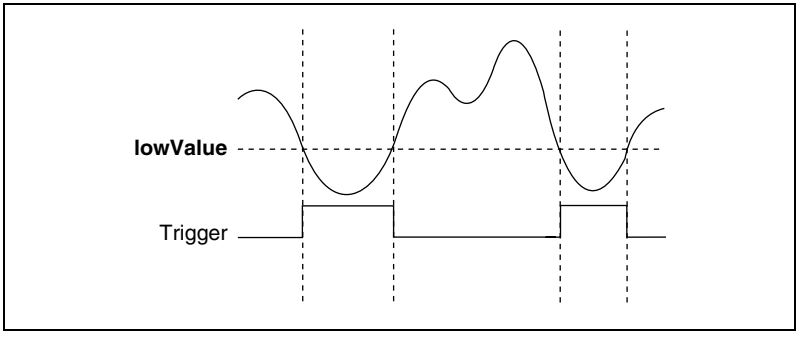

Figure 3-4. Below-Low-Level Analog Triggering Mode

In above-high-level analog triggering mode, the trigger is generated when the signal value is greater than **highValue**, as shown in Figure 3-5. **LowValue** is unused.

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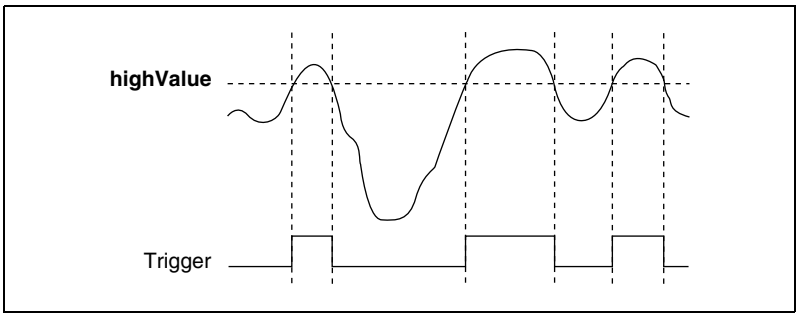

Figure 3-5. Above-High-Level Analog Triggering Mode

In inside-region analog triggering mode, the trigger is generated when the signal value is between the **lowValue** and the **highValue**, as Figure 3-6 shows.

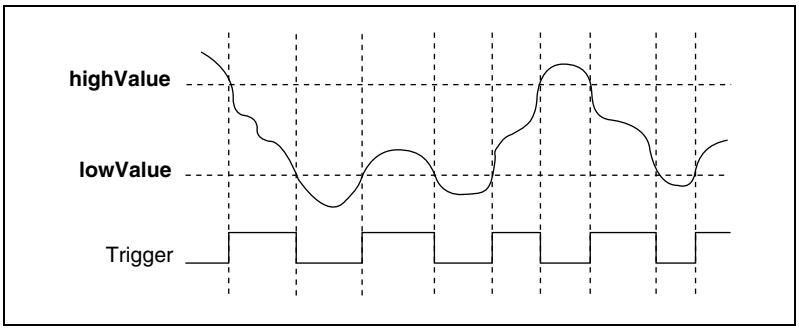

Figure 3-6. Inside-Region Analog Triggering Mode

In high-hysteresis analog triggering mode, the trigger is generated when the signal value is greater than **highValue**, with the hysteresis specified by **lowValue**, as Figure 3-7 shows.

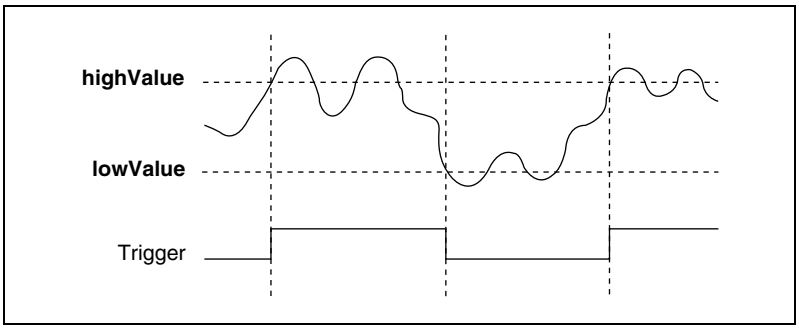

Figure 3-7. High-Hysteresis Analog Triggering Mode

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In low-hysteresis analog triggering mode, the trigger is generated when the signal value is less than **lowValue**, with the hysteresis specified by **highValue**, as Figure 3-8 shows.

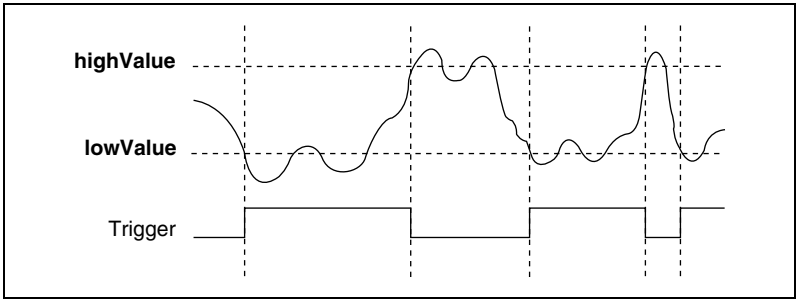

Figure 3-8. Low-Hysteresis Analog Triggering Mode

The analog trigger circuit generates an internal digital trigger based on the AI signal and the user-defined trigger levels. This digital trigger can be used by any of the timing sections of the DAQ-STC, including the AI, AO, and general-purpose counter/timer sections. For example, the AI section can be configured to acquire *n* scans after the AI signal crosses a specific threshold. As another example, the AO section can be configured to update its outputs whenever the AI signal crosses a specific threshold.

Antialiasing Filters

Each AI channel on the NI 6115/6120 is equipped with a programmable antialaising Bessel filter. On the NI 6115, you can program the filters to provide a third-order 50 kHz lowpass filter, a third-order 500 kHz lowpass filter, or a pass-through mode with no filtering. On the NI 6120, you can program the filters to provide a five-pole 100 kHz low-pass filter or pass-through. These Bessel filters are highly effective at reducing signal aliasing and are designed for use with software filters.

Existing software algorithms alone provide good roll-off at the cut-off frequency as shown in Figure 3-9. However, aliasing can cause high-frequency harmonics to make it through passbands in the filter. By combining hardware and software filtering, it is possible to obtain both steep roll-off and clean filtering of high-frequency aliases.

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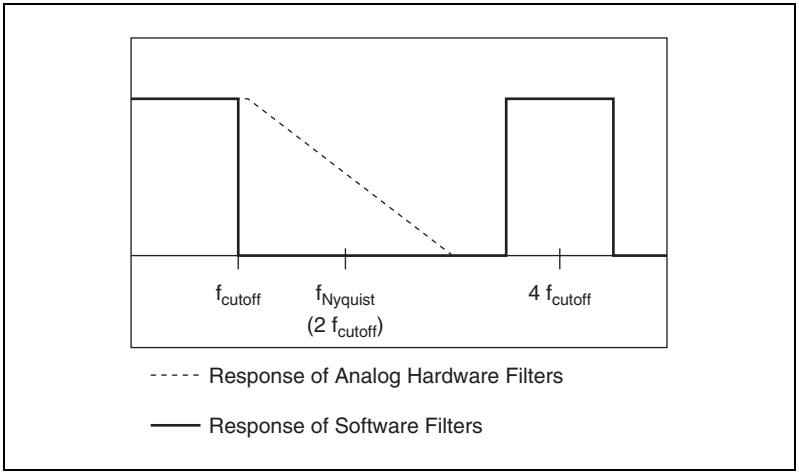

Figure 3-9. Effects of Hardware and Software Filtering on Antialiasing

Phase-Locked Loop Circuit

- NI PXI-6115/6120

A phase-locked loop (PLL) circuit accomplishes the synchronization of multiple NI PXI-6115/6120 devices or other PXI devices which support PLL synchronization by allowing these devices to all lock to the same reference clock present on the PXI backplane. This circuit allows you to trigger input or output operations on different devices and ensures that samples occur at the same time.

The PLL circuitry consists of a voltage-controlled crystal oscillator (VCXO) with a tuning range of ±50 ppm. The VCXO generates the 60 MHz master clock used onboard the NI PXI-6115/6120.

The PLL locks to the 10 MHz oscillator line on the PXI backplane bus. A phase comparator running at 1 MHz compares the PXI Bus and VCXO clock. The loop filter then processes the error signal and outputs a control voltage for the VCXO. Figure 3-10 illustrates the block diagram for the NI PXI-6115/6120.

Note This feature is *not* available on the NI PCI-6115/6120.

The PLL circuit is automatically enabled when the NI 6115/6120 is powered up. No configuration steps are required in order to utilize PLL synchronization.

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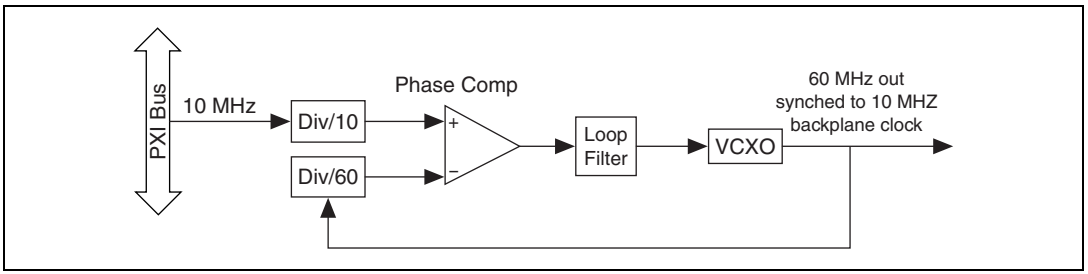

Figure 3-10. PLL Block Diagram

Correlated Digital I/O

The NI 6115/6120 contains eight lines of DIO for general-purpose use. You can software-configure groups of individual lines for either input or output. The NI 6115/6120 includes a FIFO for buffered operation. This operation allows you to read/write an array of data, using either an internal or external clock source, at a maximum rate of 10 MHz. In addition, you can correlate DIO and AI/AO operations to the same clock. Refer to the *Correlating DIO Signal Connections* section of Chapter 4, *Connecting Signals*, for information on which signals you can use to clock DIO operation. At system startup and reset, the DIO ports are all high-impedance.

The hardware up/down control for general-purpose counters 0 and 1 are connected onboard to DIO6 and DIO7, respectively. Thus, you can use DIO6 and DIO7 to control the general-purpose counters. The up/down control signals, GPCTR0_UP_DOWN and GPCTR1_UP_DOWN, are input only and do not affect the operation of the DIO lines.

Timing Signal Routing

The DAQ-STC provides a flexible interface for connecting timing signals to other devices or external circuitry. The NI 6115/6120 uses the RTSI bus to interconnect timing signals between devices, and it uses the programmable function input (PFI) pins on the I/O connector to connect the device to external circuitry. These connections are designed to enable the NI 6115/6120 to both control and be controlled by other devices and circuits.

There are 13 timing signals internal to the DAQ-STC that can be controlled by an external source. These timing signals can also be controlled by signals generated by the DAQ-STC, and these selections are fully software

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configurable. For example, Figure 3-11 shows the signal routing multiplexer for controlling the STARTSCAN signal.

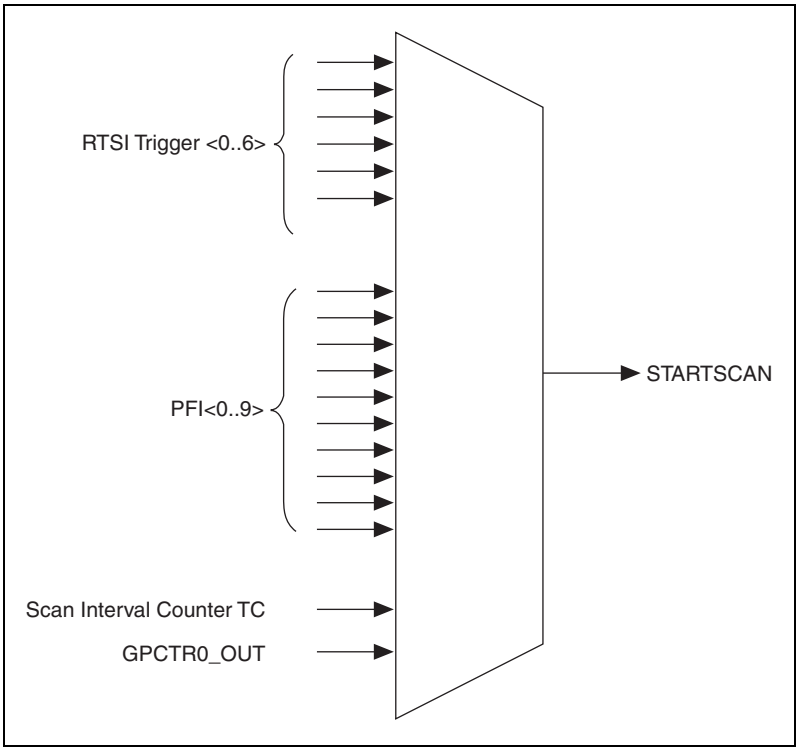

Figure 3-11. STARTSCAN Signal Routing

This figure shows that STARTSCAN can be generated from a number of sources, including the external signals RTSI<0..6> and PFI<0..9> and the internal signals Scan Interval Counter TC and GPCTR0_OUT.

Many of these timing signals are also available as outputs on the RTSI pins, as indicated in the *RTSI Triggers* section later in this chapter, and on the PFI pins, as indicated in Chapter 4, *Connecting Signals*.

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Programmable Function Inputs

The 10 PFIs are connected to the signal routing multiplexer for each timing signal, and software can select one of the PFIs as the external source for a given timing signal. It is important to note that any PFI can be used as an input by any timing signal and that multiple timing signals can simultaneously use the same PFI. This flexible routing scheme reduces the need to change physical connections to the I/O connector for different applications. You also can individually enable each PFI pin to output a specific internal timing signal. For example, if you need the UPDATE* signal as an output on the I/O connector, software can enable the output driver for the PFI5/UPDATE* pin.

Device and RTSI Clocks

Many functions performed by the NI 6115/6120 require a frequency timebase to generate the necessary timing signals for controlling A/D conversions, updates, or general-purpose signals at the I/O connector.

The NI 6115/6120 can use either its internal 20 MHz timebase or a timebase received over the RTSI bus. In addition, if you configure the device to use the internal timebase, you can also program the device to drive its internal timebase over the RTSI bus to another device that is programmed to receive this timebase signal. This clock source, whether local or from the RTSI bus, is used directly by the device as the primary frequency source. The default configuration at startup is to use the internal timebase without driving the RTSI bus timebase signal. This timebase is software selectable.

RTSI Triggers

The seven RTSI trigger lines on the RTSI bus provide a very flexible interconnection scheme for any device sharing the RTSI bus. These bidirectional lines can drive any of eight timing signals onto the RTSI bus and can receive any of these timing signals. The RTSI trigger lines connect to other devices through the PXI bus on the PXI backplane or through a special ribbon cable that must be installed for PCI. Figure 3-12 shows the PCI signal connection scheme and Figure 3-13 shows the PXI connection scheme.

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In PCI, you can access all seven RTSI lines (RTSI<0..6>) through their RTSI cable. With the NI PXI-6115/6120, RTSI<0..5> connects to PXI Trigger <0..5>, respectively, through the NI PXI-6115/6120 backplane. In PXI, RTSI<6> connects to the PXI Star Trigger line, allowing the NI 6115/6120 to receive triggers from any Star Trigger controller plugged into slot 2 of the chassis. For more information on the Star Trigger, refer to the *PXI Specification Revision 2.0*.

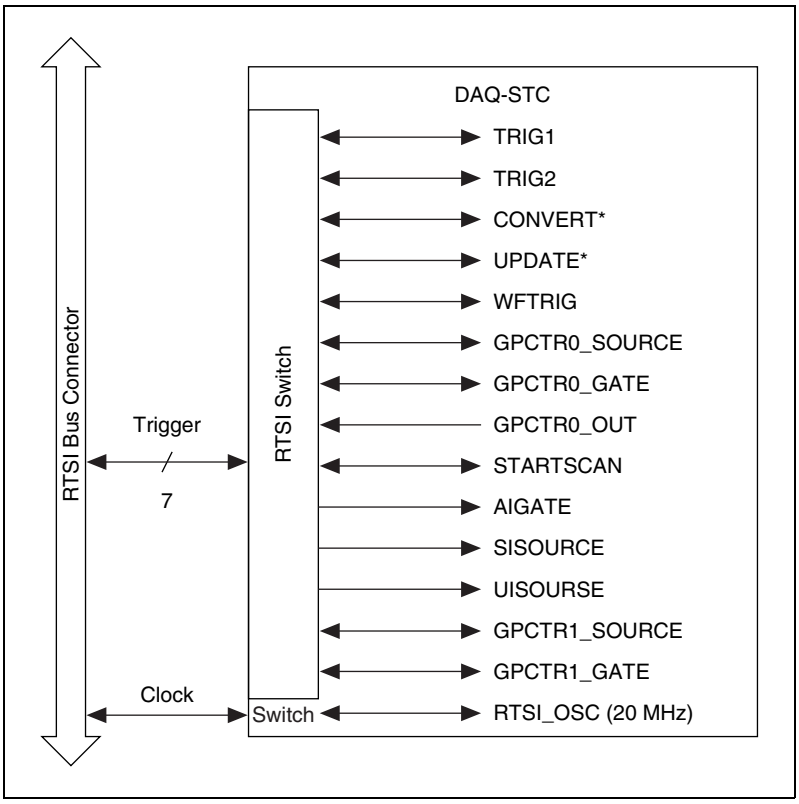

Figure 3-12. PCI RTSI Bus Signal Connection

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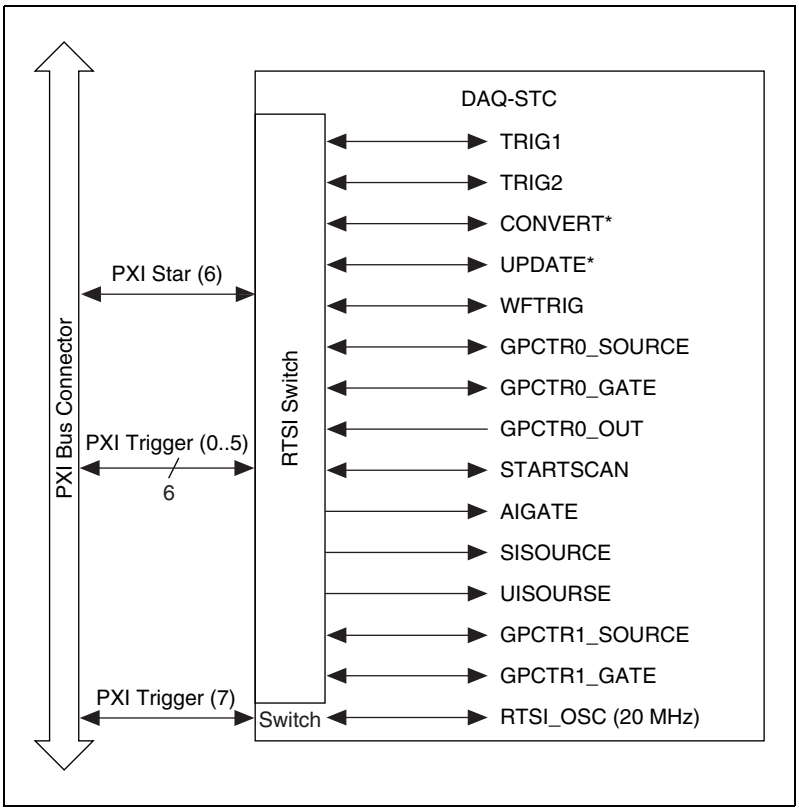

Figure 3-13. PXI RTSI Bus Signal Connections

Refer to the *Connecting Timing Signals* section of Chapter 4, *Connecting Signals*, for a description of the signals shown in Figures 3-12 and 3-13.

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4

Connecting Signals

This chapter describes how to connect input and output signals to the NI 6115/6120 using the device I/O connector.

Table 4-1. I/O Connector Details

Device with I/O Connector	Number of Pins	Cable for Connecting to 100-pin Accessories	Cable for Connecting to 68-pin Accessories
NI 6115, NI 6120	68	N/A	SH6868 Shielded Cable, SH68-68-EP, R6868, SH68-68R1-EP

I/O Connector

Figure 4-1 shows the pin assignments for the 68-pin I/O connector on the NI 6115/6120. A signal description follows the connector pinouts.

Caution Connections that exceed any of the maximum ratings of input or output signals on the NI 6115/6120 can damage the device and the computer. NI is *not* liable for any damage resulting from such signal connections. The *Protection* column of Tables 4-3, 4-4, and 4-5 show the maximum input ratings for each signal.

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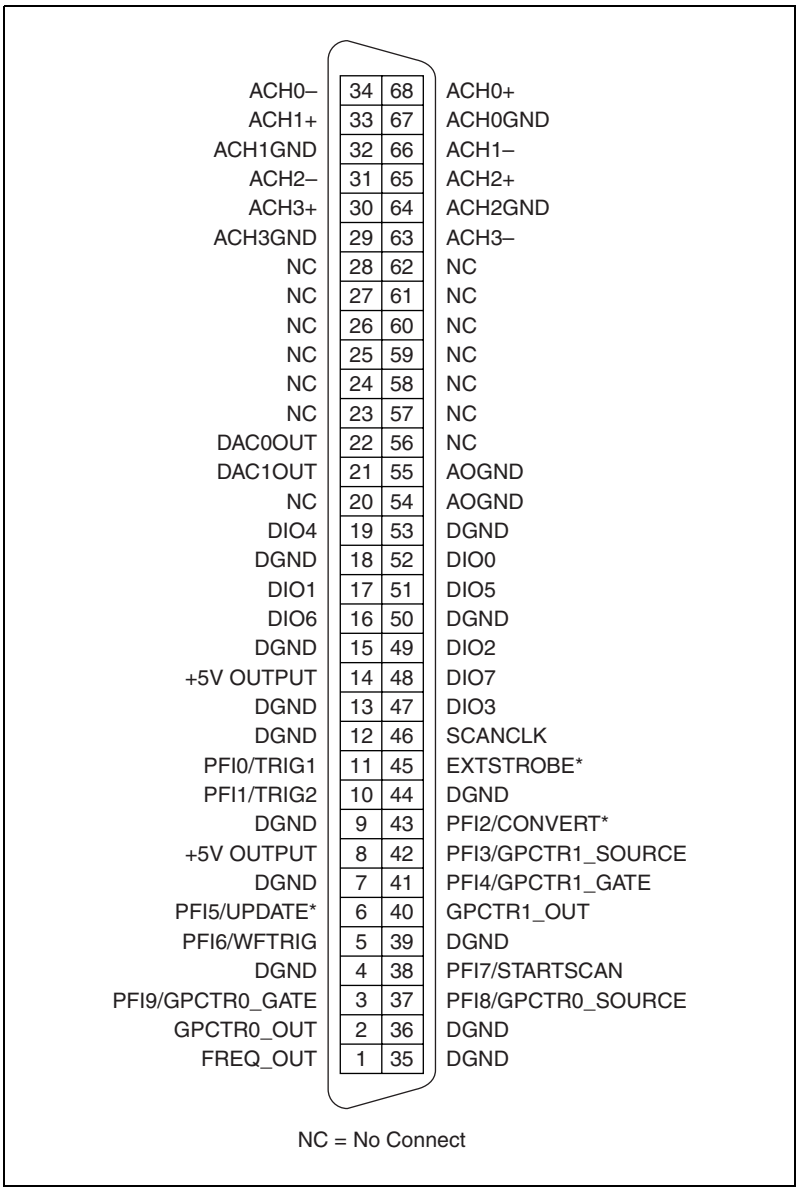

Figure 4-1. I/O Connector Pin Assignment for the NI 6115/6120

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I/O Connector Signal Descriptions

Table 4-2. Signal Descriptions for I/O Connector Pins

Signal Name	Reference	Direction	Description
ACH<0..3>GND	—	—	Ground for Analog Input Channels 0 through 3—These pins are the bias current return point for pseudodifferential measurements.
ACH<0..3>+	ACH<0..3>GND	Input	Analog Input Channels 0 through 3 (+)—These pins are routed to the (+) terminal of the respective channel amplifier and carry the input signal.
ACH<0..3>–	ACH<0..3>GND	Input	Analog Input Channels 0 through 3 (–)—These pins are routed to the (–) terminal of the respective channel amplifier and are the DC reference for the (+) input signal of that channel.
DAC0OUT	AOGND	Output	Analog Channel 0 Output—This pin supplies the voltage output of AO channel 0.
DAC1OUT	AOGND	Output	Analog Channel 1 Output—This pin supplies the voltage output of AO channel 1.
AOGND	—	—	Analog Output Ground—The AO voltages are referenced to this node.
DGND	—	—	Digital Ground—This pin supplies the reference for the digital signals at the I/O connector as well as the +5 VDC supply.
DIO<0..7>	DGND	Input Output	Digital I/O Signals—DIO6 and 7 can control the up/down signal of general-purpose counters 0 and 1, respectively.
+5V	DGND	Output	+5 VDC Source—These pins are fused for up to 1 A of +5 V supply. The fuse is self-resetting.
SCANCLK	DGND	Output	Scan Clock—This pin pulses once for each A/D conversion when enabled. The low-to-high edge indicates when the input signal can be removed from the input or switched to another signal.
EXTSTROBE*	DGND	Output	External Strobe—This output can be toggled under software control to latch signals or trigger events on external devices.

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Table 4-2. Signal Descriptions for I/O Connector Pins (Continued)

Signal Name	Reference	Direction	Description
PFI0/TRIG1	DGND	Input Output	PFI0/Trigger 1—As an input, this is either a PFI or the source for the hardware analog trigger. PFI signals are explained in the *Connecting Timing Signals* section later in this chapter. The hardware analog trigger is explained in the *Analog Trigger* section of Chapter 3, *Hardware Overview*. As an output, this is the TRIG1 signal. In posttrigger DAQ sequences, a low-to-high transition indicates the initiation of the DAQ sequence. In pretrigger applications, a low-to-high transition indicates the initiation of the pretrigger conversions.
PFI1/TRIG2	DGND	Input Output	PFI1/Trigger 2—As an input, this is a PFI. As an output, this is the TRIG2 signal. In pretrigger applications, a low-to-high transition indicates the initiation of the posttrigger conversions. TRIG2 is not used in posttrigger applications.
PFI2/CONVERT*	DGND	Input Output	PFI2/Convert—As an input, this is a PFI. As an output, this is the CONVERT* signal. A high-to-low edge on CONVERT* indicates that an A/D conversion is occurring.
PFI3/GPCTR1_SOURCE	DGND	Input Output	PFI3/Counter 1 Source—As an input, this is a PFI. As an output, this is the GPCTR1_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 1.
PFI4/GPCTR1_GATE	DGND	Input Output	PFI4/Counter 1 Gate—As an input, this is a PFI. As an output, this is the GPCTR1_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 1.
GPCTR1_OUT	DGND	Output	Counter 1 Output—This output is from the general-purpose counter 1 output.
PFI5/UPDATE*	DGND	Input Output	PFI5/Update—As an input, this is a PFI. As an output, this is the UPDATE* signal. A high-to-low edge on UPDATE* indicates that the AO primary group is being updated.
PFI6/WFTRIG	DGND	Input Output	PFI6/Waveform Trigger—As an input, this is a PFI. As an output, this is the WFTRIG signal. In timed AO sequences, a low-to-high transition indicates the initiation of the waveform generation.
PFI7/STARTSCAN	DGND	Input Output	PFI7/Start of Scan—As an input, this is a PFI. As an output, this is the STARTSCAN signal. This pin pulses once at the start of each AI scan in the interval scan. A low-to-high transition indicates the start of the scan.

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Table 4-2. Signal Descriptions for I/O Connector Pins (Continued)

Signal Name	Reference	Direction	Description
PFI8/GPCTR0_SOURCE	DGND	Input Output	PFI8/Counter 0 Source—As an input, this is a PFI. As an output, this is the GPCTR0_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 0.
PFI9/GPCTR0_GATE	DGND	Input Output	PFI9/Counter 0 Gate—As an input, this is a PFI. As an output, this is the GPCTR0_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 0.
GPCTR0_OUT	DGND	Output[1]	Counter 0 Output—This output is from the general-purpose counter 0 output.
FREQ_OUT	DGND	Output	Frequency Output—This output is from the frequency generator output.

[1] The GPCTR0_OUT acts as an input when using external clock mode with correlated DIO.

Table 4-3. Analog I/O Signal Summary for the NI 6115

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
ACH<0..3>+	AI	1 MΩ in parallel with 100 pF[1] or 10 kΩ in parallel with 40 pF[2]	42 V	—	—	—	±300 pA
ACH<0..3>–	AI	10 nF to ACH<0..3> GND	42 V	—	—	—	±300 pA
DAC0OUT	AO	50 Ω	Short-circuit to ground	5 at 10	5 at –10	—	—
DAC1OUT	AO	50 Ω	Short-circuit to ground	5 at 10	5 at –10	—	—

[1] Applies to range ≤ ±10 V, impedance refers to ACH<0..3>–.
[2] Applies to range > ±10 V, impedance refers to ACH<0..3>–.

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Table 4-4. Analog I/O Summary for the NI 6120

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
ACH<0..3>+	AI	100 GΩ to GND	±42 V to GND	—	—	—	±300 pA
ACH<0..3>–	AI	100 GΩ to GND	±42 V to GND	—	—	—	±200 pA
Differential Pair ACH<0..3>+ to ACH<0..3>–	AI	1 MΩ in parallel with 100 pF[1] or 10k in parallel with 40 pF[2]	—	—	—	—	±300 pA
DAC0OUT	AO	50 Ω	Short-circuit to ground	5 at 10	5 at –10	—	—
DAC1OUT	AO	50 Ω	Short-circuit to ground	5 at 10	5 at –10	—	—

[1] Applies to range ≤ ±10 V, impedance refers to ACH<0..3>–.
[2] Applies to range > ±10 V, impedance refers to ACH<0..3>–.

Table 4-5. Digital I/O Signal Summary

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
VCC	DO	0.1 Ω	Short-circuit to ground	1 A	—	—	—
DIO<0..7>	DIO	—	V_{CC} +0.5	13 at (V_{CC} –0.4)	24 at 0.4	1.1	50 kΩ pu
SCANCLK	DO	—	—	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
EXTSTROBE*	DO	—	—	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI0/TRIG1	AI DIO	10 kΩ	±35 V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	9 kΩ pu and 10 kΩ pd
PFI1/TRIG2	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI2/CONVERT*	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu

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Table 4-5. Digital I/O Signal Summary (Continued)

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
PFI3/GPCTR1_SOURCE	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI4/GPCTR1_GATE	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR1_OUT	DO	—	—	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI5/UPDATE*	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI6/WFTRIG	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI7/STARTSCAN	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI8/GPCTR0_SOURCE	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI9/GPCTR0_GATE	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR0_OUT	DIO	—	V_{CC} +0.5	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu
FREQ_OUT	DO	—	—	3.5 at (V_{CC} –0.4)	5 at 0.4	1.5	50 kΩ pu

pu = pull up; pd = pull down; DO = Digital Output

The tolerance on the 50 kΩ pull-up and pull-down resistors is very large. Actual value may range between 17 and 100 kΩ.

Types of Signal Sources

When making signal connections, you must first determine whether the signal sources are floating or ground-referenced. The following sections describe these two types of signals.

Floating Signal Sources

A floating signal source is not connected in any way to the building ground system but, rather, has an isolated ground-reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolator outputs, and isolation amplifiers. An instrument or device that has an isolated output is a floating signal

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source. You must tie the ground reference of a floating signal to the NI 6115/6120 AI ground to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies as the source floats out of the common-mode input range.

Ground-Referenced Signal Sources

A ground-referenced signal source is connected in some way to the building system ground and is, therefore, already connected to a common ground point with respect to the NI 6115/6120, assuming that the computer is plugged into the same power system. Non-isolated outputs of instruments and devices that plug into the building power system fall into this category.

The difference in ground potential between two instruments connected to the same building power system is typically between 1 and 100 mV but can be much higher if power distribution circuits are not properly connected. If a grounded signal source is improperly measured, this difference may appear as an error in the measurement. The connection instructions for grounded signal sources are designed to eliminate this ground potential difference from the measured signal.

Connecting Analog Input Signals

The NI 6115/6120 channels are configured as pseudodifferential inputs. The input signal of each channel, ACH<0..3>+, is tied to the positive input of its PGIA, and each reference signal, ACH<0..3>–, is tied to the negative input of its PGIA. The inputs are differential only in the sense that ground loops are broken. The reference signal, ACH<0..3>–, is not intended to carry signals of interest but only to provide a DC reference point for ACH<0..3>+ that may be different from ground.

Pseudodifferential signal connections increase common-mode noise rejection. They also allow input signals to float within the common-mode limits of the PGIA.

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Connections for Ground-Referenced Signal Sources

Figures 4-2 and 4-3 show how to connect a ground-referenced signal source to a channel on the NI 6115 and NI 6120, respectively.

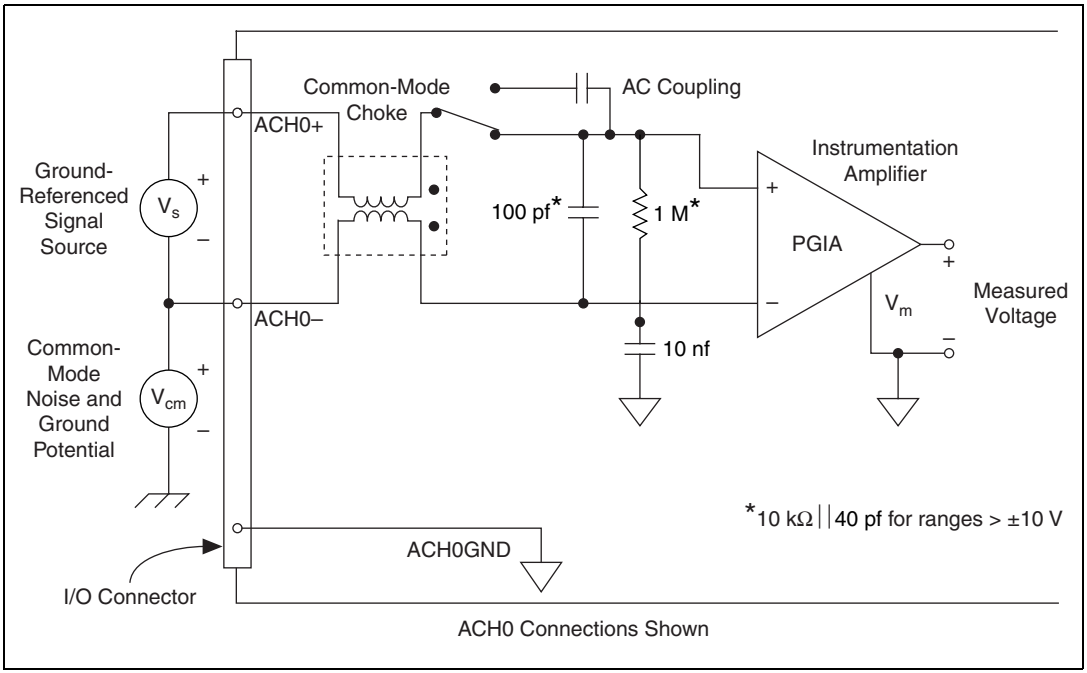

Figure 4-2. Pseudodifferential Input Connections on the NI 6115 for Ground-Referenced Signals

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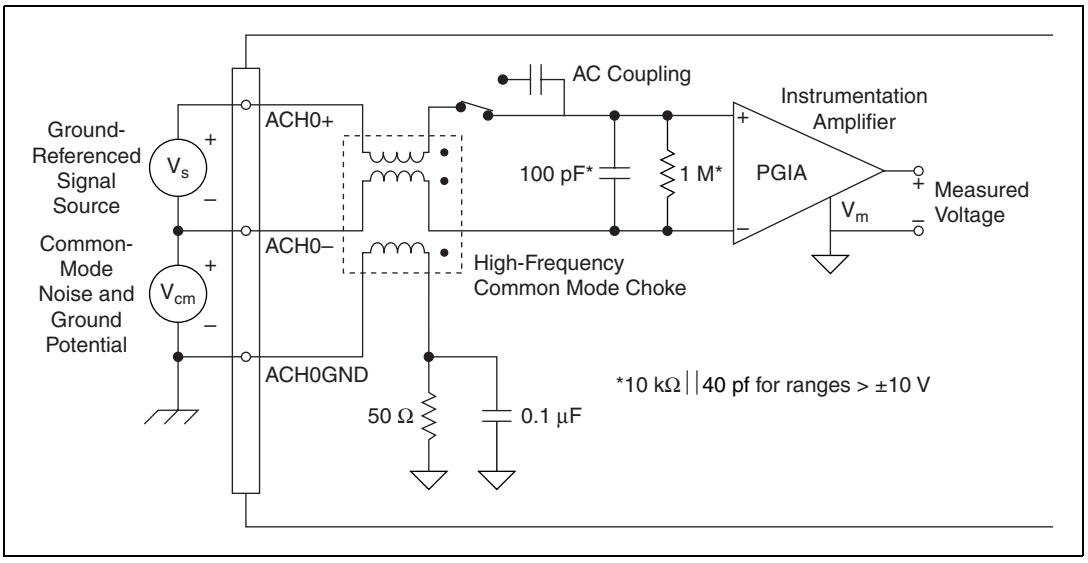

Figure 4-3. Pseudodifferential Input Connections on the NI 6120 for Ground-Referenced Signals

With this type of connection, the PGIA rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the device ground, shown as V_{cm} in Figures 4-2 and 4-3.

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Connections for Nonreferenced or Floating Signal Sources

Figures 4-4 and 4-5 show how to connect a floating signal source to a channel on the NI 6115 and NI 6120, respectively.

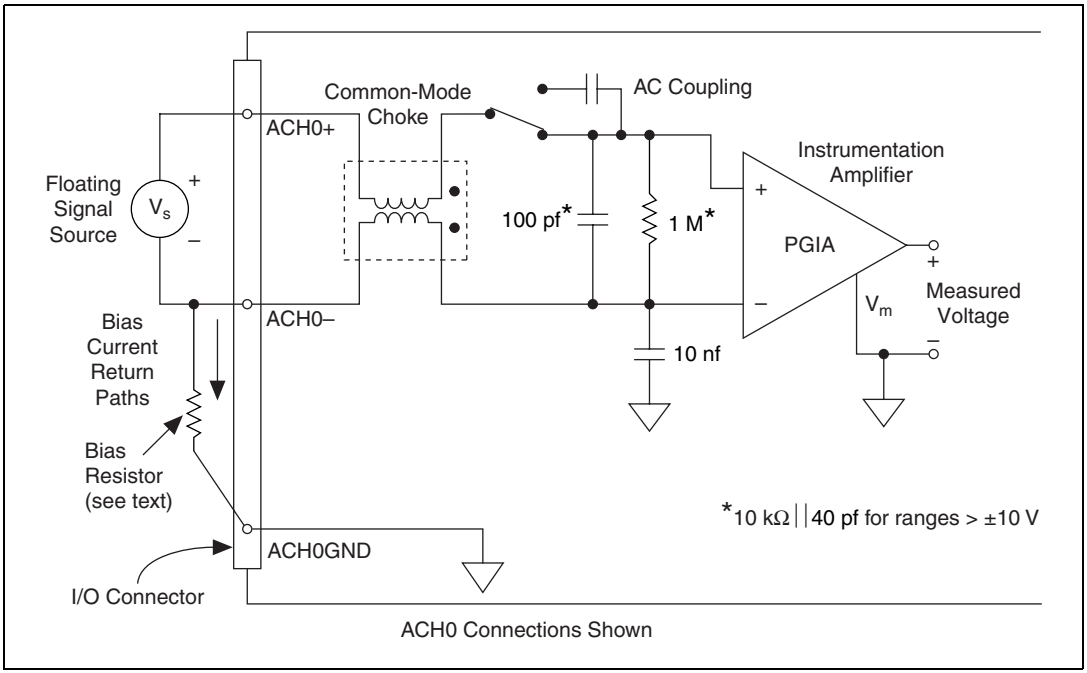

Figure 4-4. Differential Input Connections on the NI 6115 for Nonreferenced Signals

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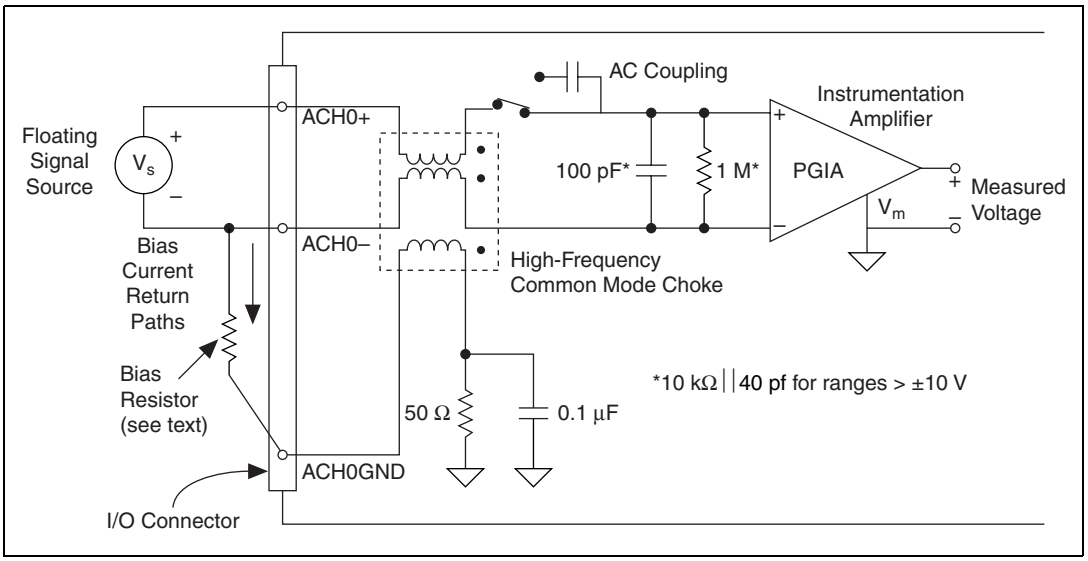

Figure 4-5. Differential Input Connections on the NI 6120 for Nonreferenced Signals

Figures 4-4 and 4-5 show a bias resistor connected between ACH0– and the floating signal source ground. This resistor provides a return path for the ±200 pA bias current. A value of 10 kΩ to 100 kΩ is usually sufficient. If you do not use the resistor and the source is truly floating, the source is not likely to remain within the common-mode signal range of the PGIA, and the PGIA saturates, causing erroneous readings. You must reference the source to the respective channel ground.

Common-mode rejection might be improved by using another bias resistor from the ACH0+ input to ACH0GND. This connection gives a slight measurement error due to the voltage divider formed with the output impedance of the floating source, but it also gives a more balanced input for better common-mode rejection.

Common-Mode Signal Rejection Considerations

Figures 4-2 and 4-3 show connections for signal sources that are already referenced to some ground point with respect to the NI 6115/6120. In theory, the PGIA can reject any voltage caused by ground-potential differences between the signal source and the device. In addition, with pseudodifferential input connections, the PGIA can reject common-mode noise pickup in the leads connecting the signal sources to the device.

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Like any amplifier, the common-mode rejection ratio (CMRR) of the PGIA is limited at high frequency. This limitation has been compensated for in the design of the NI 6115/6120 by using a common-mode choke on each channel.

- NI 6115

  The purpose of the 10 nF capacitance on the ACH<0..3>– connection of the NI 6115 is to provide an impedance for this choke to work against at high frequency, thus improving the high-frequency CMRR. Depending on your application and the type of common noise at your source, further common-noise rejection might be gained by placing a 0.1 μF ceramic bypass capacitor between ACH– and ACH0GND.

Working Voltage Range

The PGIA operates normally by amplifying signals of interest while rejecting common-mode signals as long as the following three conditions are met:

1. The common-mode voltage (V_{cm}), which is equivalent to subtracting ACH<0..3>GND from ACH<0..3>– and which is shown in Figure 4-2, must be less than ±2.5 V. This V_{cm} is a constant for all range selections.
2. The signal voltage (V_s), which is equivalent to subtracting ACH<0..3>– from ACH<0..3>+ and which is shown in Figure 4-2, must be less than or equal to the range selection of the given channel. If V_s is greater than the range selected, the signal clips and information is lost.
3. The total working voltage of the positive input, which can be thought of as ($V_{cm} + V_s$) or simply as subtracting ACH<0..3>GND from ACH<0..3>+, must be less than ±11 V for ranges ≤ ±10 V or less than ±42 V for ranges > ±10 V.

If any of these conditions are exceeded, current limiters limit the input current to 20 mA maximum into any input until the fault condition is removed.

Note All inputs are protected at up to ±42 V.

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Connecting Analog Output Signals

The AO signals are DAC0OUT, DAC1OUT, and AOGND.

DAC0OUT is the voltage output signal for AO channel 0. DAC1OUT is the voltage output signal for AO channel 1.

AOGND is the ground-reference signal for the AO channels. AOGND is a hard ground.

Figure 4-6 shows how to connect AO signals to the NI 6115/6120.

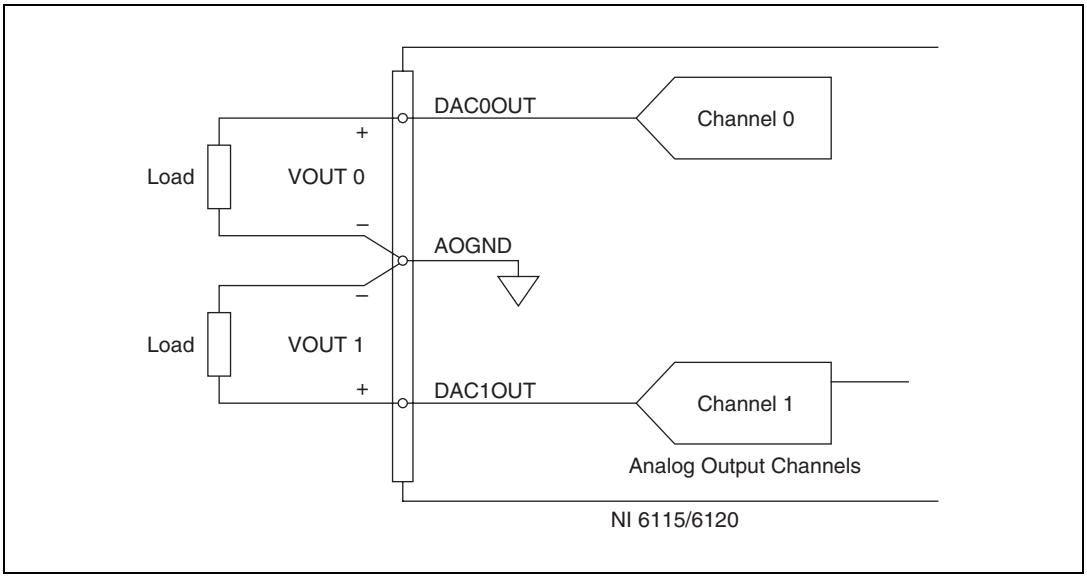

Figure 4-6. Analog Output Connections

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Connecting Digital I/O Signals

The DIO signals are DIO<0..7> and DGND. DIO<0..7> are the signals making up the DIO port, and DGND is the ground-reference signal for the DIO port. You can program groups of individual lines to be inputs or outputs.

Caution Exceeding the maximum input voltage ratings, which are listed in Table 4-3, can damage the NI 6115/6120 and the computer. NI is *not* liable for any damage resulting from such signal connections.

Figure 4-7 shows signal connections for three typical DIO applications.

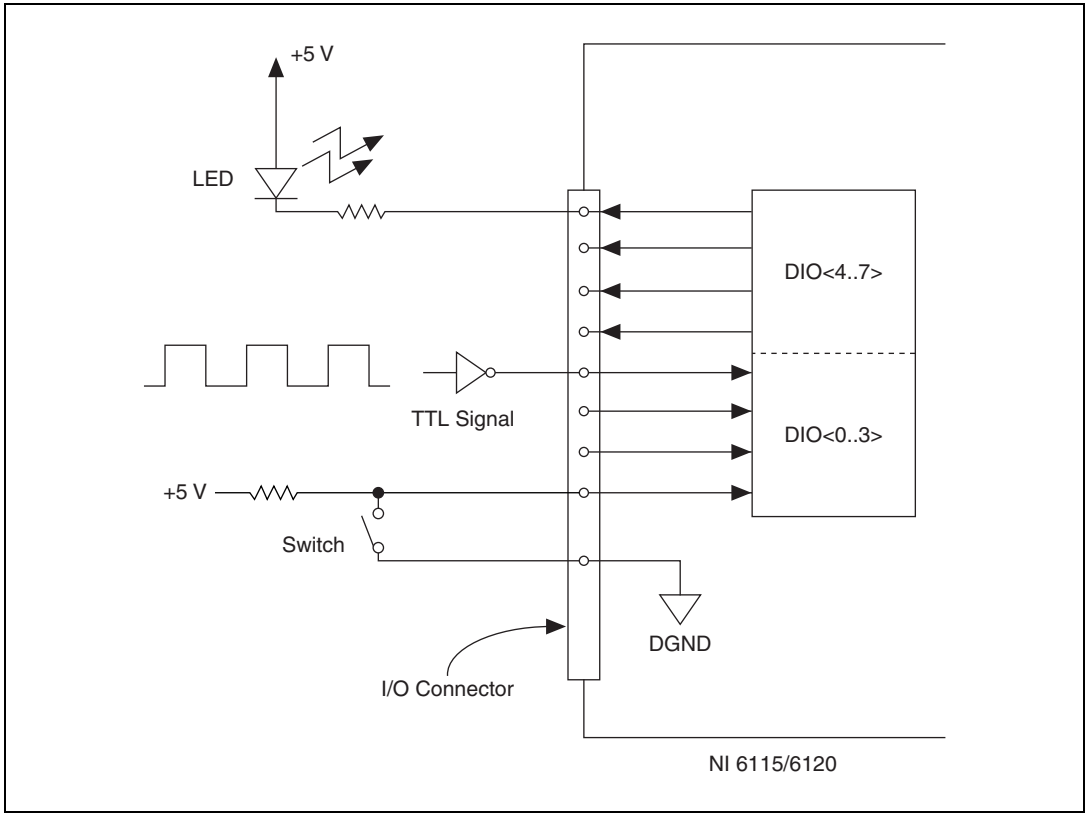

Figure 4-7. Digital I/O Connections

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Figure 4-7 shows DIO<0..3> configured for digital input and DIO<4..7> configured for digital output. Digital input applications include receiving TTL signals and sensing external device states such as the switch state shown in Figure 4-7. Digital output applications include sending TTL signals and driving external devices such as the LED shown in Figure 4-7.

Correlating DIO Signal Connections

You can correlate DIO and AI/AO operations to the same clock on the NI 6115/6120. You can use any of the following signals as the clock source:

- AI Scan Start
- AO Update
- GPCTR
- RTSI<0..5>
- External Clock

Notes To use either of the GPCTR signals or the external clock to clock DIO operations, you must use one RTSI<0..5> pin.

To use an external clock for correlated DIO, the clock must have input on the Counter 0 output pin (GPCTR0_OUT). In this case, be sure that this counter is not used in any other operation.

The following timing diagrams illustrate the use of these signals as clock sources. You can software-configure DIO operations for either rising or falling edge on whichever clock you choose as the source. Figure 4-8 shows any clock signal, in general, driving two separate groups of lines configured for digital input (DI) and DO. The DI operation is using the rising edge of the clock and the DO operation is using its falling edge.

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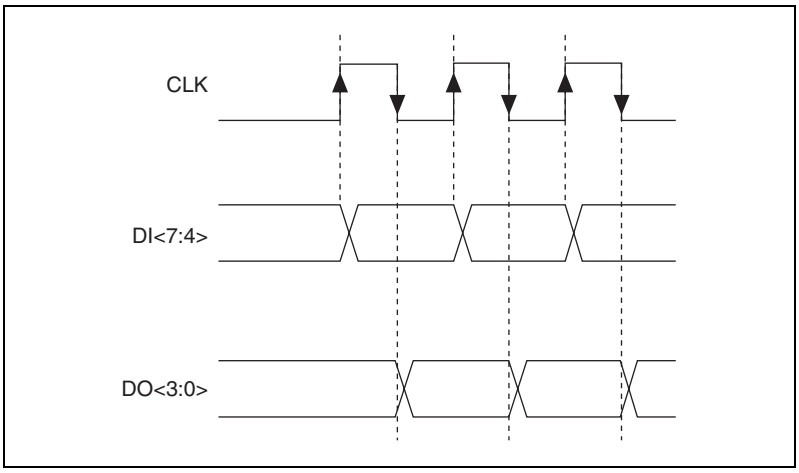

Figure 4-8. Clock Signal Driving DI and DO Signals

Figure 4-9 shows a DIO operation driven by the AO Update signal on its rising edge.

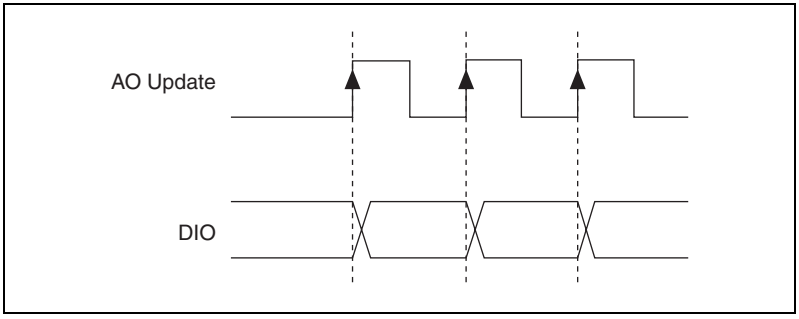

Figure 4-9. Rising-Edge AO Update Signal Driving a DIO Signal

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Figure 4-10 shows a DIO operation driven by an RTSI clock signal on its falling edge.

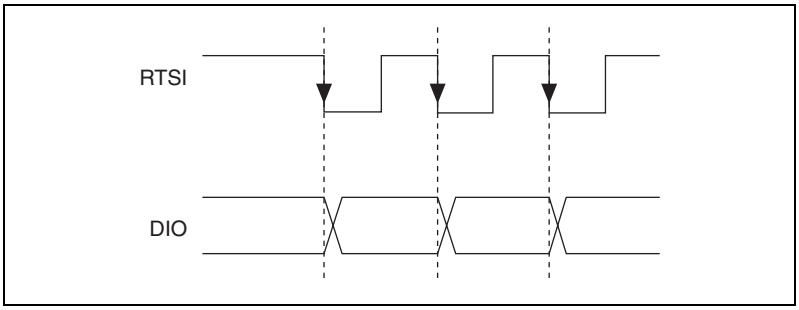

Figure 4-10. Falling-Edge RTSI Clock Signal Driving a DIO Signal

Power Connections

Two pins on the I/O connector supply +5 V from the computer power supply using a self-resetting fuse. The fuse resets automatically within a few seconds after the overcurrent condition is removed. These pins are referenced to DGND and can be used to power external digital circuitry. The power rating is +4.65 to +5.25 VDC at 1 A.

Caution Under *no* circumstances should you connect these +5 V power pins directly to analog or digital ground or to any other voltage source on the NI 6115/6120 or any other device. Doing so can damage the NI 6115/6120 and the computer. NI is *not* liable for damage resulting from such connections.

Connecting Timing Signals

Caution Exceeding the maximum input voltage ratings, which are listed in Table 4-3, can damage the NI 6115/6120 and the computer. NI is *not* liable for any damage resulting from such signal connections.

All external control over the timing of the NI 6115/6120 is routed through the 10 PFIs, labeled PFI0 through PFI9. These signals are explained in detail in the *Programmable Function Input Connections* section. These PFIs are bidirectional; as outputs they are not programmable and reflect the state of many DAQ, waveform generation, and general-purpose timing signals. There are five other dedicated outputs for the remainder of the timing signals. As inputs, the PFI signals are programmable and can control DAQ, waveform generation, and general-purpose timing signals.

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The DAQ signals are explained in the *DAQ Timing Connections* section later in this chapter. The *Waveform Generation Timing Connections* section later in this chapter explains the waveform generation signals, and the *General-Purpose Timing Signal Connections* section later in this chapter explains the general-purpose timing signals.

All digital timing connections are referenced to DGND. This reference is demonstrated in Figure 4-11, which shows how to connect an external TRIG1 source and an external STARTSCAN source to two PFI pins on the NI 6115/6120.

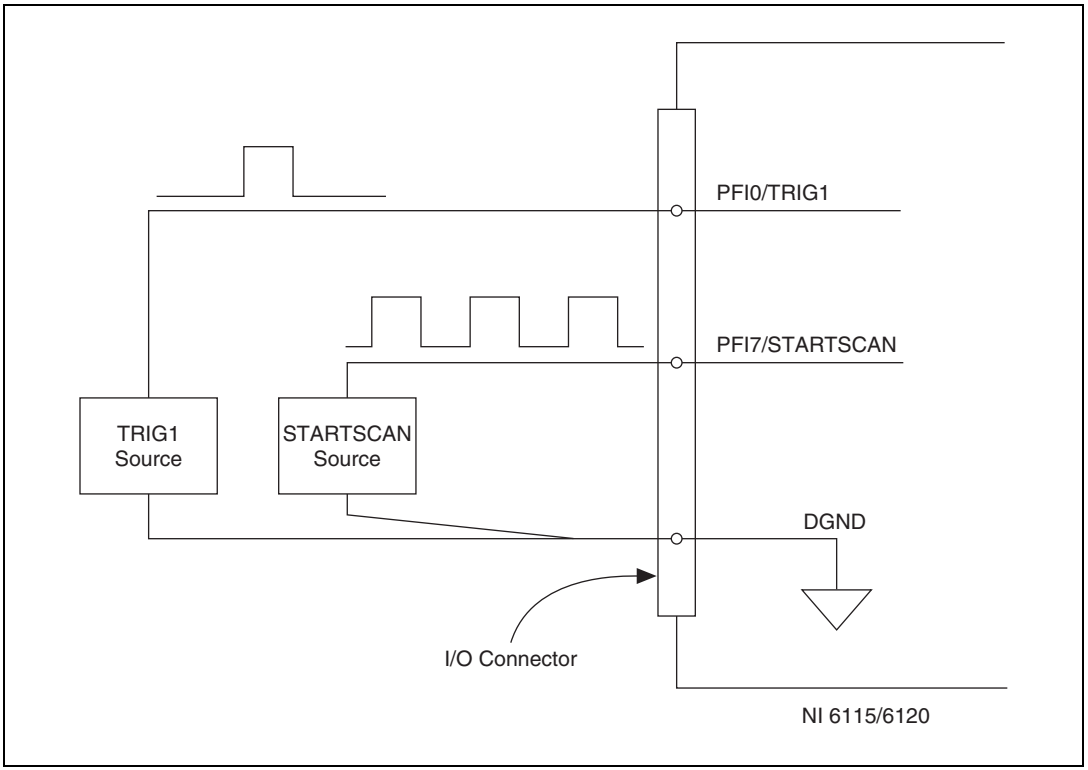

Figure 4-11. Timing I/O Connections

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Programmable Function Input Connections

You can externally control 13 internal timing signals from the PFI pins. The source for each of these signals is software selectable from any PFI when you want external control. This flexible routing scheme reduces the need to change the physical wiring to the device I/O connector for different applications requiring alternative wiring.

You can individually enable each of the PFI pins to output a specific internal timing signal. For example, if you need the STARTSCAN signal as an output on the I/O connector, software can turn on the output driver for the PFI7/STARTSCAN pin. Be careful not to drive a PFI signal externally when it is configured as an output.

As an input, each PFI can be individually configured for edge or level detection and for polarity selection, as well. You can use the polarity selection for any of the timing signals, but the edge or level detection depends upon the particular timing signal being controlled. The detection requirements for each timing signal are listed within the section that discusses that individual signal.

In edge-detection mode, the minimum pulse width required is 10 ns. This setting applies for both rising-edge and falling-edge polarity settings. Edge-detect mode does not have a maximum pulse-width requirement.

In level-detection mode, the PFIs themselves do not impose a minimum or maximum pulse-width requirement, but the particular timing signal being controlled can impose limits. These requirements are listed later in this chapter.

DAQ Timing Connections

The DAQ timing signals are TRIG1, TRIG2, STARTSCAN, CONVERT*, AIGATE, SISOURCE, SCANCLK, and EXTSTROBE*.

Posttriggered data acquisition allows you to view only data that is acquired after a trigger event is received. A typical posttriggered DAQ sequence is shown in Figure 4-12.

Note On the NI 6115/6120, each STARTSCAN pulse initiates one CONVERT* pulse, which simultaneously samples all channels.

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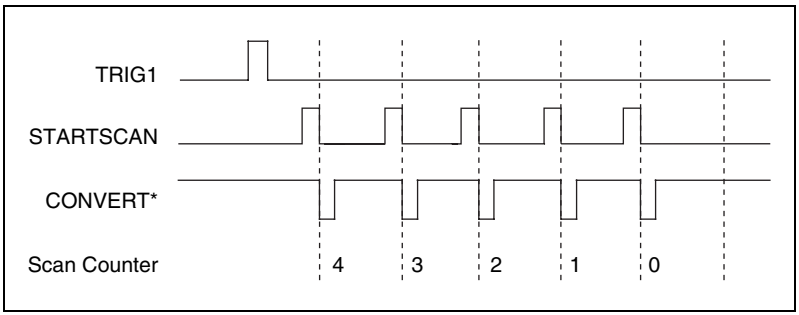

Figure 4-12. Typical Posttriggered Acquisition

Pretriggered data acquisition allows you to view data that is acquired before the trigger of interest in addition to data acquired after the trigger. Figure 4-13 shows a typical pretriggered DAQ sequence. The description for each signal shown in these figures appears later in this chapter.

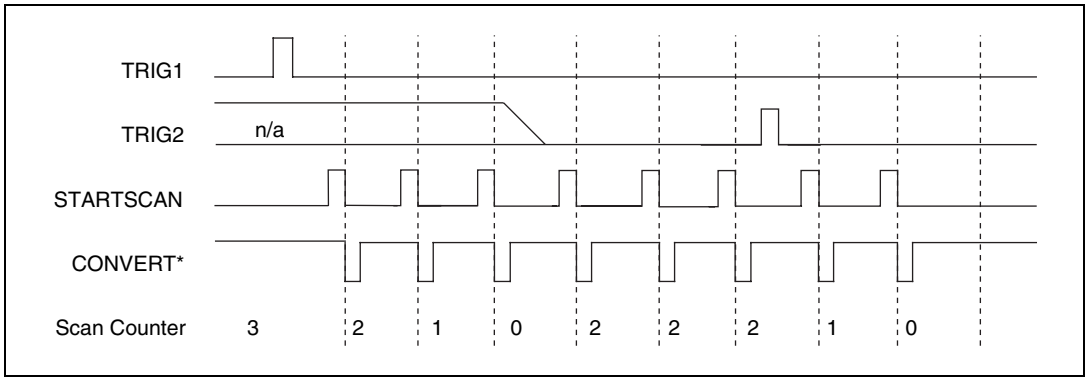

Figure 4-13. Typical Pretriggered Acquisition

TRIG1 Signal

Any PFI pin can receive as an input the TRIG1 signal, which is available as an output on the PFI0/TRIG1 pin.

Refer to Figures 4-12 and 4-13 for the relationship of TRIG1 to the DAQ sequence.

As an input, TRIG1 is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG1 and configure the polarity selection for either rising or falling edge. The selected edge of TRIG1 starts the DAQ sequence for both posttriggered and pretriggered acquisitions. The NI 6115/6120 supports analog triggering on the PFI0/TRIG1 pin.

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Refer to Chapter 3, *Hardware Overview*, for more information on analog triggering.

As an output, TRIG1 reflects the action that initiates a DAQ sequence even if another PFI is externally triggering the acquisition. The output is an active high pulse with a pulse width of 25 to 50 ns. This output is set to high-impedance at startup.

Figures 4-14 and 4-15 show the timing requirements for TRIG1.

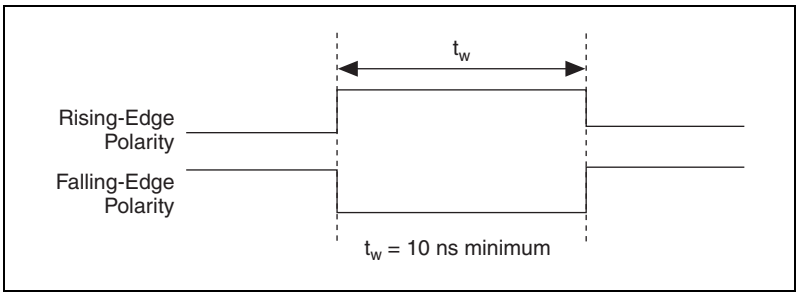

Figure 4-14. TRIG1 Input Signal Timing

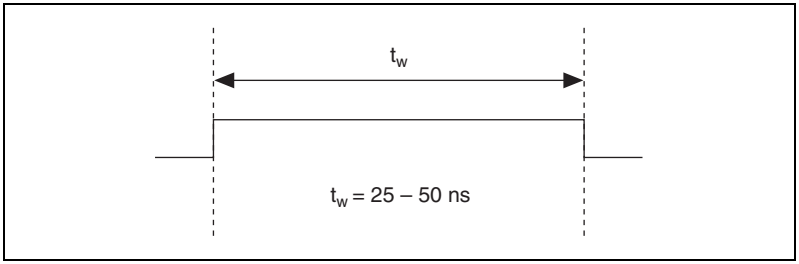

Figure 4-15. TRIG1 Output Signal Timing

The device also uses TRIG1 to initiate pretriggered DAQ operations. In most pretriggered applications, TRIG1 is generated by a software trigger. Refer to the TRIG2 signal description for a complete description of the use of TRIG1 and TRIG2 in a pretriggered DAQ operation.

TRIG2 Signal

Any PFI pin can receive as an input the TRIG2 signal, which is available as an output on the PFI1/TRIG2 pin. Refer to Figure 4-13 for the relationship of TRIG2 to the DAQ sequence.

As an input, TRIG2 is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG2 and configure the polarity

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selection for either rising or falling edge. The selected edge of TRIG2 initiates the posttriggered phase of a pretriggered DAQ sequence. In pretriggered mode, the TRIG1 signal initiates the acquisition. The scan counter indicates the minimum number of scans before TRIG2 can be recognized. After the scan counter decrements to zero, it is loaded with the number of posttrigger scans to acquire while the acquisition continues. The device ignores TRIG2 if it is asserted prior to the scan counter decrementing to zero. After the selected edge of TRIG2 is received, the device acquires a fixed number of scans and the acquisition stops. This mode acquires data both before and after receiving TRIG2.

As an output, TRIG2 reflects the posttrigger in a pretriggered DAQ sequence even if another PFI is externally triggering the acquisition. TRIG2 is not used in posttriggered data acquisition. The output is an active high pulse with a pulse width of 25 to 50 ns. This output is set to high-impedance at startup.

Figures 4-16 and 4-17 show the timing requirements for TRIG2.

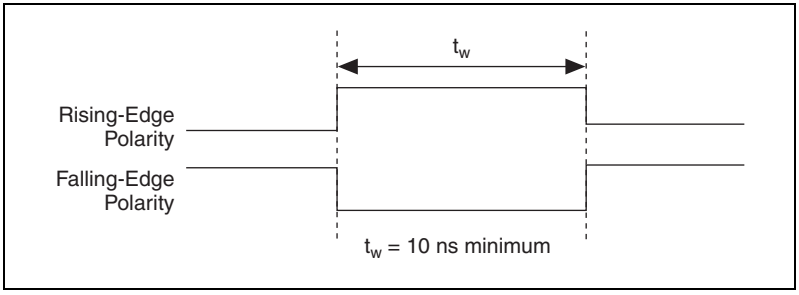

Figure 4-16. TRIG2 Input Signal Timing

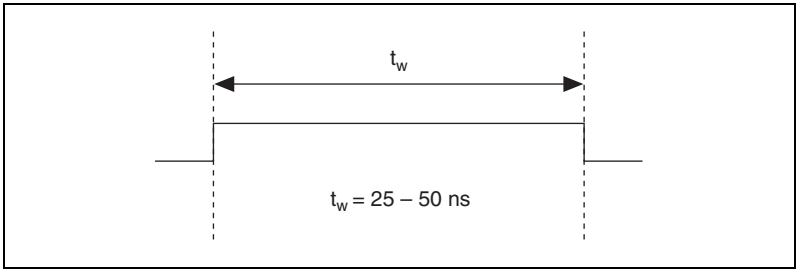

Figure 4-17. TRIG2 Output Signal Timing

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STARTSCAN Signal

Any PFI pin can receive as an input the STARTSCAN signal, which is available as an output on the PFI7/STARTSCAN pin. Refer to Figures 4-18 and 4-19 for the relationship of STARTSCAN to the DAQ sequence.

As an input, STARTSCAN is configured in the edge-detection mode. You can select any PFI pin as the source for STARTSCAN and configure the polarity selection for either rising or falling edge. The selected edge of STARTSCAN initiates a scan. The sample interval counter starts if you select internally triggered CONVERT*.

As an output, STARTSCAN reflects the actual start pulse that initiates a scan even if another PFI is externally triggering the starts. You have two output options. The first is an active high pulse with a pulse width of 25 to 50 ns, which indicates the start of the scan. The second action is an active high pulse that terminates at the start of the last conversion in the scan, which indicates a scan in progress. STARTSCAN is deasserted t_{off} after the last conversion in the scan is initiated. This output is set to high-impedance at startup.

Figures 4-18 and 4-19 show the timing requirements for STARTSCAN.

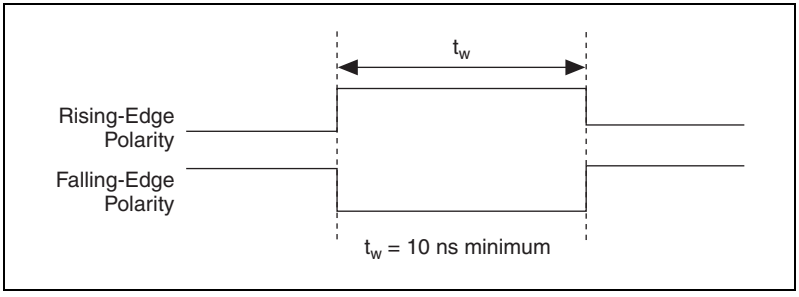

Figure 4-18. STARTSCAN Input Signal Timing

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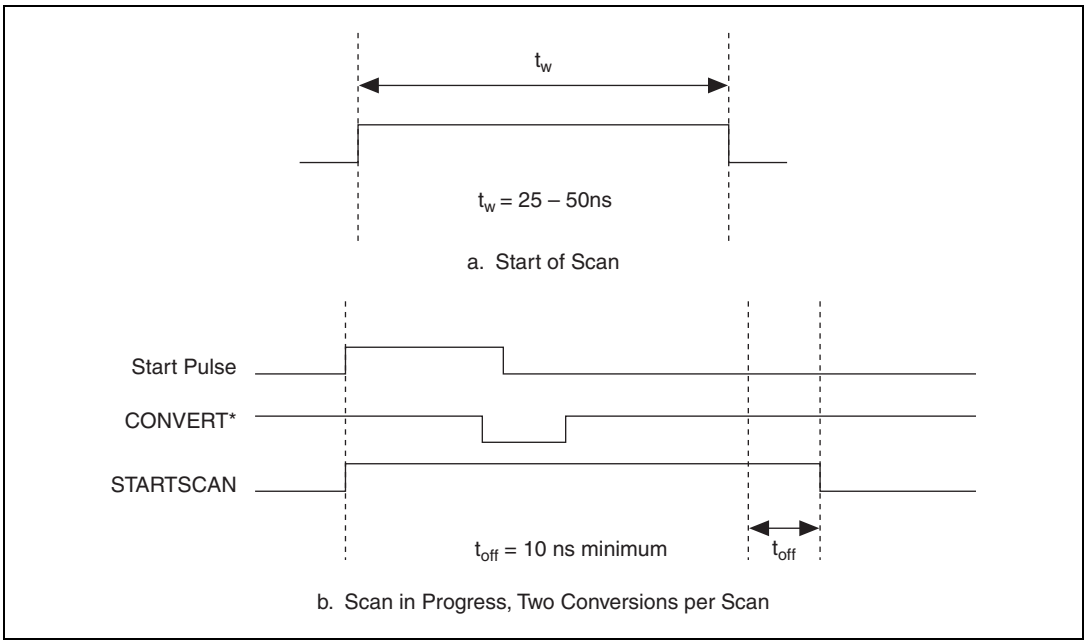

Figure 4-19. STARTSCAN Output Signal Timing

The CONVERT* pulses are masked off until the device generates STARTSCAN. If you are using internally generated conversions, the first CONVERT* appears when the onboard sample interval counter reaches zero. If you select an external CONVERT*, the first external pulse after STARTSCAN generates a conversion. STARTSCAN pulses should be separated by at least one scan period.

A counter on the NI 6115/6120 internally generates STARTSCAN unless you select some external source. This counter is started by the TRIG1 signal and is stopped by either software or the sample counter.

Scans generated by either an internal or external STARTSCAN signal are inhibited unless they occur within a DAQ sequence. Scans occurring within a DAQ sequence may be gated by either the hardware signal AIGATE or the software command register gate.

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CONVERT* Signal

Any PFI pin can receive as an input the CONVERT* signal, which is available as an output on the PFI2/CONVERT* pin.

Refer to Figures 4-20 and 4-21 for the relationship of CONVERT* to the DAQ sequence.

As an input, CONVERT* is configured in the edge-detection mode. You can select any PFI pin as the source for CONVERT* and configure the polarity selection for either rising or falling edge. The selected edge of CONVERT* initiates an A/D conversion.

As an output, CONVERT* reflects the actual convert pulse that is connected to the ADC even if another PFI is externally generating the conversions. The output is an active low pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures 4-20 and 4-21 show the input and output timing requirements for CONVERT*.

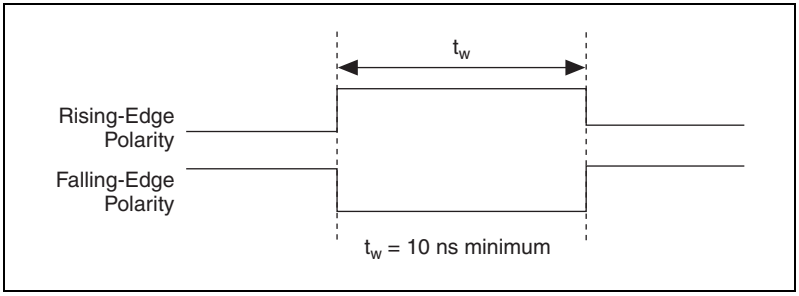

Figure 4-20. CONVERT* Input Signal Timing

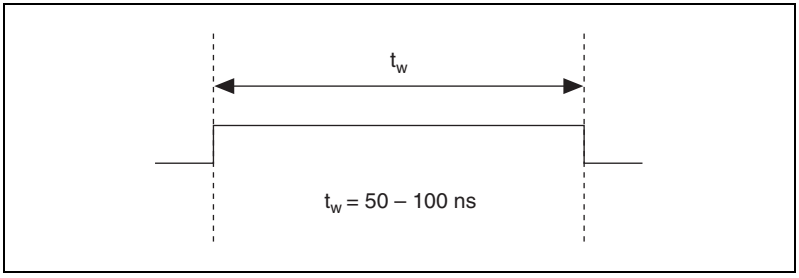

Figure 4-21. CONVERT* Output Signal Timing

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The ADC switches to hold mode within 20 ns of the selected edge. This hold-mode delay time is a function of temperature and does not vary from one conversion to the next.

The sample interval counter on the NI 6115/6120 device normally generates CONVERT* unless you select some external source. The counter is started by the STARTSCAN signal and continues to count down and reload itself until the scan is finished. It then reloads itself in preparation for the next STARTSCAN pulse.

A/D conversions generated by either an internal or external CONVERT* signal are inhibited unless they occur within a DAQ sequence. Scans occurring within a DAQ sequence may be gated by either the hardware signal AIGATE or the software command register gate.

AIGATE Signal

Any PFI pin can receive as an input the AIGATE signal, which is not available as an output on the I/O connector. The AIGATE signal can mask off scans in a DAQ sequence. You can configure the PFI pin you select as the source for AIGATE in level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

In the level-detection mode if AIGATE is active, the STARTSCAN signal is masked off and no scans can occur.

AIGATE can neither stop a scan in progress nor continue a previously gated-off scan. Once a scan has started, AIGATE does not gate off conversions until the beginning of the next scan and, conversely, if conversions are being gated off, AIGATE does not gate them back on until the beginning of the next scan.

SISOURCE Signal

Any PFI pin can receive as an input the SISOURCE signal, which is not available as an output on the I/O connector. The onboard scan interval counter (SI) uses SISOURCE as a clock to time the generation of the STARTSCAN signal. You must configure the PFI pin you select as the source for SISOURCE in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

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Either the 20 MHz or 100 kHz internal timebase generates SISOURCE unless you select some external source. Figure 4-22 shows the timing requirements for SISOURCE.

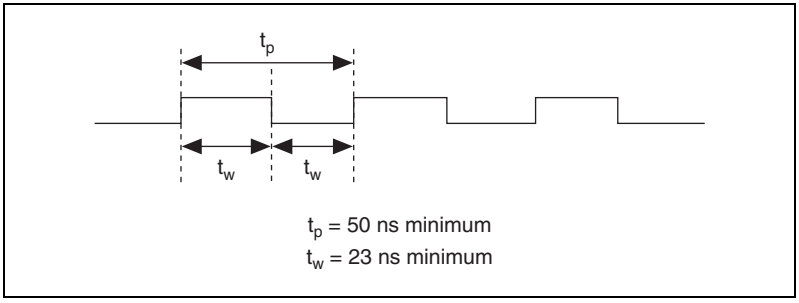

Figure 4-22. SISOURCE Signal Timing

SCANCLK Signal

SCANCLK is an output-only signal that generates a pulse with the leading edge occurring approximately 50 to 100 ns after an A/D conversion begins. The polarity of this output is software selectable but is typically configured so that a low-to-high leading edge can clock external AI multiplexers indicating when the input signal has been sampled and can be removed. This signal has a 450 ns pulse width and is software enabled.

Note When using NI-DAQ, SCANCLK polarity is low-to-high and cannot be changed programmatically.

Figure 4-23 shows the timing for SCANCLK.

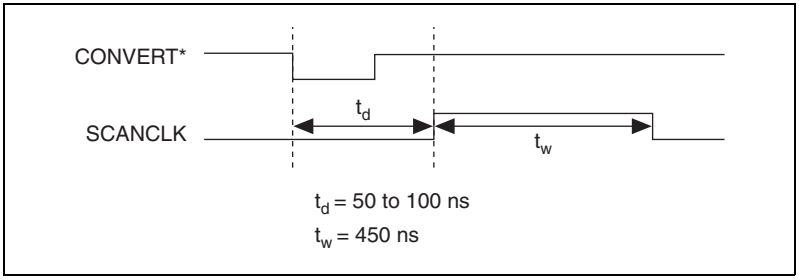

Figure 4-23. SCANCLK Signal Timing

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EXTSTROBE* Signal

EXTSTROBE* is an output-only signal that generates either a single pulse or a sequence of eight pulses in the hardware-strobe mode. An external device can use this signal to latch signals or to trigger events. In the single-pulse mode, software controls the level of EXTSTROBE*. A 10 µs and a 1.2 µs clock are available for generating a sequence of eight pulses in the hardware-strobe mode.

Note EXTSTROBE* cannot be enabled through NI-DAQ.

Figure 4-24 shows the timing for the hardware-strobe mode EXTSTROBE* signal.

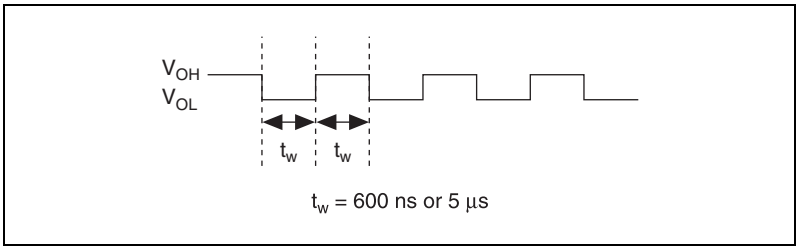

Figure 4-24. EXTSTROBE* Signal Timing

Waveform Generation Timing Connections

The AO group defined for the NI 6115/6120 is controlled by WFTRIG, UPDATE*, and UISOURCE.

WFTRIG Signal

Any PFI pin can receive as an input the WFTRIG signal, which is available as an output on the PFI6/WFTRIG pin.

As an input, WFTRIG is configured in the edge-detection mode. You can select any PFI pin as the source for WFTRIG and configure the polarity selection for either rising or falling edge. The selected edge of WFTRIG starts the waveform generation for the DACs. If you select internally generated UPDATE*, the UI counter starts.

As an output, WFTRIG reflects the trigger that initiates waveform generation, even if another PFI is externally triggering the waveform generation. The output is an active high pulse with a pulse width of 25 to 50 ns. This output is set to high-impedance at startup.

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Figures 4-25 and 4-26 show the timing requirements for WFTRIG.

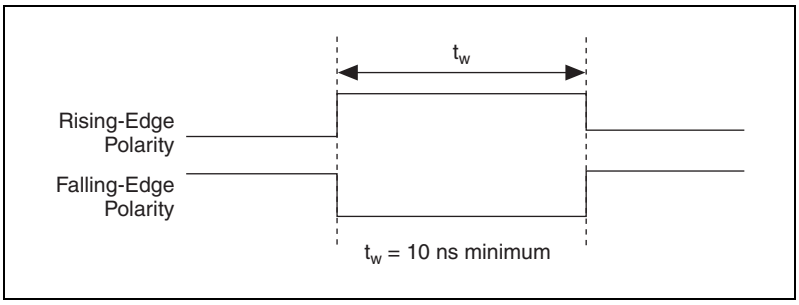

Figure 4-25. WFTRIG Input Signal Timing

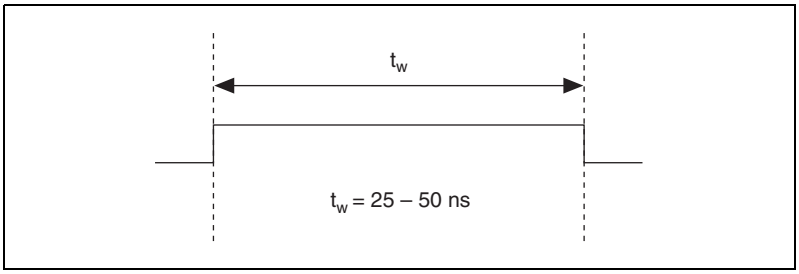

Figure 4-26. WFTRIG Output Signal Timing

UPDATE* Signal

Any PFI pin can receive as an input the UPDATE* signal, which is available as an output on the PFI5/UPDATE* pin.

As an input, UPDATE* is configured in the edge-detection mode. You can select any PFI pin as the source for UPDATE* and configure the polarity selection for either rising or falling edge. The selected edge of UPDATE* updates the outputs of the DACs. In order to use UPDATE*, you must set the DACs to posted-update mode.

As an output, UPDATE* reflects the actual update pulse that is connected to the DACs, even if another PFI is externally generating the updates. The output is an active low pulse with a pulse width of 50 to 75 ns. This output is set to high-impedance at startup.

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Figures 4-27 and 4-28 show the timing requirements for UPDATE*.

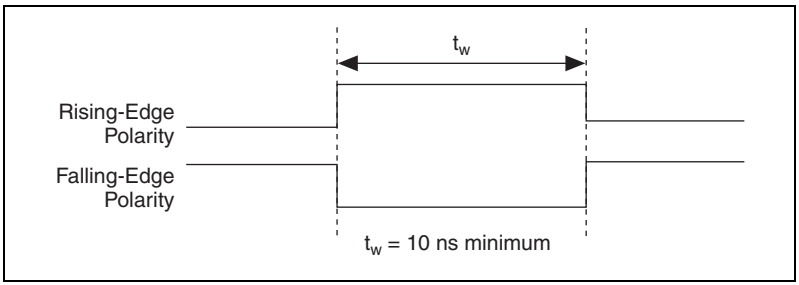

Figure 4-27. UPDATE* Input Signal Timing

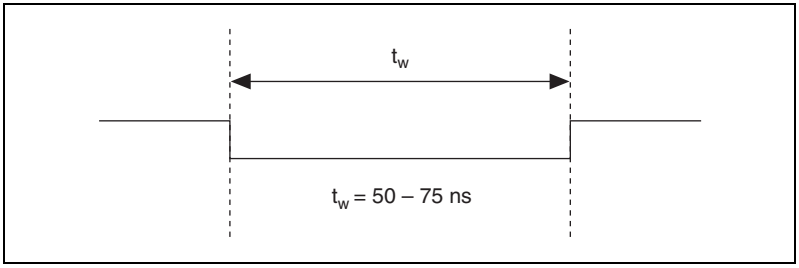

Figure 4-28. UPDATE* Output Signal Timing

The DACs are updated within 100 ns of the leading edge. Separate the UPDATE* pulses with enough time that new data can be written to the DAC latches.

The UI counter for the NI 6115/6120 normally generates UPDATE* unless you select some external source. The UI counter is started by the WFTRIG signal and can be stopped by software or the internal buffer counter (BC).

D/A conversions generated by either an internal or external UPDATE* signal do not occur when gated by the software command register gate.

UISOURCE Signal

Any PFI pin can receive as an input the UISOURCE signal, which is not available as an output on the I/O connector. The UI counter uses UISOURCE as a clock to time the generation of the UPDATE* signal. You must configure the PFI pin you select as the source for UISOURCE in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low. Figure 4-29 shows the timing requirements for UISOURCE.

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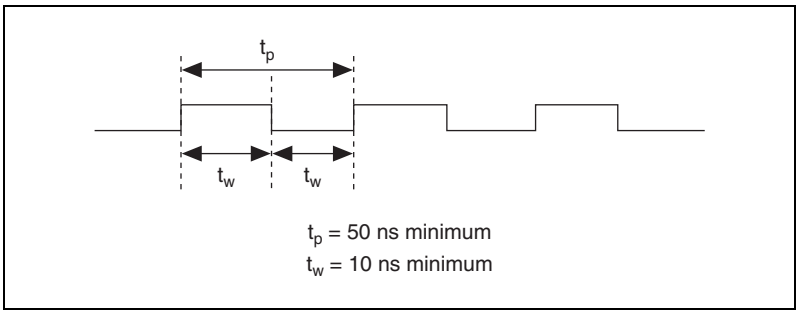

Figure 4-29. UISOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 10 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase normally generates UISOURCE unless you select some external source.

General-Purpose Timing Signal Connections

The general-purpose timing signals are GPCTR0_SOURCE, GPCTR0_GATE, GPCTR0_OUT, GPCTR0_UP_DOWN, GPCTR1_SOURCE, GPCTR1_GATE, GPCTR1_OUT, GPCTR1_UP_DOWN, and FREQ_OUT.

GPCTR0_SOURCE Signal

Any PFI pin can receive as an input the GPCTR0_SOURCE signal, which is available as an output on the PFI8/GPCTR0_SOURCE pin.

As an input, GPCTR0_SOURCE is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, GPCTR0_SOURCE reflects the actual clock connected to general-purpose counter 0, even if another PFI is externally inputting the source clock. This output is set to high-impedance at startup.

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Figure 4-30 shows the timing requirements for GPCTR0_SOURCE.

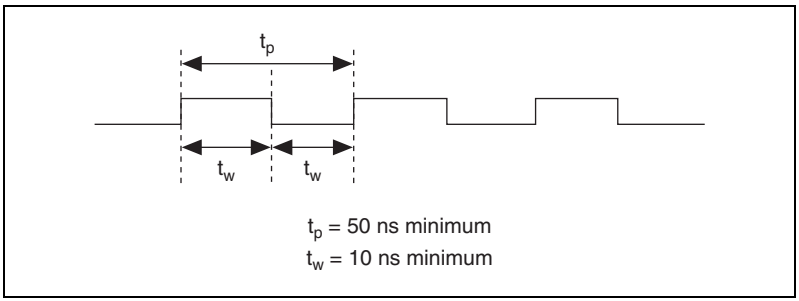

Figure 4-30. GPCTR0_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 10 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates GPCTR0_SOURCE unless you select some external source.

GPCTR0_GATE Signal

Any PFI pin can receive as an input the GPCTR0_GATE signal, which is available as an output on the PFI9/GPCTR0_GATE pin.

As an input, GPCTR0_GATE is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of applications to perform actions such as starting and stopping the counter, generating interrupts, and saving the counter contents.

As an output, GPCTR0_GATE reflects the actual gate signal connected to general-purpose counter 0, even if another PFI is externally generating the gate. This output is set to high-impedance at startup.

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Figure 4-31 shows the timing requirements for GPCTR0_GATE.

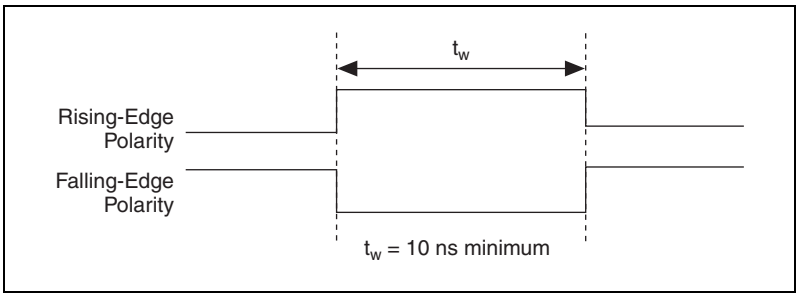

Figure 4-31. GPCTR0_GATE Signal Timing in Edge-Detection Mode

GPCTR0_OUT Signal

This signal is available as an output on the GPCTR0_OUT pin. The GPCTR0_OUT signal reflects the terminal count (TC) of general-purpose counter 0. You have two software-selectable output options: pulse on TC and toggle output polarity on TC. The output polarity is software-selectable for both options. This output is set to high-impedance at startup. Figure 4-32 shows the timing of GPCTR0_OUT.

Note When using external clocking mode with correlated DIO, this pin is used as an input for the external clock.

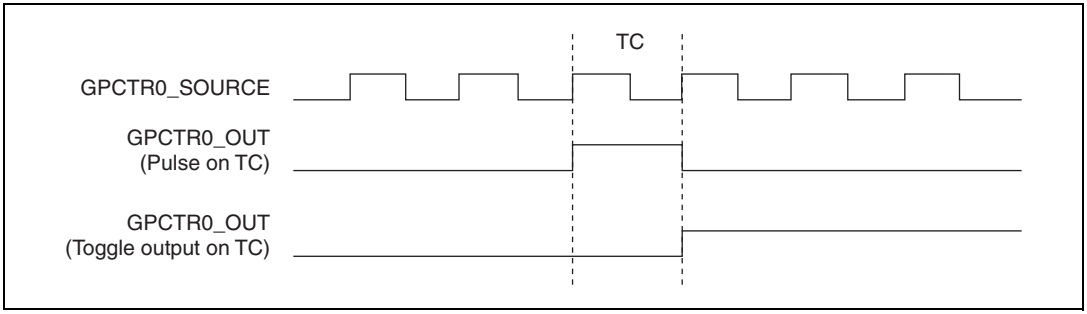

Figure 4-32. GPCTR0_OUT Signal Timing

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GPCTR0_UP_DOWN Signal

This signal can be received as an input on the DIO6 pin and is not available as an output on the I/O connector. The general-purpose counter 0 counts down when this pin is at a logic low and count up when it is at a logic high. You can disable this input so that software can control the up-down functionality and leave the DIO6 pin free for general use.

GPCTR1_SOURCE Signal

Any PFI pin can receive as an input the GPCTR1_SOURCE signal, which is available as an output on the PFI3/GPCTR1_SOURCE pin.

As an input, GPCTR1_SOURCE is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR1_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, GPCTR1_SOURCE monitors the actual clock connected to general-purpose counter 1, even if another PFI is externally generating the source clock. This output is set to high-impedance at startup.

Figure 4-33 shows the timing requirements for GPCTR1_SOURCE.

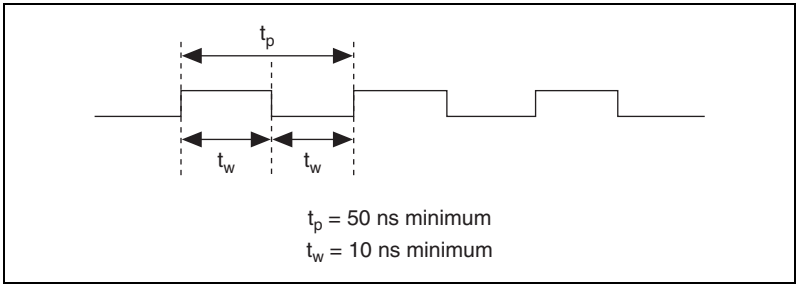

Figure 4-33. GPCTR1_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 10 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates GPCTR1_SOURCE unless you select some external source.

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GPCTR1_GATE Signal

Any PFI pin can receive as an input the GPCTR1_GATE signal, which is available as an output on the PFI4/GPCTR1_GATE pin.

As an input, GPCTR1_GATE is configured in edge-detection mode. You can select any PFI pin as the source for GPCTR1_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of applications to perform actions such as starting and stopping the counter, generating interrupts, and saving the counter contents.

As an output, GPCTR1_GATE monitors the actual gate signal connected to general-purpose counter 1, even if another PFI externally generates the gate. This output is set to high-impedance at startup.

Figure 4-34 shows the timing requirements for the GPCTR1_GATE signal.

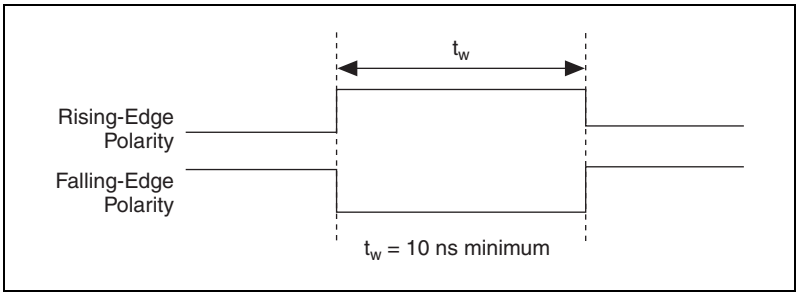

Figure 4-34. GPCTR1_GATE Signal Timing in Edge-Detection Mode

GPCTR1_OUT Signal

This signal is available only as an output on the GPCTR1_OUT pin. The GPCTR1_OUT signal monitors the TC device general-purpose counter 1. You have two software-selectable output options: pulse on TC and toggle output polarity on TC. The output polarity is software selectable for both options. This output is set to high-impedance at startup.

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Figure 4-35 shows the timing requirements for GPCTR1_OUT.

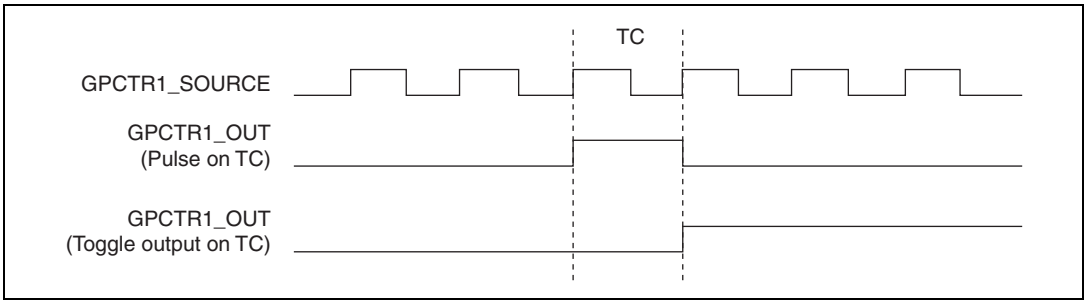
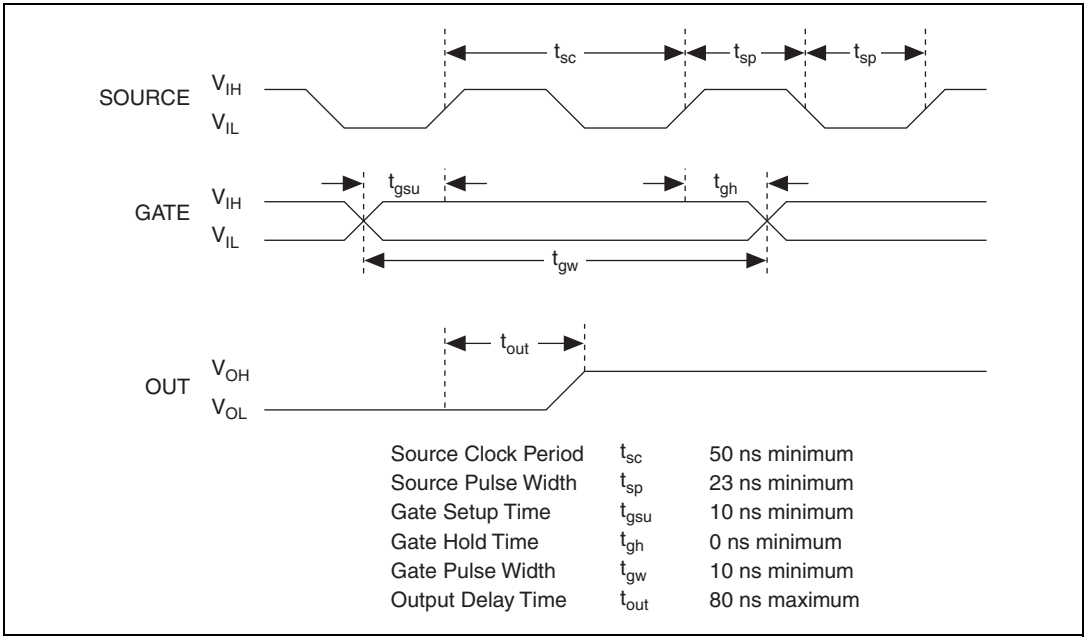


Figure 4-35. GPCTR1_OUT Signal Timing

GPCTR1_UP_DOWN Signal

This signal can be received as an input on the DIO7 pin and is not available as an output on the I/O connector. General-purpose counter 1 counts down when this pin is at a logic low and counts up at a logic high. This input can be disabled so that software can control the up-down functionality and leave the DIO7 pin free for general use. Figure 4-36 shows the timing requirements for the GATE and SOURCE input signals and the timing specifications for the OUT output signals.



Source Clock Period	t_{sc}	50 ns minimum
Source Pulse Width	t_{sp}	23 ns minimum
Gate Setup Time	t_{gsu}	10 ns minimum
Gate Hold Time	t_{gh}	0 ns minimum
Gate Pulse Width	t_{gw}	10 ns minimum
Output Delay Time	t_{out}	80 ns maximum

Figure 4-36. GPCTR Timing Summary

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The GATE and OUT signal transitions shown in Figure 4-36 are referenced to the rising edge of the SOURCE signal. This timing diagram assumes that the counters are programmed to count rising edges. The same timing diagram, but with the source signal inverted and referenced to the falling edge of the source signal, would apply when the counter is programmed to count falling edges.

The GATE input timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated signals on the NI 6115/6120. Figure 4-36 shows the GATE signal referenced to the rising edge of a source signal. The gate must be valid (either high or low) for at least 10 ns before the rising or falling edge of a source signal for the gate to take effect at that source edge, as shown by t_{gsu} and t_{gh} in Figure 4-36. The gate signal is not required to be held after the active edge of the source signal.

If you use an internal timebase clock, the gate signal cannot be synchronized with the clock. In this case, gates applied close to a source edge take effect either on that source edge or on the next one. This arrangement results in an uncertainty of one source clock period with respect to unsynchronized gating sources.

The OUT output timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated clock signals on the NI 6115/6120. Figure 4-36 shows the OUT signal referenced to the rising edge of a source signal. Any OUT signal state changes occur within 80 ns after the rising or falling edge of the source signal.

FREQ_OUT Signal

This signal is available only as an output on the FREQ_OUT pin. The frequency generator for the NI 6115/6120 outputs the FREQ_OUT pin. The frequency generator is a 4-bit counter that can divide its input clock by the numbers 1 through 16. The input clock of the frequency generator is software selectable from the internal 10 MHz and 100 kHz timebases. The output polarity is software selectable. This output is set to high-impedance at startup.

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Field Wiring Considerations

Environmental noise can seriously affect the measurement accuracy of the NI 6115/6120 if you do not take proper care when running signal wires between signal sources and the device. The following recommendations apply mainly to AI signal routing, although they also apply to signal routing in general.

Minimize noise pickup and maximize measurement accuracy by taking the following precautions:

- Use differential AI connections to reject common-mode noise.
- Use individually shielded, twisted-pair wires to connect AI signals to the device. With this type of wire, the signals attached to the ACH+ and ACH– inputs are twisted together and then covered with a shield. You then connect this shield only at one point to the signal source ground. This kind of connection is required for signals traveling through areas with large magnetic fields or high electromagnetic interference.
- Route signals to the device carefully. Keep cabling away from noise sources. The most common noise source in a PCI DAQ system is the video monitor. Separate the monitor from the analog signals as far as possible.

The following recommendations apply for all signal connections to the NI 6115/6120:

- Separate the NI 6115/6120 signal lines from high-current or high-voltage lines. These lines can induce currents in or voltages on the NI 6115/6120 signal lines if they run in parallel paths at a close distance. To reduce the magnetic coupling between lines, separate them by a reasonable distance if they run in parallel, or run the lines at right angles to each other.
- Do not run signal lines through conduits that also contain power lines.
- Protect signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running them through special metal conduits.

For more information, refer to the NI Developer Zone tutorial, *Field Wiring and Noise Consideration for Analog Signals*, available at `ni.com/zone`.

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5

Calibration

This chapter discusses the calibration procedures for the NI 6115/6120. NI-DAQ includes calibration functions for performing all of the steps in the calibration process.

Calibration refers to the process of minimizing measurement and output voltage errors by making small circuit adjustments. On the NI 6115/6120, these adjustments take the form of writing values to onboard calibration DACs (CalDACs).

Some form of device calibration is required for most applications. If you do not calibrate the device, the signals and measurements could have very large offset, gain, and linearity errors.

Three levels of calibration are available to you and are described in this chapter. The first level is the fastest, easiest, and least accurate; whereas the last level is the slowest, most difficult, and most accurate.

Loading Stored Calibration Constants

The NI 6115/6120 is factory calibrated before shipment at approximately 25 °C to the levels indicated in Appendix A, *Specifications*. The associated calibration constants—the values that were written to the CalDACs to achieve calibration in the factory—are stored in the onboard nonvolatile memory (EEPROM). Because the CalDACs have no memory capability, they do not retain calibration information when the device is unpowered. Loading calibration constants refers to the process of loading the CalDACs with the values stored in the EEPROM. NI-DAQ determines when this is necessary and does it automatically.

In the EEPROM, there is a user-modifiable calibration area in addition to the permanent factory calibration area. Hence, you can load the CalDACs with values either from the original factory calibration or from a calibration that you subsequently performed.

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This method of calibration is not very accurate because it does not take into account the fact that the device measurement and output voltage errors can vary with time and temperature. It is better to self-calibrate when the device is installed in the environment in which it is used.

Self-Calibration

The NI 6115/6120 can measure and correct for almost all of its calibration-related errors without any external signal connections. NI-DAQ software provides a self-calibration method. This self-calibration process, which generally takes two to five minutes, is the preferred method of assuring accuracy in your application. Initiate self-calibration to minimize the effects of any offset and gain drifts, particularly those caused by warming.

Immediately after self-calibration, the only significant residual calibration error could be gain error due to time or temperature drift of the onboard voltage reference. This error is addressed by external calibration, which is discussed in the following section. If you are interested primarily in relative measurements, you can ignore a small amount of gain error, and self-calibration should be sufficient.

External Calibration

The NI 6115/6120 has an onboard calibration reference to ensure the accuracy of self-calibration. Its specifications are listed in Appendix A, *Specifications*. The reference voltage is measured at the factory and stored in the EEPROM for subsequent self-calibrations. This voltage is stable enough for most applications, but if you are using the device at an extreme temperature or if the onboard reference has not been measured for a year or more, you may wish to externally calibrate the device.

An external calibration refers to calibrating the device with a known external reference rather than relying on the onboard reference. Redetermining the value of the onboard reference is part of this process and the results can be saved in the EEPROM, so you should not have to perform an external calibration very often. You can externally calibrate the device by calling the NI-DAQ calibration function.

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To externally calibrate your device, be sure to use a very accurate external reference. The reference should be several times more accurate than the device itself.

For a detailed calibration procedure for the NI 6115/6120, click **Manual Calibration Procedures** at `ni.com/calibration`.

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A

Specifications

This appendix lists the specifications of the NI 6115/6120. These specifications are typical at 25 °C unless otherwise noted.

Analog Input

Input Characteristics

Number of channels ..... 4 pseudodifferential

Type of ADC

Resolution

NI 6115 ..... 12 bits, 1 in 4,096

NI 6120 ..... 16 bits, 1 in 65,536

Pipeline

NI 6115 4

NI 6120 0

Sampling rate

Maximum

NI 6115 ..... 10 million S/s

NI 6120 ..... 800 kS/s

Minimum

NI 6115 ..... 20 kS/s

NI 6120 ..... No minimum

Input impedance

ACH+ to ACH–

Range ≤ ±10 V ..... 1 MΩ in parallel with 100 pF

Range > ±10 V ..... 10 kΩ in parallel with 40 pF

ACH– to ACHGND

NI 6115 ..... 10 nF

NI 6120 ..... 100 GΩ

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ACH+ to ACHGND

NI 6115.....100 GΩ

NI 6120.....100 GΩ

Input bias current.....±300 pA

Input offset current.....±200 pA

Input coupling.....DC/AC

Max working voltage for all analog input channels

Positive input (ACH+).....±11 V for ranges < ±10 V;
±42 V for ranges ≥ ±10 V

Negative input (ACH–).....±2.5 V

Overvoltage protection.....±42 V

Input current during
overvoltage conditions.....±20 mA max

Input FIFO size..... 16 or 32 MS

Data transfers.....DMA, interrupts,
programmed I/O

DMA modes.....Scatter-gather

DC Transfer Characteristics

INL

NI 6115.....±0.35 LSB typ, ±1 LSB max

NI 6120.....2.5 LSB max

DNL

NI 6115.....±0.25 LSB typ, ±1 LSB max

NI 6120.....0.75 LSB typ, no missing codes

Offset, gain error

NI 6115.....Refer to Table A-1

NI 6120.....Refer to Table A-2

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Table A-1. NI 6115 Analog Input DC Accuracy Information

Nominal Range (V)	Absolute Accuracy							Relative Accuracy	
	% of Reading		Offset (mV)	Noise + Quantization (mV)		Temp Drift (%/°C)	Absolute Accuracy at Full Scale (±mV)	Resolution (mV)	
Full Scale	24 Hours	1 Year		Single Pt.	Averaged			Single Pt.	Averaged
±50	0.346	0.348	33	42	3.6	0.0229	211.0	48	4.8
±20	0.271	0.273	13	17	1.4	0.0229	69.4	19	1.9
±10	0.026	0.028	6.7	8.3	0.72	0.0004	10.22	10	1.0
±5	0.016	0.018	3.4	4.2	0.36	0.0004	4.61	4.8	0.48
±2	0.036	0.038	1.3	1.8	0.16	0.0004	2.26	2.1	0.21
±1	0.043	0.045	0.68	1.1	0.09	0.0004	1.23	1.2	0.12
±0.5	0.058	0.060	0.35	0.69	0.061	0.0004	0.71	0.80	0.080
±0.2	0.103	0.105	0.15	0.43	0.039	0.0004	0.39	0.51	0.051

Table A-2. NI 6120 Analog Input DC Accuracy Information[1]

Nominal Range (V)	Absolute Accuracy							Relative Accuracy	
	% of Reading		Offset (µV)[2,3]	Noise + Quantization (µV)		Temp Drift (%/°C)	Absolute Accuracy at Full Scale (±mV)	Resolution (µV)	
Full Scale	24 Hours	1 Year		Single Pt.	Averaged			Single Pt.	Averaged
±50	0.157	0.159	7,799.2	5,621.9	503.5	0.0106	86.92	6,629.9	663.0
±20	0.139	0.141	3,120.7	2,248.7	201.4	0.0106	31.11	2652.0	265.2
±10	0.033	0.034	1,561.1	1,124.4	100.7	0.0006	4.94	1326.0	132.6
±5	0.036	0.37	781.4	562.2	50.4	0.0006	2.61	663.0	66.3
±2	0.039	0.041	344.0	224.9	20.1	0.0006	1.15	265.2	26.5
±1	0.077	0.079	264.4	150.0	13.7	0.0006	1.05	180.8	18.1
±0.5	0.100	0.102	178.8	144.3	13.7	0.0006	0.69	180.8	18.1
±0.2	0.123	0.125	90.8	112.8	11.0	0.0006	0.35	144.7	14.5

[1] Accuracies are valid for measurements following an internal calibration. Averaged numbers assume dithering and averaging of 100 single-channel readings. Measurement accuracies are listed for operational temperatures within ±1 °C of internal calibration temperature and ±10 °C of external or factory-calibration temperature.
[2] The offset might degrade by 3 LSB with filter enabled.
[3] The offset might degrade by 1 LSB when sampling above 500 kS/s.

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Dynamic Characteristics

Interchannel skew .....1 ns typ

Analog filters

- Number
  - NI 6115.....2
  - NI 6120.....1
- Type
  - NI 6115.....3-pole Bessel
  - NI 6120.....5-pole Bessel
- Frequency
  - NI 6115.....50 and 500 kHz (software-enabled)
  - NI 6120.....100 kHz (software-enabled)

Crosstalk .....–80 dB, DC to 100 kHz

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Table A-3. NI 6115 Analog Input Dynamic Characteristics

Input Range	Bandwidth (MHz)[1]	SFDR Typ (dB)[2]	SFDR Max (dB)	CMRR (dB)[3]	System Noise (LSB_{rms})[4]
±50 V	5.5	78	70	34	0.35
±20 V	4.4	78	70	40	0.45
±10 V	7.2	81	75	46	0.35
±5 V	4.8	81	75	52	0.35
±2 V	4.8	85	75	60	0.45
±1 V	4.4	85	75	66	0.60
±500 mV	4.4	85	75	70	0.80
±200 mV	4.1	81	70	72	1.3

[1] –3 dB frequency for input amplitude at 96% of the input range (–0.3 dB)
[2] Measured at 100 kHz with twelfth-order bandpass filter after signal source
[3] DC to 60 Hz
[4] LSB_{rms}, including quantization

Table A-4. NI 6120 Analog Input Dynamic Characteristics

Input Range	Bandwidth (MHz)[1]	SFDR Typ (dB)[2]	SFDR Max (dB)[3]	CMRR (dB)[4]	System Noise (LSB_{rms})[5]
±50 V	1.0	95	90	60	1.2
±20 V	1.0	96	90	68	1.2
±10 V	1.0	95	90	76	1.2
±5 V	1.0	95	90	82	1.5
±2 V	1.0	96	90	90	1.7
±1 V	1.0	94	90	95	2.0
±500 mV	1.0	90	85	100	2.2
±200 mV	1.0	85	80	105	2.8

[1] –3 dB frequency for input amplitude at 10% of the input range (–20 dB)
[2] Measured at 100 kHz with twelfth-order bandpass filter after signal source
[3] 100% production tested at 100 kHz
[4] DC to 60 Hz
[5] LSB_{rms}, not including quantization

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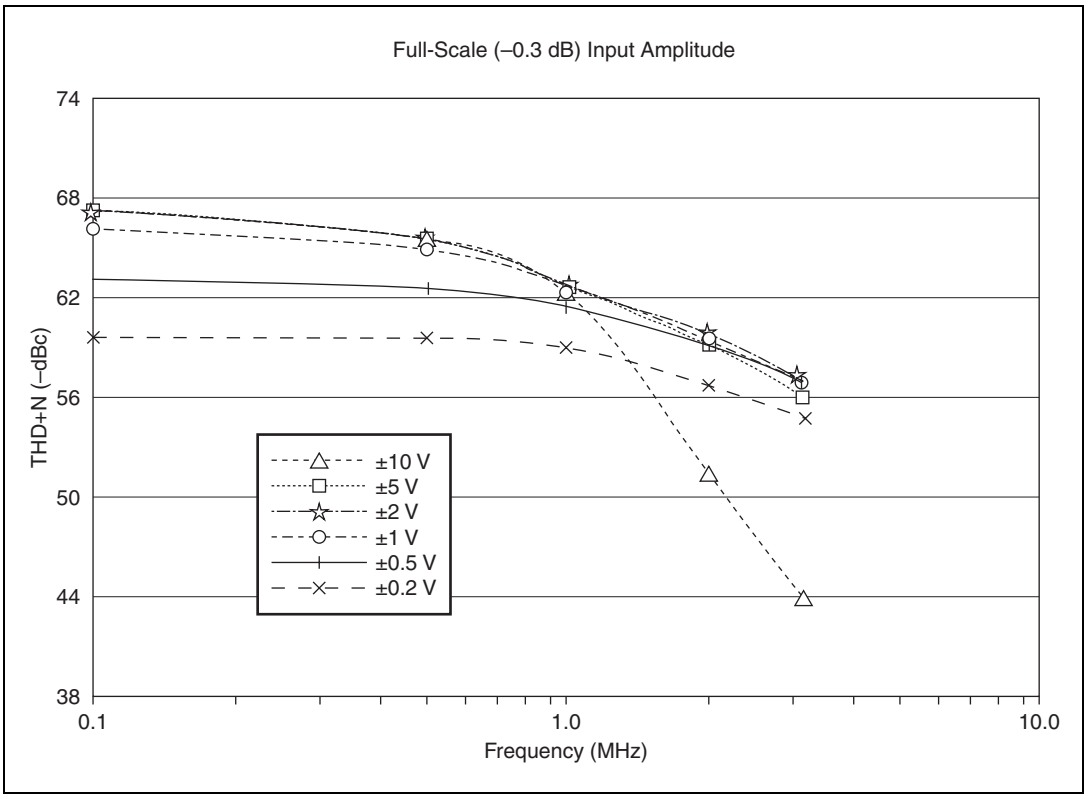

Figure A-1. NI 6115 Total Harmonic Distortion Plus Noise (THD + N)

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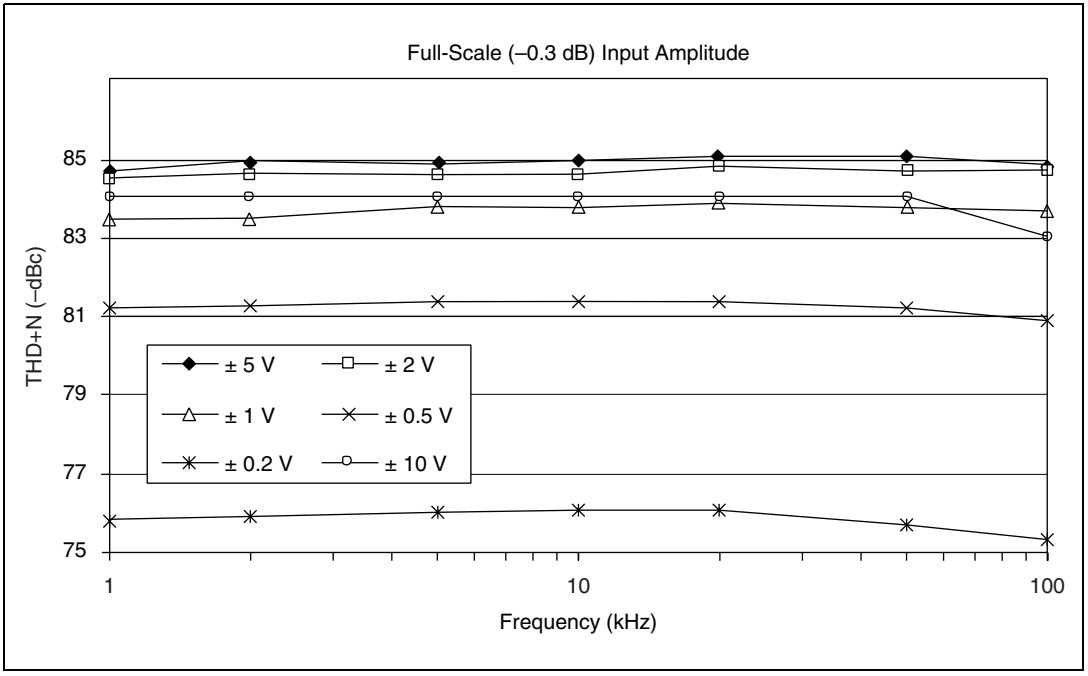

Figure A-2. NI 6120 Total Harmonic Distortion Plus Noise (THD + N)

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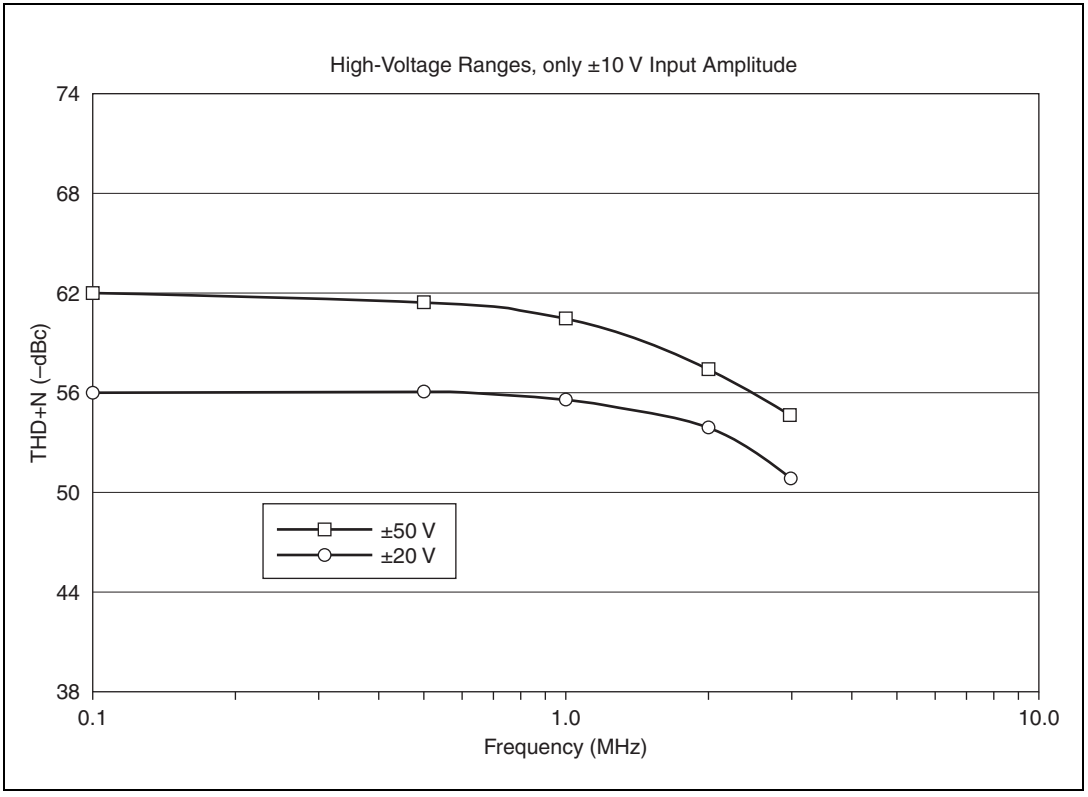

Figure A-3. NI 6115 High-Voltage THD + N

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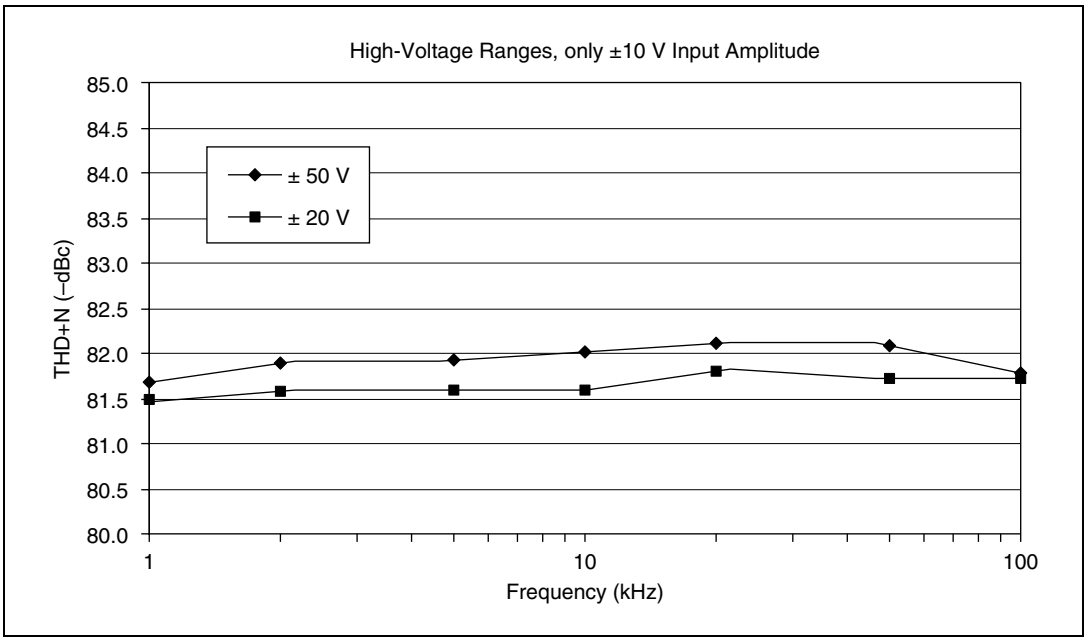

Figure A-4. NI 6120 High-Voltage THD + N

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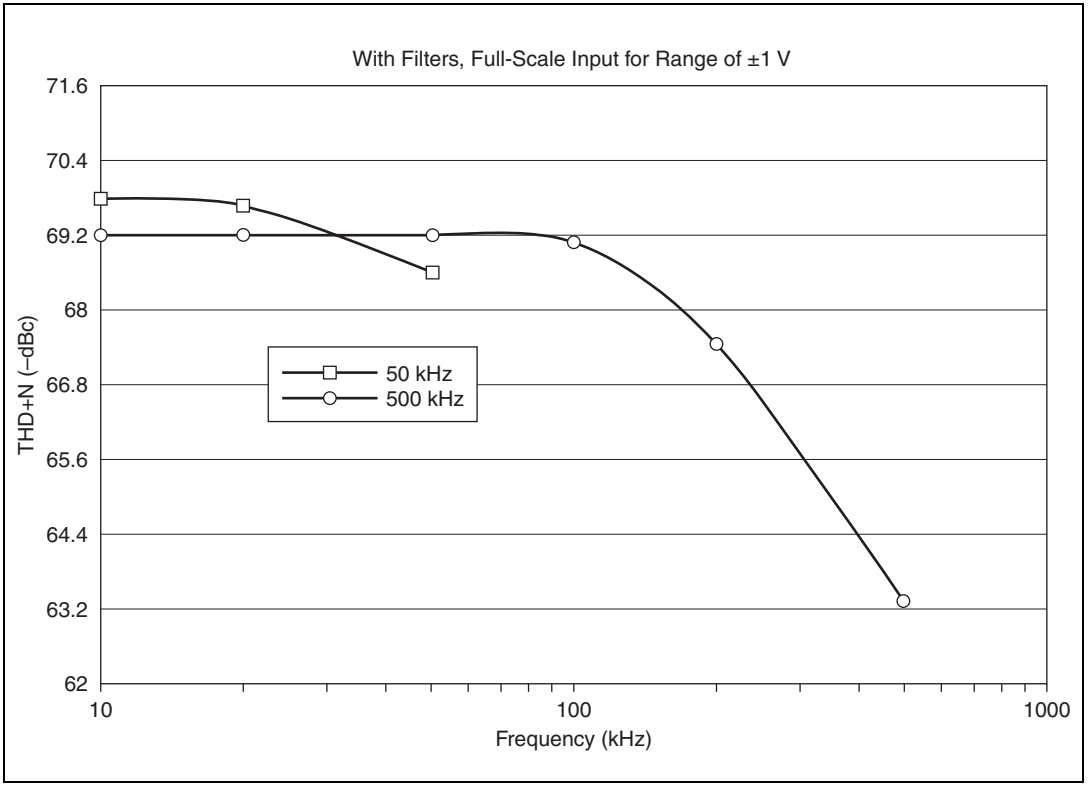

Figure A-5. NI 6115 THD + N with Filters

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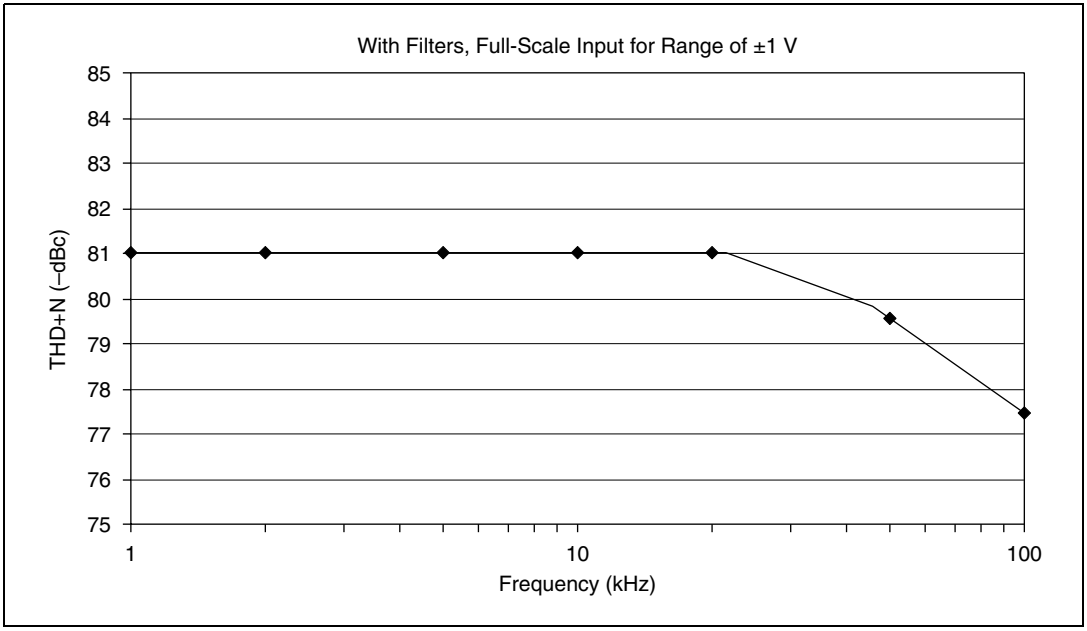

Figure A-6. NI 6120 THD + N with Filters

Stability

Recommended warm-up time ..... 15 min

Offset temperature coefficient

Pregain

NI 6115 ..... ±12 µV/°C

NI 6120 ..... ±1.5 µV/°C

Postgain

NI 6115 ..... ±64 µV/°C

NI 6120 ..... ±2.1 LSB/°C

Gain temperature coefficient

NI 6115 ..... ±21.3 ppm/°C

NI 6120 ..... ±22.2 ppm/°C

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Onboard calibration reference

Level.....5.000 V (±2.5 mV)
(actual value stored in EEPROM)

Temperature coefficient.....±4.1 ppm/°C max

Long-term stability.....±6 ppm/$\sqrt{1{,}000\ \text{h}}$

Analog Output

Output Characteristics

Number of channels.....2 voltage

Resolution

NI 6115.....12 bits, 1 in 4,096

NI 6120.....16 bits, 1 in 65,536

Max update rate

1 channel.....4 MS/s, system dependent

2 channel.....2.5 MS/s, system dependent

Output buffer size.....16 or 32 MS

Data transfers.....DMA, interrupts, programmed I/O

DMA modes.....Scatter-gather

DC Transfer Characteristics

INL

NI 6115.....±0.5 LSB typ, ±2 LSB max

NI 6120.....±0.35 LSB typ, ±1 LSB max

DNL

NI 6115.....±0.25 LSB typ, ±1 LSB max

NI 6120.....±0.2 LSB typ, ±1 LSB max

Offset, gain error

NI 6115.....Refer to Table A-5

NI 6120.....Refer to Table A-6

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Table A-5. NI 6115 Analog Output DC Accuracy Information

Nominal Range at Full Scale (V)	Absolute Accuracy						Relative Accuracy
	% of Reading			Offset (mV)	Temp Drift (%/°C)	Absolute Acc. at Full Scale (mV)	Theoretical Resolution (mV)
	24 Hrs	90 Days	1 Year				
±10	0.0437	0.0445	0.0454	8.9	0.0006	13.5	4.88

Table A-6. NI 6120 Analog Output DC Accuracy Information

Nominal Range at Full Scale (V)	Absolute Accuracy						Relative Accuracy
	% of Reading			Offset (mV)	Temp Drift (%/°C)	Absolute Acc. at Full Scale (mV)	Theoretical Resolution (µV)
	24 Hrs	90 Days	1 Year				
±10	0.0512	0.0520	0.0529	1.9	0.0006	6.7	305.2

Voltage Output

Ranges ..... ±10 V

Output coupling ..... DC

Output impedance ..... 50 Ω ±5%

Current drive ..... ±5 mA

Output stability ..... Any passive load

Protection ..... Short-circuit to ground

Power-on output voltage
(before software loads calibration values)

NI 6115 ..... ±400 mV

NI 6120 ..... ±80 mV

Initial power-up glitch

Magnitude ..... ±2 V

Duration ..... 200 ms

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Dynamic Characteristics

Slew rate

NI 6115.....300 V/µs

NI 6120.....15 V/µs

Noise

NI 6115.....600 μV_{rms}, DC to 5 MHz

NI 6120.....100 μV_{rms}, DC to 1 MHz

Glitch energy at midscale transition

NI 6115.....±30 mV for 1 µs

NI 6120.....±10 mV for 1 µs

Settling time

NI 6115.....300 ns to 0.01%

NI 6120.....4 µs to ±1 LSB

Stability

Offset temperature coefficient

NI 6115.....±35 µV/°C

NI 6120.....±35 µV/°C

Gain temperature coefficient

NI 6115.....±56.9 ppm/°C

NI 6120.....±6.5 ppm/°C

Onboard calibration reference

Level.....5.000 V (±2.5 mV)
(actual value stored in EEPROM)

Temperature coefficient.....±0.9 ppm/°C max

Long-term stability.....±6 ppm/$\sqrt{1{,}000\ \text{h}}$

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Digital I/O

Number of channels ..... 8 input/output

Compatibility ..... TTL/CMOS

Table A-7. Digital logic levels

Level	Min	Max
Input low voltage	0.0 V	0.8 V
Input high voltage	2.0 V	5.0 V
Input low current (V_{in} = 0 V)	—	–320 µA
Input high current (V_{in} = 5 V)	—	10 µA
Output low voltage (I_{OL} = 24 mA)	—	0.4 V
Output high voltage (I_{OH} = 13 mA)	4.35 V	—

Power-on state ..... Input (high-impedance)

Data transfers ..... DMA, interrupts, programmed I/O

Input buffer ..... 2,000 bytes

Output buffer ..... 2,000 bytes

Transfer rate (1 word = 8 bits) ..... 10 Mwords/s

Timing I/O

Number of channels ..... 2 up/down counter/timers, 1 frequency scaler

Resolution

- Counter/timers ..... 24 bits
- Frequency scaler ..... 4 bits

Compatibility ..... TTL/CMOS

Base clocks available

- Counter/timers ..... 20 MHz, 100 kHz
- Frequency scaler ..... 10 MHz, 100 kHz

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Base clock accuracy.....±0.01%

Max source frequency.....20 MHz

Min source pulse duration .....10 ns, edge-detect mode

Min gate pulse duration .....10 ns, edge-detect mode

Data transfers.....DMA, interrupts, programmed I/O

DMA modes .....Scatter-gather

Triggers

Analog Trigger

NI 6115/6120 source .....All analog input channels, external trigger (PFI0/TRIG1)

Level .....± full-scale, internal; ±10 V, external

Slope .....Positive or negative (software selectable)

Resolution

- NI 6115.....8 bits, 1 in 256
- NI 6120.....12 bits, 1 in 4,096

Hysteresis.....Programmable

Bandwidth .....(–3 dB) 5 MHz internal/external

External input (PFI0/TRIG1)

- Impedance.....10 kΩ
- Coupling .....AC/DC
- Protection.....–0.5 V to (V_{CC} + 0.5) V when configured as a digital signal, ±35 V when configured as an analog trigger signal or disabled, ±35 V powered off

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Digital Trigger

Compatibility ..... TTL

Response ..... Rising or falling edge

Pulse width ..... 10 ns min

RTSI

Trigger lines ..... 7[1]

Bus Interface

Type ..... Master, slave

Power Requirement

+5 VDC (±5%)

NI 6115 ..... 2.2 A

NI 6120 ..... 3.0 A

+3.3 V ..... 0.8 A

Power available at I/O connector ..... +4.65 to +5.25 VDC at 1 A

Physical

Dimensions (not including connectors)

NI PCI-6115/6120 ..... 31.2 by 10.6 cm (12.3 by 4.2 in.)

NI PXI-6115/6120 ..... 16 by 10 cm (6.3 by 3.9 in.)

I/O connector ..... 68-pin male SCSI-II type

Environmental

Operating temperature ..... 0 to 50 °C

Storage temperature ..... –20 to 70 °C

[1] RTSI Trigger<6> is configured as the PXI Star Trigger for the NI PXI-6115/6120. Refer to the *RTSI Triggers* section of Chapter 3, *Hardware Overview*, for more information.

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Relative humidity .....10 to 90% noncondensing

Pollution Degree (indoor use only) 2

Safety

The NI 6115/6120 was evaluated using the criteria of EN 61010-1 a-2:1995 and meets the requirements of the following standards for safety and electrical equipment for measurement, control and laboratory use:

- EN 61010-1, IEC 61010-1
- UL 3111-1
- CAN/CSA C22.2 No. 1010.1

Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Channel-to-earth .....42 V, Installation Category I

Channel-to-channel.....42 V, Installation Category I

Electromagnetic Compatibility

EMC/EMI .....CE, C-Tick, and FCC Part 15 (Class A) Compliant

Emissions.....EN 55011 Class A at 10 m
FCC Part 15A above 1 GHz

Immunity .....Evaluated to EN 61326:1998, Table 1

Note For full EMC and EMI compliance, you must operate this device with shielded cabling. In addition, all covers and filler panels must be installed. Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by the product, and a link to the DoC (in Adobe Acrobat format) appears. Click the Acrobat icon to download or read the DoC.

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B

Common Questions

This appendix contains a list of commonly asked questions and their answers relating to usage and special features of the NI 6115/6120.

General Information

What is the NI 6115/6120?

The NI 6115/6120 is a switchless and jumperless enhanced MIO device that uses the DAQ-STC for timing.

What is the DAQ-STC?

The DAQ-STC is the system timing control application-specific integrated circuit (ASIC) designed by NI and is the backbone of the NI 6115/6120 device. The DAQ-STC contains seven 24-bit counters and three 16-bit counters. The counters are divided into the following three groups:

- AI—two 24-bit, two 16-bit counters
- AO—three 24-bit, one 16-bit counters
- General-purpose counter/timer functions—two 24-bit counters

The groups can be configured independently with timing resolutions of 50 ns or 10 µs. With the DAQ-STC, you can interconnect a wide variety of internal timing signals to other internal blocks. The interconnection scheme is quite flexible and completely software configurable. New capabilities such as buffered pulse generation and equivalent time sampling are possible.

What does the maximum sampling rate mean to me?

Maximum sampling rate is the fastest you can acquire data on the device and still achieve accurate results. The NI 6115 device has a maximum sampling rate of 10 MS/s. This sampling rate is at 10 MS/s regardless if 1 or 4 channels are acquiring data. The NI 6120 has a maximum sampling rate of 800 kS/s.

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What type of 5 V protection does the NI 6115/6120 have?

The NI 6115/6120 has 5 V lines equipped with a self-resetting 1 A fuse.

How do I use the NI 6115/6120 with the NI-DAQ C API?

The *NI-DAQ User Manual for PC Compatibles* describes the general programming flow when using the NI-DAQ C API as well as contains example code. For a list of functions that support the NI 6115/6120, you can refer to the *NI-DAQ Function Reference Help*. You can access this help file by clicking **Start»Programs»National Instruments»NI-DAQ» NI-DAQ Help**.

Installing and Configuring the Device

How do you set the base address for the NI 6115/6120?

The base address of the NI 6115/6120 is assigned automatically through the PCI bus protocol. This assignment is completely transparent to you.

What jumpers should I be aware of when configuring the NI 6115/6120?

The NI 6115/6120 is jumperless and switchless.

Which NI document should I read first to get started using DAQ software?

The *DAQ Quick Start Guide* and the NI-DAQ or application software release notes documentation are good places to start.

What is the best way to test the NI 6115/6120 without programming the device?

Measurement & Automation Explorer (MAX) has a Test Panel option that is available by selecting **Devices and Interfaces** and then selecting the device. The test panels are excellent tools for performing simple functional tests of the device, such as AI, DIO and counter/timer tests.

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Analog Input and Output

Why is there a minimum sampling rate on the NI 6115?

The NI 6115 makes use of a pipelined ADC in order to achieve high sampling rates. Sampling at rates below 20 kS/s can result in improper digitization, which appear as noise in the acquired data.

How do I enable the programmable antialiasing filter on the NI 6115/6120?

In LabVIEW, select **Data Acquisition»Analog Input»Advanced Analog Input»AI Parameter.vi** from the function palette to set the filter values of 50 kHz and 500 kHz for the NI 6115, or to enable the 100 kHz filter for the NI 6120, on a per channel basis. To disable the filter, set the filter value to `0`.

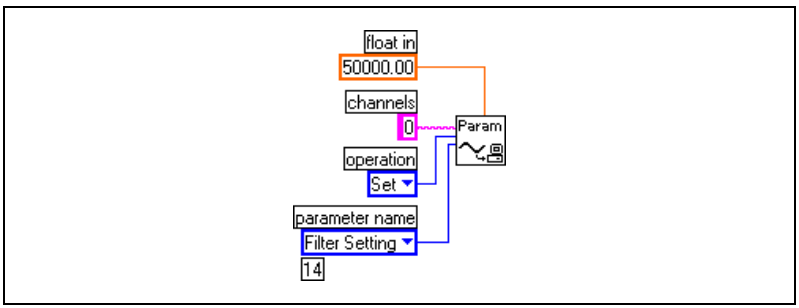

Figure B-1. Setting Filter Values in LabVIEW

In NI-DAQ, use the `AI_Change_Parameter` function to set the filter value. Set **paramID** to `ND_Digital_Filter`. Set **ParamValue** to `ND_High` for a filter value of 500 kHz on the NI 6115 or 100 kHz on the NI 6120. Use `ND_Low` for a filter value of 50 kHz on the NI 6115. Use `ND_None` to disable the filter. The filter is disabled by default.

I have connected a differential input signal, but my readings are random and drift rapidly. What is wrong?

Check your ground-reference connections. The signal may be referenced to a level that is considered *floating* with reference to the device ground reference. Even if you are in differential mode, the signal *must* still be referenced to the same ground level as the device reference. There are various methods of achieving this reference while maintaining a high common-mode rejection ratio (CMRR). These methods are outlined in Chapter 4, *Connecting Signals*.

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I'm using the DACs to generate a waveform, but I discovered with a digital oscilloscope that there are glitches on the output signal. Is this normal?

When the DAC switches from one voltage to another, any DAC produces glitches due to released charges. The largest glitches occur when the most significant bit (MSB) of the D/A code switches. You can build a lowpass deglitching filter to remove some of these glitches, depending on the frequency and nature of your output signal.

Can I synchronize a one-channel AI data acquisition with a one-channel AO waveform generation on the NI 6115/6120?

Yes. One way to accomplish synchronization is to use the waveform generation timing pulses to control the AI data acquisition. To do this, follow steps 1 through 4 below, in addition to the usual steps for data acquisition and waveform generation configuration.

1. Enable the PFI5 line for output, as follows:
   - If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_PFI_5, ND_OUT_UPDATE, ND_HIGH_TO_LOW).`
   - If you are using LabVIEW, select **Data Acquisition»Calibration and Configuration»Route Signal.vi** from the function palette and set **signal name** to `PFI5` and **signal source** to `AO Update`.
2. Set up data acquisition timing so that the timing signal for A/D conversion comes from PFI5, as follows:
   - If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_IN_SCAN_START, ND_PFI_7, ND_HIGH_TO_LOW).`
   - If you are using LabVIEW, select **Data Acquisition»Analog Input»Advanced Analog Input»AI Clock Config.vi** with **clock source code** set to `PFI pin, high to low`, and **clock source string** set to `5`.
3. Initiate AI data acquisition, which starts only when the AO waveform generation starts.
4. Initiate AO waveform generation.

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Timing and Digital I/O

What types of triggering can be hardware-implemented on the NI 6115/6120?

Hardware digital and analog triggering are both supported on the NI 6115/6120.

If I'm using one of the general-purpose counter/timers on the NI 6115/6120, but I do not see the counter/timer output on the I/O connector, what am I doing wrong?

If you are using NI-DAQ or LabWindows/CVI, you must configure the output line to output the signal to the I/O connector. Use the `Select_Signal` call in NI-DAQ to configure the output line. By default, all timing I/O lines except EXTSTROBE* are high-impedance.

What are the PFIs and how do I configure these lines?

PFIs are Programmable Function Inputs. These lines serve as connections to virtually all internal timing signals.

If you are using NI-DAQ or LabWindows/CVI, use the `Select_Signal` function to route internal signals to the I/O connector, route external signals to internal timing sources, or tie internal timing signals together.

If you are using NI-DAQ with LabVIEW and you want to connect external signal sources to the PFI lines, you can use AI Clock Config, AI Trigger Config, AO Clock Config, AO Trigger and Gate Config, and Counter Set Attribute advanced-level VIs to indicate which function the connected signal serves. Use the Route Signal VI to enable the PFI lines to output internal signals.

Table B-1. Signal Name Equivalencies

Hardware Signal Name	LabVIEW Route Signal	NI-DAQ Select_Signal
TRIG1	AI Start Trigger	ND_IN_START_TRIGGER
TRIG2	AI Stop Trigger	ND_IN_STOP_TRIGGER
STARTSCAN	AI Scan Start	ND_IN_SCAN_START
SISOURCE	—	ND_IN_SCAN_CLOCK_TIMEBASE
CONVERT*	AI Convert	ND_IN_CONVERT

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Table B-1. Signal Name Equivalencies (Continued)

Hardware Signal Name	LabVIEW Route Signal	NI-DAQ Select_Signal
AIGATE	—	ND_IN_EXTERNAL_GATE
WFTRIG	AO Start Trigger	ND_OUT_START_TRIGGER
UPDATE*	AO Update	ND_OUT_UPDATE
UISOURCE	—	ND_OUT_UPDATE_CLOCK_TIMEBASE
AOGATE	—	ND_OUT_EXTERNAL_GATE

Caution If you enable a PFI line for output, do *not* connect any external signal source to it; if you do, you can damage the device, the computer, and the connected equipment.

What are the power-on states of the PFI and DIO lines on the I/O connector?

At system power-on and reset, both the PFI and DIO lines are set to high-impedance by the hardware. Hence, the device circuitry is not actively driving the output either high or low. However, these lines may have pull-up or pull-down resistors connected to them as shown in Table 4-5, *Digital I/O Signal Summary*. These resistors weakly pull the output to either a logic-high or logic-low state. For example, DIO(0) is in the high-impedance state after power on, and Table 4-5 shows that there is a 50 kΩ pull-up resistor. This pull-up resistor sets the DIO(0) pin to a logic high when the output is in a high-impedance state.

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C

Technical Support and Professional Services

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- **Support**—Online technical support resources include the following:
  - **Self-Help Resources**—For immediate answers and solutions, visit our extensive library of technical support resources available in English, Japanese, and Spanish at ni.com/support. These resources are available for most products at no cost to registered users and include software drivers and updates, a KnowledgeBase, product manuals, step-by-step troubleshooting wizards, hardware schematics and conformity documentation, example code, tutorials and application notes, instrument drivers, discussion forums, a measurement glossary, and so on.
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If you searched `ni.com` and could not find the answers you need, contact your local office or NI corporate headquarters. Phone numbers for our worldwide offices are listed at the front of this manual. You also can visit the Worldwide Offices section of `ni.com/niglobal` to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

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Glossary

Prefix	Meaning	Value
p-	pico-	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}

Numbers/Symbols

°	degree
>	greater than
≥	greater than or equal to
<	less than
≤	less than or equal to
/	per
%	percent
±	plus or minus
+	positive of, or plus
–	negative of, or minus
Ω	ohm
$\sqrt{\ }$	square root of
+5 V	+5 VDC source signal

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A

A	amperes
A/D	analog-to-digital
AC	alternating current
ACH	analog input channel signal
ACH0GND	analog input channel ground signal
ADC	analog-to-digital converter—an electronic device, often an integrated circuit, that converts an analog voltage to a digital number
ADE	application development environment such as LabVIEW, LabWindows/CVI, Measurement Studio, Visual Basic, C, and C++
AI	analog input
AIGATE	analog input gate signal
aliasing	the consequence of sampling that causes signals with frequencies higher than half the sampling frequency to appear as lower frequency components in a frequency spectrum
ANSI	American National Standards Institute
AO	analog output
AOGND	analog output ground signal
ASIC	application-specific integrated circuit—a proprietary semiconductor component designed and manufactured to perform a set of specific functions

B

Bessel filter	a filter with a maximally flat response in both magnitude and phase. The phase response in the passband, which is usually the region of interest, is nearly linear. Bessel filters reduce nonlinear phase distortion inherent in all IIR filters.
bipolar	a signal range that includes both positive and negative values

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C

C	Celsius
CalDAC	calibration DAC
cm	centimeter
CMOS	complementary metal-oxide semiconductor
CMRR	common-mode rejection ratio—a measure of an instrument to reject interference from a common-mode signal, usually expressed in decibels (dB)
CompactPCI	a Eurocard configuration of the PCI bus for industrial applications
CONVERT*	convert signal
correlated DIO	can clock digital I/O on the same clock as analog I/O
counter/timer	a circuit that counts external pulses or clock pulses (timing)
CTR	counter

D

D/A	digital-to-analog
DAC	digital-to-analog converter—an electronic device that converts a digital number into a corresponding analog voltage or current
DAC0OUT	analog channel 0 output signal
DAC1OUT	analog channel 1 output signal
DAQ	data acquisition—(1) collecting and measuring electrical signals from sensors, transducers, and test probes or fixtures and inputting them to a computer for processing; (2) collecting and measuring the same kinds of electrical signals with A/D and/or DIO devices plugged into a computer, and possibly generating control signals with D/A and/or DIO devices in the same computer

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DAQ-STC	data acquisition system timing controller—an application-specific integrated circuit (ASIC) for the system timing requirements of a general A/D and D/A system, such as a system containing the National Instruments E Series devices
dB	decibel—the unit for expressing a logarithmic measure of the ratio of two signal levels: dB = 20log10 V1/V2, for signals in volts
DC	direct current
DGND	digital ground signal
DI	digital input
DIFF	differential mode—an analog input mode consisting of two terminals, both of which are isolated from computer ground, whose difference is measured
DIO	digital input/output
DIP	dual inline package
dithering	the addition of Gaussian noise to an analog input signal for the purpose of increasing the resolution of a measurement when using averaging
DMA	direct memory access—a method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else; the fastest method of transferring data to/from computer memory
DNL	differential nonlinearity—a measure in least significant bit of the worst-case deviation of code widths from their ideal value of 1 LSB
DO	digital output

E

EEPROM	electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed
ENOB	effective number of bits

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ESD	electrostatic discharge
EXTSTROBE*	external strobe signal

F

F	farad—a measurement unit of capacitance
FIFO	first-in first-out memory buffer—the first data stored is the first data sent to the acceptor; often used on DAQ devices to temporarily store incoming or outgoing data until that data can be retrieved or output
floating signal sources	signal sources, including batteries, transformers, or thermocouples, with voltage signals that are not connected to an absolute reference or system ground; also called nonreferenced signal sources
FPGA	field programmable gate array
FREQ_OUT	frequency output signal

G

gain	the factor by which a signal is amplified, sometimes expressed in decibels
GATE	gate signal
GPCTR	general-purpose counter signal
GPCTR0_GATE	general-purpose counter 0 gate signal
GPCTR0_OUT	general-purpose counter 0 output signal
GPCTR0_SOURCE	general-purpose counter 0 clock source signal
GPCTR0_UP_DOWN	general-purpose counter 0 up down signal
GPCTR1_GATE	general-purpose counter 1 gate signal
GPCTR1_OUT	general-purpose counter 1 output signal
GPCTR1_SOURCE	general-purpose counter 1 clock source signal

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GPCTR1_UP_DOWN	general-purpose counter 1 up down signal
grounded signal sources	signal sources with voltage signals that are referenced to a system ground, such as the earth or a building ground; also called grounded signal sources

H

h	hour
Hz	hertz—the number of scans read or updates written per second

I

I/O	input/output—the transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces
impedance	resistance
in.	inch or inches
INL	integral nonlinearity—a measurement in least significant bits of the worst-case deviation from the ideal A/D or D/A transfer characteristic of the analog I/O circuitry
I_{OH}	current, output high
I_{OL}	current, output low
IRQ	interrupt request

K

kHz	kilohertz

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L

LabVIEW	Laboratory Virtual Instrument Engineering Workbench—a program development application based on the programming language G and used commonly for test and measurement purposes
LED	light emitting diode
LSB	least significant bit

M

master	a functional part of a MXI/VME/VXIbus device that initiates data transfers on the backplane; a transfer can be either a read or a write
MAX	Measurement and Automation Explorer
MB	megabytes of memory
Measurement Studio	a set of test and measurement-oriented software tools from National Instruments for C, C++, and Visual Basic users
MHz	megahertz
MIO	multifunction I/O
MITE	MXI Interface to Everything
MSB	most significant bit
mux	multiplexer—a switching device with multiple inputs that sequentially connects each of its inputs to its output, typically at high speeds, in order to measure several signals with a single analog input channel
mV	millivolts
MXI	a high-performance communication link that interconnects devices using round, flexible cables

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N

NC	not connected (signal)
NI	National Instruments
NI-DAQ	National Instruments driver software for DAQ hardware
noise	an undesirable electrical signal from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, soldering irons, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors; noise corrupts signals you are trying to send or receive
nonreferenced signal sources	signal sources, including batteries, transformers, or thermocouples, with voltage signals that are not connected to an absolute reference or system ground; also called nonreferenced signal sources
Nyquist frequency	the maximum signal frequency that a sampling system can accurately represent in frequency spectrum measurement, which is half the sampling frequency

O

OUT	output pin—a counter output pin where the counter can generate various TTL pulse waveforms

P

PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA; is achieving widespread acceptance as a standard for PCs and work-stations, and offers a theoretical maximum transfer rate of 132 Mbytes/s
pd	pull down
PFI	programmable function input
PFI0/TRIG1	PFI0/trigger 1
PFI1/TRIG2	PFI1/trigger 2

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PFI2/CONVERT*	PFI2/convert
PFI3/GPCTR1_SOURCE	PFI3/general purpose counter 1 source
PFI4/GPCTR1_GATE	PFI4/general-purpose counter 1 gate
PFI5/UPDATE*	PFI5/update
PFI6/WFTRIG	PFI6/waveform trigger
PFI7/STARTSCAN	PFI7/start of scan
PFI8/GPCTR0_SOURCE	PFI8/general-purpose counter 0 source
PFI9/GPCTR0_GATE	PFI9/general-purpose counter 0 gate
PGIA	programmable gain instrumentation amplifier
PLL	phase-locked loop
ppm	parts per million
pseudodifferential channels	pseudodifferential channels are all referred to a common ground, but this ground is not directly connected to the computer ground. Often this connection is made by a relatively low value resistor to give some isolation between the two grounds.
pu	pull up
PWB	printed wire board
PXI	PCI eXtensions for Instrumentation—an open specification that builds off the CompactPCI specification by adding instrumentation-specific features

R

range	the maximum and minimum parameters between which a sensor, instrument, or device operates with a specified set of characteristics
referenced signal sources	signal sources with voltage signals that are referenced to a system ground, such as the earth or a building ground; also called grounded signal sources

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rise time	the difference in time between the 10% and 90% points of the step response of a system
rms	root mean square
RTD	resistive temperature detector—a metallic probe that measures temperature based upon its coefficient of resistivity
RTSI bus	real-time system integration bus—the National Instruments timing bus that connects DAQ devices directly, by means of connectors on top of the devices for precise synchronization of functions
RTSI_OSC	RTSI Oscillator—RTSI bus master clock

S

s	seconds
S	samples
S/s	samples per second—used to express the rate at which a DAQ device samples an analog signal
SCANCLK	scan clock signal
scatter-gather	a term that describes very high-speed DMA burst-mode transfers that are made only by the bus master
signal conditioning	the manipulation of signals to prepare them for digitizing
SFDR	spurious free dynamic range
SISOURCE	SI counter clock signal
SOURCE	source signal
STARTSCAN	start scan signal
STC	system timing controller
system noise	a measure of the amount of noise present in an analog circuit or when the analog inputs are grounded

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T

TC	terminal count—the ending value of a counter
t_{gh}	gate hold time
t_{gsu}	gate setup time
t_{gw}	gate pulse width
THD	total harmonic distortion—the ratio of the total rms signal due to harmonic distortion to the overall rms signal, in decibel or a percentage
thermocouple	a temperature sensor created by joining two dissimilar metals whose junction produces a small voltage as a function of the temperature
t_{off}	an offset (delayed) pulse; the offset is t nanoseconds from the falling edge of the CONVERT* signal
t_{out}	output delay time
t_p	period of a pulse train
TRIG	trigger signal
t_{sc}	source clock period
t_{sp}	source pulse width
TTL	transistor-transistor logic
t_w	pulse width

U

UI	update interval
UISOURCE	update interval counter clock signal
UPDATE*	update signal

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V

V	volts
V_{CC}	collector common voltage—power supply voltage
V_{cm}	common-mode noise and ground potential
VCXO	voltage-controlled crystal oscillator
VDC	volts direct current
VI	virtual instrument—(1) a combination of hardware and/or software elements, typically used with a PC, that has the functionality of a classic stand-alone instrument; (2) a LabVIEW software module (VI), which consists of a front panel user interface and a block diagram program
V_{in}	volts in
V_m	measured voltage
V_{OH}	volts, output high
V_{OL}	volts, output low
V_{OUT}	volts out
V_{rms}	volts, root mean square
V_s	ground-referenced signal source

W

WFTRIG	waveform generation trigger signal

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