

# DATA SHEET

## **TDA1510AQ** 24 W BTL or 2 x 12 W stereo car radio power amplifier

Product specification  
File under Integrated Circuits, IC01

January 1992

## 24 W BTL or 2 x 12 W stereo car radio power amplifier

### TDA1510AQ

#### GENERAL DESCRIPTION

The TDA1510AQ is a class-B integrated output amplifier encapsulated in a 13-lead single in-line (SIL) plastic power package. Developed primarily for car radio application, the device can also be used to drive low impedance loads (down to 1,6  $\Omega$ ). With a supply voltage ( $V_P$ ) of 14,4 V, an output power of 24 W can be delivered into a 4  $\Omega$  Bridge Tied Load (BTL), or when used as a stereo amplifier, 2  $\times$  12 W into 2  $\Omega$  or 2  $\times$  7 W into 4  $\Omega$ .

#### Features

- Flexibility – stereo as well as mono BTL
- Low offset voltage at the output (important for BTL)
- Load dump protection
- A.C. short-circuit-safe to ground
- Low number, small sized external components
- Internal limiting of bandwidth for high frequencies
- High output power
- Large useable gain variation
- Good ripple rejection
- Thermal protection
- Low stand-by current possibility
- High reliability.

#### QUICK REFERENCE DATA

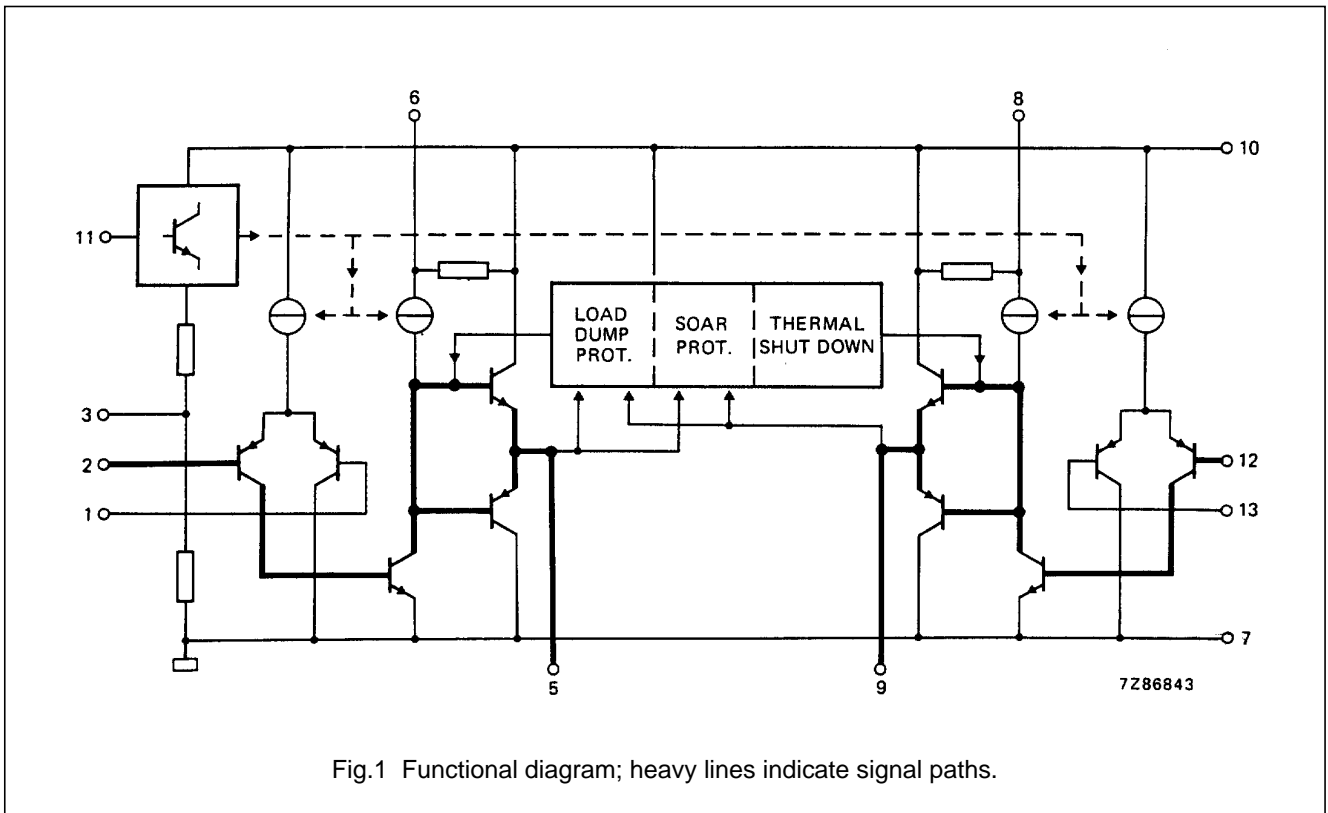
PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage range:						
operating		$V_P$	6,0	14,4	18,0	V
non-operating		$V_P$	–	–	28,0	V
non-operating, load dump protection		$V_P$	–	–	45,0	V
Repetitive peak output current		$I_{ORM}$	–	–	4,0	A
Total quiescent current		$I_{tot}$	–	75	120	mA
Stand-by current		$I_{sb}$	–	–	2	mA
Switch-on current		$I_{so}$	0,15	0,35	0,80	mA
Input impedance	pins 1, 2, 12 and 13	$ Z_I $	1	–	–	M $\Omega$
Storage temperature range		$T_{stg}$	–65	–	+ 150	$^{\circ}\text{C}$
Crystal temperature		$T_C$	–	–	150	$^{\circ}\text{C}$

#### PACKAGE OUTLINE

TDA1510AQ: 13-lead SIL-bent-to-DIL; plastic power (SOT 141C); SOT141-6; 1996 Aug 01.

24 W BTL or 2 x 12 W stereo car radio  
power amplifier

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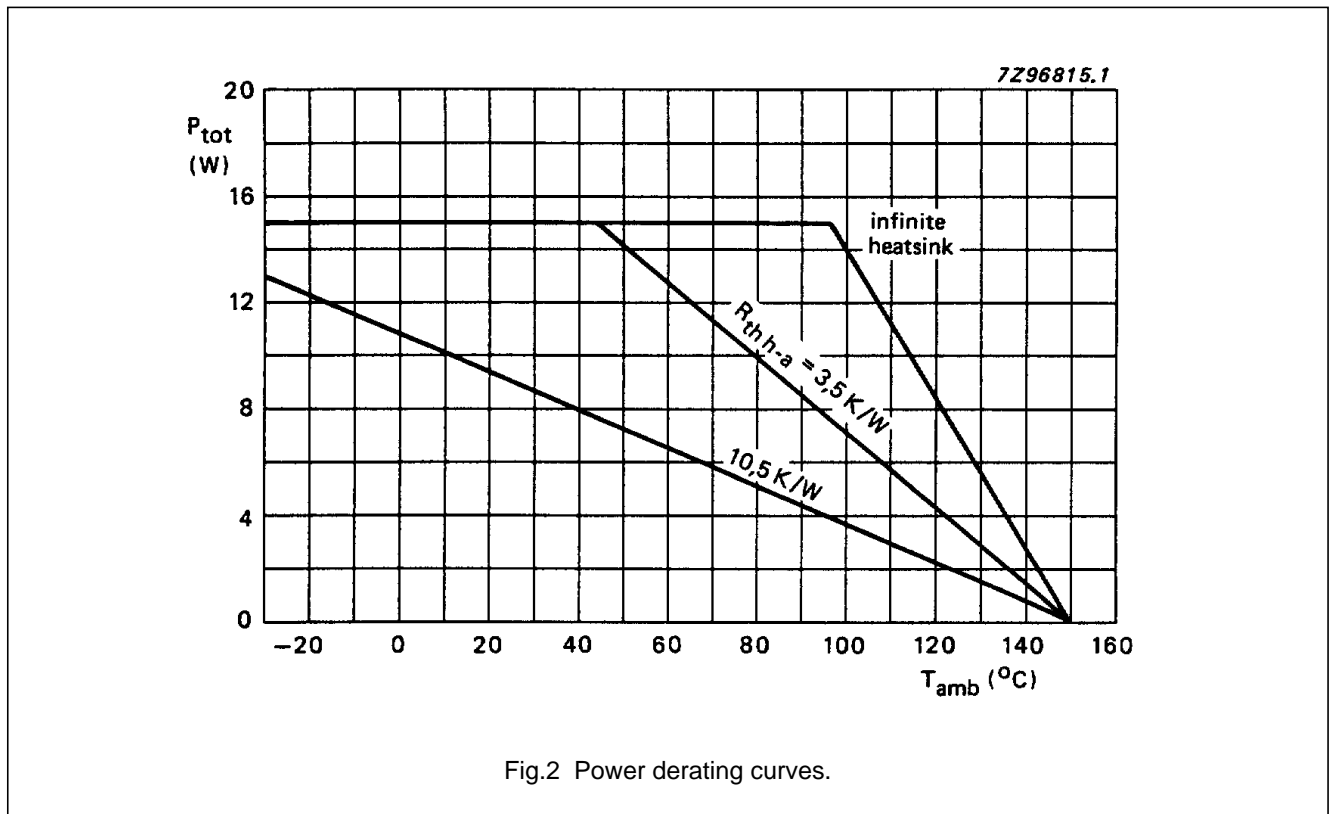
24 W BTL or 2 x 12 W stereo car radio  
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**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Supply voltage:					
operating	pin 10	$V_P$	–	18	V
non-operating		$V_P$	–	28	V
non-operating, load dump protection	during 50 ms	$V_P$	–	45	V
Peak output current		$I_{OM}$	–	6	A
Total power dissipation	see Fig.2	$P_{tot}$			
Storage temperature range		$T_{stg}$	–65	+ 150	°C
Crystal temperature		$T_C$	–	+ 150	°C



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### HEATSINK DESIGN EXAMPLE

The derating of the encapsulation requires the following external heatsink (for sine-wave drive):

$$(R_{th\ j-mb}) = 3,5\text{ K/W}$$

24 W BTL (4  $\Omega$ ) or 2 x 12 W stereo (2  $\Omega$ ); maximum sine-wave dissipation = 12 W;

$T_{amb} = 65\text{ }^{\circ}\text{C}$  (maximum):

$$R_{th\ h-a} = \frac{150 - 65}{12} - 3,5 = 3,5\text{ K/W}$$

2 x 7 W stereo (4  $\Omega$ ); maximum sine-wave dissipation = 6 W;  $T_{amb} = 65\text{ }^{\circ}\text{C}$  (maximum):

$$R_{th\ h-a} = \frac{150 - 65}{12} - 3,5 = 10,5\text{ K/W}$$

### D.C. CHARACTERISTICS

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage range		$V_P$	6,0	14,4	18,0	V
Repetitive peak output current		$I_{ORM}$	–	–	4,0	A
Total quiescent current		$I_{tot}$	–	75	120	mA
Stand-by current		$I_{sb}$	–	–	2	mA
Switch-on current	$V_{11} \leq V_{10}$ ; note 1	$I_{so}$	0,15	0,35	0,80	mA

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### A.C. CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $V_P = 14,4\text{ V}$ ;  $f = 1\text{ kHz}$ ; unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
<b>Bridge Tied Load application (BTL)</b>						
Output power with bootstrap	note 6; $R_L = 4\ \Omega$ $V_P = 13,2\text{ V}$ $d_{tot} = 0,5\%$ $d_{tot} = 10\%$	$P_o$	–	15,0	–	W
	$V_P = 14,4\text{ V}$ $d_{tot} = 0,5\%$ $d_{tot} = 10\%$	$P_o$	15,5	18,0	–	W
		$P_o$	20,0	24,0	–	W
Open loop voltage gain		$G_o$	–	75	–	dB
Closed loop voltage gain	note 2	$G_c$	39,5	40,0	40,5	dB
Frequency response	at $-3\text{ dB}$ ; note 3	$f_r$	–	20 to $> 20\text{ k}$	–	Hz
Input impedance	note 4	$ Z_i $	1	–	–	$M\Omega$
Noise output voltage (r.m.s. value)	$f = 20\text{ Hz to } 20\text{ kHz}$ $R_S = 0\ \Omega$ $R_S = 10\ \Omega$ $R_S = 10\text{ k}\Omega$ ; according to IEC 179 curve A	$V_n (rms)$	–	0,2	–	mV
		$V_n (rms)$	–	0,35	0,8	mV
		$V_n (rms)$	–	0,25	–	mV
Supply voltage ripple rejection	$f = 100\text{ Hz}$ ; note 5	SVRR	42	50	–	dB
D.C. output offset voltage between channels		$ \Delta V_{5-9} $	–	2	50	mV
Power bandwidth	$-1\text{ dB}$ ; $d_{tot} = 0,5\%$	B	–	30 to $> 40\text{ k}$	–	Hz

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PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
<b>Stereo application</b>						
Output power; with bootstrap	note 6;					
	$R_L = 4 \Omega$					
	$V_P = 13,2 \text{ V}$					
	$d_{\text{tot}} = 0,5\%$	$P_o$	–	4,5	–	W
	$d_{\text{tot}} = 10\%$	$P_o$	–	6,0	–	W
	$V_P = 14,4 \text{ V}$					
	$d_{\text{tot}} = 0,5\%$	$P_o$	4,5	5,5	–	W
	$d_{\text{tot}} = 10\%$	$P_o$	6,0	7,0	–	W
	$R_L = 2 \Omega$					
	$V_P = 13,2 \text{ V}$					
Output power; without bootstrap	$d_{\text{tot}} = 0,5\%$	$P_o$	–	7,5	–	W
	$d_{\text{tot}} = 10\%$	$P_o$	–	10,0	–	W
	$V_P = 14,4 \text{ V}$					
	$d_{\text{tot}} = 0,5\%$	$P_o$	7,75	9,0	–	W
	$d_{\text{tot}} = 10\%$	$P_o$	10,0	12,0	–	W
	notes 6, 8 and 9					
	$R_L = 4 \Omega$					
	$V_P = 14,4 \text{ V}$					
	$d_{\text{tot}} = 10\%$	$P_o$	–	6	–	W
	Frequency response	notes 3 and 6				
	–3 dB	$f_r$	–	40 to > 20 k	–	Hz
Supply voltage ripple rejection	note 5					
	$f = 1 \text{ kHz}$	SVRR	–	50	–	dB
Channel separation	$R_S = 10 \text{ k}\Omega$ ;					
	$f = 1 \text{ kHz}$	$\alpha$	40	50	–	dB
Closed loop voltage gain	note 7	$G_c$	39,5	40,0	40,5	dB
Noise output voltage (r.m.s. value)	$f = 20 \text{ Hz to } 20 \text{ kHz}$ ;					
	$R_S = 0 \Omega$	$V_n \text{ (rms)}$	–	0,15	–	mV
	$R_S = 10 \text{ k}\Omega$	$V_n \text{ (rms)}$	–	0,25	–	mV
	$R_S = 10 \text{ k}\Omega$ ;					
	according to					
	IEC179 curve A	$V_n \text{ (rms)}$	–	0,2	–	mV

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**TDA1510AQ****Notes to the characteristics**

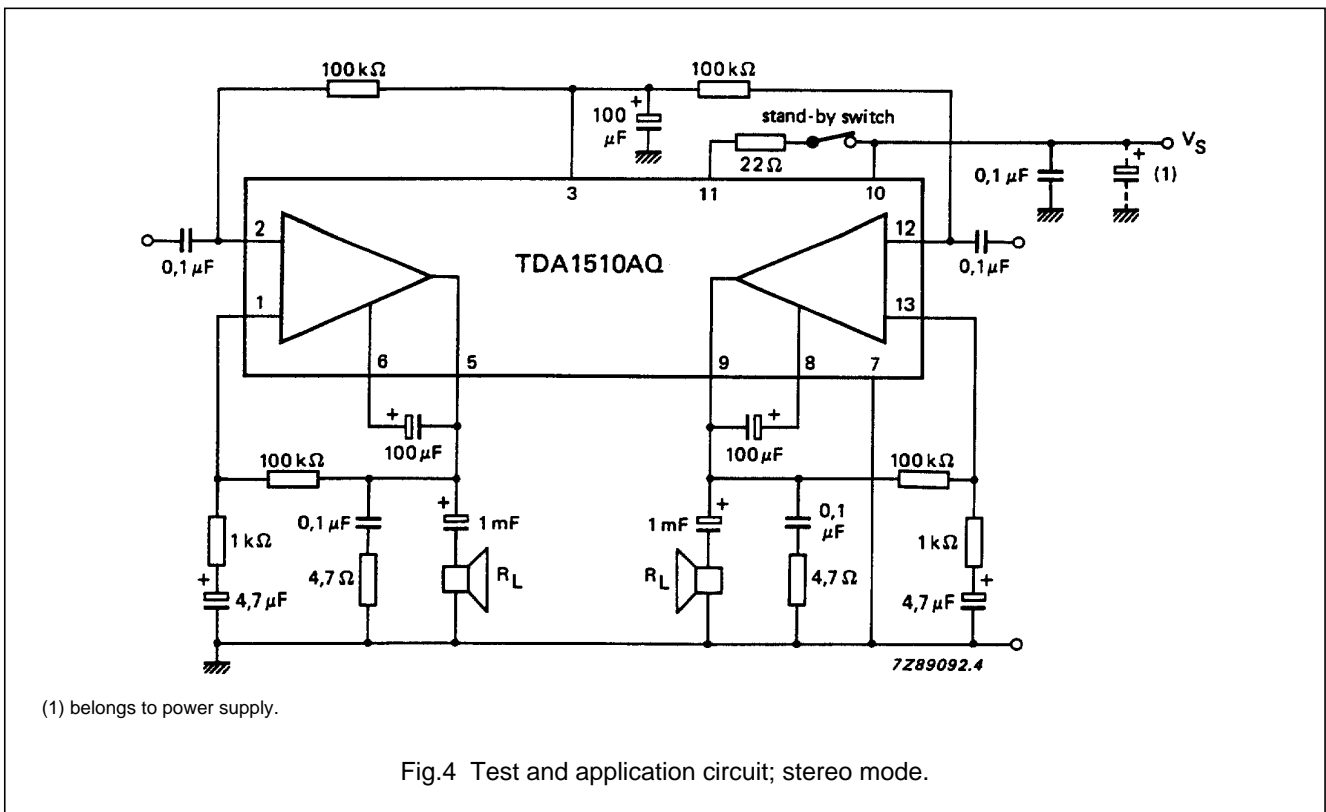
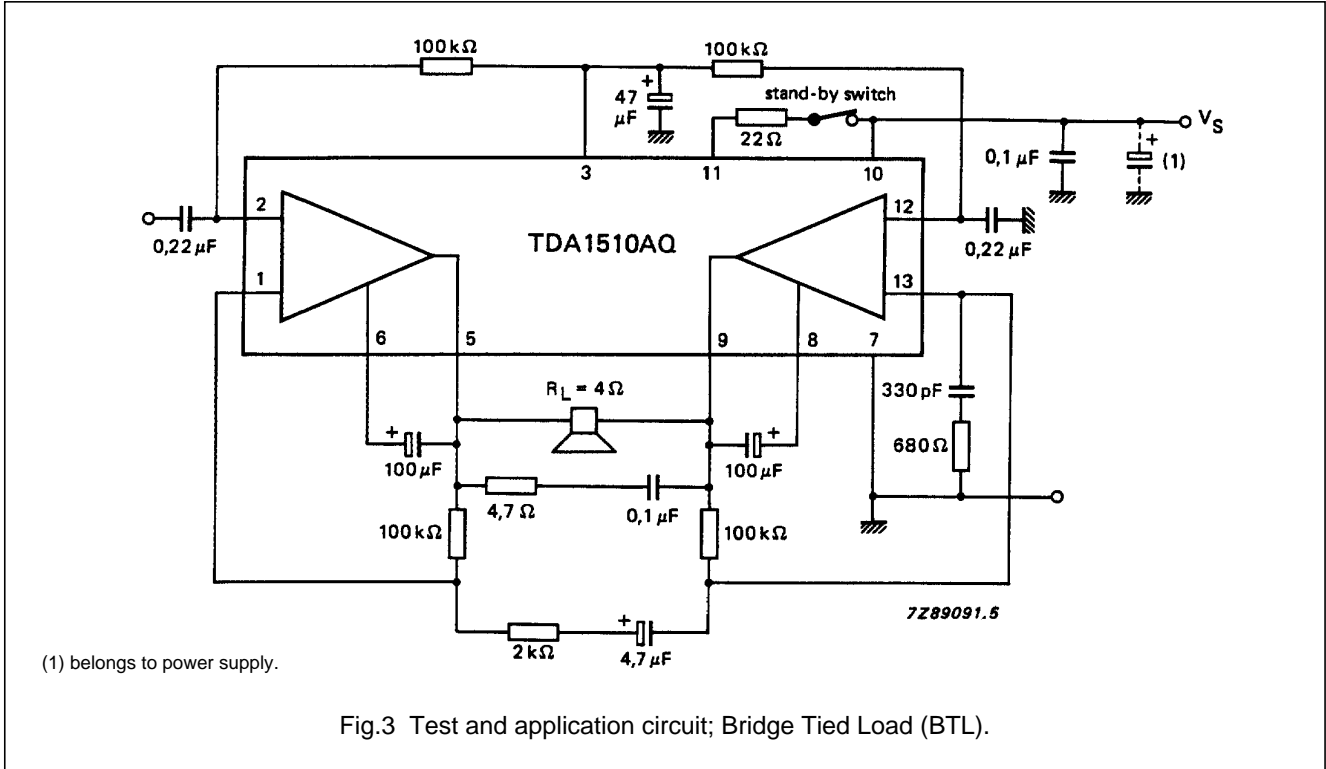
1. If  $V_{11} > V_{10}$  then  $I_{11}$  must be  $< 10$  mA.
2. Closed loop voltage gain can be chosen between 32 and 56 dB (BTL), and is determined by external components.
3. Frequency response externally fixed.
4. The input impedance in the test circuit (Fig.3) is typ. 100 k $\Omega$ .
5. Supply voltage ripple rejection measured with a source impedance of 0  $\Omega$  (maximum ripple amplitude 2 V).
6. Output power is measured directly at the output pins of the IC.
7. Closed loop voltage gain can be chosen between 26 and 50 dB (stereo), and is determined by external components.
8. A resistor of 56 k $\Omega$  between pins 3 and 7 is required for symmetrical clipping.
9. Without bootstrap the 100  $\mu$ F capacitor between pins 5 and 6 and the 100  $\mu$ F capacitor between pins 8 and 9 can be omitted. Pins 6 and 8 connected to pin 10.



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APPLICATION INFORMATION



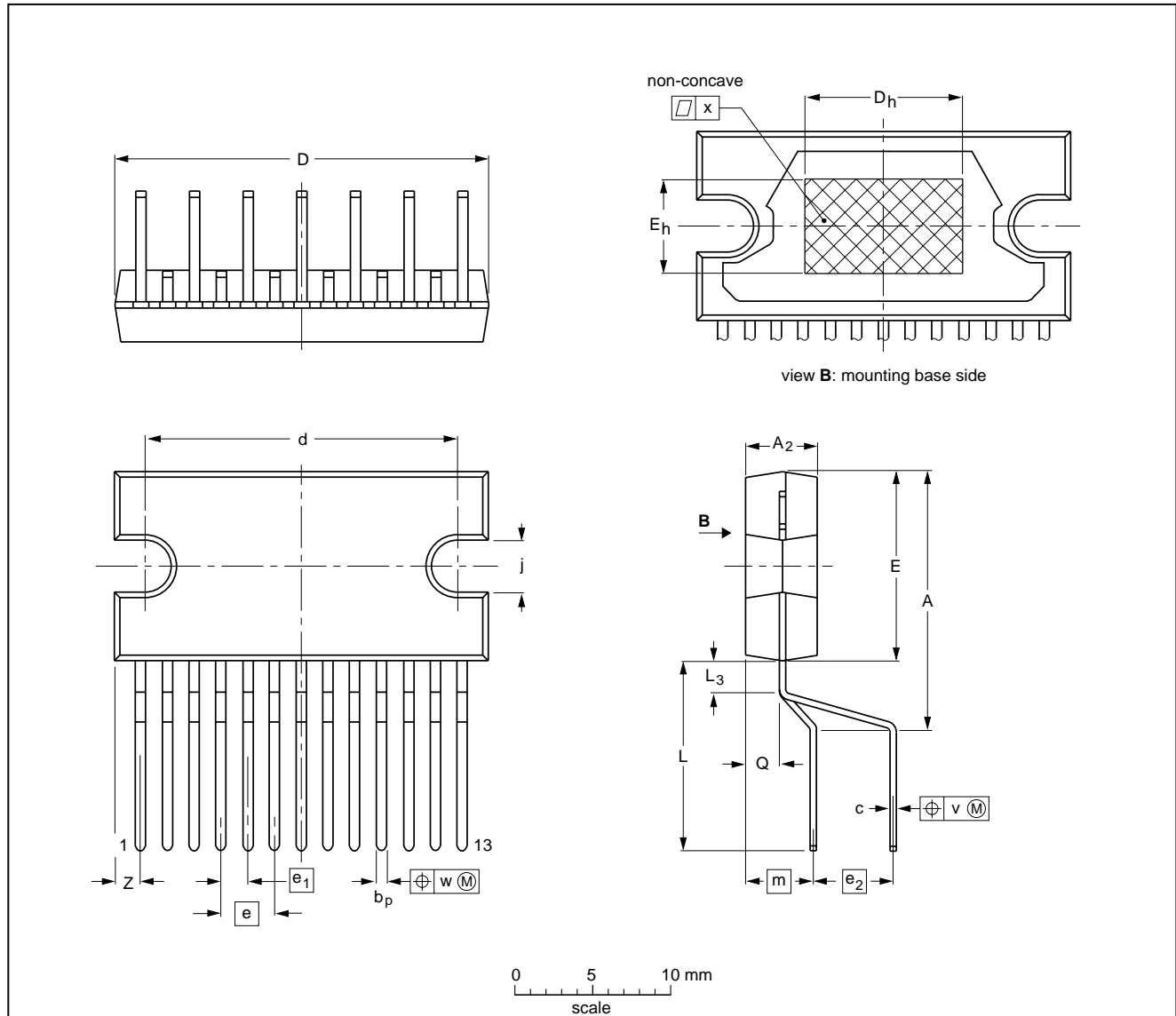
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PACKAGE OUTLINE

DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)

SOT141-6



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>2</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	d	D <sub>h</sub>	E <sup>(1)</sup>	e	e <sub>1</sub>	e <sub>2</sub>	E <sub>h</sub>	j	L	L <sub>3</sub>	m	Q	v	w	x	Z <sup>(1)</sup>
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT141-6						95-03-11 97-12-16

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**SOLDERING**

**Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

**Soldering by dipping or by wave**

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

**Repairing soldered joints**

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**LIFE SUPPORT APPLICATIONS**

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