

LC640.480.33-AC

HIGH BRIGHTNESS 10.4" COLOR TFT AMLCD



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LC640.480.33-AC Display

The LC640.480.33-AC is a 1000 nit 10.4" diagonal VGA color AMLCD flat panel display module intended for commercial applications requiring outdoor viewability and long life. Special attention to the total backlight design gives the display a wide, "single-BEF" viewing angle while maintaining luminance efficiency greater than 45 nit/W.

The display is convection cooled and does not require a fan, yet features a wide operating temperature range. It is lightweight, compact, and rugged, and includes an integrated inverter in a package approximately one inch thick. With fast cell response and an 18-bit (6 bits per color) video interface, this display can show full motion video images.

The LC640.480.33-AC is designed, tested, and characterized as an integrated system made up of two subassemblies. The LCD subassembly includes a sealed optical cavity, and the backlight/inverter subassembly includes a cold cathode fluorescent (CCFL) backlight and inverter. Due to the sealed optical cavity, the backlight subassembly may be replaced without exposing the back of the LCD cell and optical films to airborne contaminants.

Features and Benefits

- ◆ 1000 nit typical luminance for sunlight-readability
- ◆ 3:1 contrast @ 100K Lux ambient for outdoor daylight use
- ◆ Wide +40/-60° vertical / ±70° horizontal viewing angle
- ◆ 100:1 digital dimming for efficient control over a wide range of ambient light
- ◆ 18-bit (6 bits per color) display interface for wide color range (262,144 colors)
- ◆ 30,000 hours MTBF for long service-free operating life
- ◆ Durable and lightweight enclosure for rugged conditions
- ◆ Convection cooling for operation without cooling fans
- ◆ 3H diffuse hard coated front surface for scratch protection
- ◆ Modular design for easy field replacement of backlight and inverter
- ◆ Automatic shutdown at low and high temperature extremes for product safety

Installation and Handling

Do not drop, bend, or flex the display. Do not allow objects to strike the surface of the display.

Mounting the Display

To maximize shock and vibration performance, the display must be properly mounted using all four mounting hole locations. There are two recommended mounting configurations as shown in Figure 1 using the hardware listed in Table 1 below. Appropriate changes to these mounting configurations may be needed to meet specific requirements or applications.

Figure 1. Mounting Options.

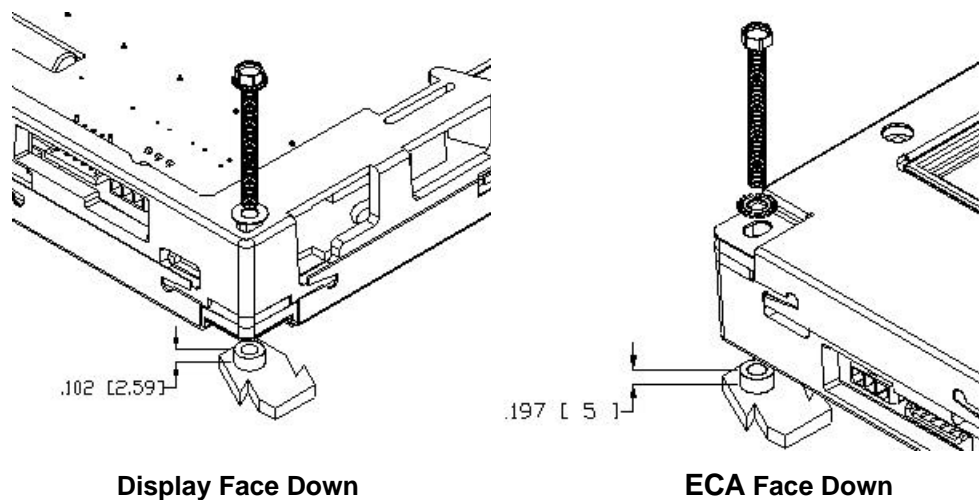


Table 1. Mounting Hardware.

Screw	#6 SS, hex head or hex washer head, or M3 SS hex head or hex washer head
Washer	Bearing washer for display face down bearing application only Lockwasher, external type
Tightening torque	4 oz-in \ 2.8x10 ⁵ dyne – cm

Mounting Display Face Down

Standoff spacers with a minimum height of 0.102" (2.59 mm) must be used at all four mounting locations to prevent binding and deflection of the display. Threaded studs anchored in a bezel would be a design variation of this mounting option.

Mounting ECA Face Down

When mounting the display with the mounting screws installed from the viewing side, it is not necessary to incorporate a flat washer. Provide for proper vent clearance and an air gap/isolation allowance of 0.197" (5 mm) or better as described below.

Vent Clearance

The LC640.480.33-AC display is a wide temperature display utilizing convection cooling. It is imperative to allow ambient air unrestricted access to the cooling vents in order to reliably operate the display at high temperatures

The vents for the lamp cavity are along the top and bottom edges of the display with the openings facing the rear. The vents for the inverter cavity are along the top and bottom faces of the display: four along the top surface and four along the bottom surface. Refer to the mechanical outline drawing in Figure 15 for vent locations.

Isolation/Air Gap

The display generates high voltage AC to drive the CCFL tubes. High voltage is present at numerous points on the backlight/inverter ECA which forms the rear surface of the display, so your application should not place metal too near the ECA. In the interests of both high voltage isolation and airflow for cooling, it is recommended that an air gap of .197" (5 mm) or greater be maintained behind the display.

Ambient Light Sensor Clearance

Two backlight dimming modes utilize automatic brightness control (ABC). If the display is to be operated in either of these modes, the ambient light sensor located on the front bezel must be unobstructed. If the sensor is placed behind the same protective window as the display active (viewing) area, the sensor operation may be affected due to light scattering and reflections from display-generated light coupling to the sensor via the window.

Cable Length

Due to the high frequencies present on the video interface, unterminated video cable lengths of more than two feet (600 mm) are discouraged.

Cleaning

Care should be taken to minimize scratching. Clean the display front with a dry, soft cloth such as a professional photographic lens cleaner. Disposable cleaning cloths are recommended to minimize the risk of inadvertently scratching the display with particles embedded in a re-used cloth. Particular care should be taken when cleaning displays with polarizers or anti-glare and anti-reflective films. These films may delaminate if exposed to certain chemicals.

Avoiding Image Retention

Image retention may occur when a fixed pattern is displayed for a long time. Use a screen saver or image inversion to avoid image retention on the display.

Specifications

Performance characteristics are guaranteed with the display at room temperature (25 °C) and with the operating voltage within specifications, unless otherwise specified. Optical performance is referenced to screen center at normal incidence and with the backlight at maximum luminance unless otherwise specified.

Environmental Characteristics

Table 2. Environmental Characteristics.

Temperature	
Operating	-10 to +70 °C
Operating survival	-20 to +80 °C
Storage	-25 to +85 °C
Humidity	
Operating	95% RH @ 40 °C, Non-condensing, per IEC 68-2-3
Altitude	
Operating	10K ft per IEC 68-2-13
Non-operating	40K ft per IEC 68-2-13
Vibration (random)	
Operating	0.02 g ² /Hz, 5-500 Hz, 30 min. ea. axis, per IEC 68-2-34
Shock	
Operating	100 g, 6 ms, half sine wave, 3 shocks per surface, per IEC 68-2-27

Mechanical Characteristics

Refer to mechanical outline drawing in Figure 15 on page 24.

Table 3. Mechanical Characteristics.

Display External Dimensions (millimeters (inches))	
width	272.3 (10.72) nominal
height	199.9 (7.87) nominal
depth	27.0 (1.06) nominal
Weight (typical)	
	900 g (31.7oz)
Display Active Area (millimeters (inches))	
width	211.2 (8.31) nominal
height	158.4 (6.24) nominal
Pixel Pitch (millimeters (inches))	
width	.33 (.0129) nominal
height	.33 (.0129) nominal

Optical Characteristics

Table 4. Optical Characteristics.

Luminance	
Typical	1000 NITs at screen center, initial
Minimum	900 NITs at screen center, initial
Contrast Ratio	
Dark room ambient	200: 1 typical, 150:1 minimum
500 Lux ambient	150:1 typical
3K Lux ambient	50:1 typical
100K Lux ambient	3:1 typical
Color Coordinates	
White field	x = .339 typical y = .353 typical
Luminance Non-uniformity	
31% maximum	With a white screen, max difference between any 2 of 5 points is defined as follows: $Lnu(\%) = (1 - (Lmin/Lmax)) \times 100\%$
Luminance Control (typical)	
Dimming range	50:1 initial, 100:1 stabilized (Lmax after > 15 minutes at max. lum., then Lmin at min. lum; dimming range = Lmax/Lmin)
Ambient Light Sensor	
Response	Visible light filtered ~420 to 675nm @ 50% pts.
Field of view	±50 degrees typical to half sensitivity
Dynamic range	0 to 3000 Lux typ.; assumes 18% scene reflectance
Viewing Angle	
Horizontal	±70 degrees typ., White/black CR ≥ 5
Vertical	+40/-60 degrees typ., White/black CR ≥ 5
<i>(See Figure 10)</i>	

Safety and EMI

The display will not inhibit the end product from compliance with UL1950, CSA22.2, and IEC950. The display will not inhibit the end product from complying with FCC Part 15, Subpart J, Class B or EN55022 Class B when housed in a suitable enclosure.

Reliability and Backlight Life

The demonstrated system MTBF is to be greater than 30,000 hours with a 90% confidence level at 25 °C. Refer to the following table for backlight life.

Table 5. Backlight Life.

Usage	Backlight life (typical to 50% of initial luminance)
Continuous at full luminance	20K hours
Continuous at half luminance	100K hours
Typical use using ABC*	35K hours
* Automatic brightness control	

Interfacing and Operation

Control Basics

Power Requirements

The LC640.480.33-AC display requires two power supplies: +5 Vdc for the LCD logic and +12 Vdc for the backlight. In Table 6 below, the backlight current and power are referenced to maximum luminance, 25 °C ambient temperature.

Table 6. Input Power

	Symbol	Min	Typ	Max	Units
Backlight					
Backlight voltage	V_H	+10.8	+12.0	+13.2	Vdc
Absolute max. voltage	V_{HMAX}	0	–	+16	Vdc
Steady state current ($V_H = +12$ Vdc)	I_H	–	1.9	2.5	Adc
Peak start-up current ($V_H = +12$ Vdc)	I_{HSU}	–	–	3.5	Adc
Power ($V_H = +12$ V)	P_H	–	23	30	W
LCD					
LCD voltage	V_L	4.5	+5.0	+5.5	Vdc
Absolute max. voltage	V_{LMAX}	0	–	6.0	Vdc
V_L permissible ripple ($V_L = +5$ V)	ΔV_L	–	–	100	mVpp
Current ($V_L = +5$ V)	I_L	–	280	450	mAdc
Power ($V_L = +5$ V)	P_L	–	1.4	2.3	W

CAUTION: Absolute maximum ratings are those values beyond which damage to the device may occur.

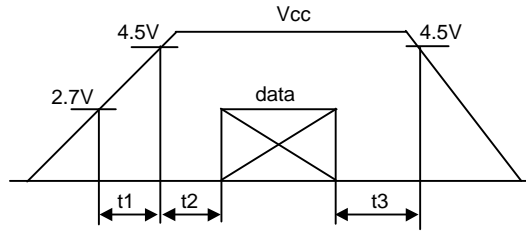
Undervoltage Lockout (Backlight only)

An undervoltage lockout (UVLO) function is included which disables the backlight under excessively low V_H conditions. The UVLO circuit will disable the backlight at approximately +8.5 Vdc as V_H falls and will enable the backlight at approximately +9.5 Vdc as V_H rises.

Power Sequencing (LCD only)

Certain restrictions on the behavior of the V_L (+5 Vdc) source and in the application of the V_L source relative to the application or removal of the video signals must be observed. These restrictions are shown in Figure 2, where “Vcc”= V_L and “data” = video signals.

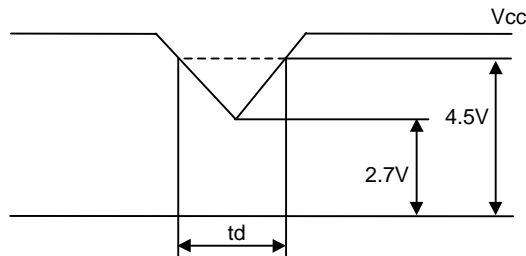
Figure 2. Power Sequencing.



where: $t_1 \leq 10\text{ms}$
 $0 < t_2 \leq 10\text{ms}$
 $0 < t_3 \leq 1\text{s}$

Applying video signals before V_L is applied may cause a latchup condition. Allowing V_L to remain “on” for a long period of time after video signals are removed—which stops the cell scanning—may produce a latent image. In addition, there is a restriction regarding dropouts on the V_L supply as illustrated in Figure 3 (“ V_{cc} ”= V_L). This is related to the reset circuit for the LCD’s internal logic. If a dip in V_L exceeds 10 ms in duration or V_L falls below 2.7 Vdc then the power sequencing procedure should be followed.

Figure 3. V_L Supply Dropouts.



where: $t_d \leq 10\text{ms}$

Backlight Signals

The dimming control and /DISABL inputs are analog, though the latter is intended to be driven from either an open collector device or CMOS logic. The /ABCOFF input is a CMOS-compatible digital input.

Table 7. Backlight Signal DC Characteristics.

Description	Min	Max	Units	Symbol
Absolute max. input voltage	-0.3	+5.3	Vdc	V_{IMAX}
Dimming input voltage range	0	+5.0	Vdc	V_{RLUM}
Recommended pot. value	10	100	K ohm	RLUM
RLUM HI source current	–	600	μA	I_{RLUM}
/ABCOFF input	+3.6	+5.0	Vdc	V_{IHA}
	0	+1.4	Vdc	V_{ILA}
	–	0.5	mA	I_{ILA}
/DISABL input	+4.5	+5.0	Vdc	V_{IHD}
	0	+1.0	Vdc	V_{ILD}
	–	1.3	mA	I_{ILD}

Note: Incorrect operation of the undervoltage lockout (UVLO) circuit may occur if the /DISABL input is allowed to operate between V_{ILD} and V_{IHD} .

Video Signals

Video Signal Characteristics

Video signal inputs on J3 are digital inputs and are compatible with CMOS logic.

Table 8. Video Signal DC Characteristics.

Description	Symbol	Minimum	Maximum	Units
Absolute Maximum Input Voltage	$V_{I\max}$	-0.3	$V_L + 0.3$	Vdc
Low-level Input Voltage	V_{IL}	0	$0.3V_L$	Vdc
High-level Input Voltage	V_{IH}	$0.7V_L$	V_L	Vdc
Low-level Input Current ¹	I_{IL1}	–	1	μA
	I_{IL2}	–	60	μA
High-level Input Current ²	I_{IH1}	–	1	μA
	I_{IH2}	–	60	μA

1. I_{IL1} applies to all signals except R/L and U/D. I_{IL2} applies to signals R/L and U/D.

2. I_{IH1} applies to all signals except ENAB, U/D, and R/L. I_{IH2} applies to signals ENAB, U/D, and R/L.

Video Modes

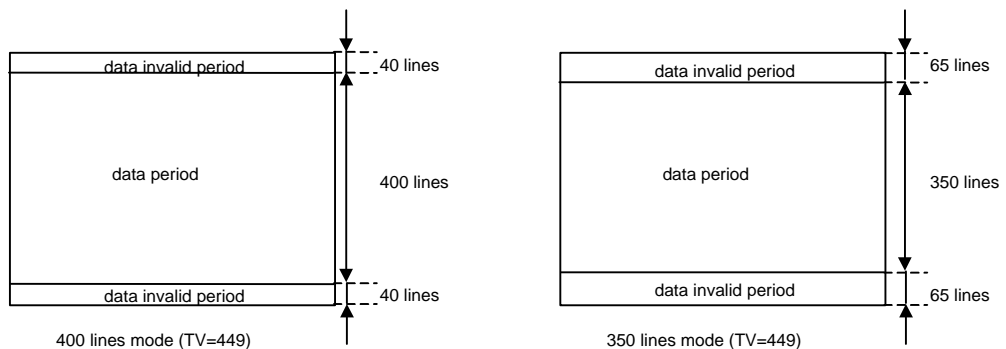
The video interface automatically recognizes 480-, 400-, and 350-line formats. Mode recognition depends on the polarity of the sync signals as shown in Table 9.

Table 9. Video Modes.

Mode	480 line	400 line	350 line
Hsync (J3-3)	negative	negative	positive
Vsync (J3-4)	negative	positive	negative

In 400-line and 350-line modes, the screen image will be automatically centered as shown in Figure 4 below.

Figure 4. Image centering.



Signal Timing

Video signal timing diagrams are shown in Figures 5, 6, and 7. The following table refers to these diagrams.

Table 10. Video signal timing.

Parameter		Symbol	Mode	Min	Typ	Max	Units
Clock	freq	1/Tc	all	–	25.18	28.33	MHz
	hi time	Tch	all	5	–	–	ns
	lo time	Tcl	all	10	–	–	ns
Data	setup time	Tds	all	5	–	–	ns
	hold time	Tdh	all	10	–	–	ns
Horiz. sync	cycle	TH	all	30.0	31.78	–	μs
				750	800	900	clock
	PW	THp	all	2	96	200	clock
Vertical sync	cycle	TV	480	515	525	560	line
			400	446	449	480	line
			350	447	449	510	line
	PW	TVp	all	1	–	34	line
Horiz.display time		THd	all	640	640	640	clock
Horiz. to clock		THc	all	10	–	Tc-10	ns
Vsync to Hsync		TVh	all	0	–	TH-THp	clock
Enable	setup time	Tes	–	5	–	Tc-10	ns
	hold time	Tep	–	2	640	640	clock
Hsync to Enable		THe	–	44	–	TH-664	clock

Table 11 below summarizes timing for the different vertical modes given typical vertical sync “cycle” (TV) values. In this table, data for line TVn is displayed as the first top row on the screen.

Table 11. Vertical mode video signal timing.

Mode	Symbol	480 line	400 line	350 line
V-data start	TVs	34	34	61
V-data period	TVd	480	400	350
V-display start	TVn	34	443-TV	445-TV
V-display period	–	480	480	480

The LC640.480.33-AC display timing is fundamentally the same as the Sharp LQ10D421 display. Horizontal display position is determined by the rising edge of the ENAB signal, and the ENAB signal has no relation to the vertical display position. If ENAB is permanently low, display starts from the data at “C104” referred to in the timing diagrams in Figures 5, 6, and 7. ENAB should not be left at a logic high permanently. In 400 and 350 line modes, data should be at a logic low during the vertical invalid period.

Figure 5. Timing Diagram, 480-line mode.

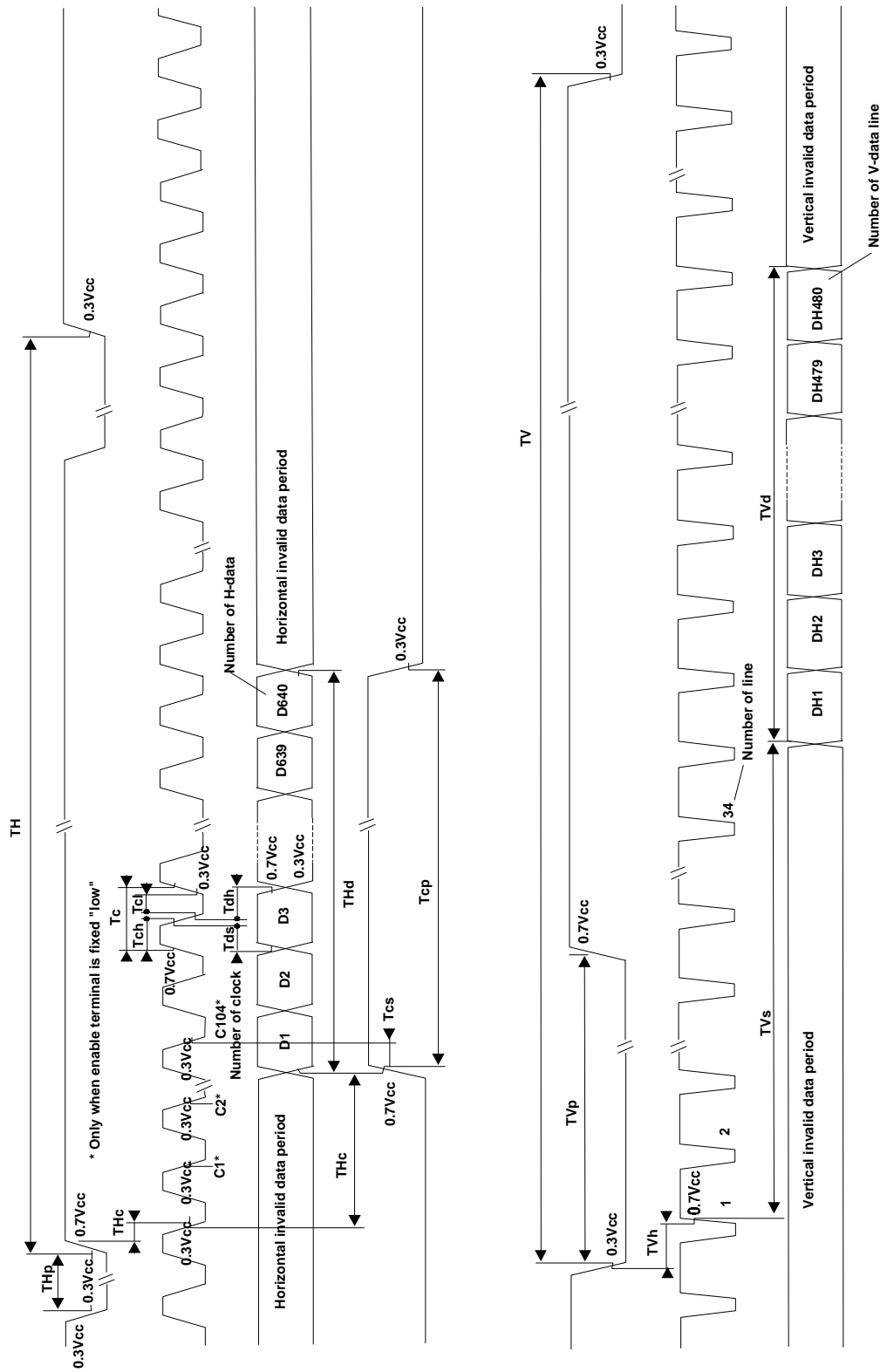
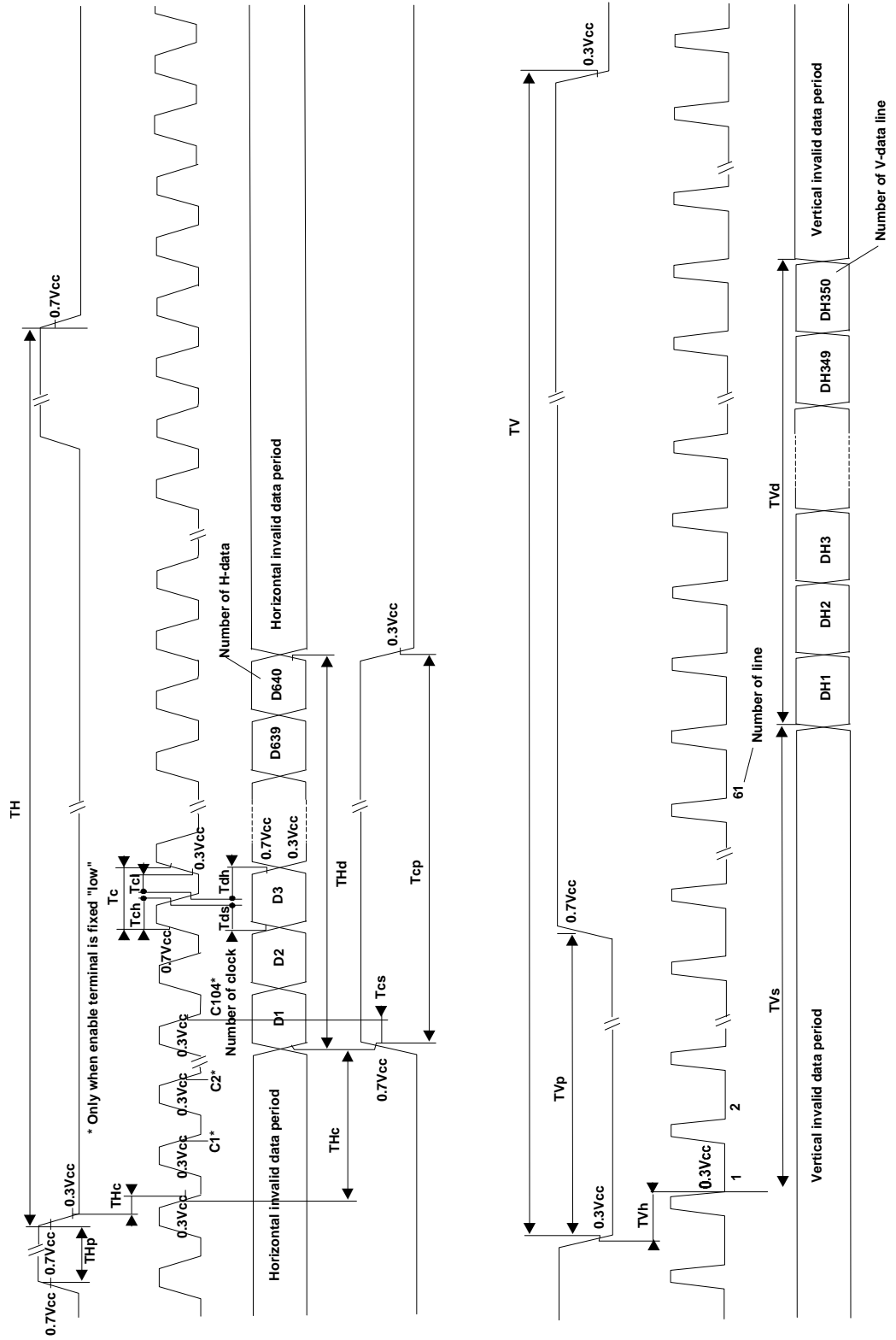


Figure 7. Timing Diagram, 350-line mode.



Video Characteristics

Colors are developed in combination with 6-bit signals (64 steps in grayscale) of each primary red, green, and blue color. This process can result in up to 262,144 (64x64x64) colors. The mapping of the eighteen video data inputs is shown in Table 12.

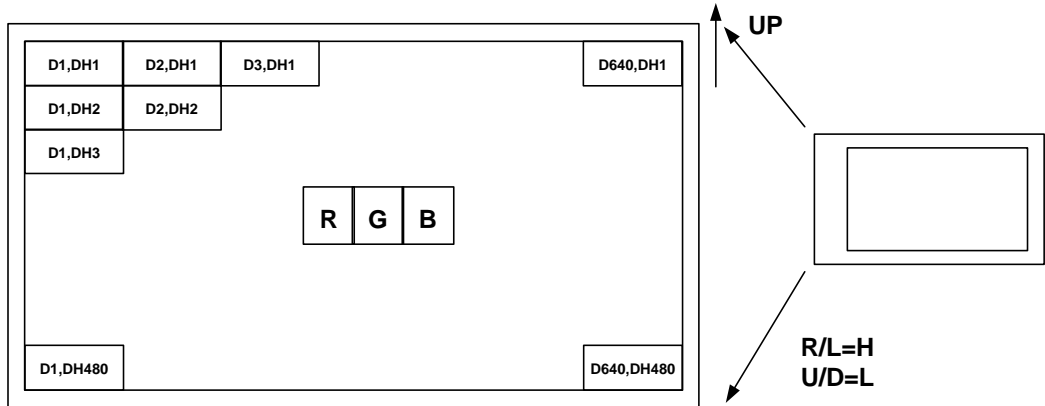
Table 12. Video Data Color/Grayscale Map

Display colors		Data signal (0: Low level, 1: High level)																	
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	↑				↑						↑					↑			
	↓				↓						↓					↓			
	bright	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Red	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Green grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	↑				↑						↑					↑			
	↓				↓						↓					↓			
	bright	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
Green	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	
Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	
Blue grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑				↑						↑					↑			
	↓				↓						↓					↓			
	bright	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	
Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	

Pixel Position

The position of pixel data, relative to the color filter orientation and scan direction inputs is shown in Figure 8. Refer to the timing diagrams in Figures 5, 6, and 7 for horizontal pixel position (D1 through D640), and for vertical line position (DH1 through DH480).

Figure 8. Pixel position of input data (480-line mode).

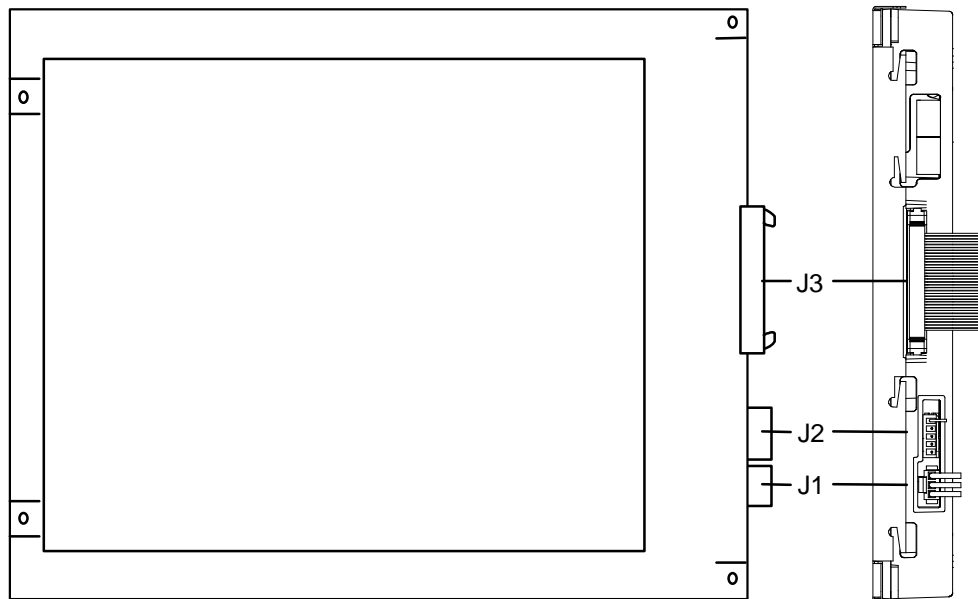


The display image may be rotated 180 degrees using the R/L and U/D signals present on J3. Refer to *Inverting the Display* on page 21 for more information.

Connectors

The LC640.480.33-AC display has three connectors on the side of the display. J3 is the video connector, J2 is the dimming connector, and J1 is the backlight power connector.

Figure 9. Connector Locations.



Video Connector (J3)

Video signals and LCD display power (V_L) are applied via a polarized 34-pin dual-row 2 mm pitch header with gold plated (30μ "") contact surfaces and ejector/latching ears. The connector is equivalent to a Samtec EHT-117-01-S-D-RA and the recommended mating cable is a Samtec TCSD-117. Consult your Samtec representative (1-800-SAMTEC9) for cable and connector options. Note that J3 is electrically and mechanically independent of the backlight assembly.

Table 13. Video Connector (J3) Pinouts.

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	2	CK	Dot Clock
3	HSync	Horiz. Sync	4	VSynC	Vert. Sync
5	GND	Ground	6	R0	Red data (LSB)
7	R1	Red data	8	R2	Red data
9	R3	Red data	10	R4	Red data
11	R5	Red data (MSB)	12	GND	Ground
13	G0	Green data (LSB)	14	G1	Green data
15	G2	Green data	16	G3	Green data
17	G4	Green data	18	G5	Green data (MSB)
19	GND	Ground	20	B0	Blue data (LSB)
21	B1	Blue data	22	B2	Blue data
23	B3	Blue data	24	B4	Blue data
25	B5	Blue data (MSB)	26	GND	Ground
27	ENAB ¹	Enable ¹	28	V_L	LCD Power
29	V_L	LCD Power	30	GND	Ground
31	R/L ²	Horiz. Scan ²	32	U/D ³	Vert. Scan ³
33	GND	Ground	34	GND	Ground

Ground (GND) is isolated from the display metal bezel.

¹ Do not keep ENAB at a static high level.

² Default is logic high or open connection. Reverse scan direction is logic low.

³ Default is logic low or open connection. Reverse scan direction is logic high.

Dimming Connector (J2)

A dimming voltage or potentiometer, plus optional backlight mode and disable logic inputs are applied via J2, which is a polarized 5-pin inline, 2.5 mm pitch header, tin plated with a friction lock. The connector is equivalent to the Molex 5268-NA ‘SPOX’ series, part number 22-05-7055. The recommended mating connector is a Molex 5264-N series housing, part number 50-37-5053 and Molex 5263 series crimp pin, part number 08-70-1040. The recommended wire size is 22-28 AWG stranded. Refer to on page 19 for more information.

Table 14. Dimming Connector (J2) Pinouts.

Pin	Symbol	Function
1	RLUM HI	Pot high side voltage source output
2	VRLUM	Analog dimming input
3	GND	Signal ground (return)
4	/ABCOFF	Automatic brightness control mode disable input
5	/DISABL	Backlight disable input

Backlight Power Connector (J1)

Backlight power (V_H) is applied via J1, which is a polarized 3 pin, 3mm pitch header with gold plated (15μ "") contact surfaces and a release latch. J1 is equivalent to a Molex 43650-0301 (“Micro-Fit 3.0” series). The recommended mating connector is a Molex part number 43645-0300 (housing) and Molex part number 43030-0008 (crimp pin). The recommended wire size is 20 AWG stranded.

Table 15. Backlight Power Connector (J1) Pinouts.

Pin	Symbol	Function
1	GND	Power ground
2	V_H	Backlight power
3	GND	Power ground

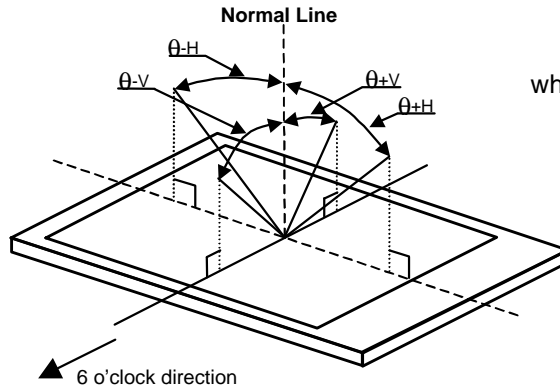
Note: Power Ground (GND) is isolated from the display metal bezel. All signals and power on the backlight are also isolated from the J3-related AMLCD display circuits.

Optical Features

Viewing Angle

Viewing angles are defined per Figure 10 below:

Figure 10. Viewing Angles.

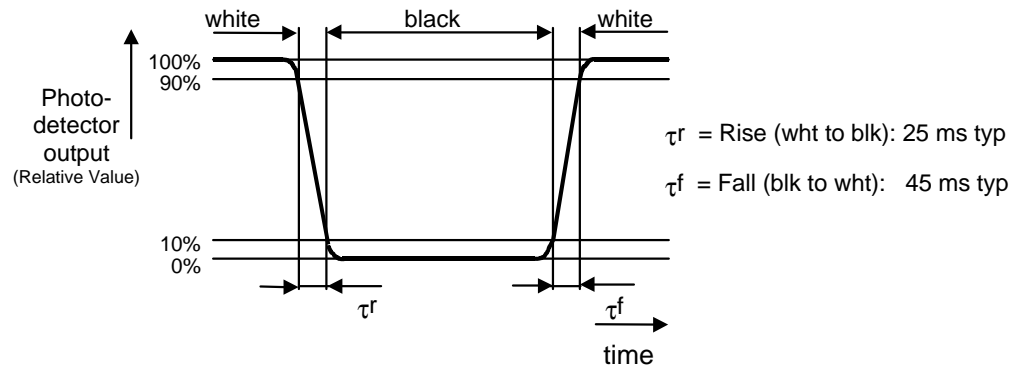


where: $\theta+H$ +Horizontal angle (+70)
 $\theta-H$ -Horizontal angle (-70)
 $\theta+V$ +Vertical angle (+40)
 $\theta-V$ -Vertical angle (-60)
 and R/L and U/D = default

Response Times

The rise response time (from white to black) is 25 ms typical and the fall response time (from black to white) is 45 ms typical. This is shown in Figure 11.

Figure 11. Response Times.



Dimming

Initial backlight dimming is performed by decreasing tube current, allowing for substantially higher tube life in applications that do not require maximum luminance. The user can adjust the display for the optimum combination of luminance, life, and power consumption for the target application.

Backlight Dimming Modes

The backlight may be operated in one of four modes without the use of jumpers or switches. The mode is selected based on the state of the /ABCOFF input and on whether the dimming input is left open or connected to a voltage source.

Table 16. Backlight Dimming Modes.

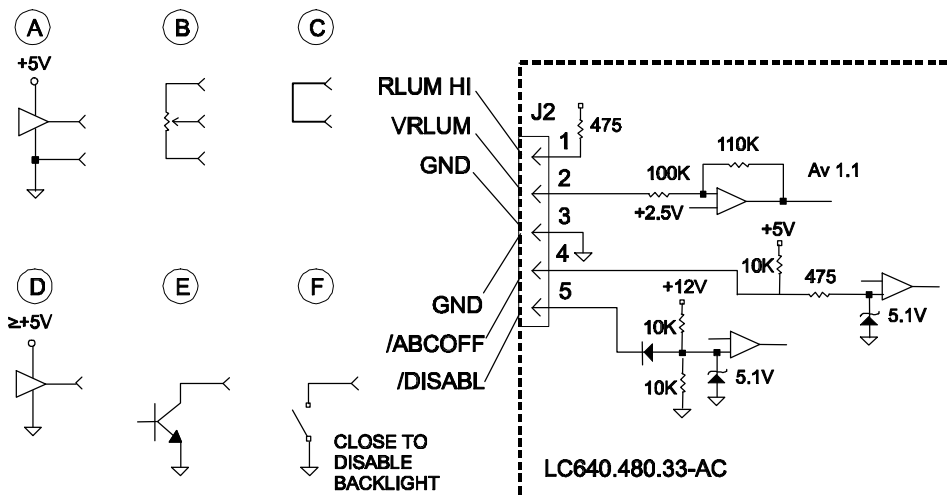
Mode	VRLUM	/ABCOFF	Comments
Extended backlight life	open	GND	Display operates at approximately half luminance.
Manual dimming	Rpot or Vin	GND	Minimum-to-maximum luminance as defined by pot or voltage at V _{RLUM} (J2-2): 0 Vdc = min, +5 Vdc = max luminance
Automatic brightness control (ABC)	open	open	Default mode. Minimum-to-maximum luminance as defined by ambient light sensor: 0 lx = min, 3000 lx = max luminance.
Biased ABC	Rpot or Vin	open	Combination of dimming control and ambient light sensor sets display luminance. In this mode, V _{RLUM} has twice the influence compared to the ambient light sensor, hence V _{RLUM} can drive luminance to either extreme regardless of ambient light conditions. Ambient light influence max is capped at 3000 lux.

Dimming Control Interfacing

An analog dimming control is available on J2. Some common methods to use this input are shown in Figure 12. In this figure, the schematic shown is an approximation of the circuitry actually present in the LC640.480.33-AC and is meant to give an indication of the dimming interface DC characteristics. The V_{RLUM} input expects a 0 to +5 Vdc voltage which may be supplied either directly or generated from a potentiometer.

In Figure 12 below, A, B, and C are analog dimming methods. D, E, and F are methods to drive the two mode set inputs.

Figure 12. Dimming Control Methods.



Method A represents sourcing the dimming input from a voltage source such as a DAC or analog op amp. The device should be powered from +5 Vdc such that the device's output will not exceed the allowable input range of the dimming input.

Method B creates the dimming voltage from a potentiometer. The recommended value for the pot is from 10K to 100K ohms. If J2 pin 1 is used as the pot high-side voltage reference as shown, then a lower pot value may restrict the maximum luminance attainable from the backlight as the drop due to the series limiting resistor becomes significant. Pot values greater than 100K ohm will result in response non-linearity due to loading from the dimming input. Some gain is provided in the dimming input path of the backlight to compensate for interface losses whereby the input dimming range provided by the source does not quite reach the 0 or +5 Vdc rails.

Method C shows a simple strap which sets the display to maximum luminance. If the input is left unconnected, the input will be in the mid-level (half luminance) condition.

Method D represents a CMOS or TTL logic gate, or a comparator to drive the backlight /DISABL input.

Method E shows an open collector device such as a bipolar transistor or FET.

Method F represents a switch or jumper.

In all cases, the return is to J2 pin 3. By its nature, the automatic brightness control disable input (/ABCOFF) would be most likely be either permanently open or permanently strapped to ground.

Inverting the Display

If the display needs to be physically inverted due to mechanical packaging or optical (e.g. vertical viewing angle) considerations, the display image can be rotated 180 degrees. This is described in Table 17.

Table 17. Inverting the Display.

Signal:	R/L	U/D	Image rightside up when:
Default orientation	1	0	J3 at left, ambient light sensor at top.
Reverse orientation	0	1	J3 at right, ambient light sensor at bottom.

Temperature Considerations

Thermal Shutdown

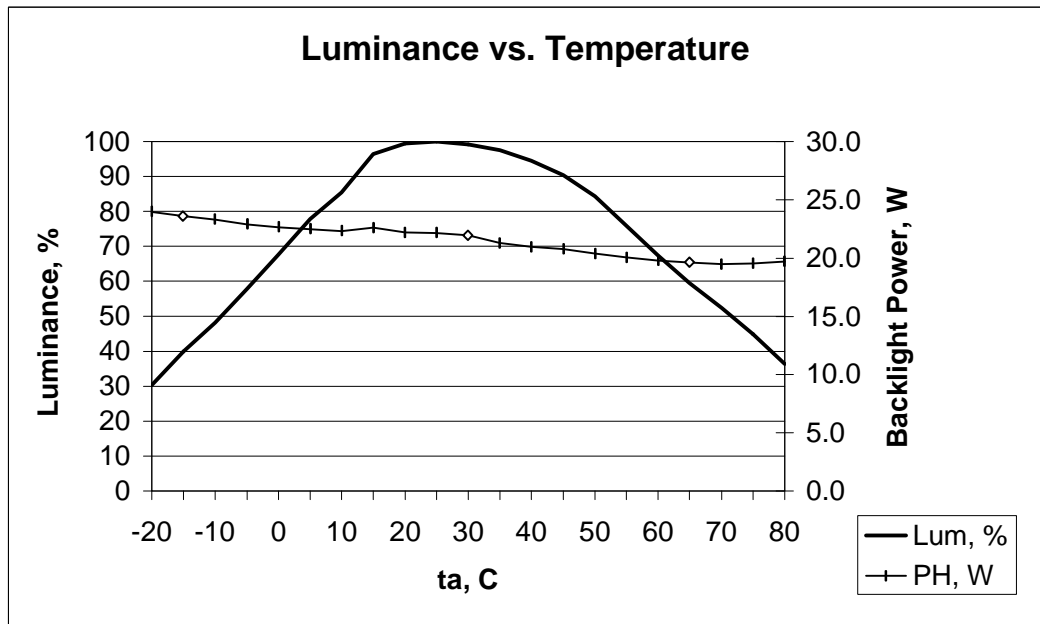
A thermal sensor referenced to the center of the backlight/inverter ECA prevents the inverter from starting at an ambient temperature of $-30\text{ }^{\circ}\text{C}$ or below, and will shut off the backlight at an ambient temperature of approximately $+90\text{ }^{\circ}\text{C}$ and above.

Luminance Variation Due to Ambient Temperature

Although the inverter features regulated lamp current drive, luminance will vary across the temperature range due to the characteristics of the CCFL tubes. Lamp luminance decreases at low temperatures as the mercury condenses out of the gas and it decreases again at high temperatures as the tube phosphors become less efficient. The LC640.480.33-AC has been designed to provide peak luminance at normal room temperatures.

Backlight power consumption decreases as temperatures climb as the working voltage of the CCFL tubes decreases. The graph in Figure 13 indicates typical performance across temperature.

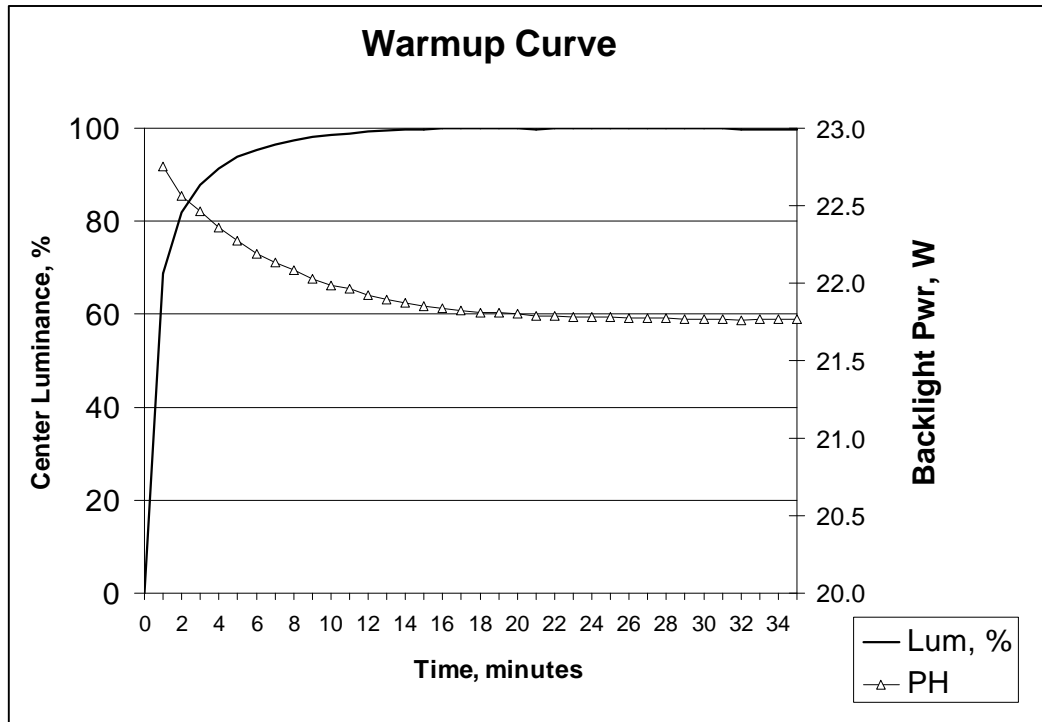
Figure 13. Luminance vs. Temperature.



Warm-up Characteristic

Some time after startup is required to allow the CCFL tubes to reach their normal operating temperature. The graph in Figure 14 shows the typical room temperature warmup curve for the LC640.480.33-AC when set to maximum luminance. As can be seen, luminance is at nearly 95% of the final value after five minutes of operation, and 99% of the final value at 10 minutes after startup.

Figure 14. Warmup Curve.



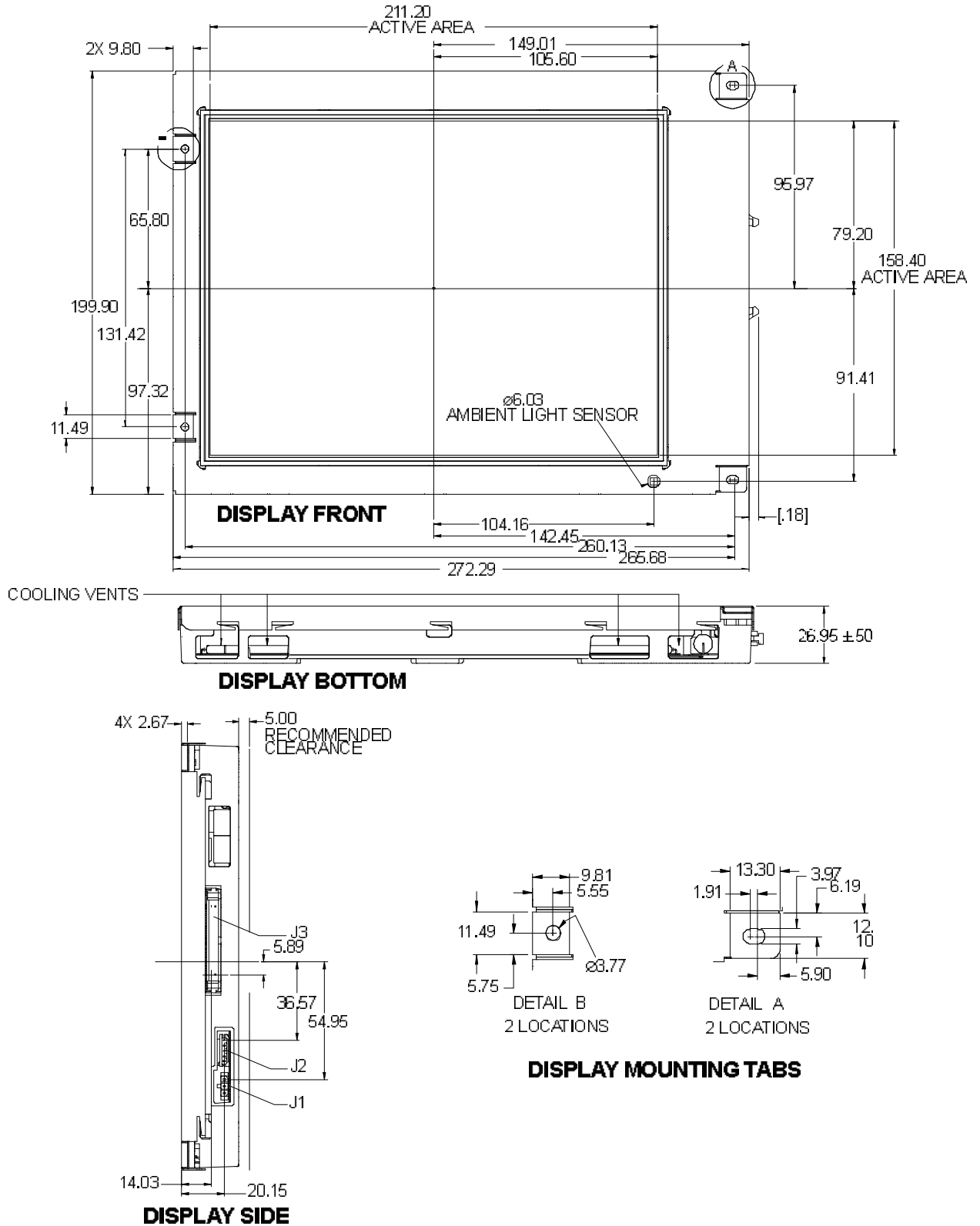
Display Dimensions

The recommended clearance shown in Figure 15 illustrates the distance behind the display ECA which should be left for free flow of air for the purposes of convection cooling. In Figure 15, dimensions are in millimeters. Tolerances unless specified are as follows:

.x ± 0.50
.xx ± 0.25

Note: The dimensions in this drawing are approximate. Please contact Planar Applications Engineering to request the actual drawing prior to beginning your design.

Figure 15. Display Dimensions.



Description of Warranty

This description is not the full warranty, and should not be construed as a substitute for the full warranty. A copy of the full warranty is available upon request.

Planar warrants that the goods it sells will be free of defects in materials and workmanship, and that these goods will substantially conform to the specifications furnished by Planar, and to any drawings or specifications furnished to the Seller by the Buyer if approved by the Seller. This warranty is effective only if Planar receives notice of such defect or non-conformance during the period of warranty, which begins the day of delivery.

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Ordering Information

Product	Part Number
LC640.480.33-AC	996-0403-00

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Planar Systems, Inc.
1400 NW Compton Drive
Beaverton, OR 97006-1992
Tel. +1 (503) 690 1100
Fax +1 (503) 690 1493
sales@planar.com
app_eng@planar.com

Europe & Asia-Pacific OEM Sales

Planar Systems, Inc.
Olarinluoma 9, P.O. Box 46
FIN-02201 Espoo, Finland
Tel. +358 9 42 0010
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