

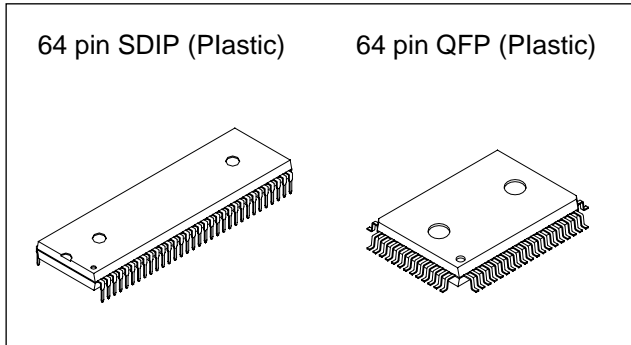
**CMOS 8-bit Single-chip Microcomputer**

**Description**

The CXP854P60 are a highly integrated micro-computers composed of a 8-bit CPU, PROM, RAM, and I/O ports. These chips feature many other high-performance circuits in a single-chip CMOS design, including an A/D converter, serial interface, timer/counter, time-base timer, vector interrupt, on-screen display function, I<sup>2</sup>C bus interface, PWM generator, remote control receiver, HSYNC counter, and watchdog timer.

Also, the CXP854P60 provides power-on reset and sleep functions. The designers have ensured low power consumption for these powerful micro-computers.

Incorporating a one-time PROM, the CXP854P60 has an equivalent function to the CXP85460 and character ROM for OSD can be written. Therefore, it is suitable for evaluation in system development and for the production of small amounts.



**Structure**

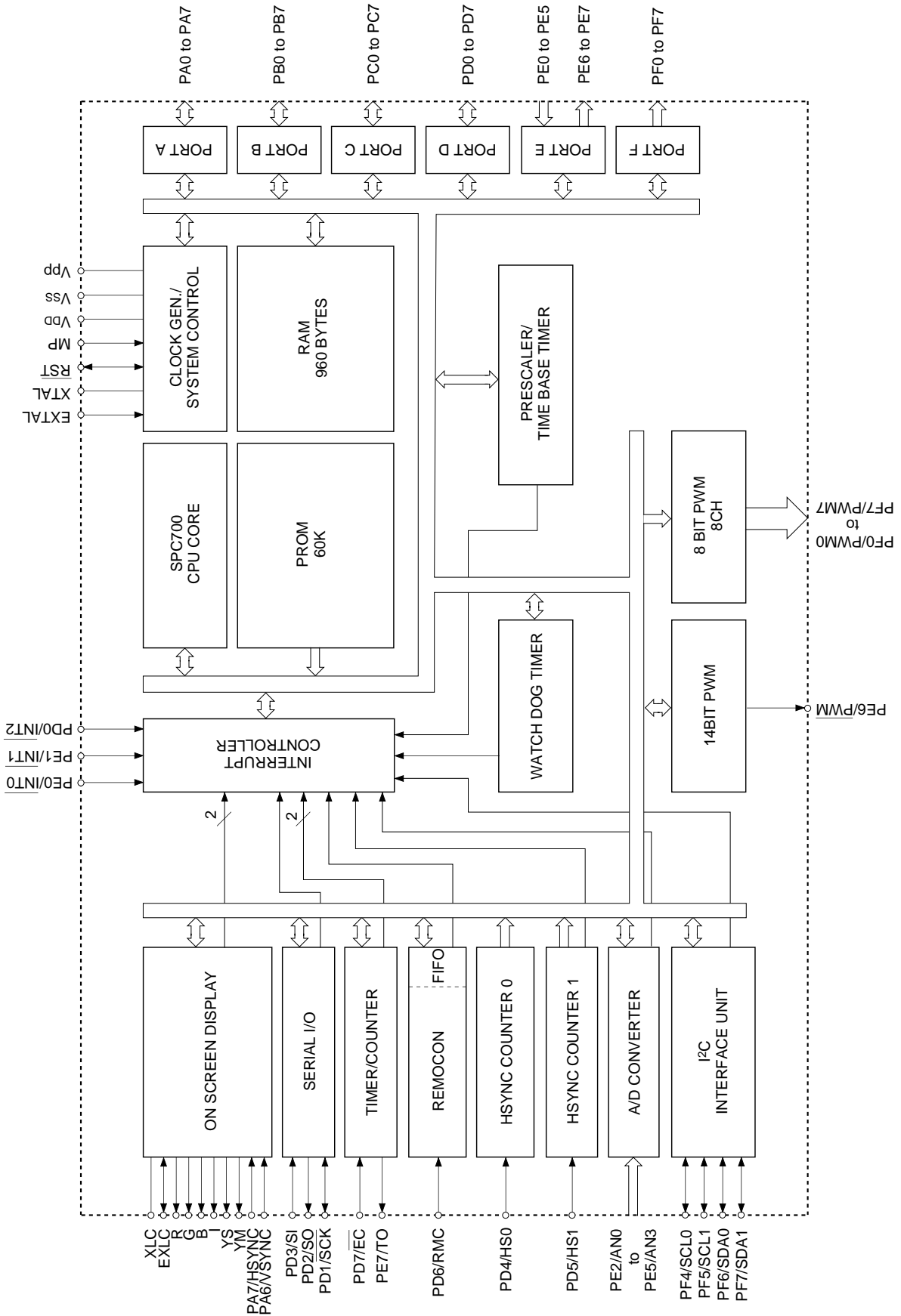
Silicon gate CMOS IC

**Features**

- Instruction set which supports a wide array of data types-213 types of instructions which include 16-bit calculations, multiplication and division arithmetic, and boolean operations.
- Minimum instruction cycle      0.5µs/8MHz
- On-chip PROM                      60K bytes (For program)  
   10K bytes (For OSD)
- On-chip RAM                        960 bytes
- On-screen display function    12 × 18 dots, 384 types, 12lines of 32 characters  
   Black frame output, half blanking, shadow, background color on full screen  
   Double scanning mode supported includes jitter elimination circuit
- I<sup>2</sup>C bus interface
- 14-bit PWM output, 8-bit PWM output (8 channels)
- Remote control receiver circuit
- 8-bit A/D converter (4 channels, 20µs conversion time/4MHz, 8MHz)
- HSYNC counter (2channels)
- Watchdog timer
- 8-bit synchronized serial I/O
- 8-bit timer, 8-bit timer/counter, 19-bit time-base timer
- General purpose input/output 32-line I/O (bit-selectable input/output), also 6-line input, 10-line output (internal 8-line Nch-O/D)
- Interrupts                            13 factors, 13 vectors, multiple interrupt possible
- Standby mode                      SLEEP
- Package                              64-pin plastic SDIP/QFP

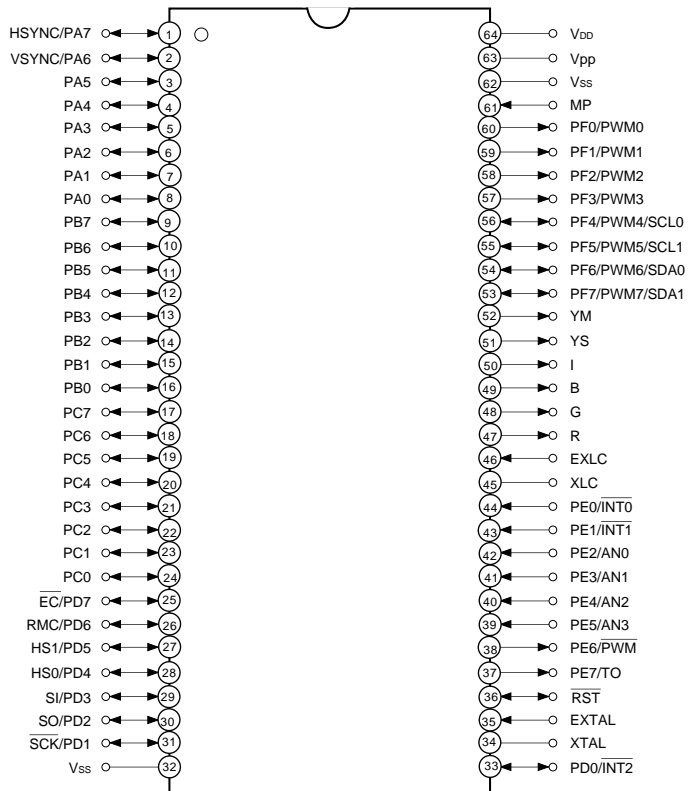
Purchase of Sony's I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specifications as defined by Philips.

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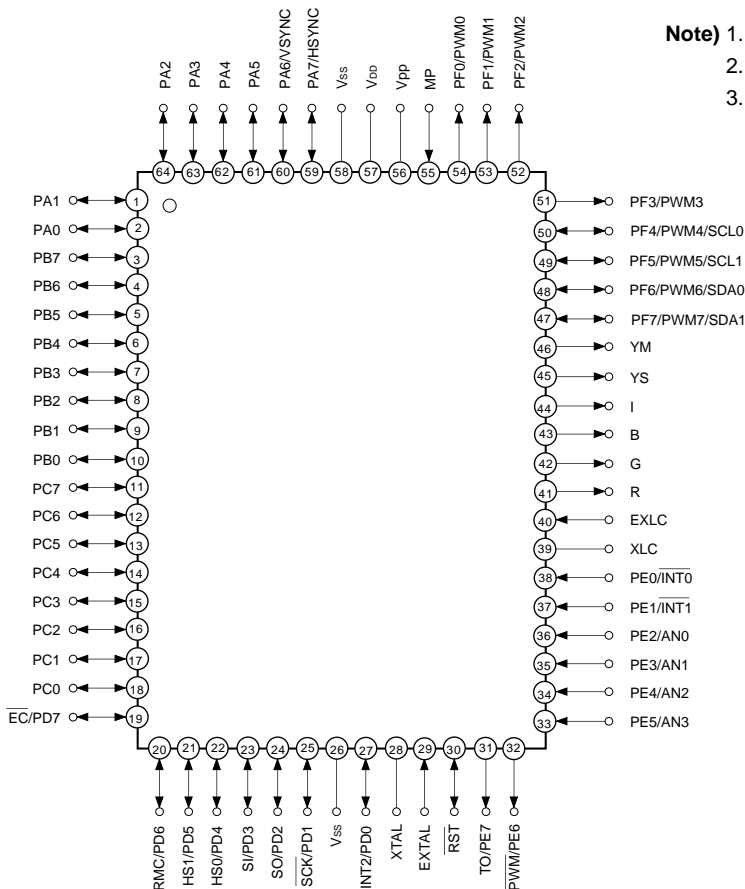


Block Diagram

Pin Assignment (Top View)



- Note)** 1. Vpp pin 63 must be connected to VDD.  
 2. Vss pins 32 and 62 must have a common GND.  
 3. MP pin 61 must be connected to GND.



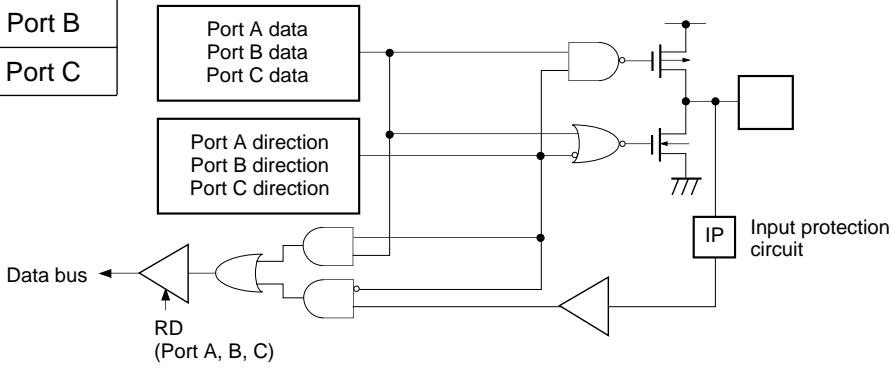
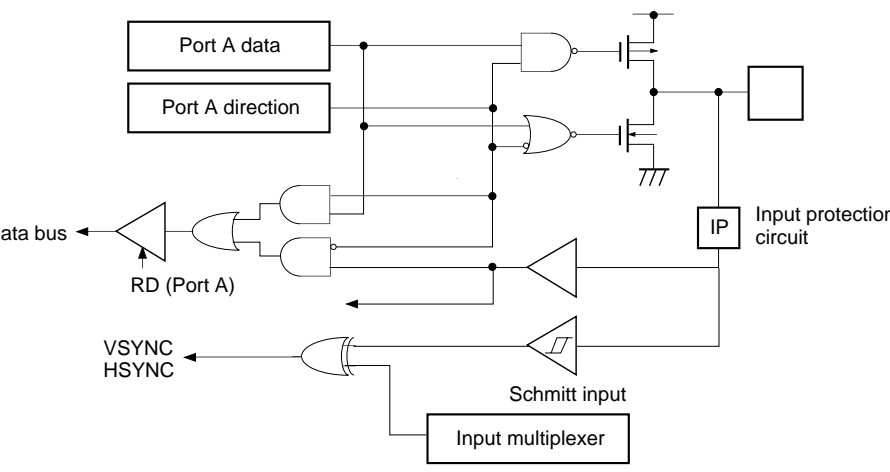
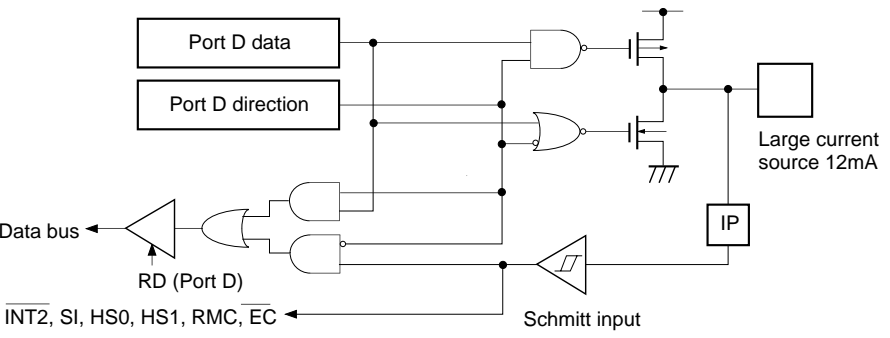
- Note)** 1. Vpp pin 56 must be connected to VDD.  
 2. Vss pins 26 and 58 must have a common GND.  
 3. MP pin 55 must be connected to GND.

**Pin Functions**

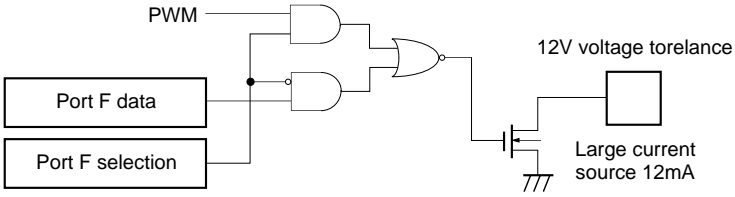
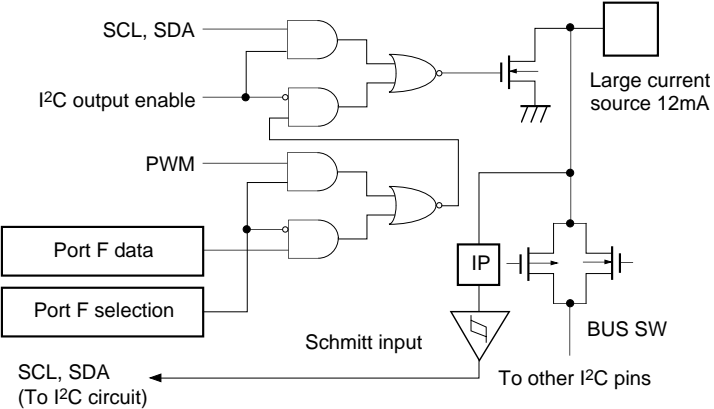
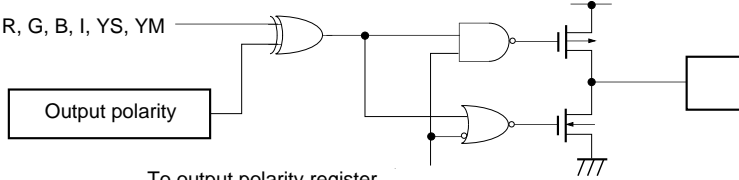
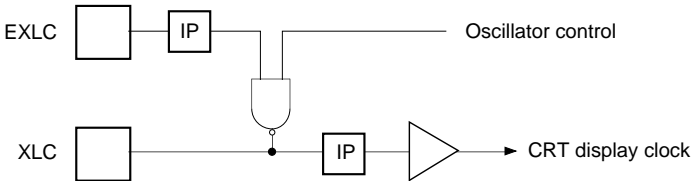
Pin Name	I/O	Function	
PA0 to PA5	I/O	(Port A) Single bit selectable 8-bit port.	
PA6/VSYNC	I/O/Input	(8 lines)	CRT display vertical synchronization signal input pin.
PA7/HSYNC	I/O/Input		CRT display horizontal synchronization signal input pin.
PB0 to PB7	I/O	(Port B) Single bit selectable 8-bit port. (8 lines)	
PC0 to PC7	I/O	(Port C) Single bit selectable 8-bit port. (8 lines)	
PD0/ $\overline{\text{INT2}}$	I/O/Input	(Port D) Single bit selectable 8-bit port. 12mA sink current drive possible. (8 lines)	Input pin for external interrupt request. Active on falling edge.
PD1/ $\overline{\text{SCK}}$	I/O/I/O		Serial clock pin.
PD2/SO	I/O/Output		Serial data output pin.
PD3/SI	I/O/Input		Serial data input pin.
PD4/HS0	I/O/Input		HSYNC counter (CH0) input pin.
PD5/HS1	I/O/Input		HSYNC counter (CH1) input pin.
PD6/RMC	I/O/Input		Remote control receiver circuit input pin.
PD7/ $\overline{\text{EC}}$	I/O/Input		External event timer/counter input pin.
PE0/ $\overline{\text{INT0}}$ PE1/ $\overline{\text{INT1}}$	Input/Input	(Port E) 8-bit port, lower 6 bits for input, upper 2 bits for output. (8 lines)	Input pin for external interrupt request. Active falling edge. (2 lines)
PE2/AN0 to PE5/AN3	Input/Input		Analog input pin for A/D converter. (4 lines)
PE6/ $\overline{\text{PWM}}$	Output/Output		14-bit PWM output pin. (CMOS output)
PE7/TO	Output/Output		Square wave output for timer 1. (50% duty cycle)
PF0/PWM0 to PF3/PWM3	Output/Output	(Port F) 8-bit output port with large current (12mA) N-ch open drain output. Lower 4 bits middle voltage tolerance (12V), upper 4 bits 5V suppression. (8 lines)	8-bit PWM output pin. (8-lines)
PF4/PWM4/ SCL0 PF5/PWM5/ SCL1	Output/Output/ I/O		I <sup>2</sup> C bus interface transfer clock I/O pin.
PF6/PWM6/ SDA0 PF7/PWM7/ SDA1	Output/Output/ I/O		I <sup>2</sup> C bus interface transfer data I/O pin.
R, G, B, I, YS, YM	Output	CRT display 6-bit output pin.	

Pin Name	I/O	Function
EXLC	Input	CRT display clock oscillator I/O pin. Oscillator frequency is determined external L, C circuit.
XLC	Output	
EXTAL	Input	System clock oscillator crystal connection pin. When using an external clock, input to EXTAL pin and leave XTAL pin open.
XTAL	Output	
$\overline{\text{RST}}$	I/O	"L" level active system reset. This pin also acts as an I/O pin during power up. While internal power-on reset function is talking place a "L" level is output.
MP	Input	Test mode input pin. Must be connected to GND.
Vpp		Positive power supply pin for incorporated PROM writing. Under normal operating conditions, connect to V <sub>DD</sub> .
V <sub>DD</sub>		Positive supply voltage pin.
V <sub>SS</sub>		GND. Both V <sub>SS</sub> pins should be connected to common GND.

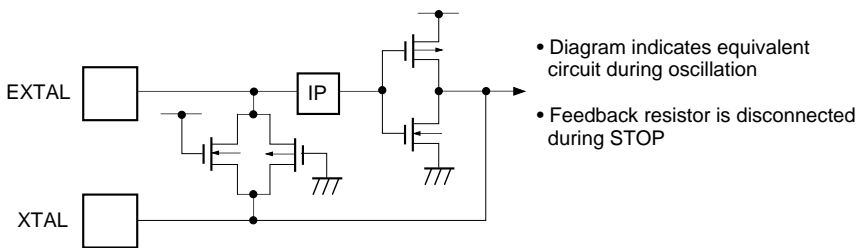
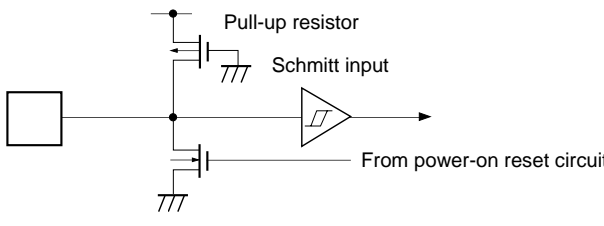
Pin Equivalent I/O Circuit

Pin	Circuit format	When reset
<p>PA0 to PA5 PB0 to PB7 PC0 to PC7</p> <p>22 lines</p>	<p>Port A Port B Port C</p>  <p>Port A data Port B data Port C data</p> <p>Port A direction Port B direction Port C direction</p> <p>Data bus</p> <p>RD (Port A, B, C)</p> <p>IP Input protection circuit</p>	<p>Hi-Z</p>
<p>PA6/VSYNC PA7/HSYNC</p> <p>2 lines</p>	<p>Port A</p>  <p>Port A data Port A direction</p> <p>Data bus</p> <p>RD (Port A)</p> <p>VSYNC HSYNC</p> <p>Schmitt input</p> <p>Input multiplexer</p> <p>IP Input protection circuit</p>	<p>Hi-Z</p>
<p>PD0/<math>\overline{\text{INT2}}</math> PD3/SI PD4/HS0 PD5/HS1</p> <p>PD6/RMC</p> <p>PD7/<math>\overline{\text{EC}}</math></p> <p>6 lines</p>	<p>Port D</p>  <p>Port D data Port D direction</p> <p>Data bus</p> <p>RD (Port D)</p> <p><math>\overline{\text{INT2}}</math>, SI, HS0, HS1, RMC, <math>\overline{\text{EC}}</math></p> <p>Schmitt input</p> <p>IP</p> <p>Large current source 12mA</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PD1/<math>\overline{\text{SCK}}</math> PD2/<math>\overline{\text{SO}}</math></p> <p>2 lines</p>	<p>Port D</p>	<p>Hi-Z</p>
<p>PE0/<math>\overline{\text{INT0}}</math> PE1/<math>\overline{\text{INT1}}</math></p> <p>2 lines</p>	<p>Port E</p>	<p>Hi-Z</p>
<p>PE2/<math>\overline{\text{AN0}}</math> to PE5/<math>\overline{\text{AN3}}</math></p> <p>4 lines</p>	<p>Port E</p>	<p>Hi-Z</p>
<p>PE6/<math>\overline{\text{PWM}}</math> PE7/<math>\overline{\text{TO}}</math></p> <p>2 lines</p>	<p>Port E</p>	<p>H level</p>

Pin	Circuit format	When reset
<p>PF0/PWM0 to PF3/PWM3</p> <p>4 lines</p>	<p>Port F</p> 	<p>Hi-Z</p>
<p>PF4/PWM4/ SCL0 PF5/PWM5/ SCL1 PF6/PWM6/ SDA0 PF7/PWM7/ SDA1</p> <p>4 lines</p>	<p>Port F</p> 	<p>Hi-Z</p>
<p>R G B I YS YM</p> <p>6 lines</p>	<p>R, G, B, I, YS, YM</p>  <p>To output polarity register Writing data to port register brings output from high impedance to active</p>	<p>Hi-Z</p>
<p>EXLC XLC</p> <p>2 lines</p>	<p>EXLC</p> 	<p>Oscillation halted</p>



Pin	Circuit format	When reset
<p>EXTAL XTAL</p> <p>2 lines</p>	 <ul style="list-style-type: none"> <li>• Diagram indicates equivalent circuit during oscillation</li> <li>• Feedback resistor is disconnected during STOP</li> </ul>	<p>Oscillation</p>
<p><math>\overline{\text{RST}}</math></p> <p>1 line</p>	 <p>Pull-up resistor</p> <p>Schmitt input</p> <p>From power-on reset circuit</p>	<p>L level</p>

## Absolute Maximum Ratings

(V<sub>SS</sub> = 0V)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V	
	V <sub>pp</sub>	-0.3 to +13.0	V	Incorporated PROM
Input voltage	V <sub>IN</sub>	-0.3 to +7.0* <sup>1</sup>	V	
Output voltage	V <sub>OUT</sub>	-0.3 to +7.0* <sup>1</sup>	V	
Medium voltage tolerance output voltage	V <sub>OUTP</sub>	-0.3 to +15.0	V	Pins PF0 to PF3
High level output current	I <sub>OH</sub>	-5	mA	
High level total output current	∑I <sub>OH</sub>	-50	mA	Total of all output pins
Low level output current	I <sub>OL</sub>	15	mA	Excludes large current output
	I <sub>OLC</sub>	20	mA	Large current output* <sup>2</sup>
Low level total output current	∑I <sub>OL</sub>	130	mA	Total of all output pins
Operating temperature	T <sub>opr</sub>	-10 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	
Allowable power dissipation	P <sub>D</sub>	1000	mW	SDIP
		600	mW	QFP

\*<sup>1</sup> V<sub>IN</sub> and V<sub>OUT</sub> should not exceed V<sub>DD</sub> + 0.3V.

\*<sup>2</sup> The large current driver for the PD and PF ports is a N-ch transistor.

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

## Recommended Operating Conditions

(V<sub>SS</sub> = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V <sub>DD</sub>	4.5	5.5	V	Safe operating range
		3.5	5.5	V	Safe operating range for low speed data* <sup>1</sup>
		2.5	5.5	V	Safe operating range for data retention during STOP
	V <sub>pp</sub>	V <sub>pp</sub> = V <sub>DD</sub>		V	* <sup>5</sup>
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	I <sup>2</sup> C Schmitt input included* <sup>2</sup>
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	CMOS Schmitt input* <sup>3</sup>
	V <sub>IHEX</sub>	V <sub>DD</sub> - 0.4	V <sub>DD</sub> + 0.3	V	EXTAL pin* <sup>4</sup>
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	I <sup>2</sup> C Schmitt input included* <sup>2</sup>
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	CMOS Schmitt input* <sup>3</sup>
	V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL pin* <sup>4</sup>
Operating temperature	T <sub>opr</sub>	-10	+75	°C	

\*<sup>1</sup> Rating for 1/16 frequency mode and sleep mode.

\*<sup>2</sup> Normal input port (All pins PA, PB, PC, PE2 to PE5), PF4 to PF7 pins.

\*<sup>3</sup> Includes PD0/ $\overline{\text{INT2}}$ , PD1/ $\overline{\text{SCK}}$ , PD2, PD3/SI, PD4/HS0, PD5/HS1, PD6/RMC, PD7/ $\overline{\text{EC}}$ , PE0/ $\overline{\text{INT0}}$ , PE1/ $\overline{\text{INT1}}$ , HSYNC, VSYNC,  $\overline{\text{RST}}$  pins.

\*<sup>4</sup> Rating applies to external clock input only.

\*<sup>5</sup> V<sub>pp</sub> and V<sub>DD</sub> should be set to a same voltage.

DC Characteristics

(Ta = -10 to +75°C, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	VOH	PA to PD, PE6, PE7, R, G, B, I, YS, YM	VDD = 4.5V, IOH = -0.5mA	4.0			V
			VDD = 4.5V, IOH = -1.2mA	3.5			V
Low level output voltage	VOL	PA to PD, PE6, PE7, R, G, B, I, YS, YM, PF0 to PF3, RST	VDD = 4.5V, IOL = 1.8mA			0.4	V
			VDD = 4.5V, IOL = 3.6mA			0.6	V
		PD, PF	VDD = 4.5V, IOL = 12.0mA			1.5	V
		PF4 to PF7 (SCL0, SCL1, SDA0, SDA1)	VDD = 4.5V, IOL = 3.0mA			0.4	V
			VDD = 4.5V, IOL = 4.0mA			0.6	V
Input current	IiHE	EXTAL	VDD = 5.5V, VIH = 5.5V	0.5		40	μA
	IiHL		VDD = 5.5V, VIL = 0.4V	-0.5		-40	μA
	IiLR	RST	VDD = 5.5V, VIL = 0.4V	-1.5		-400	μA
I/O leakage current	IIZ	PA to PE, HSYNC, VSYNC, R, G, B, I, YS, YM	VDD = 5.5V, VI = 0, 5.5V			±10	μA
Open drain output leak current (N-ch Tr off case)	ILOH	PF0 to PF3	VDD = 5.5V, VOH = 12.0V			50	μA
		PF4 to PF7	VDD = 5.5V, VOH = 5.5V			10	μA
I <sup>2</sup> C bus switch connection impedance (Output Tr off case)	RBS	SCL0: SCL1 SDA0: SDA1	VDD = 4.5V VSCL0 = VSCL1 = 2.25V VSDA0 = VSDA1 = 2.25V			120	Ω
Supply current	IDD	VDD*1	Operating mode (1/2, clock rate) 8MHz crystal oscillator (C1 = C2 = 22pF) All output pins open		20	35	mA
	IDDSL				1.0	3	mA
	IDDST				—	—	—
Input capacitance	CIN	Pins other than VDD and Vss	1MHz clock 0V for non-measurement pins		10	20	pF

\*1 Rating applies only if OSD oscillator is halted.

\*2 This device does not enter in the stop mode.

**AC Characteristics**

(1) Clock timing

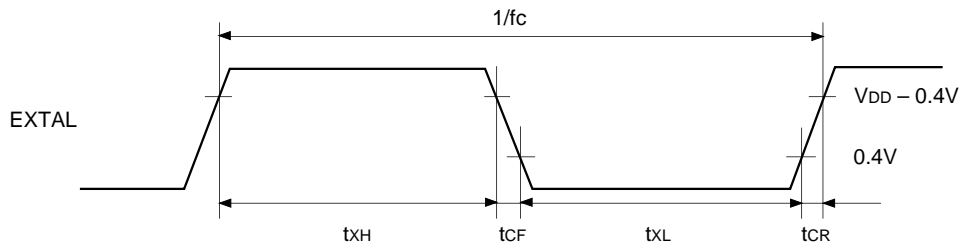
( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Item	System	Pin	Condition	Min.	Max.	Unit
System clock frequency	$f_c$	XTAL EXTAL	Fig. 1, Fig. 2	3.5	9	MHz
System clock input pulse width	$t_{XL}$ , $t_{XH}$	EXTAL	Fig. 1, Fig. 2 External clock drive	50		ns
System clock rise and fall times	$t_{CR}$ , $t_{CF}$	EXTAL	Fig 1, Fig 2 External clock drive		200	ns
Event counter input clock pulse width	$t_{EH}$ , $t_{EL}$	$\overline{\text{EC}}$	Fig. 3	$t_{\text{sys}} + 50^*$		ns
Event counter input clock rise and fall times	$t_{ER}$ , $t_{EF}$	$\overline{\text{EC}}$	Fig. 3		20	ms

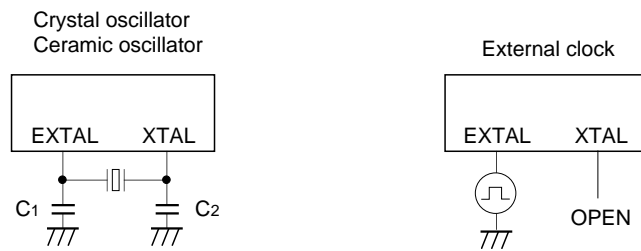
\*  $t_{\text{sys}}$  indicates one of three values according to the contents of the clock control register. (For CPU clock selection.)

$t_{\text{sys}}$  (ns) =  $2000/f_c$  (Upper 2 bits = "00"),  $4000/f_c$  (Upper 2 bits = "01"),  $16000/f_c$  (Upper 2 bits = "11")

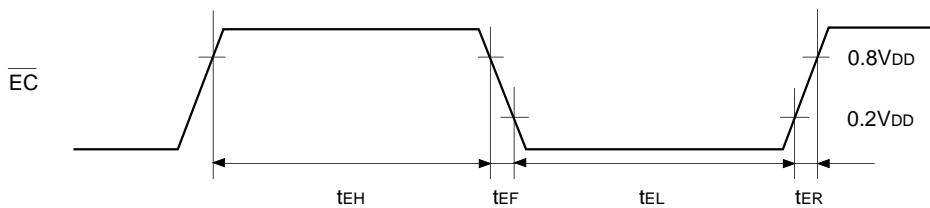
**Fig. 1. Clock timing**



**Fig. 2. Clock applied condition**



**Fig. 3. Event count clock timing**



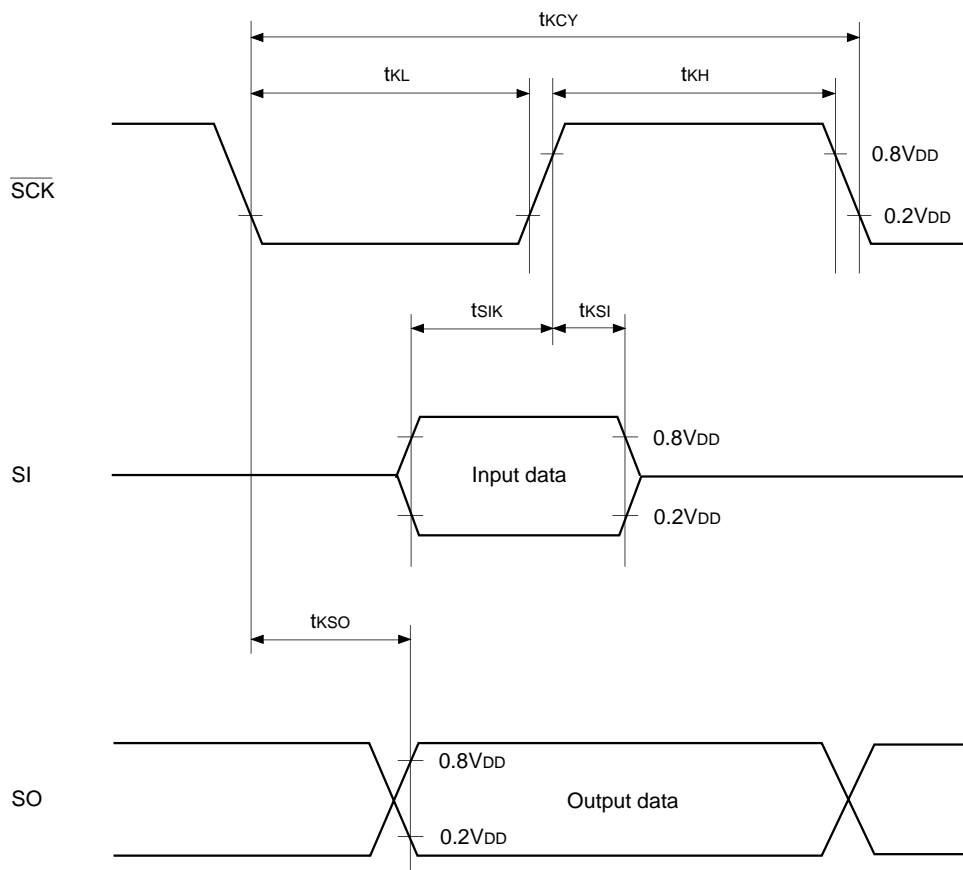
(2) Serial transfer

( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Item	System	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK}}$ cycle time	$t_{\text{KCY}}$	$\overline{\text{SCK}}$	Input mode	1000		ns
			Output mode	$8000/f_c$		ns
$\overline{\text{SCK}}$ high and low level widths	$t_{\text{KH}}$ $t_{\text{KL}}$	$\overline{\text{SCK}}$	$\overline{\text{SCK}}$ input mode	400		ns
			$\overline{\text{SCK}}$ output mode	$4000/f_c - 50$		ns
SI input set-up time (referenced to $\overline{\text{SCK}} \uparrow$ )	$t_{\text{SIK}}$	SI	$\overline{\text{SCK}}$ input mode	100		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI input hold time (referenced to $\overline{\text{SCK}} \uparrow$ )	$t_{\text{KSI}}$	SI	$\overline{\text{SCK}}$ input mode	200		ns
			$\overline{\text{SCK}}$ output mode	100		ns
$\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time	$t_{\text{KSO}}$	SO	$\overline{\text{SCK}}$ input mode		200	ns
			$\overline{\text{SCK}}$ output mode		100	ns

**Note)** For  $\overline{\text{SCK}}$  output mode, in addition to output delay time SO capacitance must be  $50\text{pF} + 1\text{TTL}$ .

Fig. 4. Serial transfer timing



(3) Interrupt, Reset input (Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interrupt high and low level widths	t <sub>IH</sub> t <sub>IL</sub>	$\overline{\text{INT0}}$ to $\overline{\text{INT2}}$		1		μs
Reset input low level width	t <sub>RSL</sub>	$\overline{\text{RST}}$		8/fc		μs

Fig. 5. Interrupt input timing

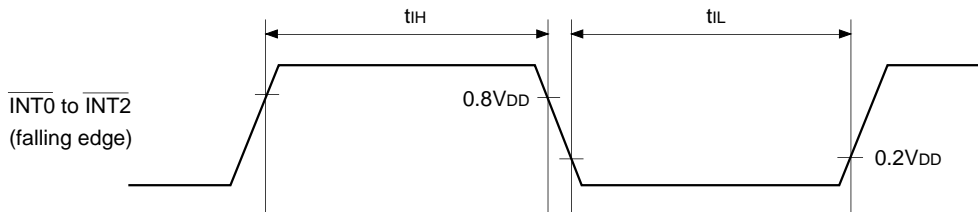
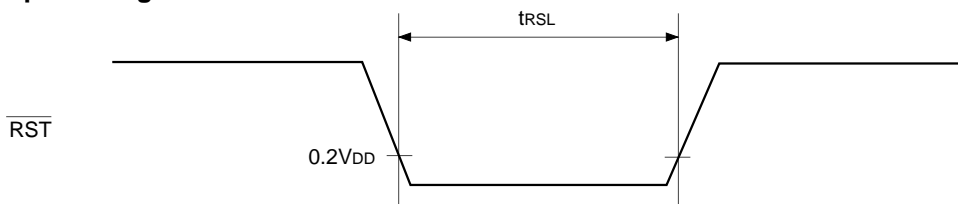


Fig. 6.  $\overline{\text{RST}}$  input timing

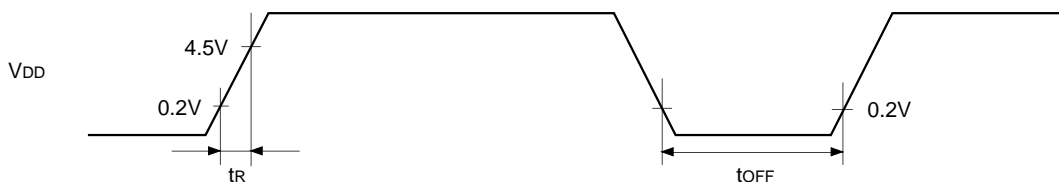


(4) Power-on reset

Power on reset (Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rise time	t <sub>R</sub>	V <sub>DD</sub>	Power-on reset	0.05	50	ms
Power supply cutt-off time	t <sub>OFF</sub>		Repeated power-on reset	1		ms

Fig. 7. Power-on reset



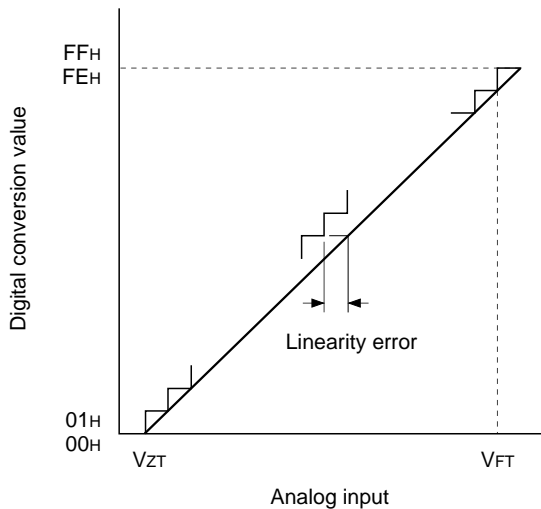
Take care when turning on power.

(5) A/D converter characteristics

( $T_a = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error						$\pm 1$	LSB
Zero transition voltage	$V_{ZT}^{*1}$		$T_a = 25^\circ\text{C}$ $V_{DD} = 5.0\text{V}$ $V_{SS} = 0\text{V}$	-10	10	70	mV
Full-scale transition voltage	$V_{FT}^{*2}$			4910	4970	5030	mV
Conversion time	$t_{CONV}$			$160/f_{ADC}^{*3}$			$\mu\text{s}$
Sampling time	$t_{SAMP}$			$12/f_{ADC}^{*3}$			$\mu\text{s}$
Analog input voltage	$V_{IAN}$	AN0 to AN3		0		$V_{DD}$	V

Fig. 8. Definitions for A/D converter terms



- \*1  $V_{ZT}$ : Digital conversion values change between  $00\text{H} \leftrightarrow 01\text{H}$ .
- \*2  $V_{FT}$ : Digital conversion values change between  $0\text{EH} \leftrightarrow 0\text{FH}$ .
- \*3  $f_{ADC}$  indicates the below values due to the bit6 (CKS) of A/D control register (address:  $00\text{F6H}$ ) and the Bit 7 (PCK1) and Bit 6 (PCK0) of clock control register (address:  $00\text{FEH}$ )

PCK1, 0	CKS	
	0 ( $\phi/2$ selection)	1 ( $\phi/2$ selection)
00 ( $\phi = f_{EX}/2$ )	$f_{ADC} = f_c/2$	$f_{ADC} = f_c$
01 ( $\phi = f_{EX}/4$ )	$f_{ADC} = f_c/4$	$f_{ADC} = f_c/2$
11 ( $\phi = f_{EX}/16$ )	$f_{ADC} = f_c/16$	$f_{ADC} = f_c/8$

(6) I<sup>2</sup>C bus timing

(Ta = -10 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
SCL clock frequency	f <sub>SCL</sub>	SCL		0	100	kHz
Bus free time before starting transfer	t <sub>BUF</sub>	SDA, SCL		4.7		μs
Hold time for starting transfer	t <sub>HD; STA</sub>	SDA, SCL		4.0		μs
Clock low level width	t <sub>LOW</sub>	SCL		4.7		μs
Clock high level width	t <sub>HIGH</sub>	SCL		4.0		μs
Set-up time for repeated transfers	t <sub>SU; STA</sub>	SDA, SCL		4.7		μs
Data hold time	t <sub>HD; DAT</sub>	SDA, SCL		0*		μs
Data set-up time	t <sub>SU; DAT</sub>	SDA, SCL		0.25		μs
SDA, SCL rise time	t <sub>R</sub>	SDA, SCL			1	μs
SDA, SCL fall time	t <sub>F</sub>	SDA, SCL			0.3	μs
Set-up time for transfer completion	t <sub>SU; STO</sub>	SDA, SCL		4.7		μs

\* Since SCL rise time (max: 300ns) is not considered part of data hold time, allow at least 300ns.

Fig. 9. I<sup>2</sup>C bus transfer data timing

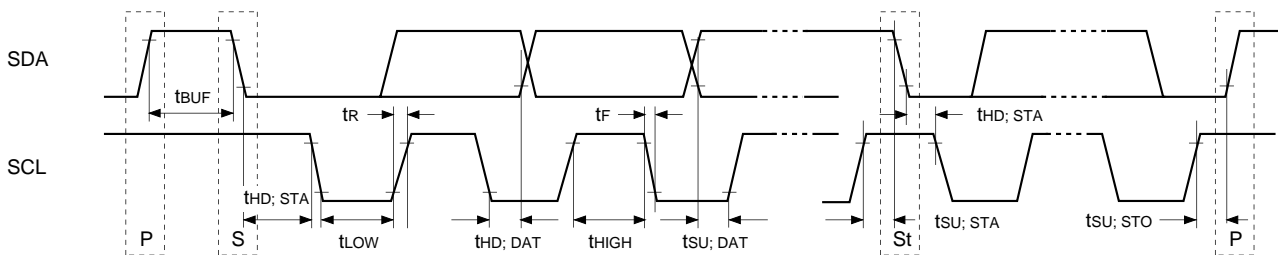
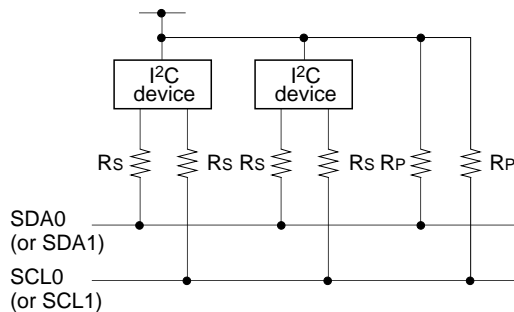


Fig. 10. I<sup>2</sup>C device suggested circuit



- A pull-up resistor must be connected to SDA0 (or SDA1), and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (Rs = 300Ω or less) can be used to reduce spike noise caused by CRT flashover.



(7) OSD (On Screen Display) timing

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Condiiton	Shadow Existent		Shadow Non-existent		Unit
				Min.	Max.	Min.	Max.	
OSD clock frequency	fosc	EXLC XLC	Fig. 12	4	7* <sup>1</sup> 14* <sup>2</sup>	4	11* <sup>1</sup> 16* <sup>2</sup>	MHz
HSYNC pulse width	t <sub>HWD</sub>	HSYNC	Fig. 11	1.2		1.2		μs
HSYNC afterwrite rise and fall times	t <sub>HCG</sub>	HSYNC	Fig. 11		200		200	ns
VSYNC afterwrite rise and fall times	t <sub>VCG</sub>	VSYNC	Fig. 11		1.0		1.0	μs

\*1 Oscillator clock at 4MHz operation

\*2 Oscillator clock at 8MHz operation

Fig. 11. OSD timing

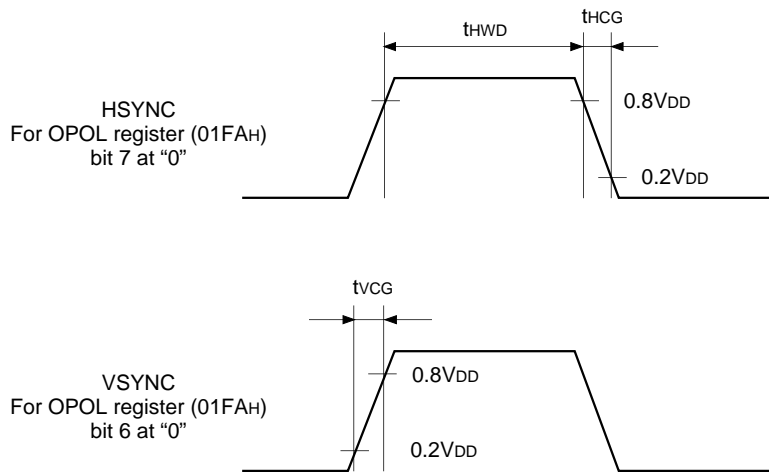
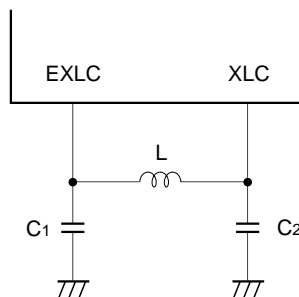


Fig. 12. LC oscillator circuit connection



Supplement

Fig. 13. SPC700 Series recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit Example
MURATA MFG CO., LTD.	CSA4.00MG	4.00	30	30	0	(i)
	CSA4.19MG	4.19				
	CSA8.00MTZ	8.00				
	CST4.00MGW*	4.00				(ii)
	CST4.19MGW*	4.19				
	CST8.00MTW*	8.00				
RIVER ELETEC CO., LTD.	HC-49/U03	4.00	12	12	0	(i)
		4.19				
		8.00				
KINSEKI LTD.	HC-49/U(-S)	4.00	27	27	0	(i)
		4.19				
		8.00				

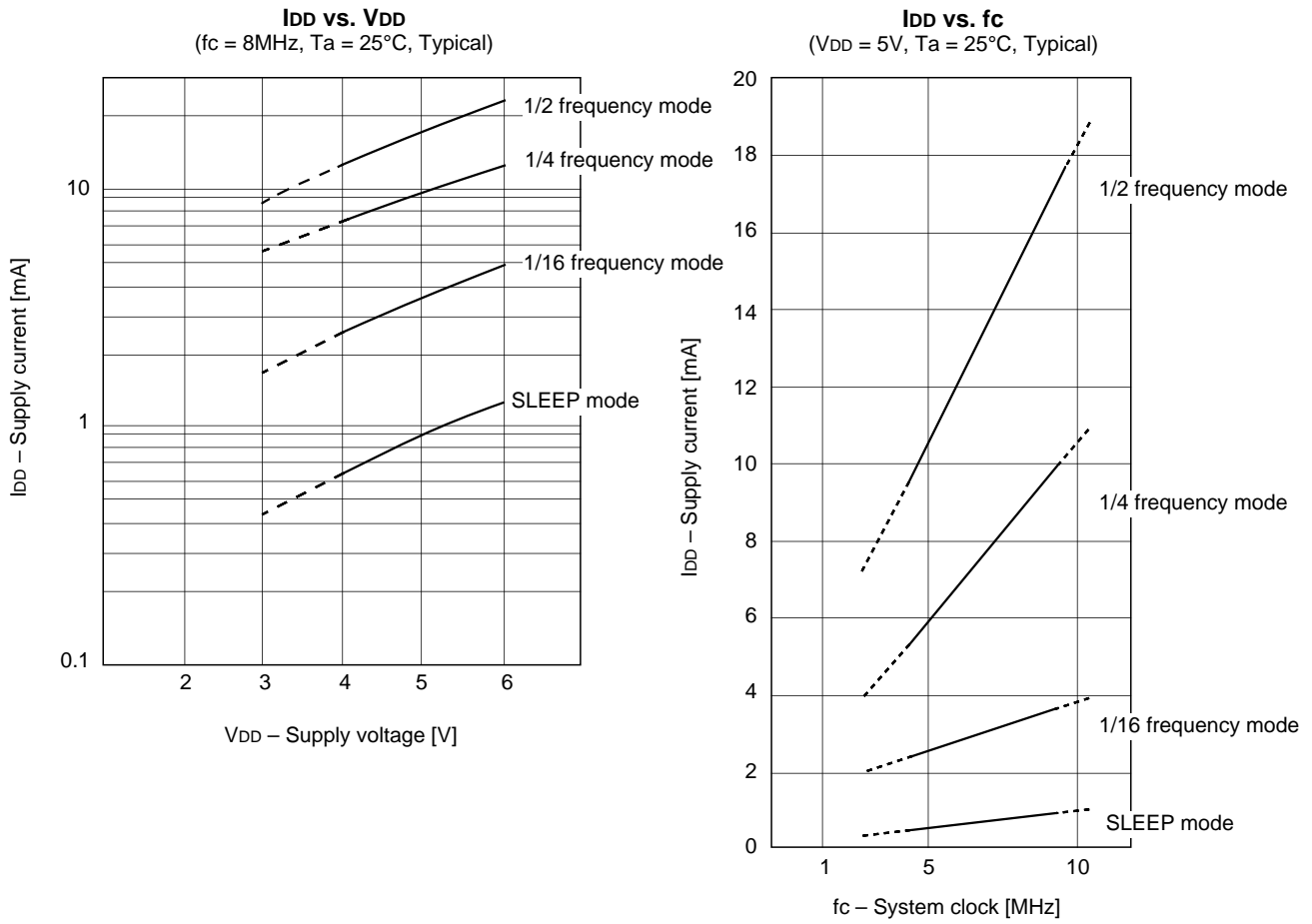
\* Indicates types with on-chip grounding capacitors (C1 and C2).

Product List

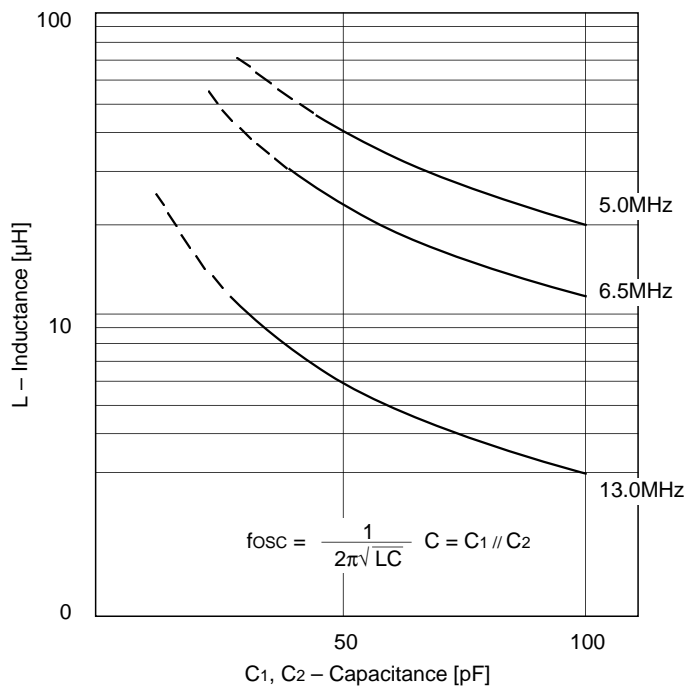
Option item	Mask product	CXP854P60S-1-□□□ CXP854P60Q-1-□□□
Package	64-pin plastic SDIP/QFP	64-pin plastic SDIP/QFP
Program ROM capacitance	52K/60K byte	PROM 60K byte
Reset pin pull-up resistor	Existent/Non-existent	Existent
Power-on reset circuit	Existent/Non-existent	Existent
Font data	User specified	User specified (PROM)*

\* The font data for the one-time PROM version is operated in the same way as the program writing.

Fig. 14. Characteristics curves



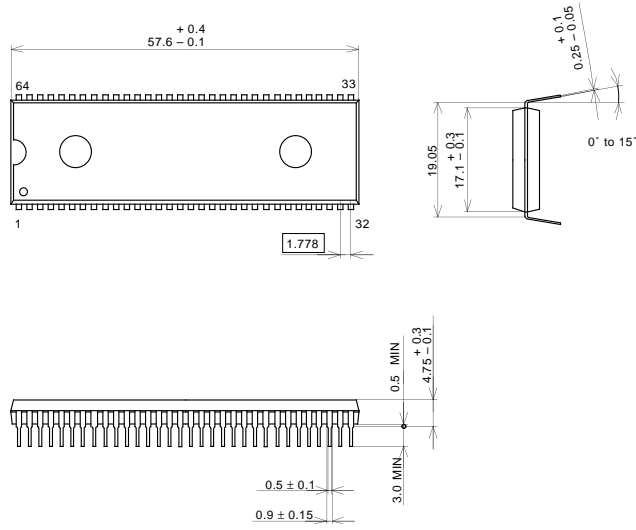
Parameter Curve for OSD Oscillator L vs. C  
(Analytically calculated value)



Package Outline

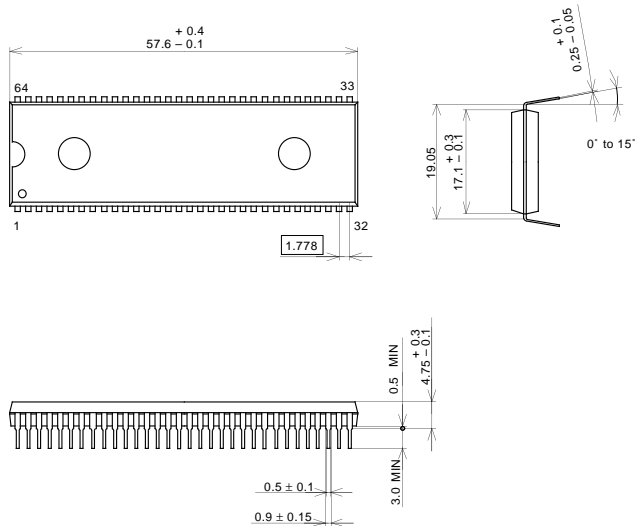
Unit: mm

64PIN SDIP (PLASTIC)



SONY CODE		SDIP-64P-01	
EIAJ CODE	P-SDIP64-17.1x57.6-1.778	PACKAGE MATERIAL	EPOXY RESIN
JEDEC CODE		LEAD TREATMENT	SOLDER PLATING
		LEAD MATERIAL	42/COPPER ALLOY
		PACKAGE MASS	8.6g

64PIN SDIP (PLASTIC)



SONY CODE		SDIP-64P-01	
EIAJ CODE	P-SDIP64-17.1x57.6-1.778	PACKAGE MATERIAL	EPOXY RESIN
JEDEC CODE		LEAD TREATMENT	SOLDER PLATING
		LEAD MATERIAL	42/COPPER ALLOY
		PACKAGE MASS	8.6g

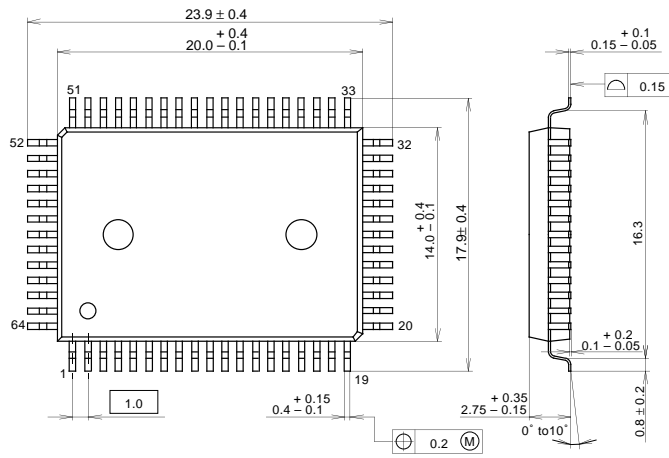
LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18 $\mu$ m

Package Outline

Unit: mm

64PIN QFP (PLASTIC)

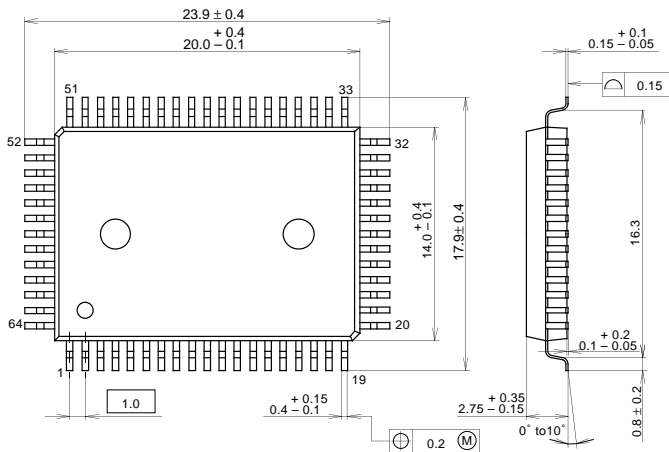


PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	P-QFP64-14x20-1.0
JEDEC CODE	—

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g

64PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	P-QFP64-14x20-1.0
JEDEC CODE	—

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18μm

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