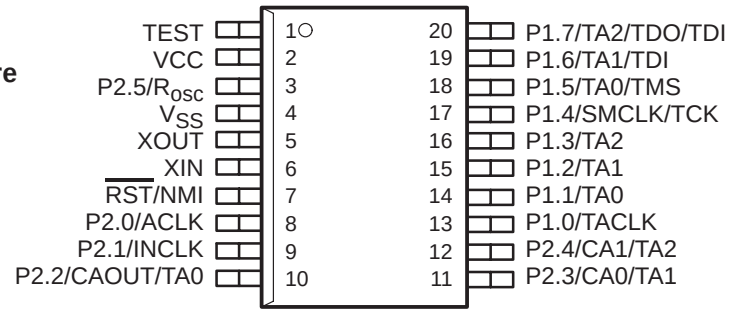
- **Low Supply Voltage Range 1.8 V – 3.6 V**
- **Ultralow-Power Consumption**
  Low Operation Current,
  1.3 μA at 4 kHz, 2.2 V
  160 μA at 1 MHz, 2.2 V
- **Five Power Saving Modes:**
  (Standby Mode: 0.8 μA,
  RAM Retention Off Mode: 0.1 μA)
- **Wake-Up From Standby Mode in 6 μs**
- **16-Bit RISC Architecture, 125 ns Instruction Cycle Time**
- **Basic Clock Module Configurations:**
  - **Various Internal Resistors**
  - **Single External Resistor**
  - **32 kHz Crystal**
  - **High Frequency Crystal**
  - **Resonator**
  - **External Clock Source**
- **16-Bit Timer With Three Capture/Compare Registers**
- **Slope A/D Converter With External Components**
- **On-Chip Comparator for Analog Signal Compare Function or Slope A/D Conversion**
- **Serial Onboard Programming**
- **Programmable Code Protection by Security Fuse (C11x1 Only)**
- **Family Members Include:**
  MSP430C1111: 2KB ROM, 128B RAM
  MSP430C1121: 4KB ROM, 256B RAM
  MSP430F1101: 1KB + 128B Flash Memory (MTP†), 128B RAM
  MSP430F1121: 4KB + 256B Flash Memory (MTP†), 256B RAM
- **Available in a 20-Pin Plastic Small-Outline Wide Body (SOWB) Package and 20-Pin Plastic Thin Shrink Small-Outline Package (TSSOP)**

DW OR PW PACKAGE
(TOP VIEW)



description

The Texas Instruments MSP430 series is an ultralow-power microcontroller family consisting of several devices featuring different sets of modules targeted to various applications. The microcontroller is designed to be battery operated for an extended-application lifetime. With 16-bit RISC architecture, 16 bit integrated registers on the CPU, and a constant generator, the MSP430 achieves maximum code efficiency. The digitally-controlled oscillator provides fast wake-up from all low-power modes to active mode in less than 6 μs.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and then process the data and display them or transmit them to a host system. Stand alone RF sensor front end is another area of application. The I/O port inputs provide single slope A/D conversion capability on resistive sensors. The MSP430x11x series is an ultralow-power mixed signal microcontroller with a built in 16-bit timer and fourteen I/O pins. The MSP430x11x1 family adds a versatile analog comparator.

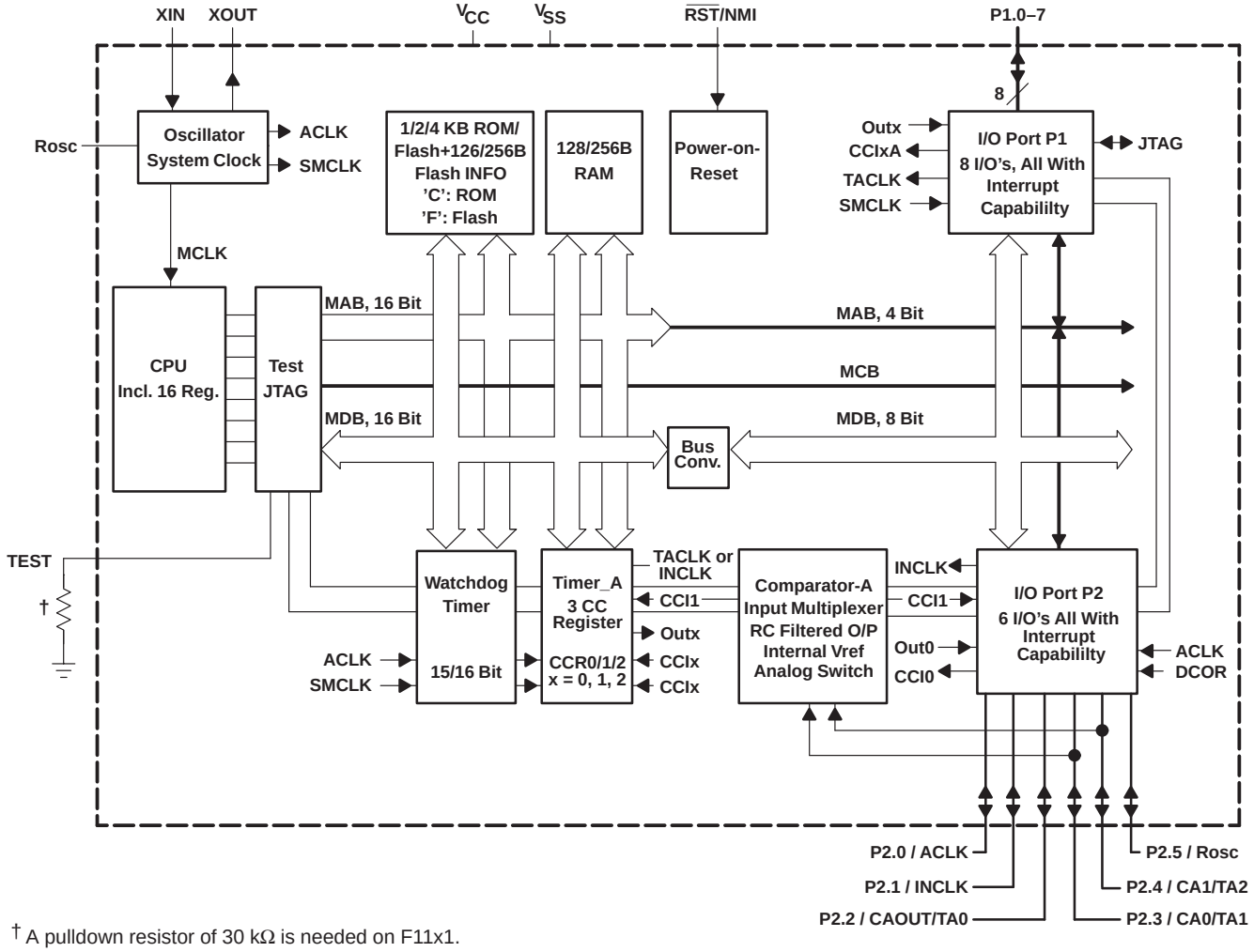
The flash memory provides added flexibility of in-system programming and data storage without significantly increasing the current consumption of the device. The programming voltage is generated on-chip, thereby alleviating the need for an additional supply, and even allowing for reprogramming of battery-operated systems.

† MTP = Multiple Time Programmable

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	PLASTIC 20-PIN SOWB (DW)	PLASTIC 20-PIN TSSOP (PW)
–40°C to 85°C	MSP430C1111IDW MSP430C1121IDW MSP430F1101IDW MSP430F1121IDW	MSP430F1101IPW MSP430F1121IPW

functional block diagram



† A pulldown resistor of 30 kΩ is needed on F11x1.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
P1.0/TACLK	13	I/O	General-purpose digital I/O pin/Timer_A, clock signal TACLK input
P1.1/TA0	14	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output
P1.2/TA1	15	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	16	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK/TCK	17	I/O	General-purpose digital I/O pin/SMCLK signal output/test clock, input terminal for device programming and test
P1.5/TA0/TMS	18	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output/test mode select, input terminal for device programming and test
P1.6/TA1/TDI	19	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output/test data input terminal
P1.7/TA2/TDO/TDI†	20	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output/test data output terminal or data input during programming
P2.0/ACLK	8	I/O	General-purpose digital I/O pin/ACLK output
P2.1/INCLK	9	I/O	General-purpose digital I/O pin/Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0	10	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0B input/comparator_A, output
P2.3/CA0/TA1	11	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output/comparator_A, input
P2.4/CA1/TA2	12	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output/comparator_A, input
P2.5/R_{OSC}	3	I/O	General-purpose digital I/O pin/Input for external resistor that defines the DCO nominal frequency
$\overline{RST}$/NMI	7	I	Reset or nonmaskable interrupt input
TEST	1	I	Select of test mode for JTAG pins on Port1. Must be tied low with less than 30 kΩ (F11x1).
VCC	2		Supply voltage
V_{SS}	4		Ground reference
XIN	6	I	Input terminal of crystal oscillator
XOUT	5	I/O	Output terminal of crystal oscillator

† TDO or TDI is selected via JTAG instruction.

short-form description

processing unit

The processing unit is based on a consistent, and orthogonally-designed CPU and instruction set. This design structure results in a RISC-like architecture, highly transparent to the application development, and noted for its programming simplicity. All operations other than program-flow instructions are consequently performed as register operations in conjunction with seven addressing modes for source, and four modes for destination operands.

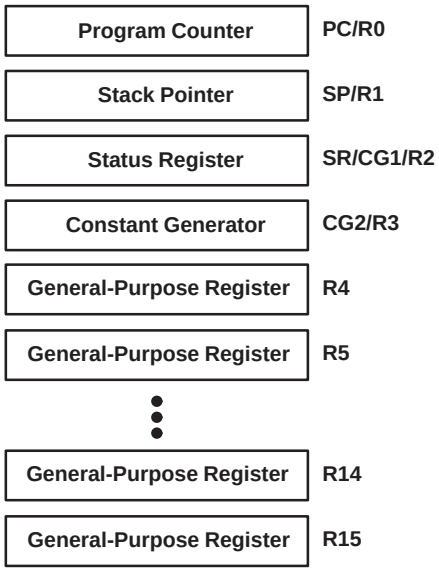
short-form description (continued)

CPU

All sixteen registers are located inside the CPU, providing reduced instruction execution time. This reduces a register-register operation execution time to one cycle of the processor.

Four registers are reserved for special use as a program counter, a stack pointer, a status register, and a constant generator. The remaining twelve registers are available as general-purpose registers.

Peripherals are connected to the CPU using a data address and control buses and can be handled easily with all instructions for memory manipulation.



instruction set

The instructions set for this register-register architecture provides a powerful and easy-to-use assembly language. The instruction set consists of 51 instructions with three formats and seven addressing modes. Table 1 provides a summation and example of the three types of instruction formats; the addressing modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD	R4, R5	R4 + R5 → R5
Single operands, destination only	e.g. CALL	R8	PC → (TOS), R8 → PC
Relative jump, un-/conditional	e.g. JNE		Jump-on equal bit = 0

Most instructions can operate on both word and byte data. Byte operations are identified by the suffix B.

Examples:	Instructions for word operation		Instructions for byte operation	
	MOV	EDE,TONI	MOV.B	EDE,TONI
	ADD	#235h,&MEM	ADD.B	#35h,&MEM
	PUSH	R5	PUSH.B	R5
	SWPB	R5	—	

Table 2. Address Mode Descriptions

ADDRESS MODE	s	d	SYNTAX	EXAMPLE	OPERATION
Register	√	√	MOV Rs, Rd	MOV R10, R11	R10 → R11
Indexed	√	√	MOV X(Rn), Y(Rm)	MOV 2(R5), 6(R6)	M(2 + R5) → M(6 + R6)
Symbolic (PC relative)	√	√	MOV EDE, TONI		M(EDE) → M(TONI)
Absolute	√	√	MOV &MEM, &TCDAT		M(MEM) → M(TCDAT)
Indirect	√		MOV @Rn, Y(Rm)	MOV @R10, Tab(R6)	M(R10) → M(Tab + R6)
Indirect autoincrement	√		MOV @Rn+, RM	MOV @R10+, R11	M(R10) → R11, R10 + 2 → R10
Immediate	√		MOV #X, TONI	MOV #45, TONI	#45 → M(TONI)

NOTE: s = source d = destination Rs/Rd = source register/destination register Rn = register number

instruction set (continued)

Computed branches (BR) and subroutine calls (CALL) instructions use the same addressing modes as the other instructions. These addressing modes provide *indirect* addressing, ideally suited for computed branches and calls. The full use of this programming capability permits a program structure different from conventional 8- and 16-bit controllers. For example, numerous routines can easily be designed to deal with pointers and stacks instead of using flag type programs for flow control.

operation modes and interrupts

The MSP430 operating modes support various advanced requirements for ultralow-power and ultralow energy consumption. This is achieved by the intelligent management of the operations during the different module operation modes and CPU states. The advanced requirements are fully supported during interrupt event handling. An interrupt event awakens the system from each of the various operating modes and returns with the *RETI* instruction to the mode that was selected before the interrupt event. The different requirements of the CPU and modules, which are driven by system cost and current consumption objectives, necessitate the use of different clock signals:

- Auxiliary clock ACLK (from LFXT1CLK/crystal's frequency), used by the peripheral modules
- Main system clock MCLK, used by the CPU and system
- Subsystem clock SMCLK, used by the peripheral modules

low-power consumption capabilities

The various operating modes are controlled by the software through controlling the operation of the internal clock system. This clock system provides many combinations of hardware and software capabilities to run the application with the lowest power consumption and with optimized system costs:

- Use the internal clock (DCO) generator without any external components.
- Select an external crystal or ceramic resonator for lowest frequency or cost.
- Select and activate the proper clock signals (LFXT1CLK and/or DCOCLK) and clock pre-divider function.
- Apply an external clock source.

Four of the control bits that influence the operation of the clock system and support fast turnon from low power operating modes are located in the status register SR. The four bits that control the CPU and the system clock generator are SCG1, SCG0, OscOff, and CPUOff:

status register R2

15 – 9	8	7	6	5	4	3	2	1	0
Reserved For Future Enhancements	V	SCG1	SCG0	OscOff	CPUOff	GIE	N	Z	C
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

The bits CPUOff, SCG1, SCG0, and OscOff are the most important low-power control bits when the basic function of the system clock generator is established. They are pushed onto the stack whenever an interrupt is accepted and thereby saved so that the previous mode of operation can be retrieved after the interrupt request. During execution of an interrupt handler routine, the bits can be manipulated via indirect access of the data on the stack. That allows the program to resume execution in another power operating mode after the return from interrupt (RETI).

SCG1: The clock signal SMCLK, used for peripherals, is enabled when bit SCG1 is reset or disabled if the bit is set.

SCG0: The dc-generator is active when SCG0 is reset. The dc-generator can be deactivated only if the SCG0 bit is set and the DCOCLK signal is not used for MCLK or SMCLK. The current consumed by the dc-generator defines the basic frequency of the DCOCLK. It is a dc current.

The clock signal DCOCLK is deactivated if it is not used for MCLK or SMCLK or if the SCG0 bit is set. There are two situations when the SCG0 bit cannot switch off the DCOCLK signal:

1. DCOCLK frequency is used for MCLK (CPUOff=0 and SELM.1=0).
2. DCOCLK frequency is used for SMCLK (SCG1=0 and SELS=0).

NOTE:

When the current is switched off (SCG0=1) the start of the DCOCLK is delayed slightly. The delay is in the µs-range (see device parameters for details).

OscOff: The LFXT1 crystal oscillator is active when the OscOff bit is reset. The LFXT1 oscillator can only be deactivated if the OscOff bit is set and it is not used for MCLK or SMCLK. The setup time to start a crystal oscillation needs consideration when oscillator off option is used. Mask programmable (ROM) devices can disable this feature so that the oscillator can never be switched off by software.

CPUOff: The clock signal MCLK, used for the CPU, is active when the CPUOff bit is reset or stopped if it is set.

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the memory with an address range of 0FFFFh-0FFE0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up, external reset, watchdog	WDTIFG (Note1) KEYV (Note 1)	Reset	0FFFEh	15, highest
NMI, oscillator fault, flash memory access violation	NMIIFG (Notes 1 and 4) OFIFG (Notes 1 and 4) ACCVIFG (Notes 1 and 4)	(non)-maskable, (non)-maskable, (non)-maskable	0FFFCh	14
			0FFFAh	13
			0FFF8h	12
Comparator_A	CAIFG	maskable	0FFF6h	11
Watchdog timer	WDTIFG	maskable	0FFF4h	10
Timer_A	CCIFG0 (Note 2)	maskable	0FFF2h	9
Timer_A	CCIFG1, CCIFG2, TAIFG (Notes 1 and 2)	maskable	0FFF0h	8
			0FFEEh	7
			0FFECh	6
			0FFEAh	5
			0FFE8h	4
I/O Port P2 (eight flags – see Note 3)	P2IFG.0 to P2IFG.7 (Notes 1 and 2)	maskable	0FFE6h	3
I/O Port P1 (eight flags)	P1IFG.0 to P1IFG.7 (Notes 1 and 2)	maskable	0FFE4h	2
			0FFE2h	1
			0FFE0h	0, lowest

NOTES: 1. Multiple source flags
2. Interrupt flags are located in the module
3. There are eight Port P2 interrupt flags, but only six Port P2 I/O pins (P2.0–5) are implemented on the 11x1 devices.
4. (non)-maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable cannot. Nonmaskable: neither the individual nor the general interrupt enable bit will disable an interrupt event.

special function registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits that are not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE: Watchdog timer enable signal
OFIE: Oscillator fault enable signal
NMIIE: Nonmaskable interrupt enable signal
ACCVIE: Access violation at flash memory

Address	7	6	5	4	3	2	1	0
01h								

interrupt flag register 1 and 2

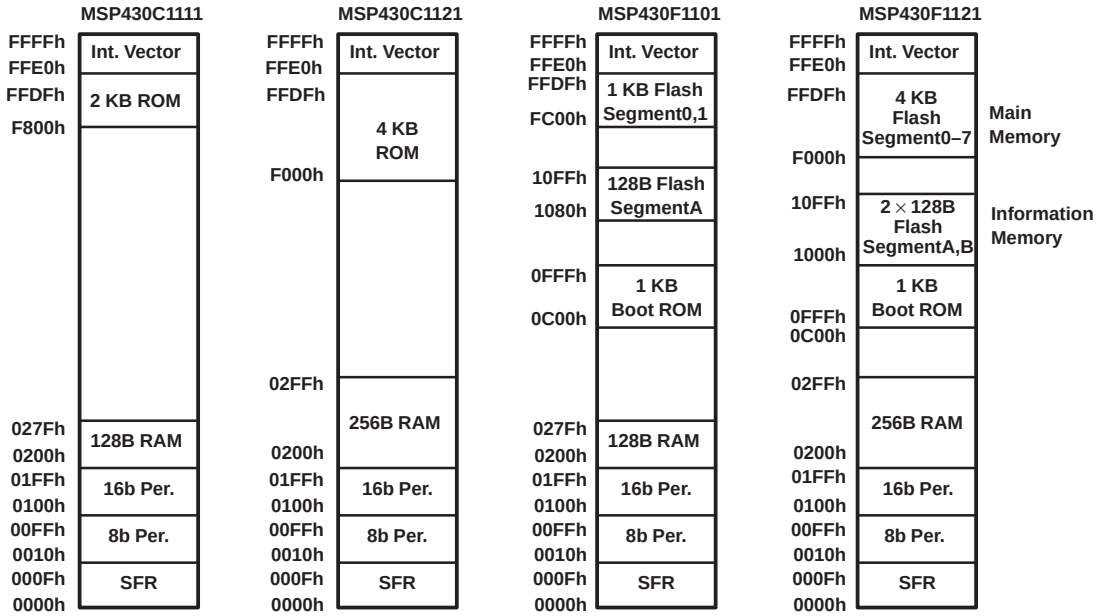
Address	7	6	5	4	3	2	1	0
02h				NMIIFG			OFIFG	WDTIFG
				rw-0			rw-1	rw-0

WDTIFG: Set on overflow or security key violation or
Reset on V_{CC} power-on or reset condition at $\overline{RST}$/NMI-pin
OFIFG: Flag set on oscillator fault
NMIIFG: Set via $\overline{RST}$/NMI-pin

Address	7	6	5	4	3	2	1	0
03h								

Legend	rw:	Bit can be read and written.
	rw-0:	Bit can be read and written. It is reset by PUC
		SFR bit is not present in device.

memory organization



boot ROM containing bootstrap loader

The intention of the bootstrap loader is to download data into the flash memory module. Various write, read, and erase operations are needed for a proper download environment. The bootstrap loader is only available on F devices.

functions of the bootstrap loader:

Definition of read: apply and transmit data of peripheral registers or memory to pin P1.1 (BSLTX)
write: read data from pin P2.2 (BSLRX) and write them into flash memory

unprotected functions

Mass erase, erase of the main memory (Segment0 to Segment7)
Access to the MSP430 via the bootstrap loader is protected. It must be enabled before any protected function can be performed. The 256 bits in 0FFE0h to 0FFFFh provide the access key.

protected functions

All protected functions can be executed only if the access is enabled.

- Write/program byte into flash memory; Parameters passed are start address and number of bytes (the segment-write feature of the flash memory is not supported and not useful with the UART protocol).
- Segment erase of Segment0 to Segment7 in the main memory and segment erase of SegmentA and SegmentB in the information memory.
- Read all data in main memory and information memory.
- Read and write to all byte peripheral modules and RAM.
- Modify PC and start program execution immediately.

NOTE:

Unauthorized readout of code and data is prevented by the user's definition of the data in the interrupt memory locations.

boot ROM containing bootstrap loader (continued)

features of the bootstrap loader are:

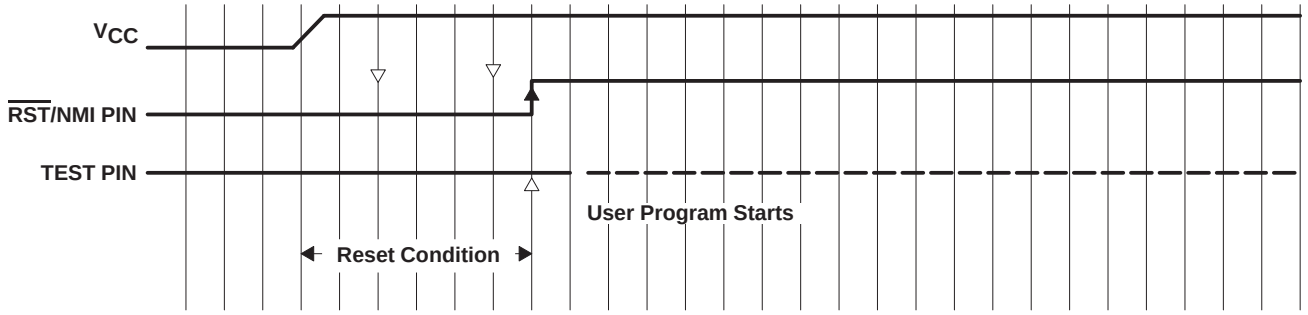
- UART communication protocol, fixed to 9600 baud
- Port pin P1.1 for transmit, P2.2 for receive
- TI standard serial protocol definition
- Implemented in flash memory version only
- Program execution starts with the user vector at 0FFFEh or with the bootstrap loader (start vector is at address 0C00h)

hardware resources used for serial input/output:

- Pins P1.1 and P2.2 for serial data transmission
- Test and $\overline{\text{RST}}$/NMI to start program execution at the reset or bootstrap loader vector
- Basic clock module: Rsel=5, DCO=4, MOD=0, DCOCLK for MCLK and SMCLK, clock divider for MCLK and SMCLK at default: dividing by 1
- Timer_A: Timer_A operates in continuous mode with MCLK source selected, input divider set to 1, using CCR0, and polling of CCIFG0.
- WDT: Watchdog timer is halted
- Interrupt: GIE=0, NMIIE=0, OFIFG=0, ACCVIFG=0
- Memory allocation and stack pointer:
  If the stack pointer points to RAM addresses above 0220h, 6 bytes of the stack are allocated plus RAM addresses 0200h to 0219h. Otherwise the stack pointer is set to 0220h and allocates RAM from 0200h to 021Fh.

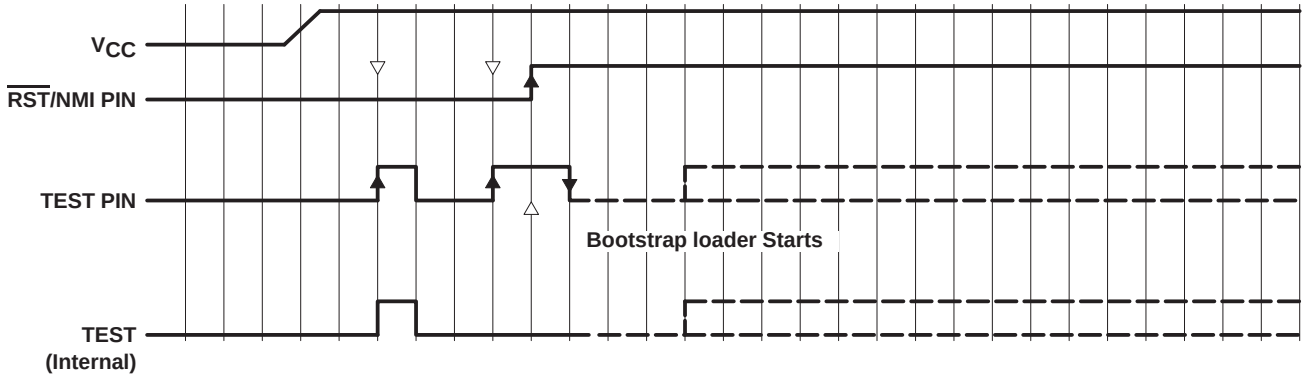
NOTE:
When writing RAM data via bootstrap loader, take care that the stack is outside the range of the data being written.

Program execution begins with the user's reset vector at FFFEh (standard method) if TEST is held low while $\overline{\text{RST}}$/NMI goes from low to high:



boot ROM containing bootstrap loader (continued)

Program execution begins with the bootstrap vector at 0C00h (boot ROM) if a minimum of two positive edges have been applied to TEST while $\overline{\text{RST}}$/NMI is low, and TEST is high when $\overline{\text{RST}}$/NMI goes from low to high. The TEST signal is normally used internally to switch pins P1.4, P1.5, P1.6, and P1.7 between their application function and the JTAG function. If the second rising edge at TEST is applied while $\overline{\text{RST}}$/NMI is held low, the internal TEST signal is held low and the pins remain in the application mode:



Test mode can be entered again after TEST is taken low and then back high.

The bootstrap loader will not be started (via the vector in address 0C00h), if:

- There were less than two positive edges at TEST while $\overline{\text{RST}}$/NMI is low
- TEST is low if $\overline{\text{RST}}$/NMI goes from low to high
- JTAG has control over the MSP430 resources
- Supply voltage VCC drops and a POR is executed

WARNING:

The bootstrap loader starts correctly only if the $\overline{\text{RST}}$/NMI pin is in reset mode. If it is switched to the NMI function, unpredictable program execution may result. However, a bootstrap-load may be started using software and the bootstrap vector, for example the instruction BR &0C00h.

flash memory

The flash memory consists of 512-byte segments in the main memory and 128-byte segments in the information memory. See device memory maps for specific device information.

Segment0 to Segment7 can be erased individually, or altogether as a group.

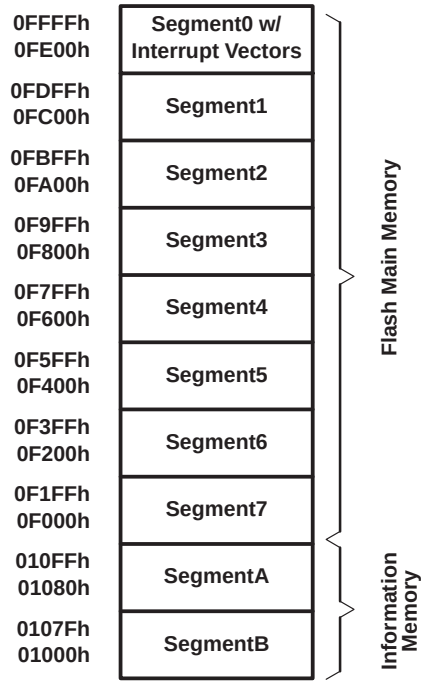
SegmentA and SegmentB can be erased individually, or as a group with segments 0–7.

The memory in SegmentA and SegmentB is also called *Information Memory.*

VPP is generated internally. VCC current increases during programming.

During program/erase cycles, VCC must not drop below the minimum specified for program/erase operation.

Program and erase timings are controlled by the flash timing generator—no software intervention is needed. The input frequency of the flash timing generator should be in the proper range and must be applied until the write/program or erase operation is completed.



NOTE: All segments not implemented on all devices.

During program or erase, no code can be executed from flash memory and all interrupts must be disabled by setting the GIE, NMIE, ACCVIE, and OFIE bits to zero. If a user program requires execution concurrent with a flash program or erase operation, the program must be executed from memory other than the flash memory (e.g., boot ROM, RAM). In the event a flash program or erase operation is initiated while the program counter is pointing to the flash memory, the CPU will execute JMP $ instructions until the flash program or erase operation is completed. Normal execution of the previously running software then resumes.

Unprogrammed, new devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to first use.

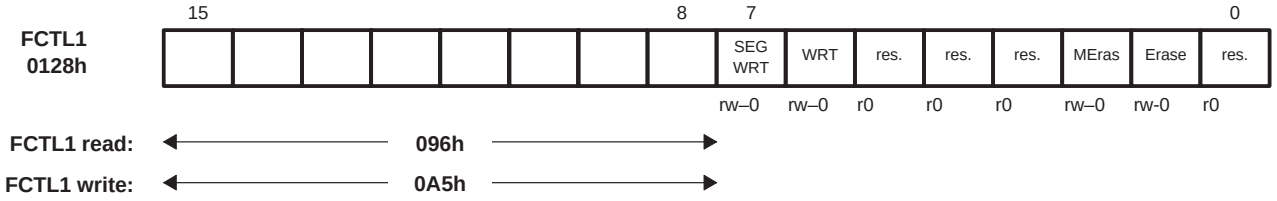
flash memory control register FCTL1

All control bits are reset during PUC. PUC is active after V_{CC} is applied, a reset condition is applied to the $\overline{\text{RST}}$/NMI pin, the watchdog timer expires, a watchdog access violation occurs, or an improper flash operation has been performed. A more detailed description of the control-bit functions is found in the flash memory module description (refer to *MSP430x1xx User's Guide*, literature number SLAU049). Any write to control register FCTL1 during erase, mass erase, or write (programming) will end in an access violation with ACCVIFG=1. Special conditions apply for segment-write mode. Refer to *MSP430x1xx User's Guide*, literature number SLAU049 for details.

flash memory control register FCTL1 (continued)

Read access is possible at any time without restrictions.

The control bits of control register FCTL1 are:



Erase 0128h, bit1, Erase a segment

0: No segment erase will be started.
1: Erase of one segment is enabled. The segment to be erased is defined by a *dummy* write into any address within the segment. The erase bit is automatically reset when the erase operation is completed.

MEras 0128h, bit2, Mass Erase, main memory segments are erased together.

0: No segment erase will be started.
1: Erase of main memory segments is enabled. Erase starts when a dummy write to any address in main memory is executed. The MEras bit is automatically reset when the erase operation is completed.

WRT 0128h, bit6, Bit WRT must be set for a successful write execution.

If bit WRT is reset and write access to the flash memory is attempted, an access violation occurs and ACVIFG is set.

SEGWRT 0128h, bit7, Bit SEGWRT may be used to reduce total programming time.

Refer to *MSP430x1xx User's Guide*, literature number SLAU049 for details.

0: No segment-write acceleration is selected.
1: Segment-write is used. This bit needs to be reset and set between segment borders.

Table 3. Allowed Combinations of Control Bits Allowed for Flash Memory Access

FUNCTION PERFORMED	SEGWRT	WRT	MEras	Erase	BUSY	WAIT	Lock
Write word or byte	0	1	0	0	0	0	0
Write word or byte in same segment, segment write mode	1	1	0	0	0 → 1	0 → 1	0
Erase one segment by writing to any address in the target segment	0	0	0	1	0	0	0
Erase all segments (0 to 7) but not the information memory (segments A and B)	0	0	1	0	0	0	0
Erase all segments (0 to 7 and A and B) by writing to any address in the flash memory module	0	0	1	1	0	0	0

NOTE: The table shows all valid combinations. Any other combination will result in an access violation.

flash memory, timing generator, control register FCTL2

The timing generator (Figure 1) generates all the timing signals necessary for write, erase, and mass erase from the selected clock source. One of three different clock sources may be selected by control bits SSEL0 and SSEL1 in control register FCTL2. The selected clock source should be divided to meet the frequency requirements specified in the recommended operating conditions.

flash memory, timing generator, control register FCTL2 (continued)

The flash timing generator is reset with PUC. It is also reset if the emergency exit bit EMEX is set.

Control register FCTL2 may not be written to if the BUSY bit is set; otherwise, an access violation will occur (ACCVIFG=1).

Read access is possible at any time without restrictions.

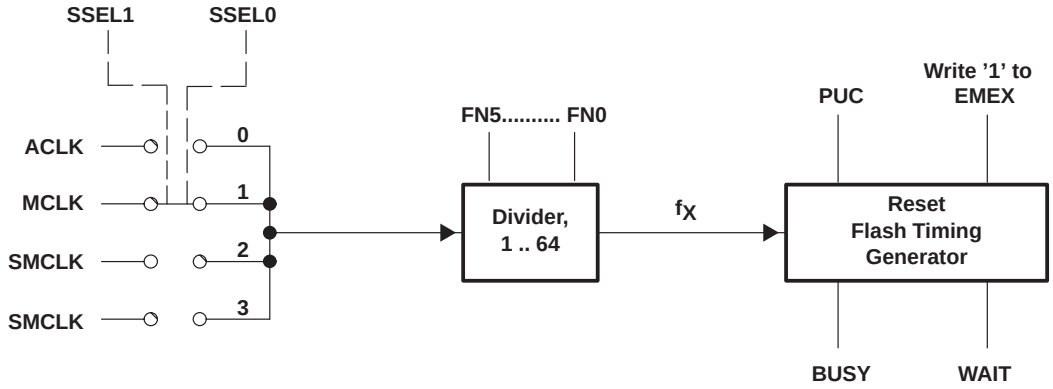
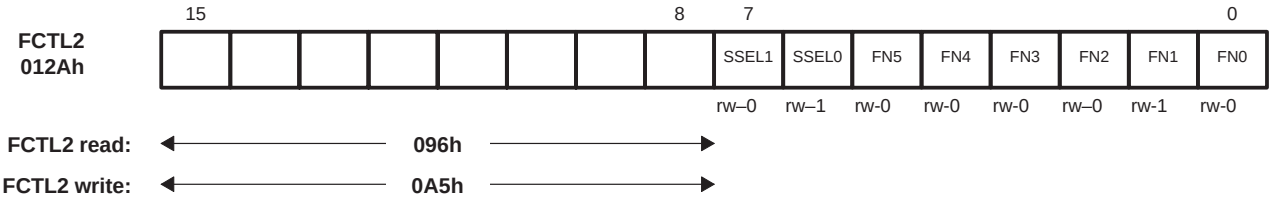


Figure 1. Flash Memory Timing Generator Diagram



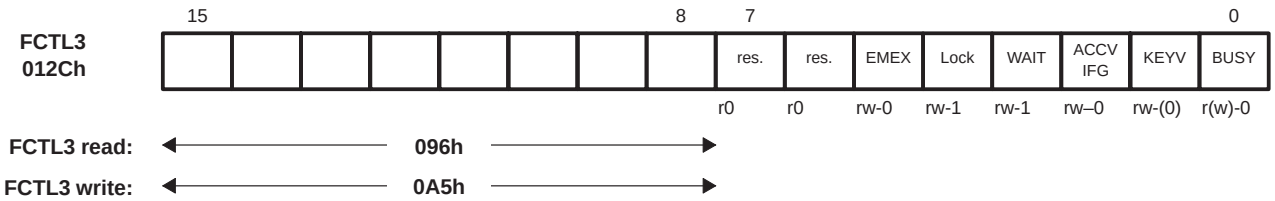
The control bits are:

FN0–FN5	012Ah, bit0–5	These six bits define the division rate of the clock signal. The division rate is 1 to 64, according to the digital value of FN5 to FN0 plus one.
SSEL0, SSEL1	012Ah, bit6,7	Clock source select 0: ACLK 1: MCLK 2: SMCLK 3: SMCLK

The flash timing generator is reset with PUC. It is also reset if the EMEX bit is set.

flash memory control register FCTL3

There are no restrictions to modify this control register.



flash memory control register FCTL3 (continued)

BUSY 012Ch, bit0, The BUSY bit shows if an access to the flash memory is allowed (BUSY=0), or if an access violation occurs. The BUSY bit is read-only, but a write operation is allowed. The BUSY bit should be tested before each write and erase cycle. The flash timing-generator hardware immediately sets the BUSY bit after start of a write, segment-write, erase, or *mass* erase operation. If the timing generator has completed the operation, the BUSY bit is reset by the hardware.

No program code can be executed from the *busy* flash memory during the entire program or erase cycle.

0: Flash memory is not busy.

1: Flash memory is busy, and remains in busy state if segment write function is in *wait* mode.

KEYV, 012Ch, bit1 Key violation

0: Key 0A5h (high byte) was not violated.

1: Key 0A5h (high byte) was violated. Violation occurs when a write access to registers FCTL1, FCTL2, or FCTL3 is executed and the *high byte* is not equal to 0A5h. If the security key is violated, bit KEYV is set and a PUC is performed.

ACCVIFG, 012Ch, bit2 Access violation interrupt flag

The access-violation flag is set when any combination of control bits other than those shown in Table 3 is attempted, or an instruction is fetched while a segment-write operation is active.

Reading the control registers will not set the ACCVIFG bit.

NOTE: The respective interrupt-enable bit ACCVIE is located in the interrupt enable register IE1 in the special function register. The software can set the ACCVIFG bit. If set by software, an NMI is also executed.

WAIT, 012CH, bit3 In the segment-write mode, the WAIT bit indicates that data has been written and the flash memory is prepared to receive the next data for programming. The WAIT bit is read only, but a write to the WAIT bit is allowed.

0: The segment-write operation has began and programming is in progress.

1: The segment-write operation is active and data programming is complete.

flash memory control register FCTL3 (continued)

LOCK 012Ch, bit4, The lock bit may be set during any write, segment-erase, or *mass*-erase request. Any active sequence in progress is completed normally. In segment-write mode, the SEGWRT bit is reset and the WAIT bit is set after the mode ends. The lock bit is controlled by software or hardware. If an access violation occurs and the ACCVIFG is set, the LOCK bit is set automatically.

0: Flash memory may be read, programmed, erased, or *mass* erased.

1: Flash memory may be read but not programmed, erased, or *mass* erased. A current program, erase, or *mass*-erase operation will complete normally. The access-violation interrupt flag ACCVIFG is set when data are written to the flash memory module while the lock bit is set.

EMEX, 012Ch, bit5, Emergency exit. The emergency exit should only be used if the flash memory write or erase operation is out of control.

0: No function.

1: Stops the active operation immediately, and shuts down all internal parts in the flash memory controller. Current consumption immediately drops back to the active mode. All bits in control register FCTL1 are reset. Since the EMEX bit is automatically reset by hardware, the software always reads EMEX as 0.

flash memory, interrupt and security key violation

One NMI vector is used for three NMI events: $\overline{\text{RST}}$/NMI (NMIIFG), oscillator fault (OFIFG), and flash-memory access violation (ACCVIFG). The software can determine the source of the interrupt request since all flags remain set until they are reset by software. The enable flag(s) should be set simultaneously with one instruction before the return-from-interrupt RETI instruction. This ensures that the stack remains under control. A pending NMI interrupt request will not increase stack demand unnecessarily.

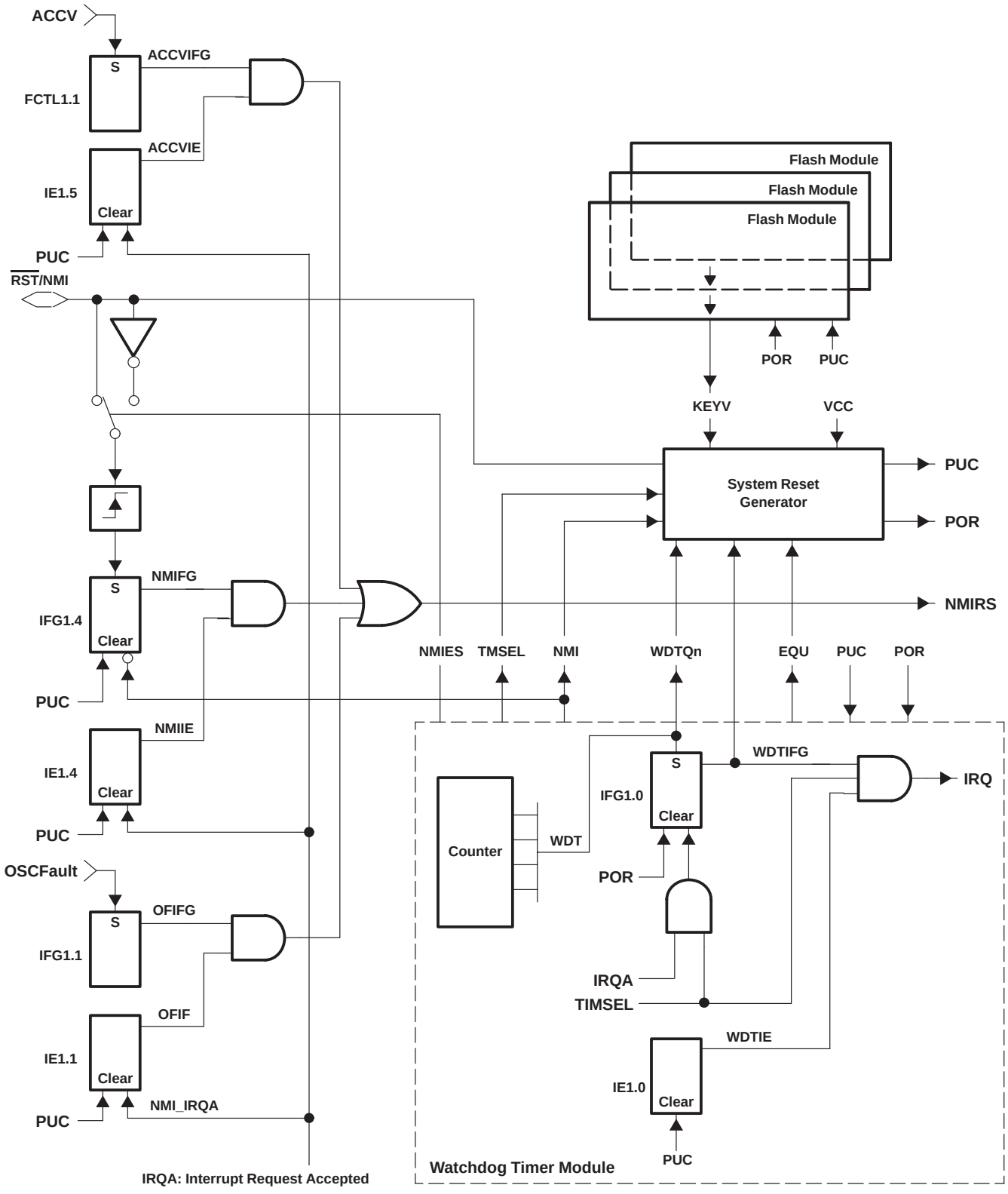


Figure 2. Block Diagram of NMI Interrupt Sources

peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled easily with memory manipulation instructions.

oscillator and system clock

Three clocks are used in the system—the system (master) clock MCLK, the subsystem (master) clock SMCLK, and the auxiliary clock ACLK:

Main system clock MCLK, used by the CPU and the system
Subsystem clock SMCLK, used by the peripheral modules
Auxiliary clock ACLK, originated by LFXT1CLK (crystal frequency) and used by the peripheral modules

After a POR, the DCOCLK is used by default, the DCOR bit is reset, and the DCO is set to the nominal initial frequency. Additionally, if LFXT1CLK fails as the source for MCLK, the DCOCLK is automatically selected to ensure fail-safe operation.

SMCLK can be generated from LFXT1CLK or DCOCLK. ACLK is always generated from LFXT1CLK.

The crystal oscillator can be defined to operate with watch crystals (32768 Hz) or with higher-frequency ceramic resonators or crystals. The crystal or ceramic resonator is connected across two terminals. No external components are required for watch-crystal operation. If the high frequency XT1 mode is selected, external capacitors from XIN to VSS and XOUT to VSS are required as specified by the crystal manufacturer.

The LFXT1 oscillator starts after applying VCC. If the OscOff bit is set to 1, the oscillator stops when it is not used for MCLK. The clock signals ACLK and SMCLK may be used externally via port pins.

Different application requirements and system conditions dictate different system clock requirements, including:

High frequency for quick reaction to system hardware requests or events
Low frequency to minimize current consumption, EMI, etc.
Stable peripheral clock for timer applications, such as real-time clock (RTC)
Start-stop operation to be enabled with minimum delay

oscillator and system clock (continued)

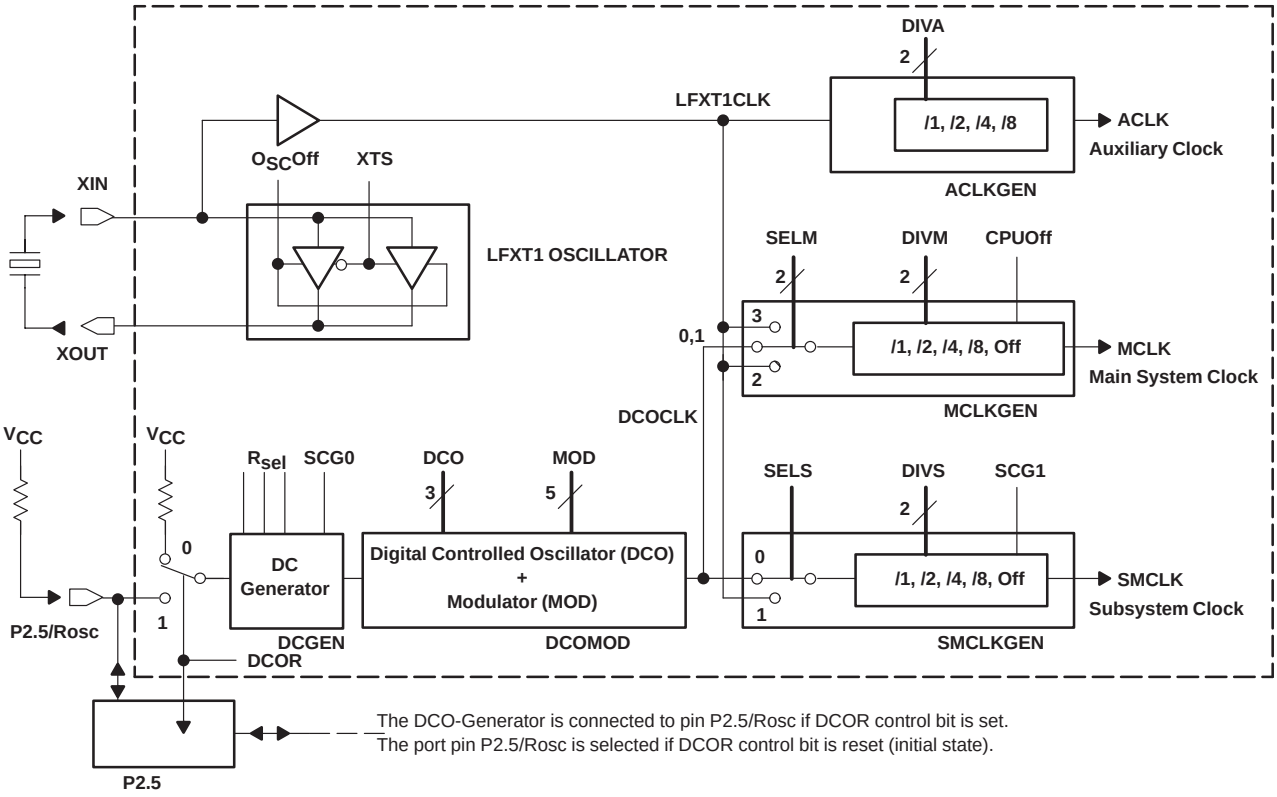


Figure 3. Clock Signals

Two clock sources, LFXT1CLK and DCOCLK, can be used to drive the MSP430 system. The LFXT1CLK is generated from the LFXT1 crystal oscillator. The LFXT1 crystal oscillator can operate in three modes—low frequency (LF), moderate frequency (XT1), and external input mode. The LFXT1 crystal oscillator may be switched off when it is not in use.

DCOCLK is generated from the DCO. The nominal DCO frequency is defined by the dc generator and can be set by one external resistor, or can be set to one of eight values with integrated resistors. Additional adjustments and modulations of DCOCLK are possible by software manipulation of registers in the DCO module. DCOCLK is stopped automatically when it is not used by the CPU or peripheral modules. The dc generator can be shut down with the SCG0 bit to realize additional power savings when DCOCLK is not in use.

NOTE:

The system clock generator always starts with the DCOCLK selected for MCLK (CPU clock) to ensure proper start of program execution. The software defines the final system clock generation through control bit manipulation.

digital I/O

There are two eight-bit I/O ports, port P1 and port P2 – implemented (11x1 parts only have six port P2 I/O signals available on external pins). Both ports, P1 and P2, have seven control registers to give maximum flexibility of digital input/output to the application:

- All individual I/O bits are programmable independently.
- Any combination of input, output, and interrupt conditions is possible.
- Interrupt processing of external events is fully implemented for all eight bits of port P1 and for six bits of port P2.
- Read/write access to all registers with all instructions

digital I/O (continued)

The seven registers are:

- Input register — 8 bits at port P1/P2 — contains information at the pins
- Output register — 8 bits at port P1/P2 — contains output information
- Direction register — 8 bits at port P1/P2 — controls direction
- Interrupt edge select — 8 bits at port P1/P2 — input signal change necessary for interrupt
- Interrupt flags — 8 bits at port P1/P2 — indicates if interrupt(s) are pending
- Interrupt enable — 8 bits at port P1/P2 — contains interrupt enable bits
- Selection (Port or Mod.) — 8 bits at port P1/P2 — determines if pin(s) have port or module function

All these registers contain eight bits. Two interrupt vectors are implemented: one commonly used for any interrupt event on ports P1.0 to P1.7, and one commonly used for any interrupt event on ports P2.0 to P2.7.

NOTE:

Six bits of port P2, P2.0 to P2.5, are available on external pins – but all control and data bits for port P2 are implemented.

watchdog timer

The primary function of the watchdog timer (WDT) module is to perform a controlled system restart after a software problem has occurred. If the selected time interval expires, a system reset is generated. If this watchdog function is not needed in an application, the module can work as an interval timer, which generates an interrupt after the selected time interval.

The watchdog timer counter (WDTCNT) is a 16-bit up-counter which is not directly accessible by software. The WDTCNT is controlled through the watchdog timer control register (WDTCTL), which is a 16-bit read/write register. Writing to WDTCTL is, in both operating modes (watchdog or timer), only possible by using the correct password in the high-byte. The low-byte stores data written to the WDTCTL. The high-byte must be the password 05Ah. If any value other than 05Ah is written to the high-byte of the WDTCTL, a system reset PUC is generated. When the password is read, its value is 069h. This minimizes accidental write operations to the WDTCTL register. In addition to the watchdog timer control bits, there are two bits included in the WDTCTL register that configure the NMI pin.

Timer_A (Three capture/compare registers)

The Timer_A module on 11x1 devices offers one sixteen bit counter and three capture/compare registers. The timer clock source can be selected to come from two external sources TACLK (SSEL=0) or INCLK (SSEL=3), or from two internal sources, the ACLK (SSEL=1) or SMCLK (SSEL=2). The clock source can be divided by one, two, four, or eight. The timer can be fully controlled (in word mode) since it can be halted, read, and written. It can be stopped, run continuously, counted up or up/down, using one compare block to determine the period. The three capture/compare blocks are configured by the application to run in capture or compare mode.

The capture mode is primarily used to measure external or internal events using any combination of positive, negative, or both edges of the signal. Capture mode can be started and stopped by software. Three different external events TA0, TA1, and TA2 can be selected. At capture/compare register CCR2 the ACLK is the capture signal if CCI2B is selected. Software capture is chosen if CCISx=2 or CCISx=3 (see Figure 4).

The compare mode is primarily used to generate timings for the software or application hardware, or to generate pulse-width modulated output signals for various purposes like D/A conversion functions or motor control. An individual output module is assigned to each of the three capture/compare registers. The output modules can run independently of the compare function, or can be triggered in several ways.

Timer_A (3 capture/compare registers) (continued)

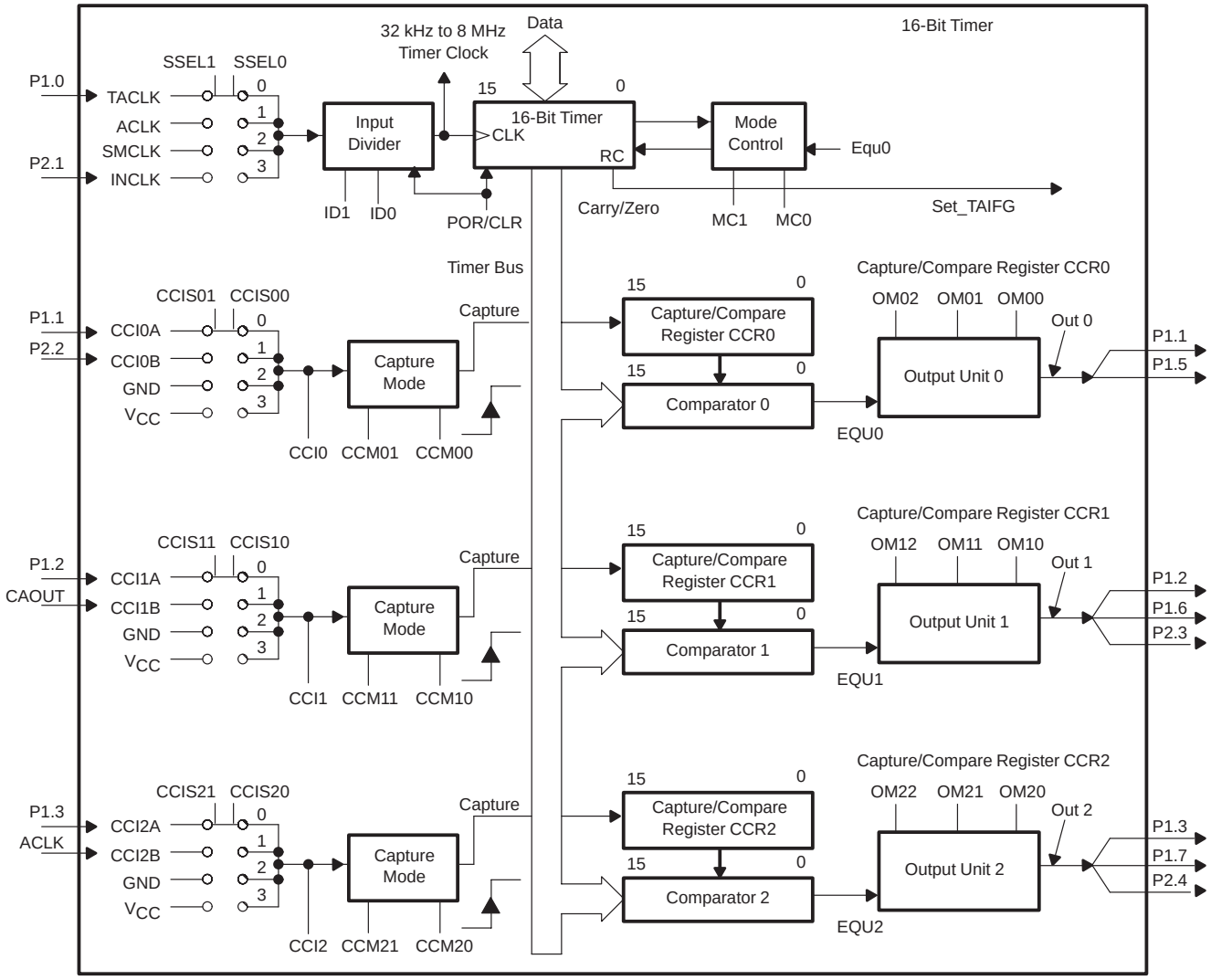


Figure 4. Timer_A, MSP430x11x1 Configuration

Two interrupt vectors are used by the Timer_A module. One individual vector is assigned to capture/compare block CCR0, and one common interrupt vector is implemented for the timer and the other two capture/compare blocks. The three interrupt events using the same vector are identified by an individual interrupt vector word. The interrupt vector word is used to add an offset to the program counter to continue the interrupt handler software at the corresponding program location. This simplifies the interrupt handler and gives each interrupt event the same overhead of 5 cycles in the interrupt handler.

UART

Serial communication is implemented by using software and one capture/compare block. The hardware supports the output of the serial-data stream, bit by bit, with the timing determined by the comparator/timer. The data input uses the capture feature. The capture flag finds the start of a character, while the compare feature latches the input-data stream, bit by bit. The software/hardware interface connects the mixed-signal controller to external devices, systems, or networks.

Comparator_A

The primary function of the comparator module is to support precision A/D slope conversion applications, battery voltage supervision, and observation of external analog signals. The comparator is connected to port pins P2.3/CA0 and to P2.4/CA1. It is controlled via twelve control bits in registers CACTL1 and CACTL2.

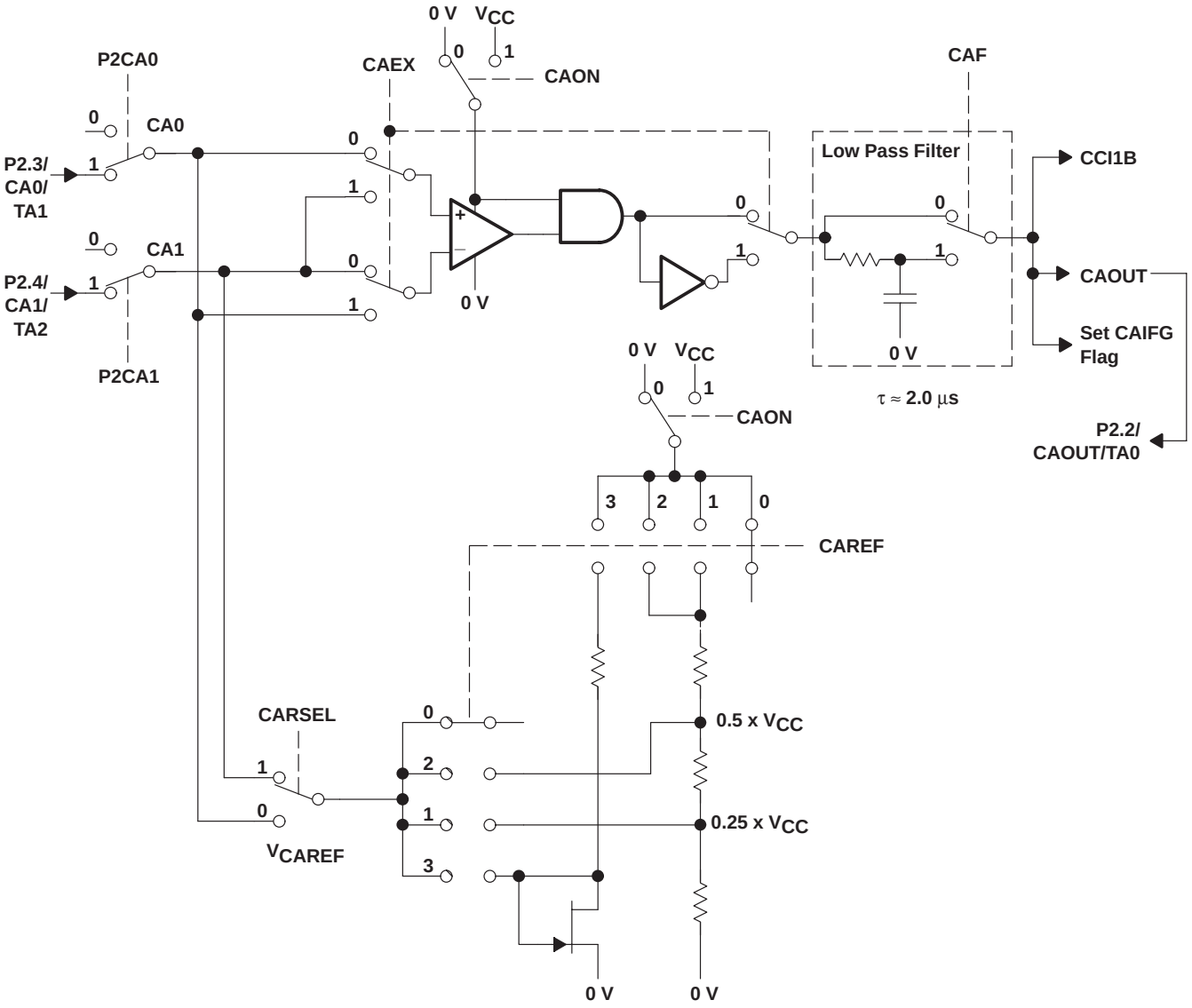


Figure 5. Block Diagram of Comparator_A

Comparator_A (continued)

The control bits are:

CAOUT,	05Ah, bit0,	Comparator output
CAF,	05Ah, bit1,	The comparator output is transparent or fed through a small filter
CA0,	05Ah, bit2,	0: Pin P2.3/CA0/TA1 is not connected to Comparator_A. 1: Pin P2.3/CA0/TA1 is connected to Comparator_A.
CA1,	05Ah, bit3,	0: Pin P2.4/CA1/TA2 is not connected to Comparator_A. 1: Pin P2.4/CA1/TA2 is connected to Comparator_A.
CACTL2.4 to CATCTL2.7	05Ah, bit4, 05Ah, bit7,	Bits are implemented but do not control any hardware in this device.
CAIFG,	059h, bit0,	Comparator_A interrupt flag
CAIE,	059h, bit1,	Comparator_A interrupt enable
CAIES,	059h, bit2,	Comparator_A interrupt edge select bit 0: The rising edge sets the Comparator_A interrupt flag CAIFG 1: The falling edge set the Comparator_A interrupt flag CAIFG
CAON,	059h, bit3,	The comparator is switched on.
CAREF,	059h, bit4,5,	Comparator_A reference 0: Internal reference is switched off, an external reference can be applied. 1: 0.25 × VCC reference selected. 2: 0.50 × VCC reference selected. 3: A diode reference selected.
CARSEL,	059h, bit6,	An internal reference V_{CAREF}, selected by CAREF bits, can be applied to signal path CA0 or CA1. The signal V_{CAREF} is only driven by a voltage source if the value of CAREF control bits is 1, 2, or 3.
CAEX,	059h, bit7,	The comparator inputs are exchanged, used to measure and compensate the offset of the comparator.

Eight additional bits are implemented into the Comparator_A module and enable the SW to switch off the input buffer of port P2. A CMOS input buffer would dissipate supply current when the input is not near VSS or VCC. Comparator_A port disable control bits CAPD0 to CAPD7 are initially reset, and the port input buffer is active. The port input buffer is disabled if the appropriate control bit is set.

Comparator_A (continued)

CACTL1 059h

7							0
CAEX	CA RSEL	CA REF1	CA REF0	CAON	CAIES	CAIE	CAIFG
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

CACTL2 05Ah

7							0
CACTL 2.7	CACTL 2.6	CACTL 2.5	CACTL 2.4	CA1	CA0	CAF	CAOUT
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	r-(0)

CAPD 05Bh

7							0
CAPD7	CAPD6	CAPD5	CAPD4	CAPD3	CAPD2	CAPD1	CAPD0
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

NOTE:

Ensure that the comparator input terminals are connected to signal, power, or ground level. Otherwise, floating levels may cause unexpected interrupts and current consumption may be increased.

slope a/d conversion

The Comparator_A is well suited for use in single or multiple-slope conversions. The internal-reference levels may be used to set a reference during timing measurement of charge or discharge operations. They can also be used externally to bias analog circuitry.

Voltage, current, and resistive or capacitive sensor measurements are basic functions. The sensors sense physical conditions like temperature, pressure, acceleration, etc.

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Timer_A	Reserved		017Eh
	Reserved		017Ch
	Reserved		017Ah
	Reserved		0178h
	Capture/compare register	CCR2	0176h
	Capture/compare register	CCR1	0174h
	Capture/compare register	CCR0	0172h
	Timer_A register	TAR	0170h
	Reserved		016Eh
	Reserved		016Ch
	Reserved		016Ah
	Reserved		0168h
	Capture/compare control	CCTL2	0166h
	Capture/compare control	CCTL1	0164h
	Capture/compare control	CCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Flash Memory	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
Watchdog	Watchdog/timer control	WDTCTL	0120h
PERIPHERALS WITH BYTE ACCESS			
Comparator_A	Comparator_A port disable	CAPD	05Bh
	Comparator_A control2	CACTL2	05Ah
	Comparator_A control1	CACTL1	059h
System Clock	Basic clock sys. control2	BCSCTL2	058h
	Basic clock sys. control1	BCSCTL1	057h
	DCO clock freq. control	DCOCTL	056h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Function	SFR interrupt flag2	IFG2	003h
	SFR interrupt flag1	IFG1	002h
	SFR interrupt enable2	IE2	001h
	SFR interrupt enable1	IE1	000h

absolute maximum ratings†

Voltage applied at V_{CC} to V_{SS} (MSP430C11x1) . . . . . –0.3 V to 4.6 V
Voltage applied at V_{CC} to V_{SS} (MSP430F11x1) . . . . . –0.3 V to 4.1 V
Voltage applied to any pin (referenced to V_{SS}) . . . . . –0.3 V to V_{CC}+0.3 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature, T_{stg} (unprogrammed device) . . . . . –55°C to 150°C
Storage temperature, T_{stg} (programmed device) . . . . . –40°C to 85°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

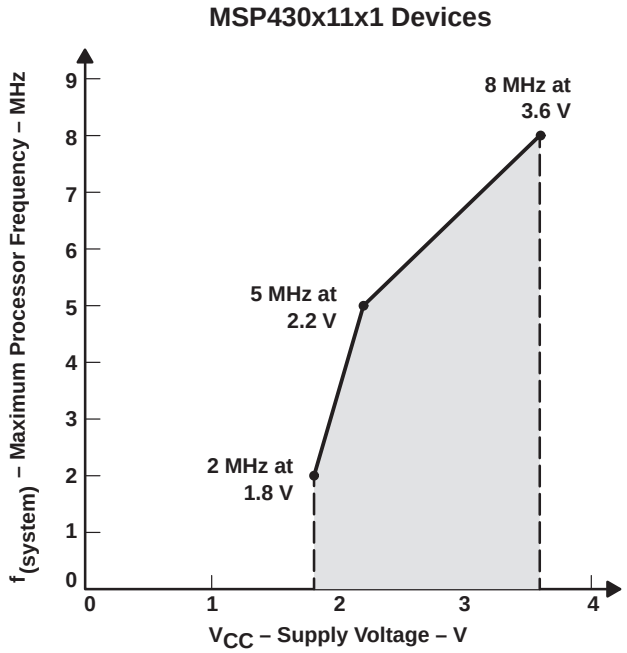
NOTE: All voltages referenced to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNITS
Supply voltage during program execution, V_{CC} (see Note 5)		MSP430C11x1	1.8		3.6	V
		MSP430F11x1	1.8		3.6	
Supply voltage during program/erase flash memory, V_{CC}		MSP430F11x1	2.7		3.6	V
Supply voltage, V_{SS}				0		V
Operating free-air temperature range, T_A		MSP430x11x1	–40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Note 6)	LF mode selected, XTS=0	Watch crystal		32 768		Hz
	XT1 mode selected, XTS=1	Ceramic resonator	450		8000	kHz
		Crystal	1000		8000	
Processor frequency $f_{(system)}$ (MCLK signal)		V_{CC} = 1.8 V, MSP430x11x1	dc		2	MHz
		V_{CC} = 2.2 V, MSP430x11x1	dc		5	
		V_{CC} = 3.6 V, MSP430x11x1	dc		8	
Flash timing generator frequency, $f_{(FTG)}$		MSP430F11x1	257		476	kHz
Cumulative program time, segment write, $t_{(CPT)}$ (see Note 7)		V_{CC} = 2.7 V/3.6 V MSP430F11x1			3	ms
Low-level input voltage (TCK, TMS, TDI, $\overline{RST}$/NMI), V_{IL} (excluding XIN, XOUT)		V_{CC} = 2.2 V/3 V	V_{SS}		V_{SS}+0.6	V
High-level input voltage (TCK, TMS, TDI, $\overline{RST}$/NMI), V_{IH} (excluding XIN, XOUT)		V_{CC} = 2.2 V/3 V	0.8V_{CC}		V_{CC}	V
Input levels at XIN, XOUT	$V_{IL(XIN, XOUT)}$	V_{CC} = 2.2 V/3 V	V_{SS}		0.2×V_{CC}	V
	$V_{IH(XIN, XOUT)}$		0.8×V_{CC}		V_{CC}	

NOTES: 5. The LFXT1 oscillator in LF-mode requires a resistor of 5.1 MΩ from XOUT to VSS when VCC <2.5 V.
The LFXT1 oscillator in XT1-mode accepts a ceramic resonator or a crystal frequency of 4 MHz at VCC ≥ 2.2 V.
The LFXT1 oscillator in XT1-mode accepts a ceramic resonator or a crystal frequency of 8 MHz at VCC ≥ 2.8 V.
6. The LFXT1 oscillator in LF-mode requires a watch crystal.
The LFXT1 oscillator in XT1-mode accepts a ceramic resonator or a crystal.
7. The cumulative program time must not be exceeded during a segment-write operation.

recommended operating conditions (continued)



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.7 V.

Figure 6. Frequency vs Supply Voltage

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

supply current (into V_{CC}) excluding external current ($f_{(system)}$ = 1 MHz)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(AM)}$	Active mode	C11x1	T_A = –40°C +85°C, $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz	V_{CC} = 2.2 V		160	200	µA
				V_{CC} = 3 V		240	300	
			T_A = –40°C +85°C, $f_{(MCLK)} = f_{(SMCLK)} = f_{(ACLK)}$ = 4096 Hz	V_{CC} = 2.2 V		1.3	2	µA
				V_{CC} = 3 V		2.5	3.2	
		F11x1	T_A = –40°C +85°C, $f_{MCLK} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz	V_{CC} = 2.2 V		200	250	µA
				V_{CC} = 3 V		300	350	
			T_A = –40°C +85°C, $f_{(MCLK)} = f_{(SMCLK)} = f_{(ACLK)}$ = 4096 Hz	V_{CC} = 2.2 V		1.6	3	µA
				V_{CC} = 3 V		3	4.3	
$I_{(CPUOff)}$	Low-power mode, (LPM0)	C11x1	T_A = –40°C +85°C, $f_{(MCLK)}$ = 0, $f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz	V_{CC} = 2.2 V		30	40	µA
				V_{CC} = 3 V		51	60	
		F11x1	T_A = –40°C +85°C, $f_{(MCLK)}$ = 0, $f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz	V_{CC} = 2.2 V		32	45	
				V_{CC} = 3 V		55	70	
$I_{(LPM2)}$	Low-power mode, (LPM2)		T_A = –40°C +85°C, $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 0	V_{CC} = 2.2 V		11	14	µA
				V_{CC} = 3 V		17	22	
$I_{(LPM3)}$	Low-power mode, (LPM3) (C11x1)		T_A = –40°C +85°C, $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1	V_{CC} = 2.2 V		1.2	1.7	µA
				V_{CC} = 3 V		2	2.7	
$I_{(LPM3)}$	Low-power mode, (LPM3) (F11x1)		T_A = –40°C	V_{CC} = 2.2 V		0.8	1.2	µA
			T_A = 25°C			0.7	1	
			T_A = 85°C			1.6	2.3	
			T_A = –40°C	V_{CC} = 3 V		1.8	2.2	µA
			T_A = 25°C			1.6	1.9	
			T_A = 85°C			2.3	3.4	
$I_{(LPM4)}$	Low-power mode, (LPM4) (C11x1)		T_A = –40°C, $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1	V_{CC} = 2.2 V/3 V		0.1	0.5	µA
			T_A = 25°C			0.1	0.5	
			T_A = 85°C			0.4	0.8	
$I_{(LPM4)}$	Low-power mode, (LPM4) (F11x1)		T_A = –40°C	V_{CC} = 2.2 V/3 V		0.1	0.5	µA
			T_A = 25°C			0.1	0.5	
			T_A = 85°C			0.8	1.9	

NOTE: All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.

current consumption of active mode versus system frequency, C version, F version

$$I_{AM} = I_{AM[1\ MHz]} \times f_{system}\ [MHz]$$

current consumption of active mode versus supply voltage, C version

$$I_{AM} = I_{AM[3\ V]} + 105\ \mu A/V \times (V_{CC} – 3\ V)$$

current consumption of active mode versus supply voltage, F version

$$I_{AM} = I_{AM[3\ V]} + 120\ \mu A/V \times (V_{CC} – 3\ V)$$

Schmitt-trigger inputs Port P1 to Port P2; P1.0 to P1.7, P2.0 to P2.5

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1		1.3	V
		V_{CC} = 3 V	1.5		1.8	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4		0.9	V
		V_{CC} = 3 V	.90		1.2	
V_{hys}	Input voltage hysteresis, ($V_{IT+} - V_{IT-}$)	V_{CC} = 2.2 V	0.3		1	V
		V_{CC} = 3 V	0.5		1.4	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

outputs Port 1 to P2; P1.0 to P1.7, P2.0 to P2.5

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage Port 1 and Port 2 (C11x1) Port 1 (F11x1)	$I_{(OHmax)}$ = –1.5 mA	V_{CC} = 2.2 V	See Note 8	V_{CC}–0.25		V_{CC}	V
		$I_{(OHmax)}$ = –6 mA		See Note 9	V_{CC}–0.6		V_{CC}	
		$I_{(OHmax)}$ = –1.5 mA	V_{CC} = 3 V	See Note 8	V_{CC}–0.25		V_{CC}	
		$I_{(OHmax)}$ = –6 mA		See Note 9	V_{CC}–0.6		V_{CC}	
V_{OH}	High-level output voltage Port 2 (F11x1)	$I_{(OHmax)}$ = –1 mA	V_{CC} = 2.2 V	See Note 10	V_{CC}–0.25		V_{CC}	V
		$I_{(OHmax)}$ = –3.4 mA		See Note 10	V_{CC}–0.6		V_{CC}	
		$I_{(OHmax)}$ = –1 mA	V_{CC} = 3 V	See Note 10	V_{CC}–0.25		V_{CC}	
		$I_{(OHmax)}$ = –3.4 mA		See Note 10	V_{CC}–0.6		V_{CC}	
V_{OL}	Low-level output voltage Port 1 and Port 2 (C11x1, F11x1)	$I_{(OLmax)}$ = 1.5 mA	V_{CC} = 2.2 V	See Note 8	V_{SS}		V_{SS}+0.25	V
		$I_{(OLmax)}$ = 6 mA		See Note 9	V_{SS}		V_{SS}+0.6	
		$I_{(OLmax)}$ = 1.5 mA	V_{CC} = 3 V	See Note 8	V_{SS}		V_{SS}+0.25	
		$I_{(OLmax)}$ = 6 mA		See Note 9	V_{SS}		V_{SS}+0.6	

NOTES: 8. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
9. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
10. One output loaded at a time.

leakage current

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current	Port P1: P1.x, 0 ≤ × ≤ 7 (see Notes 11, 12)	V_{CC} = 2.2 V/3 V,			±50	nA
		Port P2: P2.x, 0 ≤ × ≤ 5 (see Notes 11, 12)	V_{CC} = 2.2 V/3 V,			±50	

NOTES: 11. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
12. The leakage of the digital port pins is measured individually. The port pin must be selected for input and there must be no optional pullup or pulldown resistor.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

optional resistors, individually programmable with ROM code (see Note 13)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{(opt1)}$	Resistors, individually programmable with ROM code, all port pins, values applicable for pulldown and pullup	V_{CC} = 2.2 V/3 V	2.5	5	10	kΩ
$R_{(opt2)}$			3.8	7.7	15	kΩ
$R_{(opt3)}$			7.6	15	31	kΩ
$R_{(opt4)}$			11.5	23	46	kΩ
$R_{(opt5)}$			23	45	90	kΩ
$R_{(opt6)}$			46	90	180	kΩ
$R_{(opt7)}$			70	140	280	kΩ
$R_{(opt8)}$			115	230	460	kΩ
$R_{(opt9)}$			160	320	640	kΩ
$R_{(opt10)}$			205	420	830	kΩ

NOTE 13: Optional resistors R_{optx} for pulldown or pullup are not available in standard flash memory device MSP430F11x1.

inputs Px.x, TAx

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger signal for the interrupt flag, (see Note 14)	2.2 V/3 V	1.5			cycle
			2.2 V	62			ns
			3 V	50			
$t_{(cap)}$	Timer_A, capture timing	TA0, TA1, TA2. (see Note 15)	2.2 V/3 V	1.5			cycle
			2.2 V	62			ns
			3 V	50			

NOTES: 14. The external signal sets the interrupt flag every time the minimum t_{int} cycle and time parameters are met. It may be set even with trigger signals shorter than t_{int}. Both the cycle and timing specifications must be met to ensure the flag is set. t_{int} is measured in MCLK cycles.

15. The external capture signal triggers the capture event every time when the minimum t_{cap} cycles and time parameters are met. A capture may be triggered with capture signals even shorter than t_{cap}. Both the cycle and timing specifications must be met to ensure a correct capture of the 16-bit timer value and to ensure the flag is set.

internal signals TAx, SMCLK at Timer_A

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$f_{(IN)}$	Input frequency	Internal TA0, TA1, TA2, $t_H = t_L$	2.2 V			8	MHz
			3 V			10	
$f_{(TAint)}$	Timer_A clock frequency	Internally, SMCLK signal applied	2.2 V/3 V	dc		f_{System}	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

outputs P1.x, P2.x, TAx

PARAMETER		TEST CONDITIONS		VCC	MIN	TYP	MAX	UNIT
$f_{(P20)}$	Output frequency	P2.0/ACLK, C_L = 20 pF		2.2 V/3 V			f_{System}	MHz
$f_{(TAx)}$		TA0, TA1, TA2, C_L = 20 pF Internal clock source, SMCLK signal applied (see Note 16)		2.2 V/3 V	dc		f_{System}	
$t_{(Xdc)}$	Duty cycle of O/P frequency	P1.4/SMCLK, C_L = 20 pF	$f_{SMCLK} = f_{LFXT1} = f_{XT1}$	2.2 V/3 V	40%		60%	
			$f_{SMCLK} = f_{LFXT1} = f_{LF}$		35%		65%	
			$f_{SMCLK} = f_{LFXT1/n}$		50%–15 ns	50%	50%+15 ns	
			$f_{SMCLK} = f_{DCOCLK}$	2.2 V/3 V	50%–15 ns	50%	50%+15 ns	
		P2.0/ACLK, C_L = 20 pF	$f_{P20} = f_{LFXT1} = f_{XT1}$	2.2 V/3 V	40%		60%	
			$f_{P20} = f_{LFXT1} = f_{LF}$		30%		70%	
			$f_{P20} = f_{LFXT1/n}$			50%		
$t_{(TAdc)}$		TA0, TA1, TA2, C_L = 20 pF, Duty cycle = 50%		2.2 V/3 V		0	±50	ns

NOTE 16: The limits of the system clock MCLK has to be met. MCLK and SMCLK can have different frequencies.

Comparator_A (see Note 17)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(DD)}$		CAON=1, CARSEL=0, CAREF=0	V_{CC} = 2.2 V		25	40	µA
			V_{CC} = 3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON=1, CARSEL=0, CAREF=1/2/3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	V_{CC} = 2.2 V		30	50	µA
			V_{CC} = 3 V		45	71	
$V_{(IC)}$	Common-mode input voltage	CAON =1	V_{CC} = 2.2 V/3 V	0		V_{CC}–1	V
$V_{(Ref025)}$ See Figure 5	Voltage @ 0.25 V_{CC} node / V_{CC}	PCA0=1, CARSEL=1, CAREF=1, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2, See Figure 5	V_{CC} = 2.2 V/3 V	0.23	0.24	0.25	
$V_{(Ref050)}$ See Figure 5	Voltage @ 0.5 V_{CC} node / V_{CC}	PCA0=1, CARSEL=1, CAREF=2, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2, See Figure 5	V_{CC} = 2.2 V/3 V	0.47	0.48	0.5	
$V_{(RefVT)}$		PCA0=1, CARSEL=1, CAREF=3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	V_{CC} = 2.2 V	430	550	645	mV
			V_{CC} = 3 V	450	565	660	
$V_{(offset)}$	Offset voltage	See Note 18	V_{CC} = 2.2 V/3 V	–30		30	mV
V_{hys}	Input hysteresis	CAON=1	V_{CC} = 2.2 V/3 V	0	0.7	1.4	mV
$t_{(response LH)}$		T_A = 25°C, Overdrive 10 mV, Without filter: CAF=0	V_{CC} = 2.2 V	160	210	300	ns
			V_{CC} = 3 V	90	150	200	
		T_A = 25°C, Overdrive 10 mV, With filter: CAF=1	V_{CC} = 2.2 V	1.6	1.9	3.4	µs
			V_{CC} = 3 V	1.1	1.5	2.6	
$t_{(response HL)}$		T_A = 25°C, Overdrive 10 mV, without filter: CAF=0	V_{CC} = 2.2 V	160	210	300	ns
			V_{CC} = 3 V	90	150	200	
		T_A = 25°C, Overdrive 10 mV, with filter: CAF=1	V_{CC} = 2.2 V	1.6	1.9	3.4	µs
			V_{CC} = 3 V	1.1	1.5	2.6	

NOTES: 17. The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
18. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

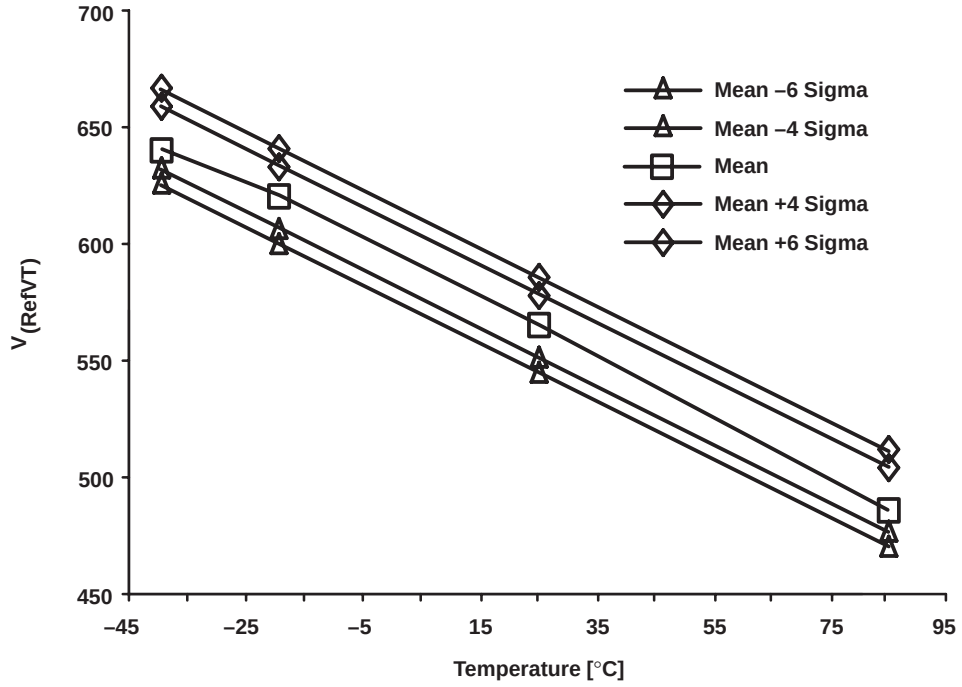


Figure 7. $V_{(RefVT)}$ vs Temperature, V_{CC} = 3 V, C1121

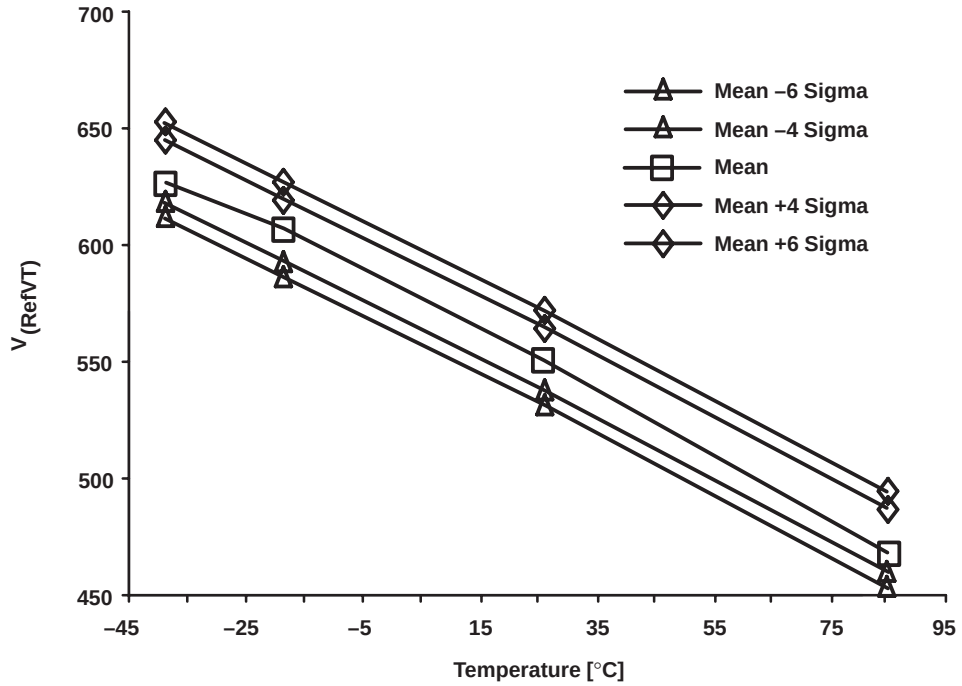


Figure 8. $V_{(RefVT)}$ vs Temperature, V_{CC} = 2.2 V, C1121

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

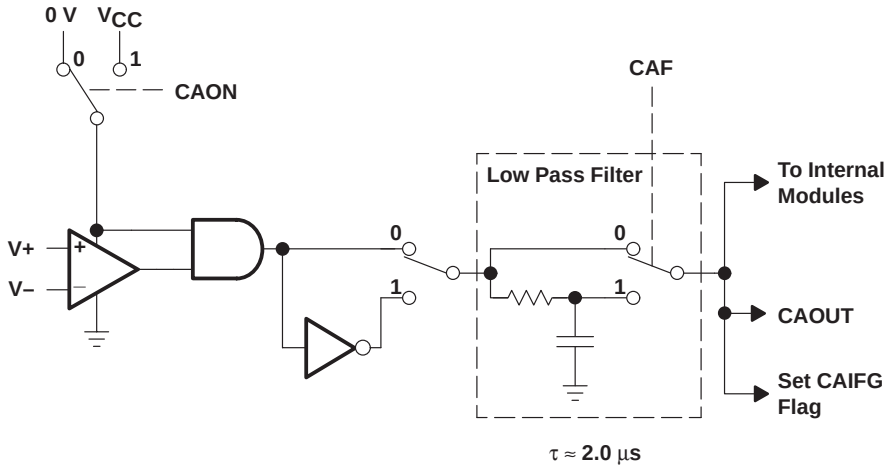


Figure 9. Block Diagram of Comparator_A Module

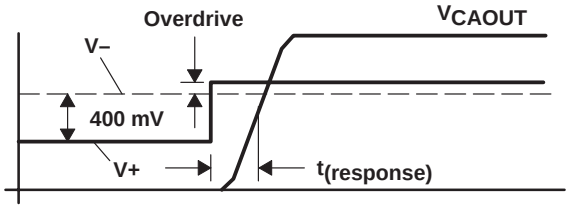


Figure 10. Overdrive Definition

PUC/POR

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(POR\_delay)}$	POR		V_{CC} = 2.2 V/3 V		150	250	µs
$V_{(POR)}$		T_A = –40°C		1.4		1.8	V
		T_A = 25°C		1.1		1.5	V
		T_A = 85°C		0.8		1.2	V
$V_{(min)}$				0		0.4	V
$t_{(reset)}$	PUC/POR	Reset is accepted internally		2			µs

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

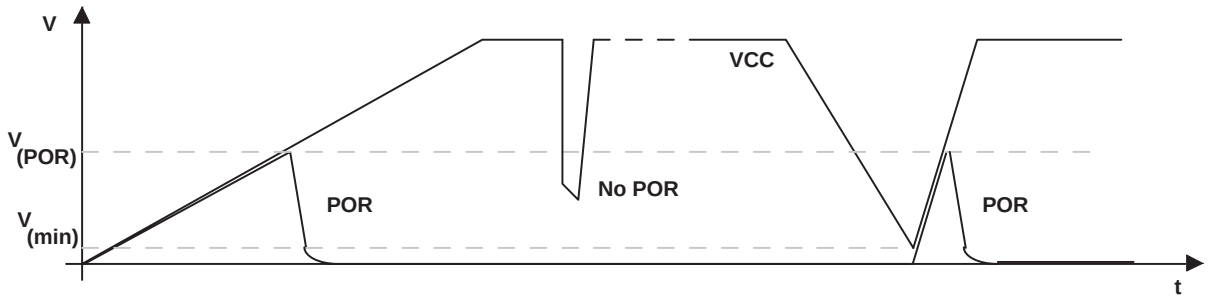


Figure 11. Power-On Reset (POR) vs Supply Voltage

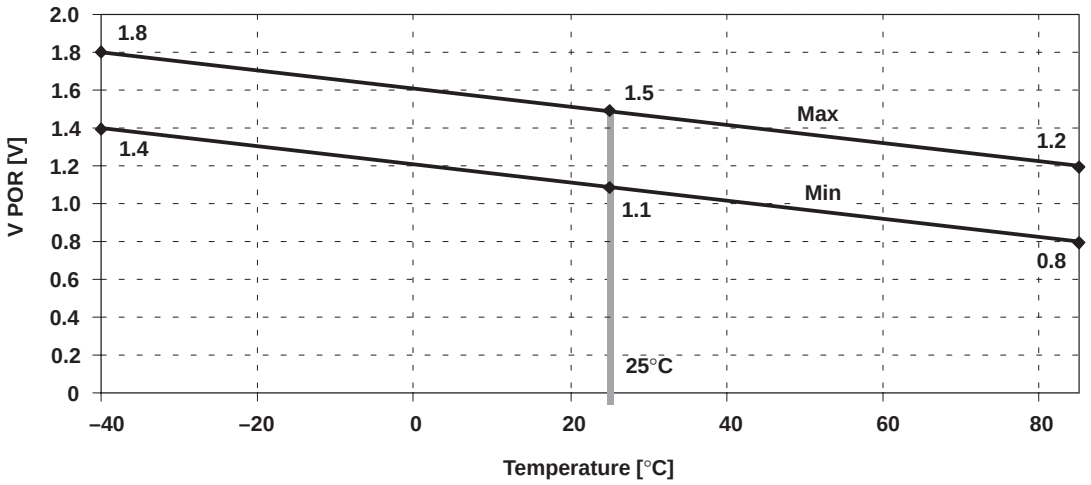


Figure 12. $V_{(POR)}$ vs Temperature

crystal oscillator,LFXT1

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{(XIN)}$	Input capacitance	XTS=0; LF mode selected. V_{CC} = 2.2 V / 3 V		12		pF
		XTS=1; XT1 mode selected. V_{CC} = 2.2 V / 3 V (Note 19)		2		
$C_{(XOUT)}$	Output capacitance	XTS=0; LF mode selected. V_{CC} = 2.2 V / 3 V		12		pF
		XTS=1; XT1 mode selected. V_{CC} = 2.2 V / 3 V (Note 19)		2		

NOTE 19: Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

RAM

PARAMETER		MIN	NOM	MAX	UNIT
$V_{(RAMh)}$	CPU halted (see Note 20)	1.6			V

NOTE 20: This parameter defines the minimum supply voltage V_{CC} when the data in the program memory RAM remains unchanged. No program execution should happen during this supply voltage condition.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

DCO

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(DCO03)}$	R_{sel} = 0, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.08	0.12	0.15	MHz
		V_{CC} = 3 V	0.08	0.13	0.16	
$f_{(DCO13)}$	R_{sel} = 1, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.14	0.19	0.23	MHz
		V_{CC} = 3 V	0.14	0.18	0.22	
$f_{(DCO23)}$	R_{sel} = 2, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.22	0.30	0.36	MHz
		V_{CC} = 3 V	0.22	0.28	0.34	
$f_{(DCO33)}$	R_{sel} = 3, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.37	0.49	0.59	MHz
		V_{CC} = 3 V	0.37	0.47	0.56	
$f_{(DCO43)}$	R_{sel} = 4, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.61	0.77	0.93	MHz
		V_{CC} = 3 V	0.61	0.75	0.9	
$f_{(DCO53)}$	R_{sel} = 5, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	1	1.2	1.5	MHz
		V_{CC} = 3 V	1	1.3	1.5	
$f_{(DCO63)}$	R_{sel} = 6, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	1.6	1.9	2.2	MHz
		V_{CC} = 3 V	1.69	2	2.29	
$f_{(DCO73)}$	R_{sel} = 7, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	2.4	2.9	3.4	MHz
		V_{CC} = 3 V	2.7	3.2	3.65	
$f_{(DCO77)}$	R_{sel} = 7, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	4	4.5	4.9	MHz
		V_{CC} = 3 V	4.4	4.9	5.4	
$f_{(DCO47)}$	R_{sel} = 4, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V/3 V	F_{DCO40} x1.7	F_{DCO40} x2.1	F_{DCO40} x2.5	MHz
$S_{(Rsel)}$	$S_R = f_{Rsel+1}/f_{Rsel}$	V_{CC} = 2.2 V/3 V	1.35	1.65	2	ratio
$S_{(DCO)}$	$S_{DCO} = f_{DCO+1}/f_{DCO}$	V_{CC} = 2.2 V/3 V	1.07	1.12	1.16	
D_t	Temperature drift, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 21)	V_{CC} = 2.2 V	–0.31	–0.36	–0.40	%/°C
		V_{CC} = 3 V	–0.33	–0.38	–0.43	
D_V	Drift with V_{CC} variation, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 21)	V_{CC} = 2.2 V/3 V	0	5	10	%/V

NOTE 21: These parameters are not production tested.

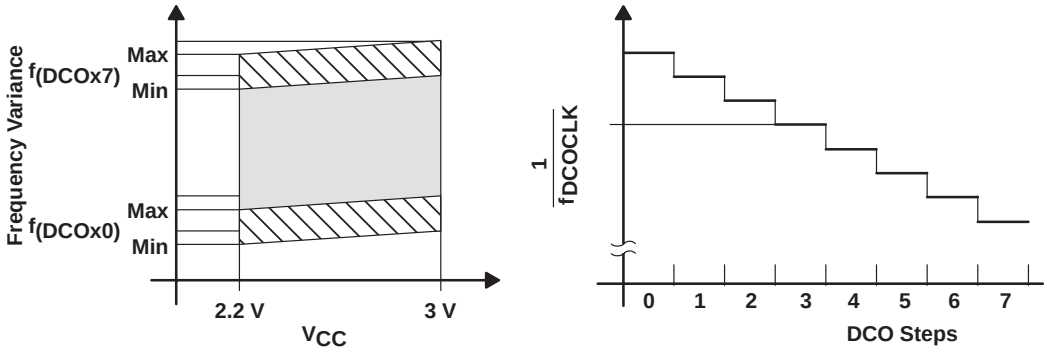


Figure 13. DCO Characteristics

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

principle characteristics of the DCO

- Individual devices have a minimum and maximum operation frequency. The specified parameters for f_{DCOx0} to f_{DCOx7} are valid for all devices.
- The DCO control bits DCO0, DCO1 and DCO2 have a step size as defined in parameter S_{DCO}.
- The modulation control bits MOD0 to MOD4 select how often f_{DCO+1} is used within the period of 32 DCOCLK cycles. f_{DCO} is used for the remaining cycles. The frequency is an average = $f_{DCO} \times (2^{MOD/32})$.
- The ranges selected by R_{Sel4} to R_{Sel5}, R_{Sel5} to R_{Sel6}, and R_{Sel6} to R_{Sel7} are overlapping.

wake-up from lower power modes (LPMx)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(LPM0)}$	Delay time (see Note 22)	V_{CC} = 2.2 V/3 V			100		ns
$t_{(LPM2)}$		V_{CC} = 2.2 V/3 V			100		ns
$t_{(LPM3)}$		$f_{(MCLK)}$ = 1 MHz,	V_{CC} = 2.2 V/3 V			6	µs
		$f_{(MCLK)}$ = 2 MHz,	V_{CC} = 2.2 V/3 V			6	µs
		$f_{(MCLK)}$ = 3 MHz,	V_{CC} = 2.2 V/3 V			6	µs
$t_{(LPM4)}$		$f_{(MCLK)}$ = 1 MHz,	V_{CC} = 2.2 V/3 V			6	µs
		$f_{(MCLK)}$ = 2 MHz,	V_{CC} = 2.2 V/3 V			6	µs
		$f_{(MCLK)}$ = 3 MHz,	V_{CC} = 2.2 V/3 V			6	µs

NOTE 22: Parameter applicable only if DCOCLK is used for MCLK.

JTAG/programming

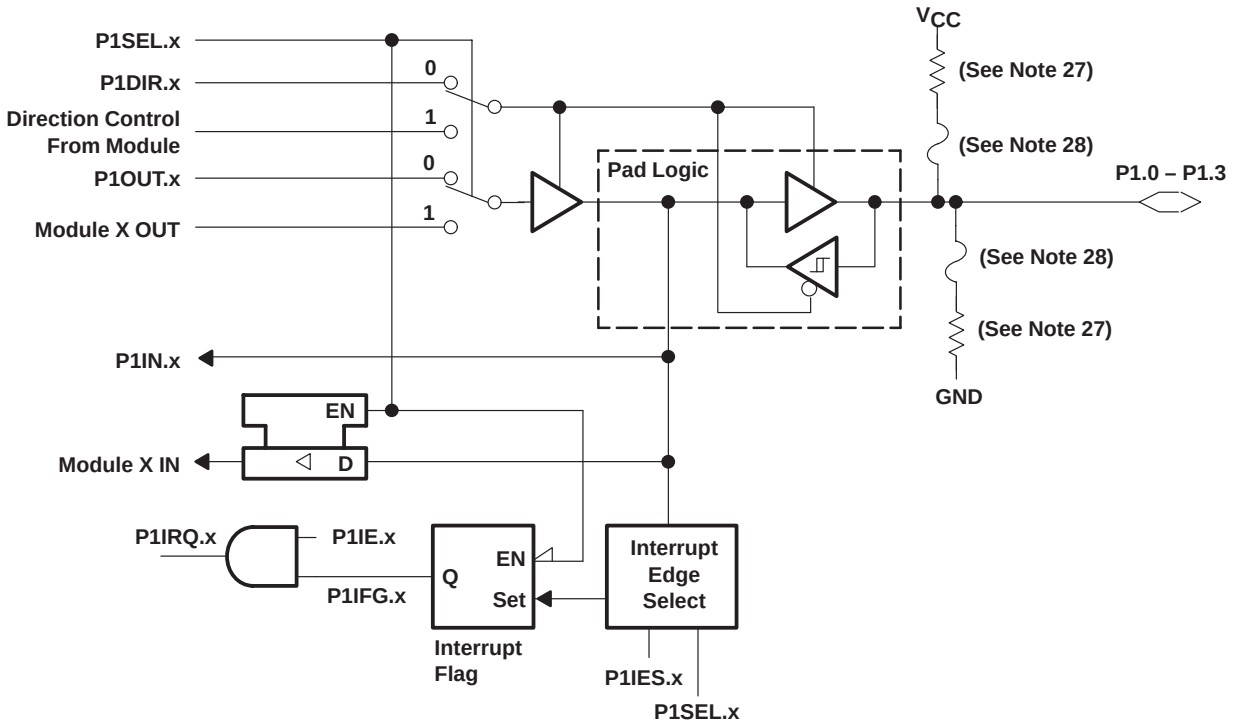
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(TCK)}$	TCK frequency, JTAG/test (see Note 25)	V_{CC} = 2.2 V	dc		5	MHz
		V_{CC} = 3 V	dc		10	MHz
$V_{(FB)}$	Fuse blow voltage, C versions (see Notes 23 and 24)	V_{CC} = 2.2 V/3 V	3.5		3.9	V
$I_{(FB)}$	Supply current on TDI during fuse blow (see Note 24) (C11x1)				100	mA
$t_{(FB)}$	Time to blow the fuse (see Note 24) (C11x1)				1	ms
$I_{(DD-PGM)}$	Current during program cycle (see Note 26)	V_{CC} = 2.7 V/3.6 V, MSP430F11x1		3	5	mA
$I_{(DD-ERASE)}$	Current during erase cycle (see Note 26)	V_{CC} = 2.7 V/3.6 V, MSP430F11x1		3	5	mA
$t_{(retention)}$	Write/erase cycles	MSP430F11x1	10^4	10^5		
	Data retention T_J = 25°C	MSP430F11x1	100			Year

NOTES: 23. The power source to blow the fuse is applied to TDI pin.
24. Once the JTAG fuse is blown, no further access to the MSP430 JTAG/test feature is possible. The JTAG block is switched to bypass mode.
25. $f_{(TCK)}$ may be restricted to meet the timing requirements of the module selected.
26. Duration of the program/erase cycle is determined by $f_{(FTG)}$ applied to the flash timing controller. It can be calculated as follows:
$t_{(word\ write)} = 35 \times 1/f_{(FTG)}$
$t_{(segment\ write,\ byte\ 0)} = 30 \times 1/f_{(FTG)}$
$t_{(segment\ write,\ byte\ 1-63)} = 20 \times 1/f_{(FTG)}$
$t_{(mass\ erase)} = 5297 \times 1/f_{(FTG)}$
$t_{(page\ erase)} = 4819 \times 1/f_{(FTG)}$

APPLICATION INFORMATION

input/output schematic

Port P1, P1.0 to P1.3, input/output with Schmitt-trigger



NOTE: x = Bit/identifier, 0 to 3 for port P1

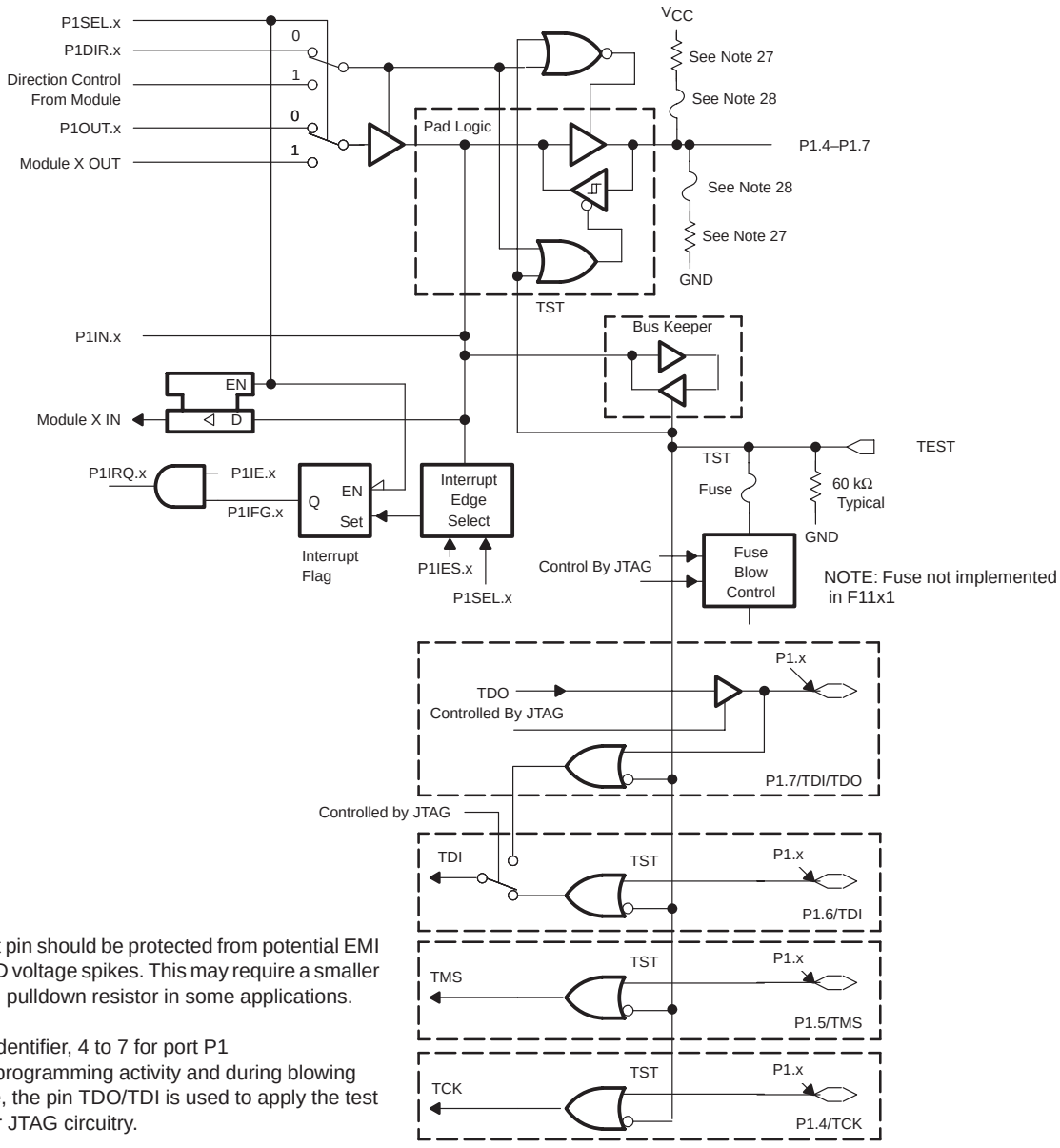
PnSel.x	PnDIR.x	Direction control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P1Sel.0	P1DIR.0	P1DIR.0	P1OUT.0	VSS	P1IN.0	TACLK†	P1IE.0	P1IFG.0	P1IES.0
P1Sel.1	P1DIR.1	P1DIR.1	P1OUT.1	Out0 signal†	P1IN.1	CCI0A†	P1IE.1	P1IFG.1	P1IES.1
P1Sel.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 signal†	P1IN.2	CCI1A†	P1IE.2	P1IFG.2	P1IES.2
P1Sel.3	P1DIR.3	P1DIR.3	P1OUT.3	Out2 signal†	P1IN.3	CCI2A†	P1IE.3	P1IFG.3	P1IES.3

† Signal from or to Timer_A

NOTES: 27. Optional selection of pullup or pulldown resistors with ROM (masked) versions.
28. Fuses for optional pullup and pulldown resistors can only be programmed at the factory (ROM versions only).

APPLICATION INFORMATION

Port P1, P1.4 to P1.7, input/output with Schmitt-trigger and in-system access features



NOTE: The test pin should be protected from potential EMI and ESD voltage spikes. This may require a smaller external pulldown resistor in some applications.

x = Bit identifier, 4 to 7 for port P1
During programming activity and during blowing the fuse, the pin TDO/TDI is used to apply the test input for JTAG circuitry.

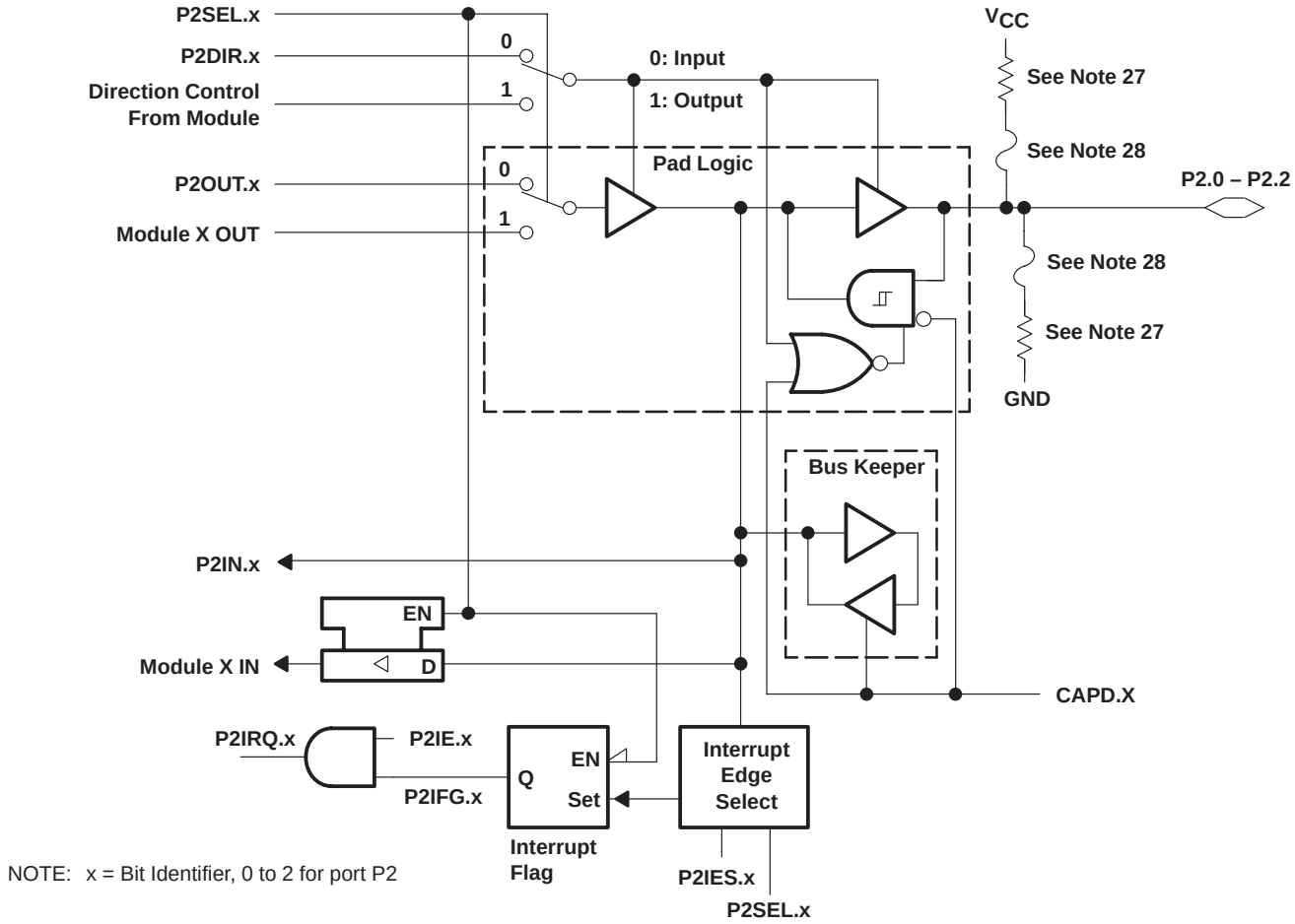
PnSel.x	PnDIR.x	Direction control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P1Sel.4	P1DIR.4	P1DIR.4	P1OUT.4	SMCLK	P1IN.4	unused	P1IE.4	P1IFG.4	P1IES.4
P1Sel.5	P1DIR.5	P1DIR.5	P1OUT.5	Out0 signal†	P1IN.5	unused	P1IE.5	P1IFG.5	P1IES.5
P1Sel.6	P1DIR.6	P1DIR.6	P1OUT.6	Out1 signal†	P1IN.6	unused	P1IE.6	P1IFG.6	P1IES.6
P1Sel.7	P1DIR.7	P1DIR.7	P1OUT.7	Out2 signal†	P1IN.7	unused	P1IE.7	P1IFG.7	P1IES.7

† Signal from or to Timer_A

NOTES: 27. Optional selection of pullup or pulldown resistors with ROM (masked) versions.
28. Fuses for optional pullup and pulldown resistors can only be programmed at the factory (ROM versions only).

APPLICATION INFORMATION

Port P2, P2.0 to P2.2, input/output with Schmitt-trigger



NOTE: x = Bit Identifier, 0 to 2 for port P2

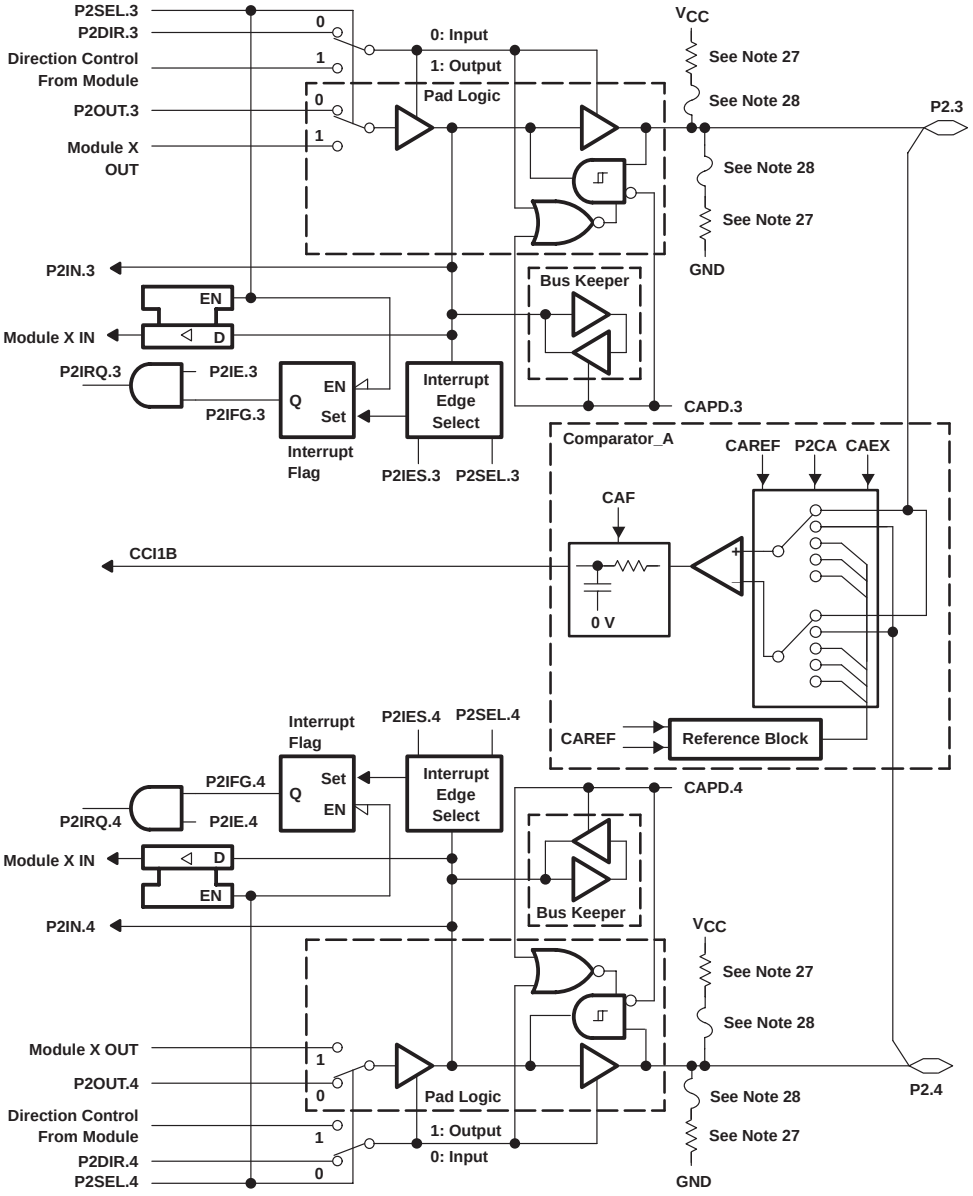
PnSel.x	PnDIR.x	Direction control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.0	P2DIR.0	P2DIR.0	P2OUT.0	ACLK	P2IN.0	unused	P2IE.0	P2IFG.0	P1IES.0
P2Sel.1	P2DIR.1	P2DIR.1	P2OUT.1	VSS	P2IN.1	INCLK†	P2IE.1	P2IFG.1	P1IES.1
P2Sel.2	P2DIR.2	P2DIR.2	P2OUT.2	CAOUT	P2IN.2	CCI0B†	P2IE.2	P2IFG.2	P1IES.2

† Signal from or to Timer_A

NOTES: 27. Optional selection of pullup or pulldown resistors with ROM (masked) versions.
28. Fuses for optional pullup and pulldown resistors can only be programmed at the factory (ROM versions only).

APPLICATION INFORMATION

Port P2, P2.3 to P2.4, input/output with Schmitt-trigger



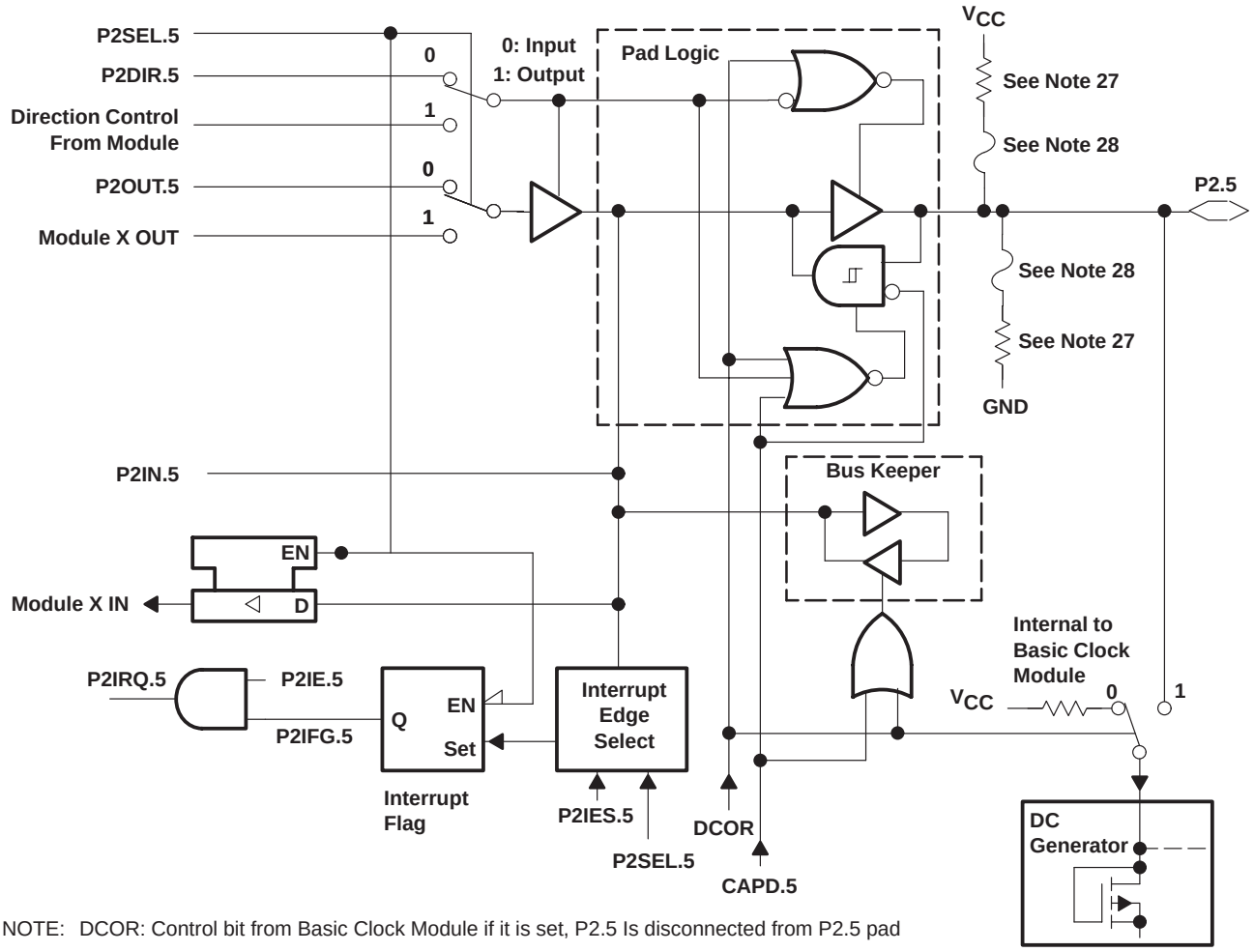
APPLICATION INFORMATION

PnSel.x	PnDIR.x	Direction control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.3	P2DIR.3	P2DIR.3	P2OUT.3	Out1 signal†	P2IN.3	unused	P2IE.3	P2IFG.3	P1IES.3
P2Sel.4	P2DIR.4	P2DIR.4	P2OUT.4	Out2 signal†	P2IN.4	unused	P2IE.4	P2IFG.4	P1IES.4

† Signal from Timer_A

NOTES: 27. Optional selection of pullup or pulldown resistors with ROM (masked) versions.
28. Fuses for optional pullup and pulldown resistors can only be programmed at the factory (ROM versions only).

Port P2, P2.5, input/output with Schmitt-trigger and R_{OSC} function for the Basic Clock module



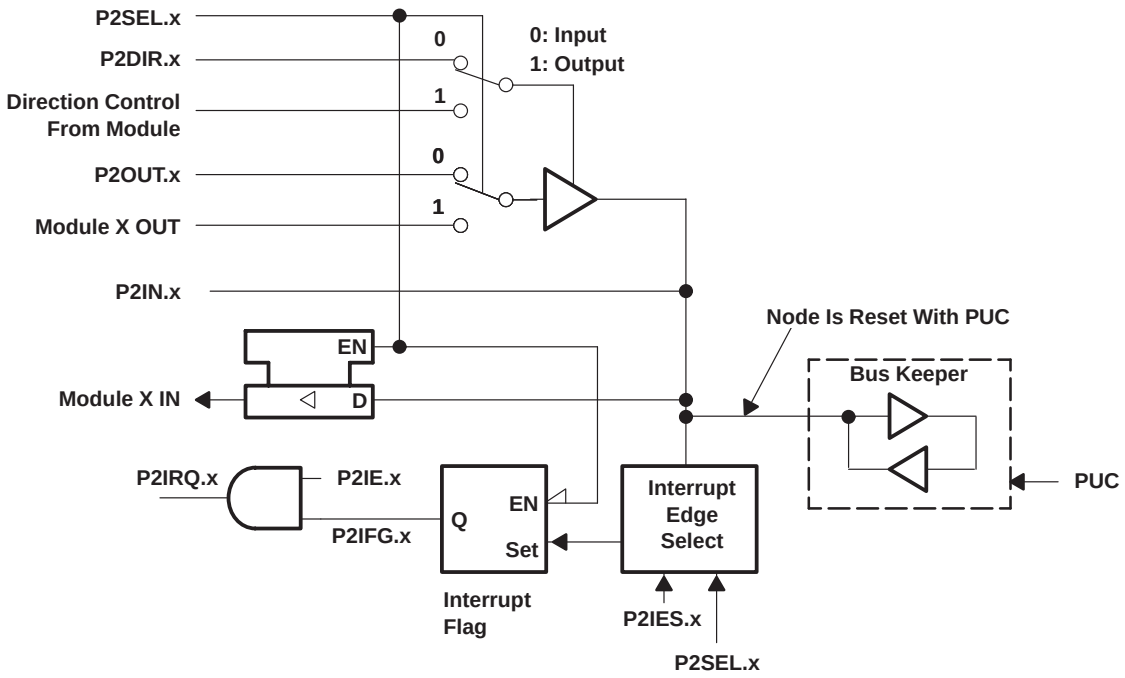
NOTE: DCOR: Control bit from Basic Clock Module if it is set, P2.5 Is disconnected from P2.5 pad

PnSel.x	PnDIR.x	Direction control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.5	P2DIR.5	P2DIR.5	P2OUT.5	VSS	P2IN.5	unused	P2IE.5	P2IFG.5	P2IES.5

NOTES: 27. Optional selection of pullup or pulldown resistors with ROM (masked) versions.
28. Fuses for optional pullup and pulldown resistors can only be programmed at the factory (ROM versions only).

APPLICATION INFORMATION

Port P2, unbonded bits P2.6 and P2.7



NOTE: x = Bit/identifier, 6 to 7 for port P2 without external pins

P2Sel.x	P2DIR.x	Direction control from module	P2OUT.x	Module X OUT	P2IN.x	Module X IN	P2IE.x	P2IFG.x	P2IES.x
P2Sel.6	P2DIR.6	P2DIR.6	P2OUT.6	VSS	P2IN.6	unused	P2IE.6	P2IFG.6	P2IES.6
P2Sel.7	P2DIR.7	P2DIR.7	P2OUT.7	VSS	P2IN.7	unused	P2IE.7	P2IFG.7	P2IES.7

NOTE: A good use of the unbonded bits 6 and 7 of port P2 is to use the interrupt flags. The interrupt flags can not be influenced from any signal other than from software. They work then as a soft interrupt.

JTAG fuse check mode

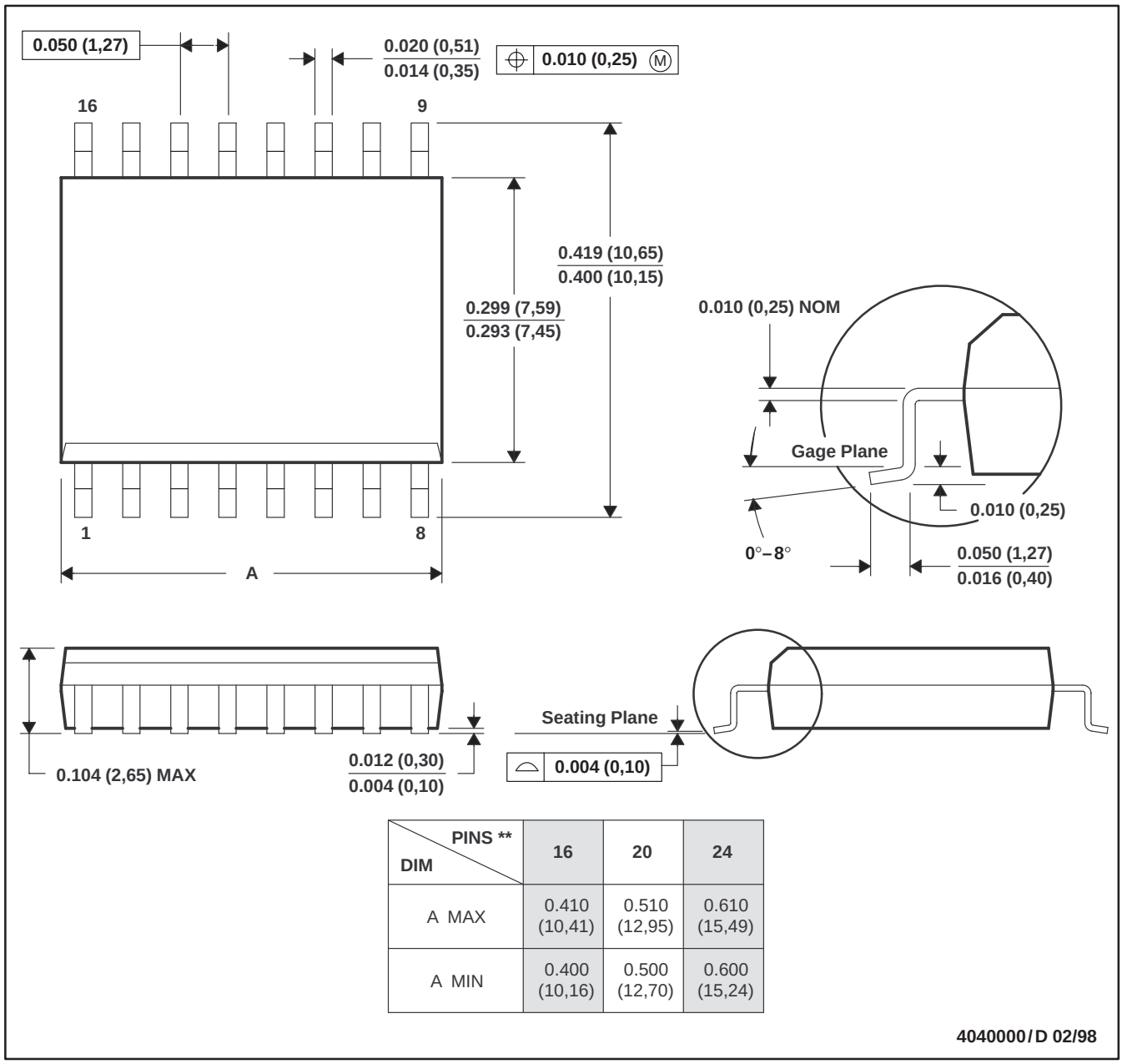
MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is taken back low after a test or programming session, the fuse check mode and sense currents are terminated.

MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN



DIM \ PINS **	16	20	24
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)

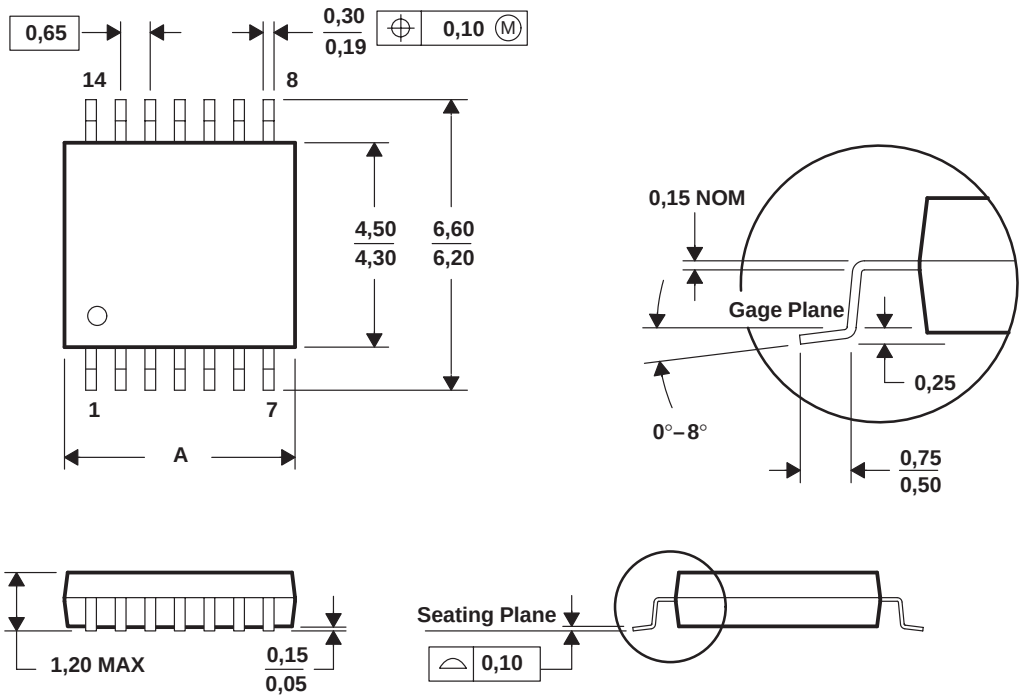
4040000/D 02/98

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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