Texas Instruments

DEM-DAI3010

User's Guide

April 2003

DAV Digital Audio/Speaker

SLEU036

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Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

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Chapter 1

Description

The DEM-DAI3010 is an evaluation board for the PCM3010 (24-bit, 96-kHz ADC and 192-kHz DAC, stereo codec). This board includes not only the PCM3010 but also analog I/O terminals, analog filter circuits, and an S/PDIF digital I/O circuit that is useful for codec evaluation. S/PDIF I/O circuits consist of a 24-bit/96-kHz digital audio interface receiver (DIR1703) and a digital audio interface transmitter (DIT4096), and include optical (TOSLINK) and coaxial S/PDIF digital I/O connectors. Removing shorting plugs from the pins of a header breaks the connection between the S/PDIF I/O circuits and the PCM3010for easier PCM3010 device evaluation.

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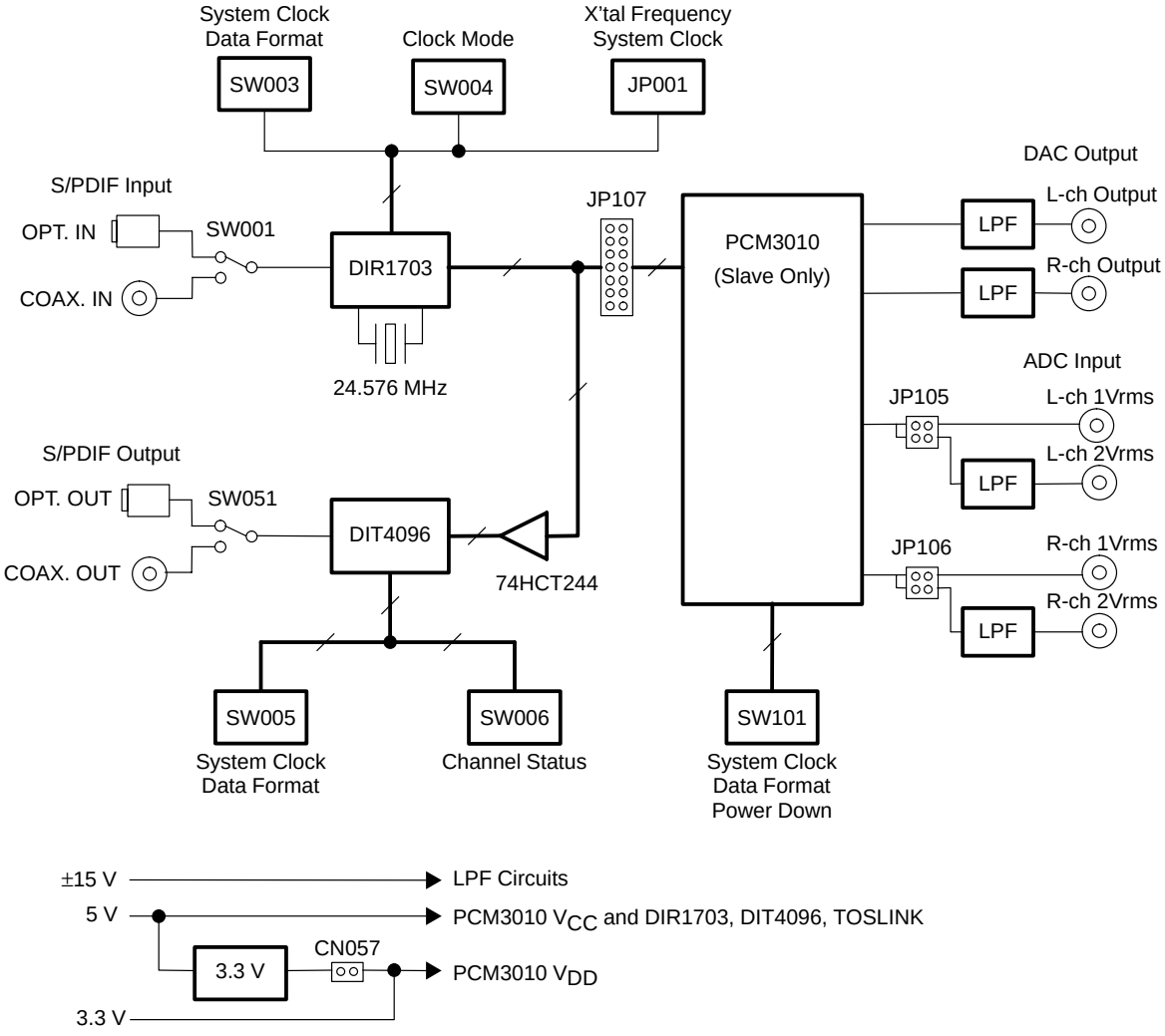
1.1 Block Diagram

Figure 1–1. DEM-DAI3010 Block DIagram



1.2 Use of the DEM-DAI3010

The DEM-DAI3010 is shipped with standard settings preset. Therefore, connecting power supplies (15-V, –15-V and 5-V) is the only requirement to prepare the board for use, unless nonstandard settings are desired.

1.2.1 Initial Settings of the DEM-DAI3010 (at shipping)

Table 1–1. Initial Settings of the DEM-DAI3010 at Shipping

Item	Initial Setting (at shipping)
Power supply voltage	15 V, –15 V, and 5 V (close CN57)
Power supply terminals	CN51–CN55 (open CN56)
Connection of PCM3010 and S/PDIF I/O	DIR1703 and DIT4096 connected with JP107
DIR1703 system clock (SCK)	256 f_S
DIR1703 output audio data format	I^2S
DIR1703 crystal clock frequency	24.576 MHz (load capacitance: 18 pF)
DIT4096 system clock (SCLK)	256 f_S
DIT4096 input audio data format	I^2S
PCM3010 system clock	Automatic selection (no setting required)
PCM3010 I/O audio data format	I^2S
PCM3010 power-down function	Disabled
PCM3010 de-emphasis function (DAC)	Disabled
PCM3010 DAC cutoff frequency	54 kHz (JP101–JP104 are closed)
PCM3010 ADC input terminal selection	CN101, CN102: 2-V rms input (with LPF)

1.2.2 How to Connect Power Supplies to the DEM-DAI3010

The DEM-DAI3010 requires 5-V, 15-V, and –15-V power supplies. Power is supplied to this board by five binding posts (one each for V_{CC} = +5 V, $+AV_{CC}$ = +15 V, $–AV_{CC}$ = –15 V, and two for ground) from stabilized dc power supplies. V_{DD} (3.3 V) for the PCM3010 is normally generated by an onboard voltage-regulator IC from V_{CC} (5 V), but it is possible to supply 3.3 V directly. To do so, open CN057, then supply 3.3 V to CN056 and 5 V to CN054. If 3.3 V is supplied externally, 5 V must still be provided to CN054 in order to supply the analog section of the PCM3010. To avoid latch-up of the PCM3010, ensure that V_{CC} and V_{DD} are powered up simultaneously.

Table 1–2. Power Supply Terminals and Supply Voltage (Depending on CN057 Setting)

Power Terminal	CN057 Closed (Default)	CN057 Open
CN051 (orange)	15 V	15 V
CN052 (green)	0 V (ground)	0 V (ground)
CN053 (blue)	–15 V	–15 V
CN054 (red)	5 V	5 V
CN055 (black)	0 V (ground)	0 V (ground)
CN056 (2-pin connector)	Open (no connection)	3.3 V

1.3 Settings and Connections for Basic Operation

The PCM3010 is an LSI codec containing an ADC and a DAC. Connections and settings depend on the evaluation object (ADC or DAC), and the setup should be checked carefully. Following are example settings for three typical evaluation situations. Note that when using S/PDIF I/O, the optical and coaxial input corresponds to f_S = 96 kHz.

When the DAC section of PCM3010 is evaluated with S/PDIF input signal (the PCM3010 operates as a slave of the DIR1703 PLL clock)

- ❑ Close all pins of JP107 with shorting plugs.
- ❑ Input an S/PDIF signal into the optical (U053) or coaxial (CN059) connector.
- ❑ CN105 (L-ch) and CN106 (R-ch) are the analog signal outputs.
- ❑ Choose an S/PDIF input terminal (optical/coaxial) with the S/PDIF input switch (SW051).
- ❑ Set the clock-mode switch (SW004) to PLL or Auto.
- ❑ The cutoff frequency of the LPF can be changed by JP101, JP102, JP103, and JP104. All these jumpers are shorted at the time of shipment, which sets the cutoff frequency to 20 kHz.

When the ADC section of PCM3010 is evaluated with S/PDIF output signal (the PCM3010 operates as a slave of the DIR1703 crystal clock)

- ❑ Short all pins of JP107 with shorting plugs.
- ❑ Connect an analog signal to CN101/CN102 using an LPF, or to CN103/CN104 using only a coupling capacitor without an LPF.
- ❑ Select the analog input terminal by changing by the settings of JP105 and JP106. (Setup at the time of shipment is for CN101 and CN102.)
- ❑ A Toslink (U052) and a pin jack (CN058) are the S/PDIF digital output terminals. Select the digital output connector by setting the S/PDIF output switch (SW051). Simultaneous use of optical and coaxial outputs is impossible.
- ❑ Set the clock mode switch (SW004) to X'tal. The X'tal mode of DIR1703 is used as a master clock for the ADC and DIT.
- ❑ Set up the channel status data using SW006.
- ❑ Because system clock frequency is 256 f_S, the ADC section operates at f_S = 96 kHz. To operate the ADC section at a different f_S, the crystal (X001) connected to DIR1703 must be changed. The system clock setup can be changed if required. The load capacitance used with the crystal is dependent on the crystal properties. Therefore, when the crystal is changed, the capacitance of C006 and C007 must be selected to match the crystal specification.

When S/PDIF I/O is not used (the PCM3010 is evaluated alone)

- ❑ Remove all shorting plugs attached to JP107.

- ❏ Data and a clock are supplied to the PCM3010 side of JP107.
- ❏ Set up FMT0 and FMT1 of SW101 according to the data format to be used.
- ❏ Set up DEMP0 and DEMP1 of SW101 for the desired de-emphasis of the DAC section and $\overline{\text{PWDN}}$ for the power-down setting.

1.4 Setting Functions

All functions of the devices (PCM3010, DIR1703, DIT4096) on the DEM-DAI3010 are controlled by DIP switches or header pins on this PCB. Therefore, the DEM-DAI3010 does not require a microcontroller or software to transmit data to internal function-setting registers. For specific information on any device, see the data sheet for that device.

1.4.1 Function Setting Switches and Header Pins

Table 1–3. Switches and Header Pins of the DEM-DAI3010

SW/JP No.	Item	Shape
SW001	S/PDIF input selection (optical/coax)	Toggle switch
SW002	Reset of DIR1703 and DIT4096	Pushbutton switch
SW003	Format and system clock setting of DIR1703	4-pole DIP switch
SW004	Output clock selection of DIR1703 (X'tal/Auto/PLL)	Toggle switch
SW005	Format and system clock setting of DIT4096	4-pole DIP switch
SW006	Channel status data setting of DIT4096	10-pole DIP switch
SW051	S/PDIF output selection (optical/coax)	Toggle switch
SW101	Setting of PCM3010 (format, de-emphasis, power down)	5-pole DIP switch
JP001	Crystal frequency and system clock setting of DIR1703	2×5 header
JP107	Connection of S/PDIF I/O circuit and PCM3010	2×7 header
JP101	Cutoff frequency setting of DAC output filter (L-ch)	2×2 header
JP102	Cutoff frequency setting of DAC output filter (R-ch)	2×2 header
JP103	Cutoff frequency setting of DAC output filter (L-ch)	2×1 header
JP104	Cutoff frequency setting of DAC output filter (R-ch)	2×1 header
JP105	Selection of L-ch ADC input terminal (CN101/CN103)	2×2 header
JP106	Selection of R-ch ADC input terminal (CN102/CN104)	2×2 header
CN057	The way of power supply of PCM3010 V_{DD} (3.3 V)	2×1 header

Note: The relation between the DIP switch setting (ON/OFF) and the setting of the IC input port is printed on the PCB. The DIP switch H position does not always set the IC input port level HIGH.

Toggle switch settings are printed on the PCB.

1.4.2 Detailed Explanation of Function Setting Switches and Header Pins

SW001: Switch to select S/PDIF input connector (optical/coaxial). Selection of the S/PDIF signal that is routed to the DIR1703 DIN port.

SW002: Reset switch for the DIR1703 and DIT4096. Pushing this switch resets the DIR1703 and DIT4096 to the initial state. A reset circuit operates at the time of power-supply connection, resetting the DIR1703 and DIT4096 automatically. Therefore, it is not usually necessary to operate this switch.

SW003: Switch for setting the DIR1703 system clock and output data format

SCF1	SCF0	System Clock
L	L	128 f_S
L	H	256 f_S (initial stting)
H	L	384 f_S
H	H	512 f_S

FMT1	FMT0	Output Data Format
L	L	16-bit right-justified, MSB-first
L	H	24-bit right-justified, MSB-first
H	L	24-bit left-justified, MSB-first
H	H	24-bit, I^2S (initial setting)

SW004: Switch for setting the DIR1703 output clock source

Position	Output Clock (SCK, BCK, LRCK)
X'tal	Crystal clock
PLL	PLL clock
Auto	PLL (PLL locked) / crystal (PLL unlocked)

Note: When using the DIR1703 as a master clock for the ADC, this switch must be set to X'tal.

When inputting S/PDIF data demodulated by the DIR1703 into the DAC, set this switch to Auto or PLL.

SW005: Switch for setting the DIT4096 system clock and input data format
Note that the OFF state of this switch sets a HIGH level.

CLK1	CLK0	System Clock
L	L	Not used
L	H	256 f_S (initial setting)
H	L	384 f_S
H	H	512 f_S

FMT1	FMT0	Input Data Format
L	L	24-bit, left-justified, MSB-first
L	H	24-bit, I^2S (initial setting)
H	L	24-bit, right-justified, MSB-first
H	H	16-bit, right-justified, MSB-first

SW006: Switch for setting channel-status data of the DIT4096. Note that the OFF state of this switch sets a HIGH level. Channel status data can set up if needed. Moreover, it is also possible to connect a microcontroller to CN002 and to write in channel-status data with the microcontroller. See the DIT4096 data sheet (TI literature number SBOS225) for details about the contents of a setting.

SW051: Switch to select the S/PDIF output connector (optical/coaxial). An S/PDIF output connector is chosen from optical (U052) and coaxial (CN058). The optical and coaxial output terminals cannot be used simultaneously.

SW101: Switch for setting the functions of the PCM3010. All the functions of PCM3010 are set up with this switch. Functions that can be set are the audio serial data I/O format, the DAC section de-emphasis, and power-down control.

FMT1	FMT0	DAC Input Data Format	ADC Output Data Format
L	L	24-bit, right-justified, MSB-first	24-bit, left-justified, MSB-first
L	H	16-bit, right-justified, MSB-first	24-bit, left-justified, MSB-first
H	L	24-bit, left-justified, MSB-first	24-bit, left-justified, MSB-first
H	H	24-bit, I^2S (initial setting)	24-bit, I^2S (initial setting)

DEMP1	DEMP0	DAC De-Emphasis
L	L	De-emphasis ON, 44.1-kHz
L	H	De-emphasis OFF (initial setting)
H	L	De-emphasis ON, 48-kHz
H	H	De-emphasis ON, 32-kHz

PDOWN	Power-Down Control
L	Power-down mode
H	Nomal operation (initial setting)

JP001: Setup of the crystal frequency and system clock for the DIR1703. When the system clock and the frequency of the crystal for the DIR1703 are changed, a shorting plug is inserted in only one position of JP001 according to the following tables. In order to avoid the loss of a shorting plug which is not being used, the plug is put in the header pin position labeled as OPEN. Because 24.576 MHz is used for a quartz crystal and the system clock is set as the 256 f_S output in initial setting at the time of shipment, the shorting plug is attached in the CSBIT position.

JP001 setting table: DIR1703 system clock and crystal frequency

f_S in X'tal Mode	128 f_S	256 f_S	384 f_S	512 f_S	BRSEL Jumper Position
32 kHz	4.096 MHz	8.192 MHz	12.288 MHz	16.384 MHz	BFRAME
44.1 kHz	5.6448 MHz	11.2896 MHz	16.9344 MHz	22.5792 MHz	EMFLG
48 kHz	6.144 MHz	12.288 MHz	18.432 MHz	24.576 MHz	OPEN (no jumper)
88.2 kHz	11.2896 MHz	22.5792 MHz	33.8688 MHz	45.1584 MHz	URBIT
96 kHz	12.288 MHz	24.576 MHz	36.864 MHz	49.152 MHz	CSBIT

Sample of a of JP001 setting

Target: system clock: 256 f_S and f_S = 48 kHz in the X'tal mode
In the preceding table, the frequency listed where the 256-f_S column intersects the 48-kHz row is 12.288 MHz.

JP101–JP104: Cutoff frequency setting of DAC output post-LPF

The cutoff frequency of the LPF inserted in the DAC output is chosen by these jumpers. The initial setting (all pins shorted) is 54 kHz at the time of shipment. The cutoff frequency with all JP101–JP104 jumper pins open is 108 kHz.

JP105–JP106: Selection of ADC input connectors (CN101 and CN102 or CN103 and CN104)

There are two pairs of ADC input connectors. One pair is coupled to the PCM3010 through capacitors (C121, C122). The other pair is connected through a 103-kHz cutoff LPF and a –6 dB amplifier.

The input connectors are chosen by JP105 and JP106. When the jumpers are on Direct-IN, then the left- and right-channel inputs on CN103 and CN104, respectively, bypass the LPF.

When the jumpers are on –6 db/LPF, then the left- and right-channel inputs on CN101 and CN102, respectively, go through the LPF to the PCM3010.

ADC Full-Scale Input	Connector No.	Details
L-ch 2 V rms	CN101	L-ch ADC input with LPF
R-ch 2 V rms	CN102	R-ch ADC input with LPF
L-ch 1 V rms	CN103	L-ch ADC input without LPF
R-ch 1 V rms	CN104	R-ch ADC input without LPF

JP107: Connection of PCM3010 and S/PDIF I/O circuits

This is the header pin which connects the clock input and data I/O of the PCM3010 with an S/PDIF I/O circuit. All pin positions have shorting plugs installed at the time of shipment.

For evaluating the PCM3010 with other DSPs, DIRs, and DITs, JP107 jumpers are removed. Connection to the alternative devices is made through the row of JP107 pins that is wired to the PCM3010.

CN057: V_{CC} supply selection for the PCM3010

This jumper determines whether V_{CC} for the PCM3010 is supplied from a 3.3-V regulator on this board (U051), or via an external power supply terminal (CN056).

In the initial setting, V_{CC} is supplied from the onboard regulator. When V_{CC} for the PCM3010 is to be provided by an external power supply, the jumper is removed from CN057 and 3.3 V is supplied to CN056. If 3.3 V is supplied externally, 5 V must still be provided to CN054 in order to supply the analog section of the PCM3010.

To avoid latch-up of the PCM3010, ensure that V_{CC} and V_{DD} are switched on simultaneously at start-up.

Chapter 2

Printed-Circuit Board and Schematic

This chapter presents the DEM-DAI3010 printed-circuit board and schematics.

Topic **Page**

2.1 DEM-DAI3010 Printed-Circuit Board

Figure 2–1. DEM-DAI3010 Silkscreen

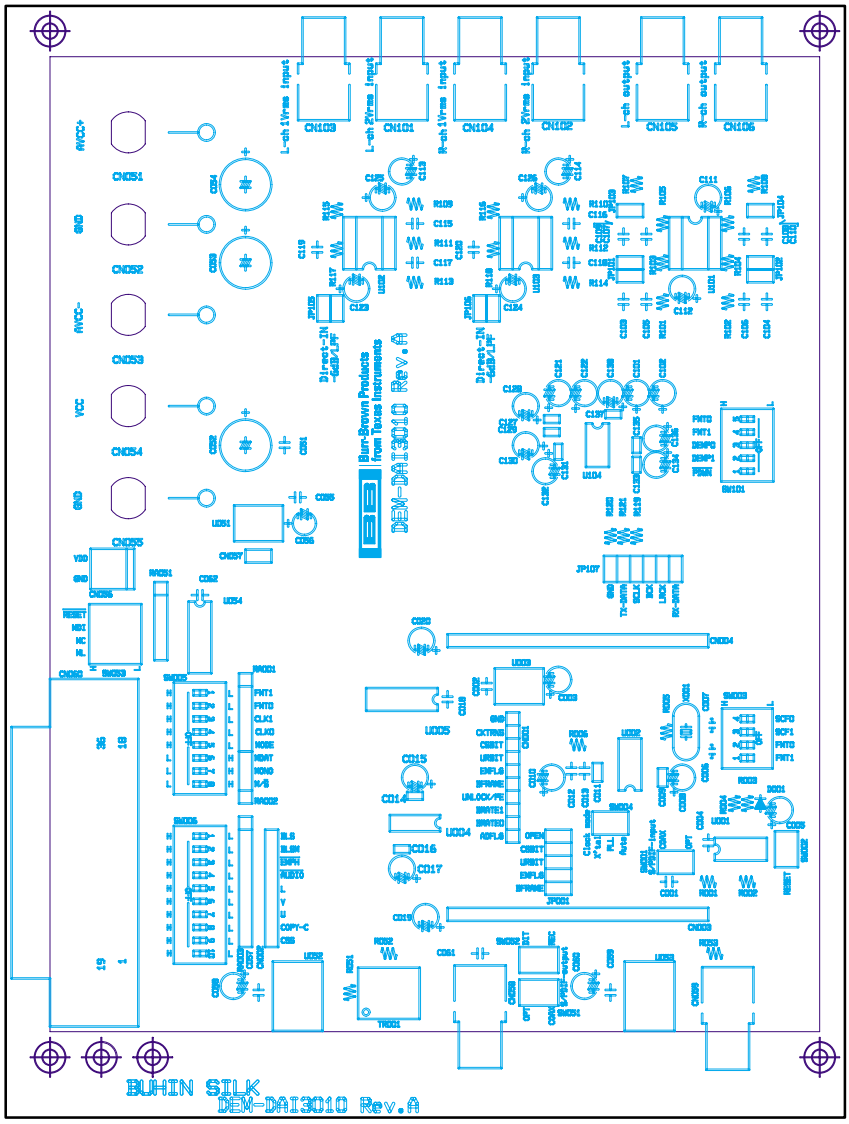


Figure 2–2. DEM-DAI3010—Top View

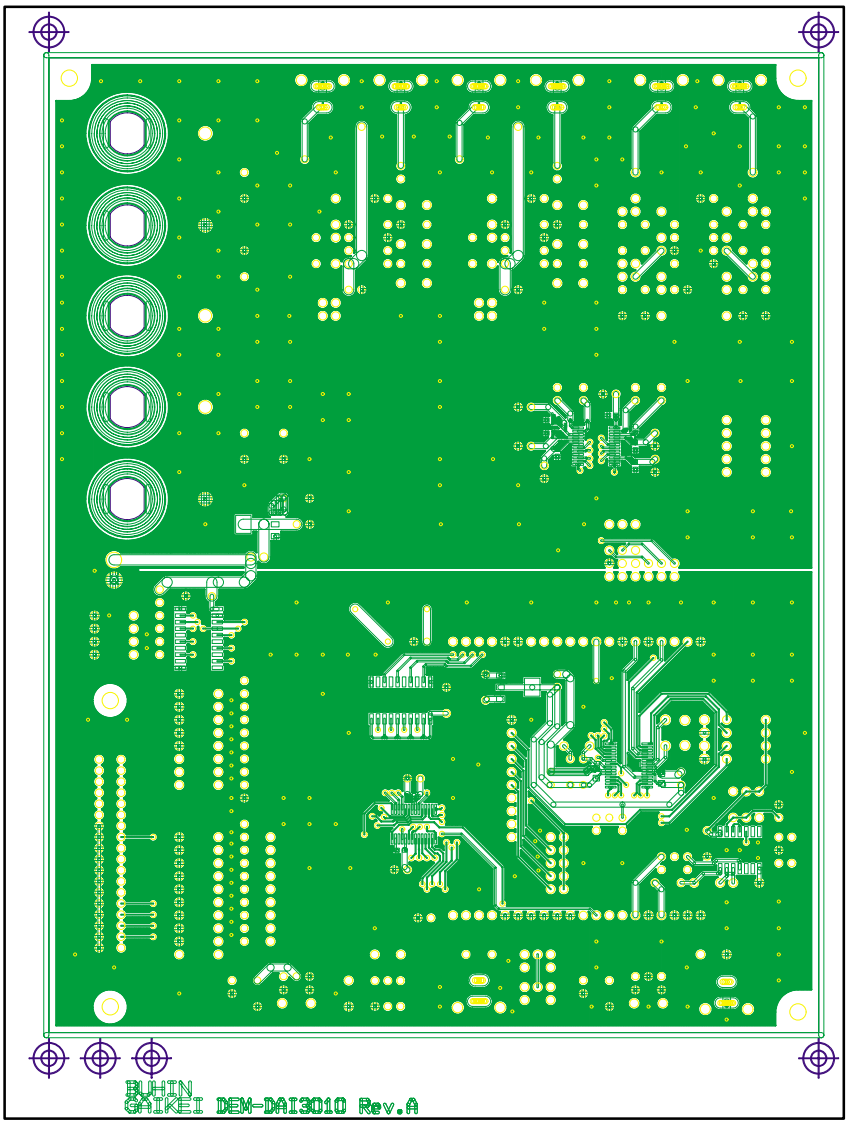
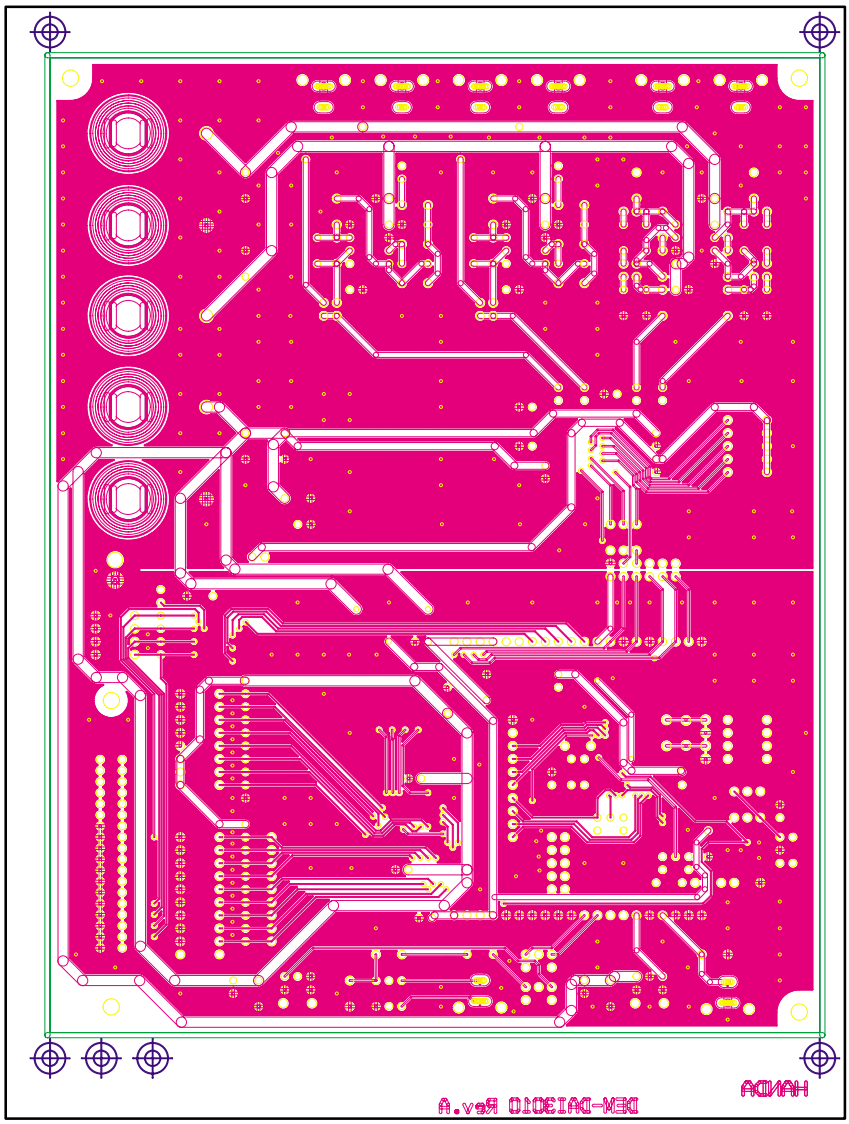


Figure 2–3. DEM-DAI3010—Bottom View



2.2 DEM-DAI3010 Schematics

Figure 2–4. DEM-DAI3010 Analog Section

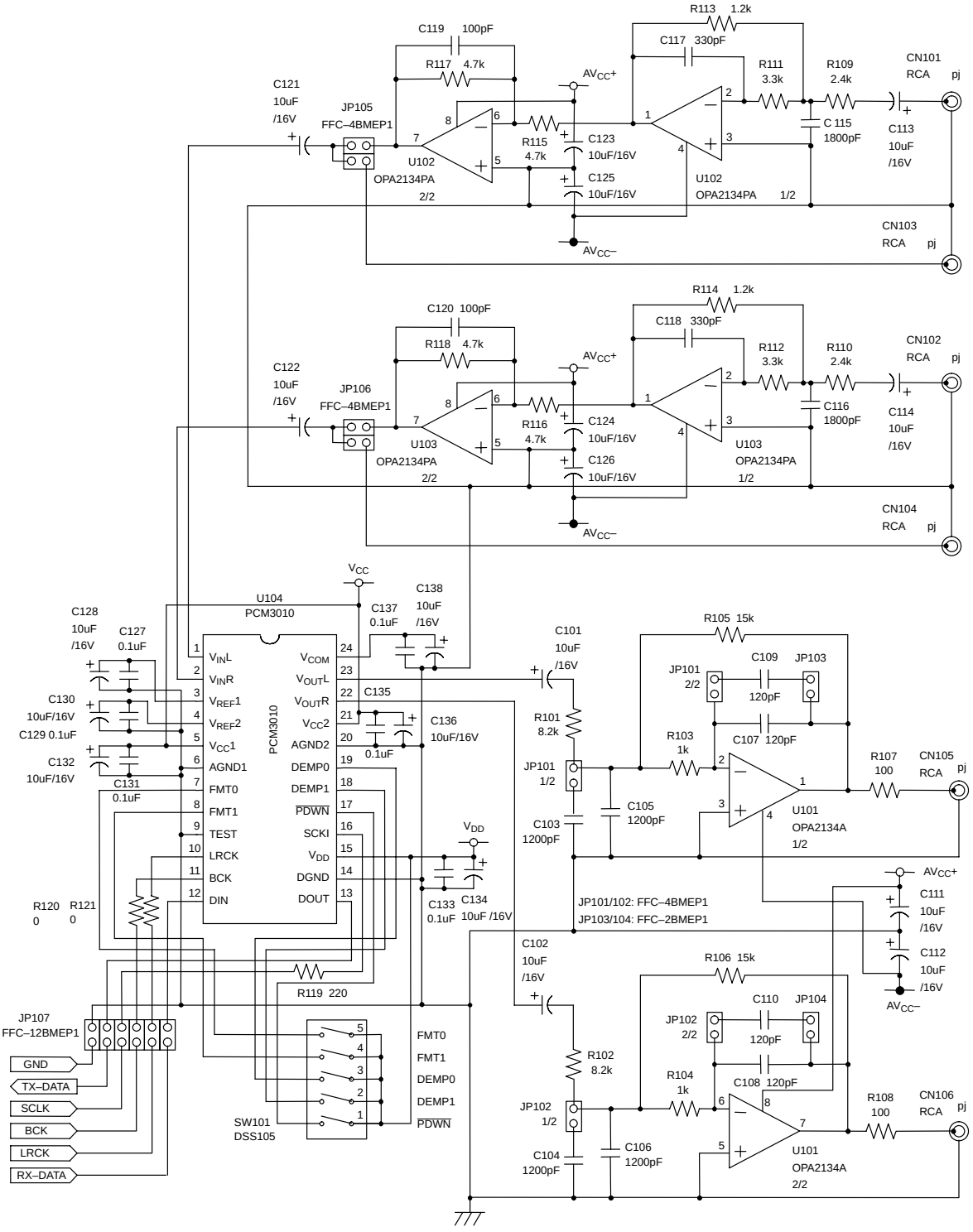


Figure 2–5. DEM-DAI3010 Regulator, Connector and Ext.-I/F

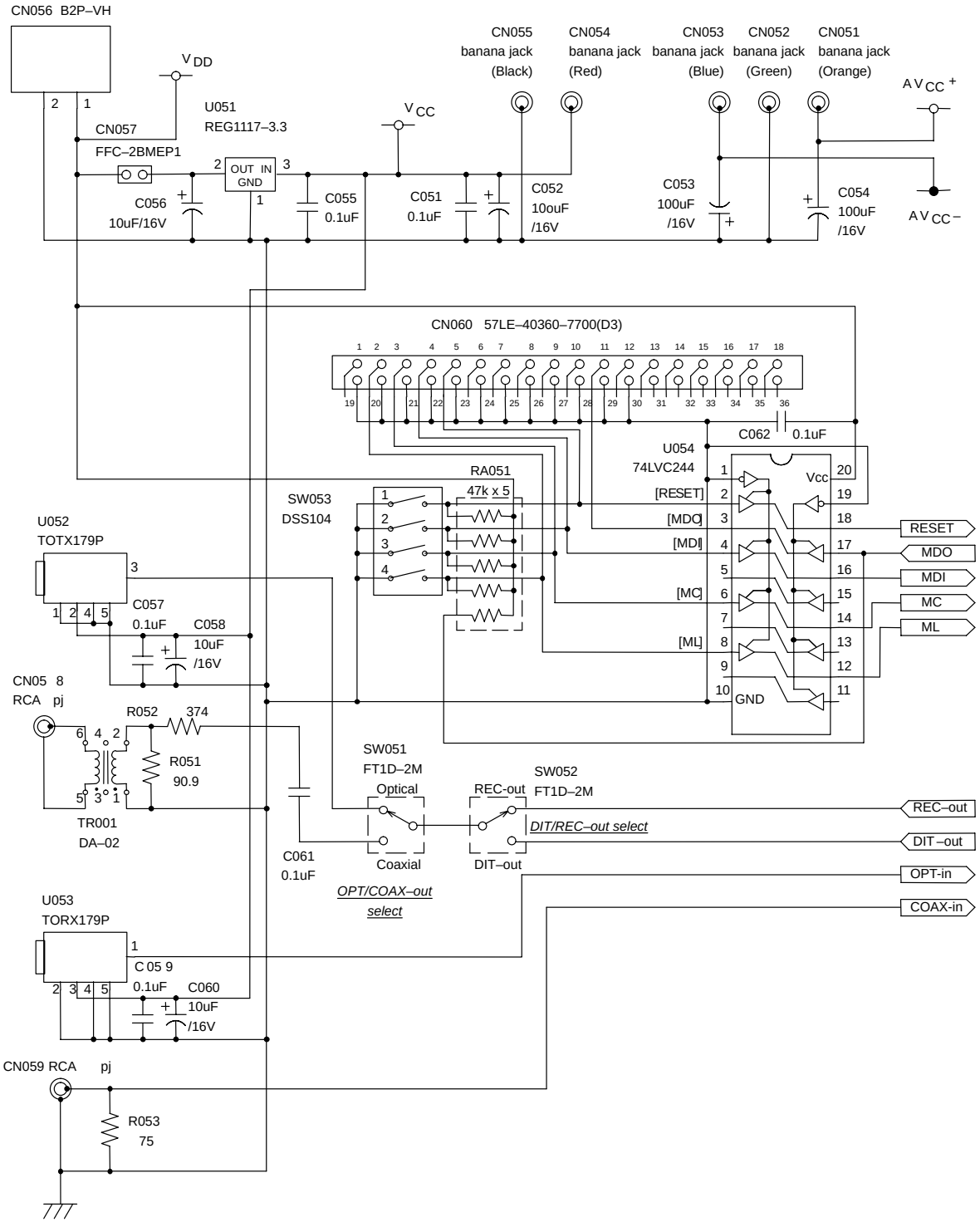


Figure 2–6. DEM-DAI3010 Digital Section (Digital Audio Interface)