Texas Instruments

TPS2151

Power Management With LDO and Dual-Current-Limited Power Switch Evaluation Module

User's Guide

March 2002

PMP Portable Power

SLVU067

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the specified input and output ranges described in the EVM User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

The TPS2151 is one of the four devices in the USB peripheral power management family TPS2140/41/50/51, which integrates both an adjustable linear low-drop voltage regulator (LDO) and a dual-current-limited power switch. The dual-current-limit power switch is designed to eliminate inrush current during power on.

The evaluation module (EVM) can help designers to evaluate the device with several different configurations by manipulating only a couple of onboard mechanical slide switches and a few jumpers.

Users need at least one dc voltage supply and a multimeter or oscilloscope to evaluate the operation of the EVM.

How to Use This Manual

This document contains the following chapters:

- Chapter 1—Introduction
- Chapter 2—Schematic, Bill of Materials, Layout, and Setup
- Chapter 3—Changeable Components and Test Points

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Contents

Figures

Tables

Chapter 1
Introduction

Each device in TPS2140/41/50/51 family integrates a dual-current-limiting power switch and an adjustable low dropout regulator (LDO). Both the switch and LDO limit inrush current by controlling the turnon slew rate and are compatible with USB 1.0 and 2.0 Specifications.

The power switch has a unique dual-current-limiting function that limits the current delivered to its load to less than 100 mA during power on. This feature allows the load to utilize high-value capacitance at the output of the switch, while keeping the inrush current low. When the output voltage from the switch reaches about 93% of the input voltage, the switch power good output goes high, and the switch current limit increases to 800 mA (minimum), at which point higher current loads can be turned on. Therefore the load, other than capacitance, on the switch output must not exceed the lower current limit (50 mA minimum) before the power good output rises to high.

Designers may activate the load by using either the power good signal or another logic signal. The higher current limit provides short circuit protection while allowing the load to draw maximum current from the source.

The switch and LDO function independently provides flexibility in many applications requiring separate core and I/O voltages.

TPS2151 has a 5-V switch and an active high /SW_EN that distinguishes itself from the other three parts (TPS2140, TPS2141, and TPS2150). For a detailed description of functions and characteristics of the TPS2140/41/50/51, refer to the data sheet (literature number SLVS399). You may check the data sheet and ordering information on the Web site:

http://focus.ti.com/docs/prod/productfolder.jhtml?genericPartNumber=TPS2151

To assist designers in the evaluation of the device, an evaluation module (SLVP202) is offered based on TPS2151. The EVM requires 5-V supplies for both the power switch and the LDO. The LDO output voltage is set to 3.3 V by an external resistor divider. Two slide switches and few jumpers on the EVM are provided to change the connections between the LDO and the power switch, so several different application configurations can be evaluated.

The required external parts for the EVM are two input capacitors (on SW_IN and LDO_IN), three output capacitors (on SW_OUT and LDO_OUT), and a resistor divider (two resistors). All of these components are placed inside a white-rectangle box on the EVM.

Chapter 2

Schematic, Bill of Materials, Layout, and Setup

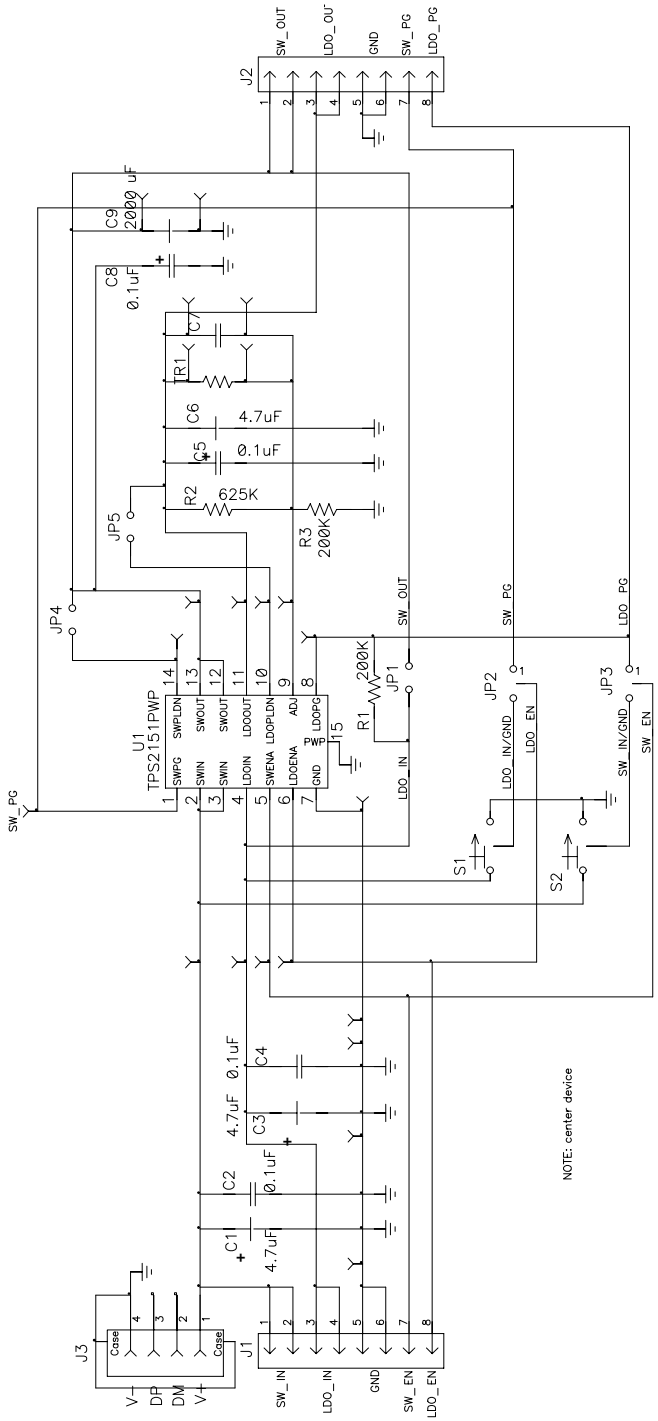
This chapter contains schematics, bill of materials, board layout, and setup of EVM.

Topic **Page**

2.1 Schematic of the EVM

Figure 2–1 shows the schematic of the EVM.

Figure 2–1. Schematic of the TPS2151 Evaluation Module (EVM)



Only C2, C4, C5, C6, C8, R2, and R3 are essential for the TPS2151 to function properly. The rest of the components on the EVM are used for different evaluations of the device. To evaluate the power switch inrush current, a large capacitor C9 can be added on the EVM.

In order to discharge SW_OUT and LDO_OUT quickly, JP4 and JP5 are shorted through jumpers on this EVM. Designers may unplug the jumpers and find the difference. Based on the schematic, the following configurations can be set by switches (S1 and S2), and jumpers on JP1, JP2, and JP3:

1) Independent operation between the switch and LDO: JP1, JP2, and JP3 are floating (no jumpers). In this configuration, header J1 inputs control the switch and the LDO, and the device outputs are connected to header J2. External loads for the switch and the LDO are connected to J2. SW_IN and LDO_IN are powered by a single supply through J1 or by separate supplies.

2) Another independent operation: only JP1 is floating (no jumper). A jumper shorts JP2 from LDO_EN pin to S1 pin, and JP3 is shorted from SW_EN to S2. In this configuration, slide switches S1 and S2 control the switch and the LDO. No external control signals are connected to SW_EN and LDO_EN on header J1. This configuration makes the evaluation easier by sliding the switches S1 and S2 to control the TPS2151 on and off. SW_IN and LDO_IN are powered by a single supply through J1, or by separate supplies.

3) LDO power good to control the power switch: JP1 is still floating, but JP3 is shorted from SW_EN to LDO_PG (no external input SW_EN allowed on J1) JP2 can be configured the same as either case 1) or case 2). The power switch of TPS2151 is controlled by the LDO power good output LDO_PG. The power switch cannot be turned on until the LDO is fully on. SW_IN and LDO_IN are powered by a single supply through J1 or by separate supplies.

4) Switch power good to control the LDO: JP1 is still floating, but JP2 is shorted from LDO_EN to SW_PG (no external input LDO_EN allowed on J1). JP3 can be configured the same as either case 1) or case 2). Then the LDO of TPS2151 is controlled by the switch power good output SW_PG. So the LDO cannot be turned on until the power switch is fully on. SW_IN and LDO_IN are powered by a single supply through J1 or by separate supplies.

5) Switch feeding power to the LDO: JP1 is shorted, and JP2 is shorted from LDO_EN to SW_PG (no external input LDO_EN allowed on J1). JP3 can be configured the same as either case 1) or case 2). Then the LDO is connected to the power switch output and controlled by the switch power good SW_PG. Only one supply is needed for SW_IN through J1, and no external supply is allowed on LDO_IN at J1.

6) Other configurations can be constructed by further manipulating the jumpers, slide switches and the input and output headers (J1 and J2).

Warning

Users must not activate the load on SW_OUT before the SW_PG rises to high, if the load current is higher than 50 mA. Otherwise, the power switch output could not be charged up to SW_IN rail.

2.2 Bill of Materials

The bill of materials (BOM) for the EVM is shown in Table 2–1.

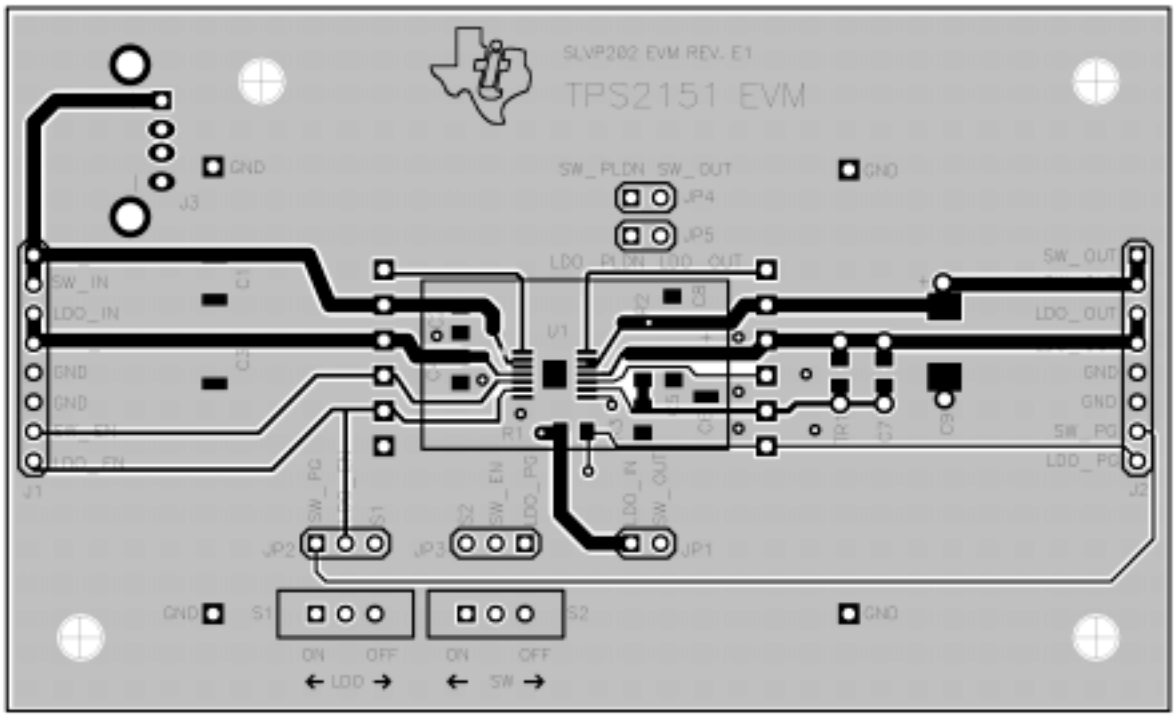
Table 2–1. Bill of Materials of the TPS2151 EVM (SLVP202)

Count	RefDes	Description	Size	MFR	Part Number
3	C1, C3, C6	Capacitor, Tantalum, 4 μF, 10 V, 20%	B Case	Panasonic	29D475X0010B2T
4	C2, C4, C5, C8	Capacitor, ceramic 0.1 μF, 50 V, X7R 10%	805	Kemet	C0805C104KRAC7800
0	C7	Note: Needed only if the LDO voltage is set to be below 3 V, refer to the data sheet			
0	C9	Note: Extra high-value capacitor on SW_OUT			
2	J1, J2	Header, 8 pin, 100 mil spacing, (36-pin strip)	0.100 x 8”	Sullins	PTC36SAAN
0	J3	Connector, USB downstream (Type A)	0.52 x 0.57”	Molex	87531–001
3	JP1, JP4, JP5	Header, 2 pin, 100 mil spacing	0.100 x 2”	Sullins	PTC36SAAN
2	JP2, JP3	Header, 3 pin, 100 mil spacing	0.100 x 3”	Sullins	PTC36SAAN
2	R1, R3	Resistor, chip, 200 KΩ, 1/10 W, 5%	805	Std	Std
1	R2	Resistor, chip, 625 kΩ, 1/10 W, 5%	805	Std	Std
2	S1, S2	Switch, 1P2T, slide, PC-mount, 200 mA	0.46 x 0.16”	E_Switch	EG1218
5	TP1, TP2, TP3, TP4, TP9	Test point, black, 1 mm	0.038”	Farnell	240–333
0	TP16, TP17, TP18, TP19, TP20, TP21	Post, wire wrap, 0.043 press-fit Note: A/A	0.015–0.025” pins	Mill-Max	1045–3–17–15–30–14–02–0
11	TP5, TP6, TP7, TP8, TP10, TP11, TP12, TP13, TP14, TP15, TP22	Test point, red, 1 mm	0.038”,	Farnell	240–345
0	TR1	Note: Paralleling with R2 to set LDO output voltage lower than 3.3 V			
1	U1	IC, USB high powered, with LDO	PWP14	TI	TPS2151PWP

2.3 Layout of the EVM

Figure 2–2 illustrates the placement of the components on the top-layer of the TPS2151 EVM. All the components are placed on the top layer only. The bottom layer is mainly a ground plane except for a few short traces. The center rectangle box includes all the essential parts for the EVM.

Figure 2–2. Top Layer of the EVM and Placement of the Components



2.4 Setup of the EVM

For proper operation of the EVM, please follow these steps for any evaluation:

1) Verify that the power supply voltages are in the required ranges: less than 5.5 V but higher than 4.1 V. Make sure the supplies have the capability to supply the current that the loads need. Turn off the supplies.

2) In order to discharge SW_OUT and LDO_OUT quickly, JP4 and JP5 are shorted through jumpers on this EVM. Designers may unplug the jumpers and find out the difference. Set one of the six configurations as explained in section 2.1. Then connect one or two supplies to the EVM through J1.

3) Connect loads to the outputs (between SW_OUT and GND, and between LDO_OUT and GND) through J2 if required. However, users can test a number of characteristics of the controller without external loads.

If users need to evaluate the dual-current limit for large output capacitance, a surface-mount D-size cap footprint is provided (C9) for that purpose. Or, you may connect the cap from SW_OUT to GND at J1.

The LDO output on the EVM is preset to 3.3V by resistor R2 and R3. If a lower output is required, either R2 can be replaced with a lower resistance resistor, or add an appropriate resistor on TR1 footprint. Refer to the data sheet to get the correct resistance value.

4) Turn on and turn off the power switch and LDO based on the configuration you choose.

5) Test points are provided for oscilloscope probes and/or multimeters.

Chapter 3

Changeable Components and Test Points

C1, C2, C3, C4—input capacitors, at least 0.047μF total on each input.

C5, C6, C8, C9—load capacitors, vary according to loads, but C5 plus C6 must be at least 4.7 μF.

R2—top resistor of the resistor divider, refer to data sheet for its resistance value.

R1—LDO_PG pullup resistor, must be at least 1kΩ.

A total of 16 test points are provided. Besides four black test points on the four corners of the EVM, there are 12 more test points (11 red and 1 black) residing on two sides of the white rectangle box at the center of the EVM. Their respective testing signals are listed in the following table, when looking at the EVM from top down. The test-point orders are listed from top to bottom on both sides.

Table 3–1. Test Points and Test Signals

Left-side Test-Point Order	Color	Signal	Right-side Test-Point Order	Color	Signal
1		SW_PG	1	Red	SW_PLDN
2	Red	SW_IN	2	Red	SW_OUT
3	Red	LDO_IN	3	Red	LDO_OUT
4	Red	SW_EN	4	Red	LDO_PLDN
5	Red	LDO_EN	5	Red	ADJ
6	Black	GND	6	Red	LDO_PG