User's Guide
SLVU364–March 2010

TPS62065/67EVM

This user's guide describes the characteristics, operation, and use of the TPS62065-67EVM-347 evaluation module (EVM). The TPS62065-67EVM-347 is a fully assembled and tested platform for evaluating the performance of both the TPS62065 and TPS62067 2-A step-down converters. This document includes schematic diagrams, printed circuit board (PCB) layout, bill of materials, and test data. Throughout this document, the abbreviations *EVM*, *TPS62065/67EVM*, and the term *evaluation module* are synonymous with the TPS62065-67EVM-347 unless otherwise noted.

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1 Introduction

The TPS62065-67EVM-347 is a fully assembled and tested pair of PCBs for evaluating the TPS62065 and TPS62067 2-A step-down converters. The EVM comes configured with both a TPS62065 IC and a TPS62067 IC; there are two PCBs, one for each respective step-down converter IC.

1.1 Features

- Input voltage range: 3.0 V to 6.0 V
- Adjustable output voltage: 0.8 V to VIN
- Up to 2.0-A output current
- 3-MHz switching frequency
- Power Good output (TPS62067EVM only)
- Clock dithering

1.2 TPS62065/67 Applications

The TPS62065 and TPS62067 step-down converters are ideal for these applications:

- POL
- Digital cameras
- PDAs, pocket PCs
- Portable media players
- DSP supply

2 Electrical Performance Specifications

Table 1 summarizes the TPS62065/67EVM performance specifications.

Table 1. TPS62065/67EVM Performance Characteristics

Parameter	Symbol	Notes and Conditions	Min	Typ	Max	Units
Input Characteristics						
Input Voltage	VIN		3.0		6.0	V
Input Undervoltage Lockout (UVLO)	V_{IN_UVLO}	Falling	1.73	1.78	1.83	V
		Rising	1.9	1.95	1.98	V
Output Characteristics						
Line Regulation				0		%/V
Load Regulation				–0.5		%/A
Output Current 1	$I_{OUT}1$	VIN = 3.0 V to 6.0 V			2000	mA
Forward Current Limit High-Side and Low Side MOSFET	I_{LIMF}	VIN = 3.0 V to 6.0 V	2300	2750	3300	mA
Systems Characteristics						
Switching Frequency	f_{SW}		2600	3000	3400	kHz
Peak Efficiency	η_{pk}	VIN =Nom			95	%
Full Load Efficiency	η	VIN = 5.0 V, VIN = 1.8 V I_{OUT} = 2,000 mA		82		%

3 TPS62056/67EVM Schematic

Figure 1 shows the TPS62065EVM schematic. Figure 2 illustrates the TPS62067EVM schematic.

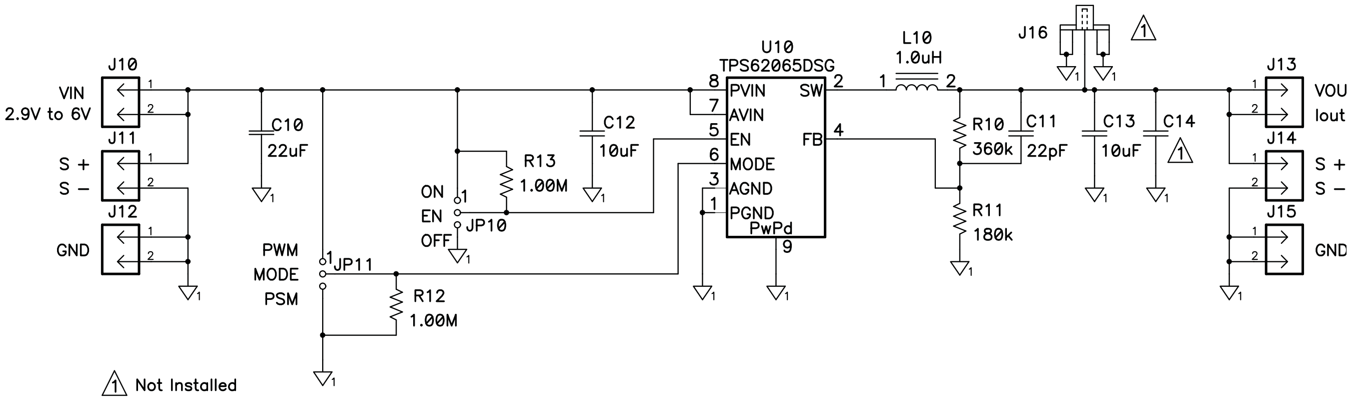


Figure 1. TPS62065EVM Schematic

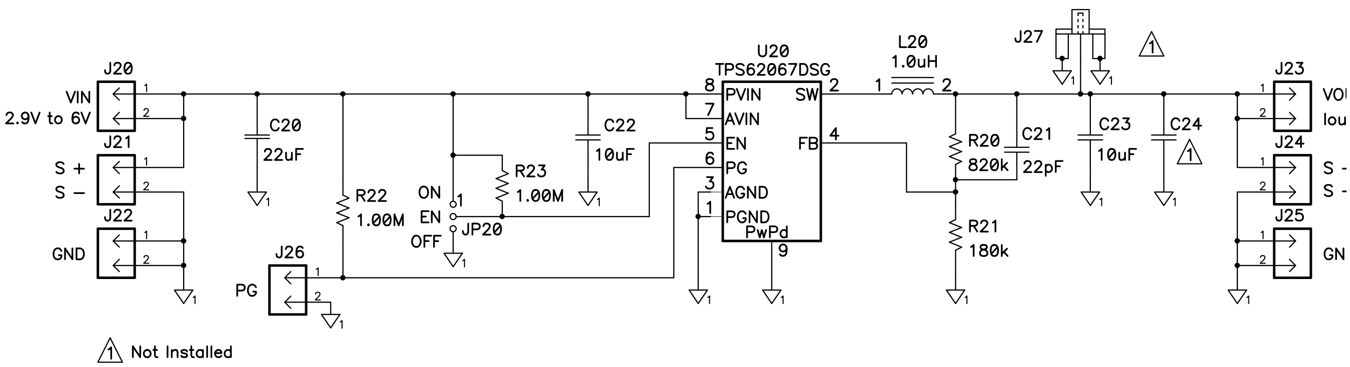


Figure 2. TPS62067EVM Schematic

NOTE: These diagrams are provided for reference only. See Table 2, the Bill of Materials, for specific component values.

4 Connector and Test Point Descriptions

4.1 *Enable Jumpers/Switches: TPS62065EVM*

4.1.1 J10 VIN

This header is the positive connection to the input power supply. The power supply must be connected between J10 and J12 (GND). The leads to the input supply should be twisted and kept as short as possible. The input voltage must be between 3.0 V and 6.0 V.

4.1.2 J11 S+/S–

J11 S+/S– are the sense connections for the input of the converter. Connect a voltmeter, or the sense connection of a power supply or oscilloscope, to this header.

4.1.3 J12 GND

This header is the return connection to the input power supply. Connect the power supply between J12 and J10 (VIN). The leads to the input supply should be twisted and kept as short as possible. The input voltage must be between 3.0 V and 6.0 V.

4.1.4 J13 VOUT

This header is the positive output of the step-down converter. The output voltage of the TPS62065 is adjustable with feedback resistors R10 and R11. On the EVM, the output voltage is set to 1.8 V by default.

NOTE: A feed-forward capacitor is required. Refer to the TPS6206x data sheet (SLVS833) for detailed information.

4.1.5 J14 S+/S–

J14 S+/S– are the sense connections for the output of the converter. Connect a voltmeter, or the sense connection of an electronic load or oscilloscope, to this header.

4.1.6 J15 GND

J15 is the return connection of the converter. A load can be connected between J15 and J13 (V_{OUT}). The converter is capable of carrying a load current up to 2000 mA.

4.1.7 JP10 EN

This jumper enables/disables the TPS62065 on the EVM. Shorting jumper JP10 between the center pin and *On* turns on the unit. Shorting the jumper between center pin and *Off* turns the unit off. A 1-MΩ pull-up resistor is connected between VIN and EN. Removing jumper JP10 turns on the converter.

4.1.8 JP11 MODE

This jumper enables/disables the power-saving mode under light loads. Shorting jumper JP11 between the center pin and PWM disables the power-saving mode; If the power save mode is disabled, the converter operates in forced PWM mode over the entire load current range. Shorting the jumper between the center pin and PWM/PSM enables the power-saving mode. The device operates in power-saving mode under light load conditions. See the TPS6206x data sheet (SLVS833) for a detailed description of this configuration. A 1-MΩ pulldown resistor is connected between GND and MODE. By removing JP11, the converter operates in power-saving mode under light load conditions.

4.1.9 J16 VOUT (SMA)

This SMA connector is connected to the output voltage of the TPS62065. It can be used to easily analyze the noise spectrum of the output voltage with a spectrum analyzer. By default, J16 is not assembled on the EVM.

4.2 Enable Jumpers/Switches: TPS62067EVM

4.2.1 J20 VIN

This header is the positive connection to the input power supply. The power supply must be connected between J10 and J12 (GND). The leads to the input supply should be twisted and kept as short as possible. The input voltage must be between 3.0 V and 6.0 V.

4.2.2 J21 S+/S–

J21 S+/S– are the sense connections for the converter input. Connect a voltmeter, or the sense connection of a power supply or an oscilloscope, to this header.

4.2.3 J22 GND

This header is the return connection to the input power supply. Connect the power supply between J22 and J20 (VIN). The leads to the input supply should be twisted and kept as short as possible. The input voltage must be between 3.0 V and 6.0 V.

4.2.4 J23 VOUT

This header is the positive output of the step-down converter. The output voltage of the TPS62067 is adjustable with the feedback resistors R20 and R21. On the EVM, the output voltage is set to 3.3 V by default.

NOTE: There is a feed-forward capacitor required. Refer to the TPS6206x data sheet (SLVS833) for detailed information.

4.2.5 J24 S+/S–

J24 S+/S– are the sense connections for the converter output. Connect a voltmeter, or the sense connection of an electronic load or an oscilloscope, to this header.

4.2.6 J25 GND

J25 is the return connection of the converter. A load can be connected between J25and J23 (V_{OUT}). The converter is capable of a load up to 2,000 mA load current.

4.2.7 J26 PG

PG (Power Good) is an open-drain output. A 1-MΩ pull-up resistor is connected between VIN and PG. This circuit is active once the device is enabled. It is driven by an internal comparatir that is connected to the FB voltage. The PG output provides a high-level output once the FB voltage reaches 95% of its nominal value. The PG output provides a low-level output when the FB voltage falls below 90% of its nominal value.

NOTE: This function is only available on the TPS62067EVM.

4.2.8 JP20 EN

This jumper enables/disables the TPS62067 device on the EVM. Shorting jumper JP20 between the center pin and *On* turns on the unit. Shorting the jumper between center pin and *Off* turns the unit off. A 1-MΩ pull-up resistor is connected between VIN and EN. Removing jumper JP20 also turns on the converter.

4.2.9 J27 VOUT (SMA)

This SMA connector is connected to the output voltage of the TPS62067. It can be used to easily analyze the noise spectrum of the output voltage with a spectrum analyzer. By default, J27 is not assembled on the EVM.

5 Test Configuration

5.1 Hardware Setup

Figure 3 illustrates a typical hardware test configuration.

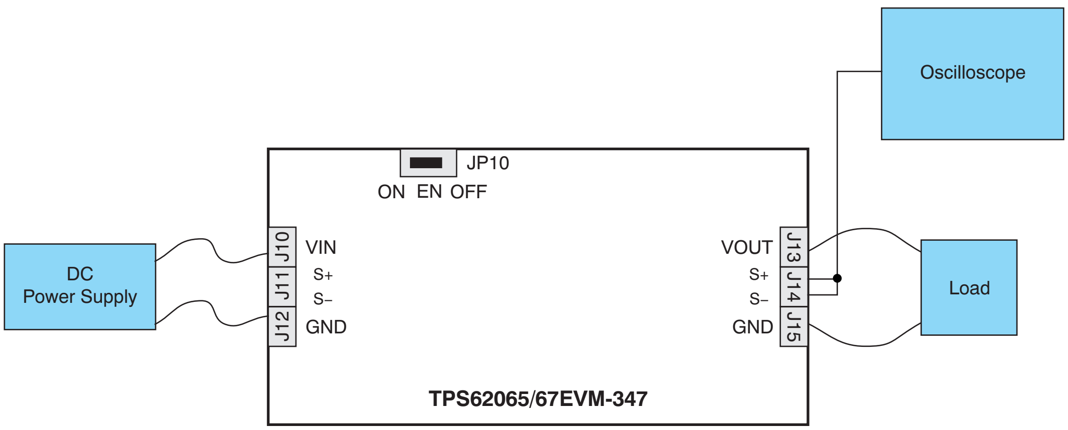


Figure 3. Hardware Board Connection

5.2 Testing Procedure

Follow these procedures when configuring the EVM for testing.

CAUTION

Many of the components on the TPS62065/67EVM-347 are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap, bootstraps, or mats at an approved ESD workstation. An electrostatic smock and safety glasses should also be worn.

1. Connect a dc power supply between J10 and J12 on the TPS62065EVM, or J20 and J22 on the TPS62067EVM. Please note that the input voltage should be between 3.0 V and 6.0 V. Keep the wires from the input power supply to the EVM as short as possible and twisted.
2. Connect a dc voltmeter or oscilloscope to the output sense connection of the EVM (J14 on the TPS62065EVM, J24 on the TPS62067EVM).
3. A load can be connected between J13 and J15 on the TPS62065EVM, or J23 and J25 on the TPS62067EVM.
4. To enable the converter, connect the shorting bar on JP10 (JP20) between EN and ON on the TPS62065EVM (TPS62067EVM).
5. The TPS62065EVM has a feature to allow the user to switch between Power-Save Mode under light loads and forced PWM mode; this feature is enabled or disabled with jumper JP11. This feature is only available on the TPS62065EVM.
6. The TPS62067EVM has a PG (Power Good) output. The PG pin on the TPS62067 is connected to J26. PG is an open-drain output. The output is pulled up with a 1-MΩ pull-up resistor (R22) to VIN. This feature is only available on the TPS62067EVM.

6 TPS62065/67EVM Test Data

Figure 4 through Figure 11 present typical performance curves for the TPS62065/67EVM. Actual performance data can be affected by measurement techniques and environmental variables; therefore, these curves are presented for reference and may differ from actual results obtained by some users.

6.1 Efficiency

Figure 4 shows the typical efficiency performance for the TPS62065 and TPS62067.

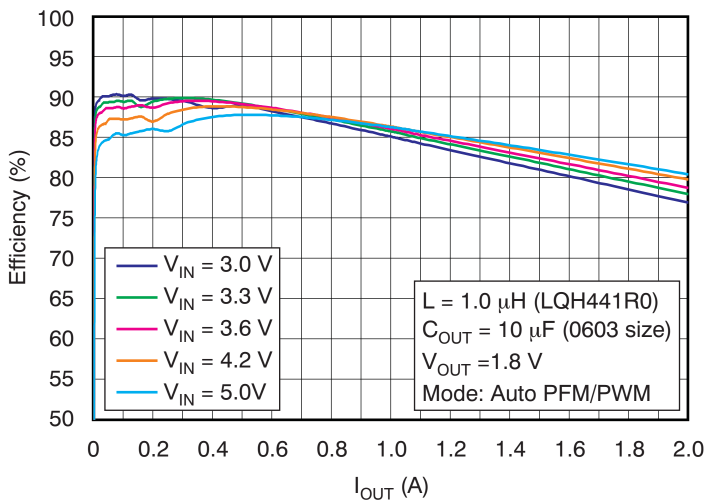
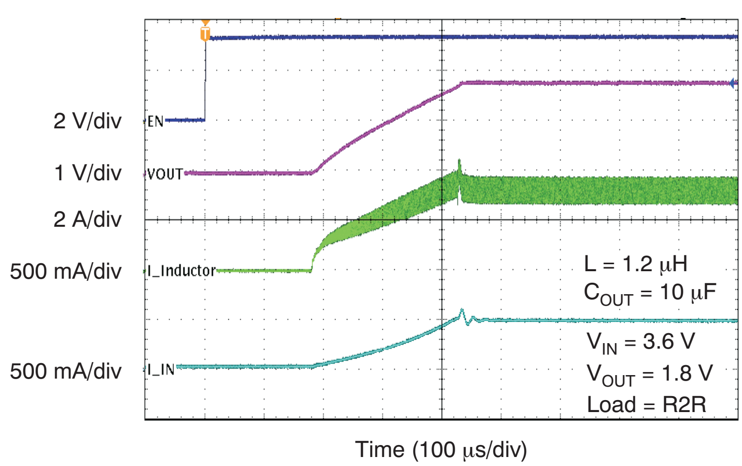


Figure 4. TPS62065, TPS62067 Efficiency vs Load Current

6.2 Start-up: TPS62065

Figure 5 shows the typical start-up performance for the TPS62065 using the TPS62065EVM.

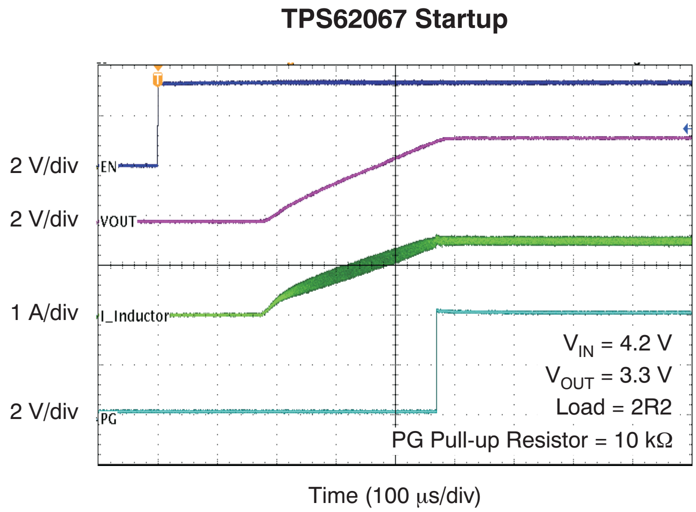


Conditions: VIN = 3.6 V, V_{OUT} = 1.8 V

Figure 5. TPS62065 Startup into 2.2-Ω Load

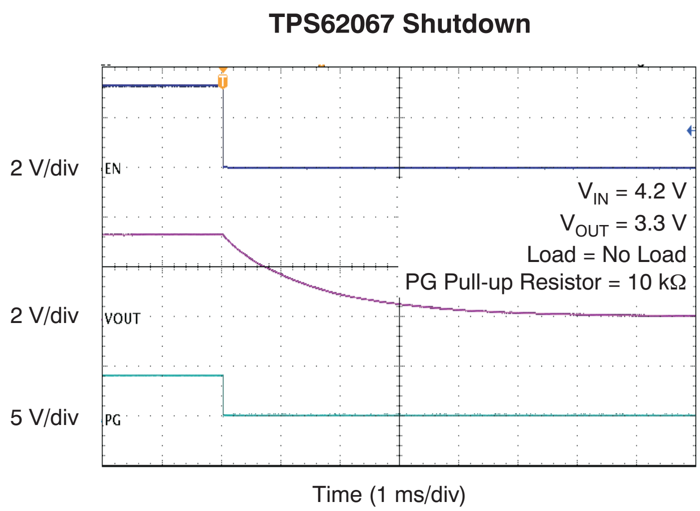
6.3 Start-up and Shutdown: TPS62067

Figure 6 and Figure 7 illustrate the typical start-up and shutdown behavior, respectively, for the TPS62067, using the TPS62067EVM.



Conditions: VIN = 4.2 V, V_{OUT} = 3.3 V

Figure 6. TPS62067 Startup into 2.2-Ω Load



Conditions: VIN = 4.2 V, V_{OUT} = 3.3 V

Figure 7. TPS62067 Shutdown: No Load

6.4 Output Voltage Ripple (Power-Save Mode)

Figure 8 and Figure 9 show the typical output voltage ripple for the TPS62065 in PFM and PWM modes, respectively, with the TPS62065EVM.

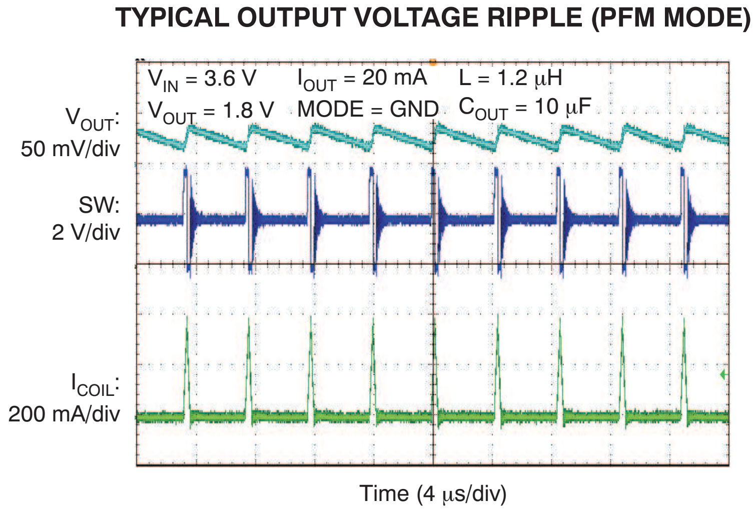


Figure 8. TPS62065 Output Voltage Ripple (PFM Mode)

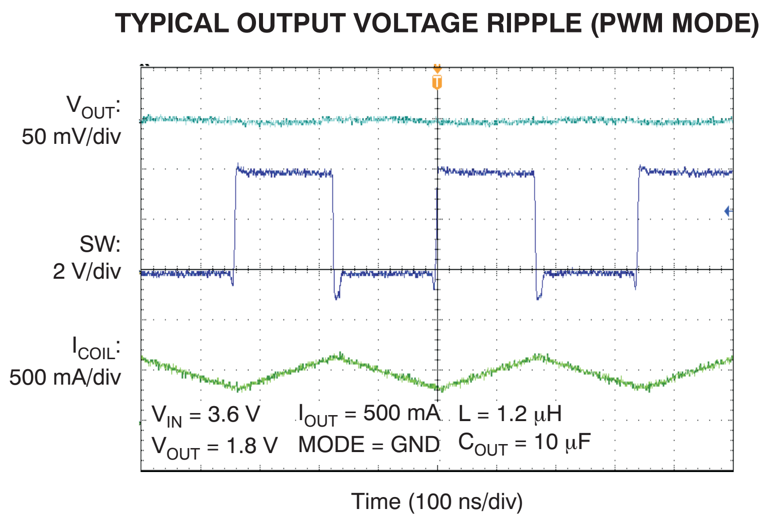
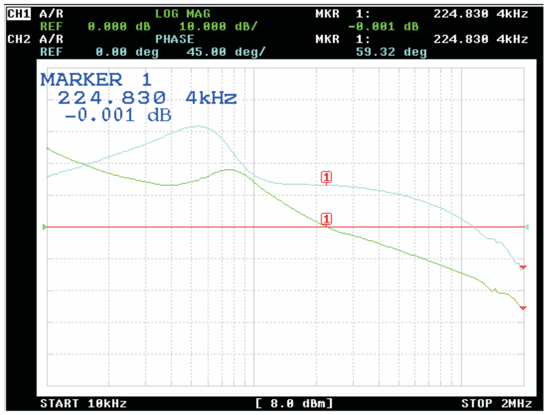


Figure 9. TPS62065 Output Voltage Ripple (PWM Mode)

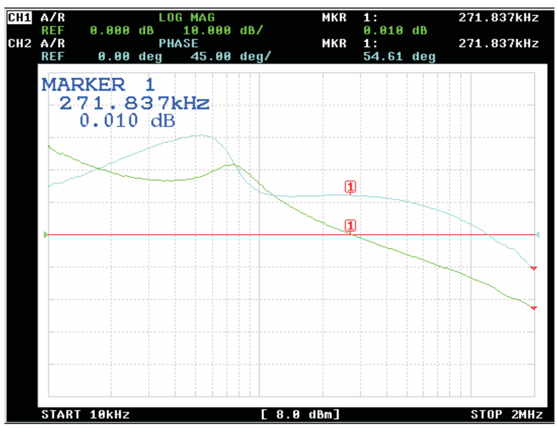
6.5 Control Loop Bode Diagrams: TPS62065

Figure 10 and Figure 11 illustrate typical TPS62065 gain and phase performance versus frequency at VIN = 3.6 V and 5.0 V, respectively, using the TPS62025EVM.



Conditions: VIN = 3.6 V, VOUT = 1.8 V, I_{OUT} = 1.6 A; bandwidth: 224 kHz, phase margin: 59°

Figure 10. TPS62065 Gain and Phase vs Frequency



Conditions: VIN = 5.0 V, VOUT = 1.8 V, I_{OUT} = 1.6 A; bandwidth: 271 kHz, phase margin: 54°

Figure 11. TPS62065 Gain and Phase vs Frequency

7 TPS62065/67EVM-347 Assembly Drawings and Layout

Figure 12 through Figure 16 show the design of the TPS62065/67EVM-347 printed circuit boards. This EVM has been designed using a four-layer, 1-ounce copper-clad PCB (3.81 cm by 4.57 cm) with all components in an active area on the top side of the board. All active traces to the top and bottom layers to allow the user to easily view, probe, and evaluate the TPS62025/67 control ICs in a practical, double-sided application environment. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space-constrained systems.

NOTE: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing TPS62065/67EVM-347 PCBs.

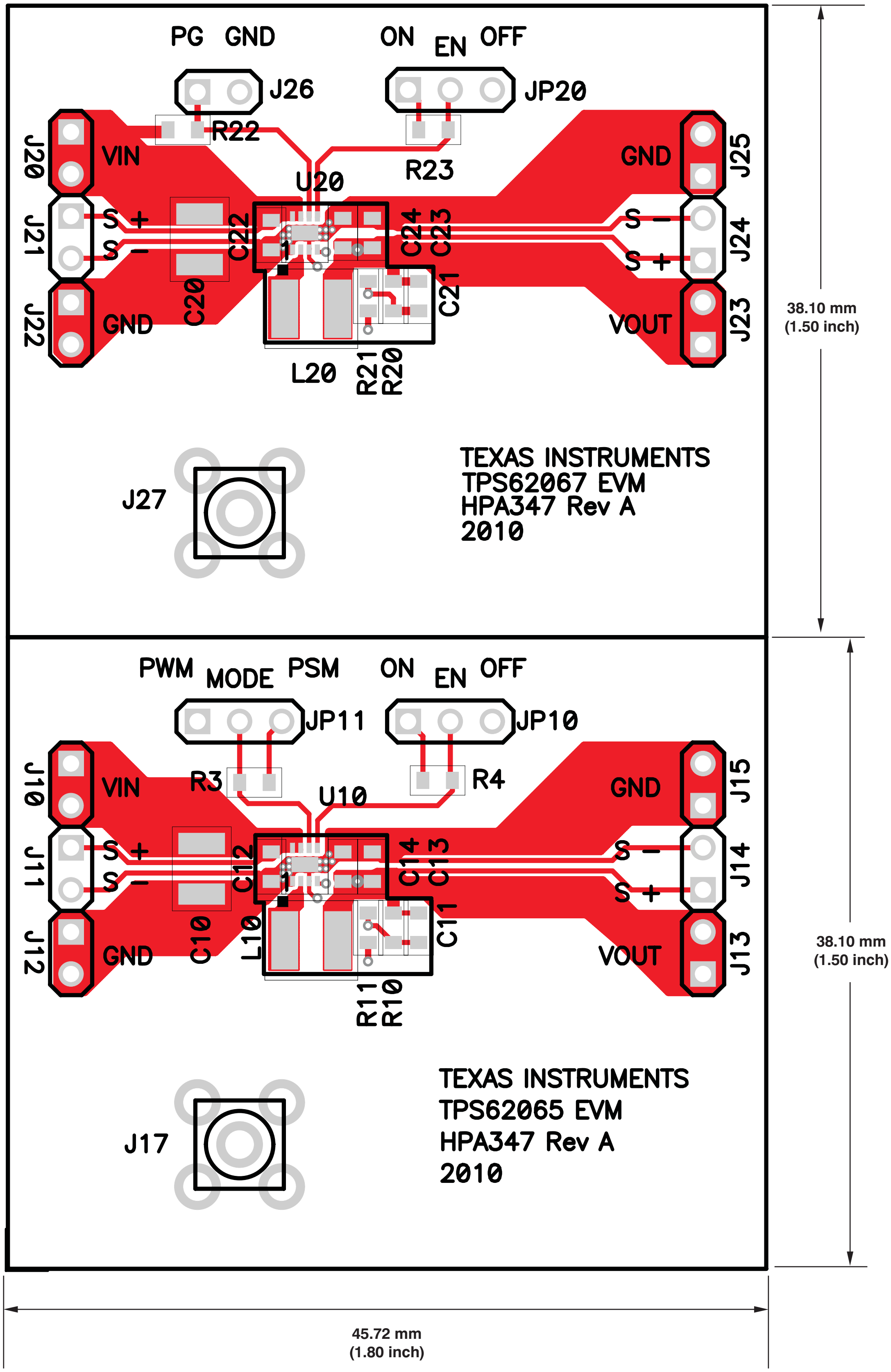


Figure 12. TPS62065/67EVM Component Placement (Top View)

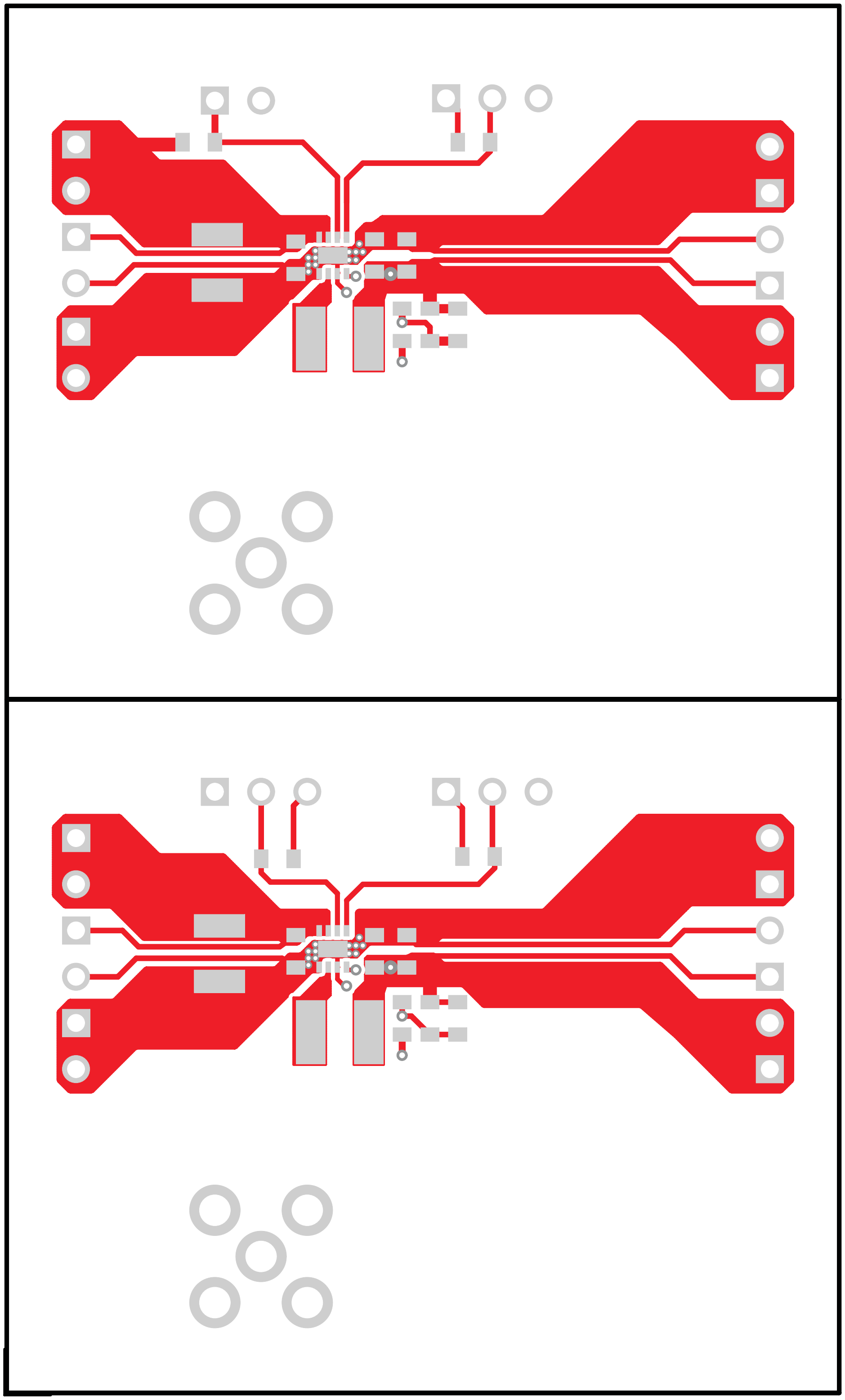


Figure 13. TPS62065/67EVM Top-Side Copper (Top View)

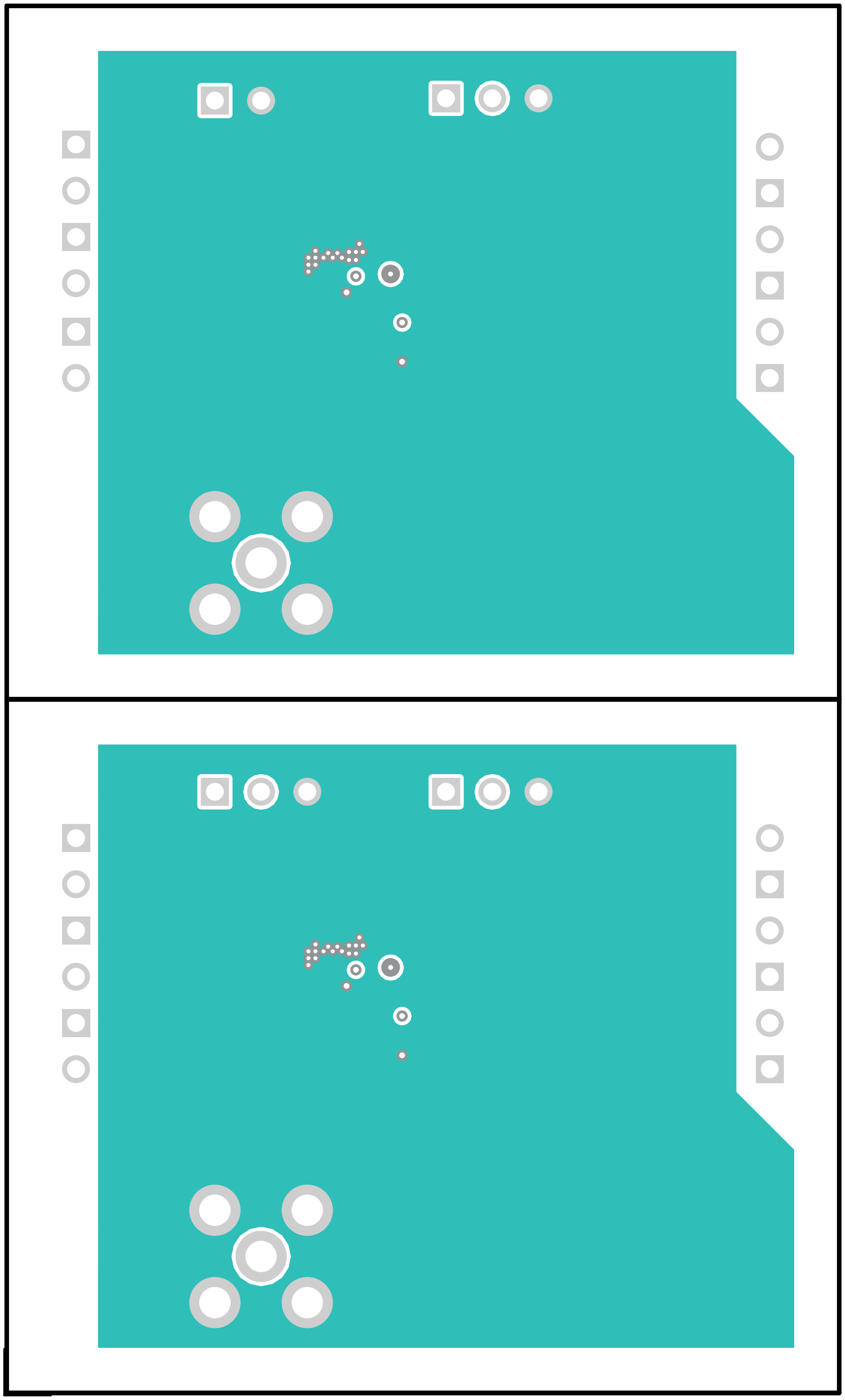


Figure 14. TPS62065/67EVM Internal Layer 2 (X-Ray View, from Top)

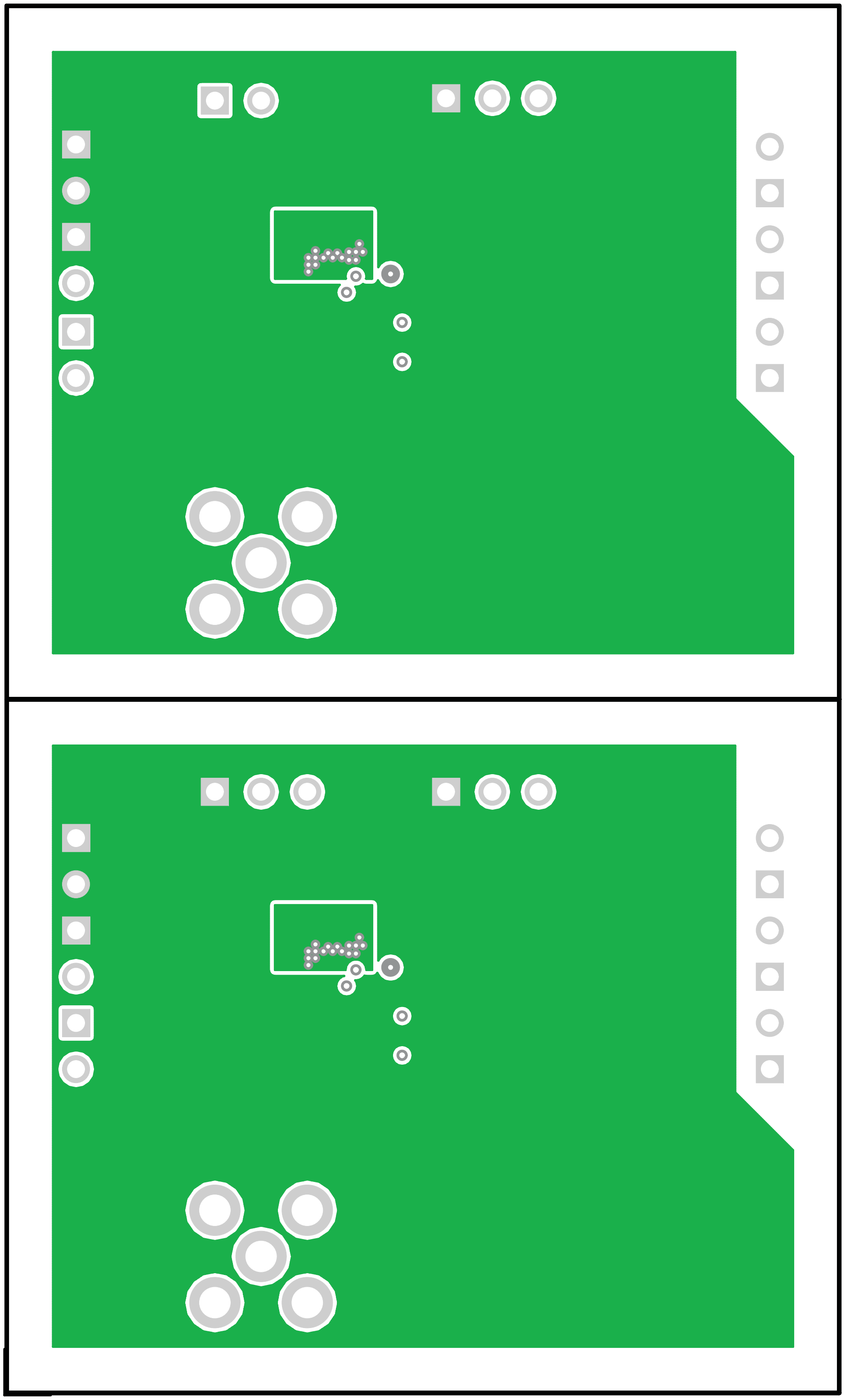


Figure 15. TPS62065/67EVM Internal Layer 1 (X-Ray View, from Top)

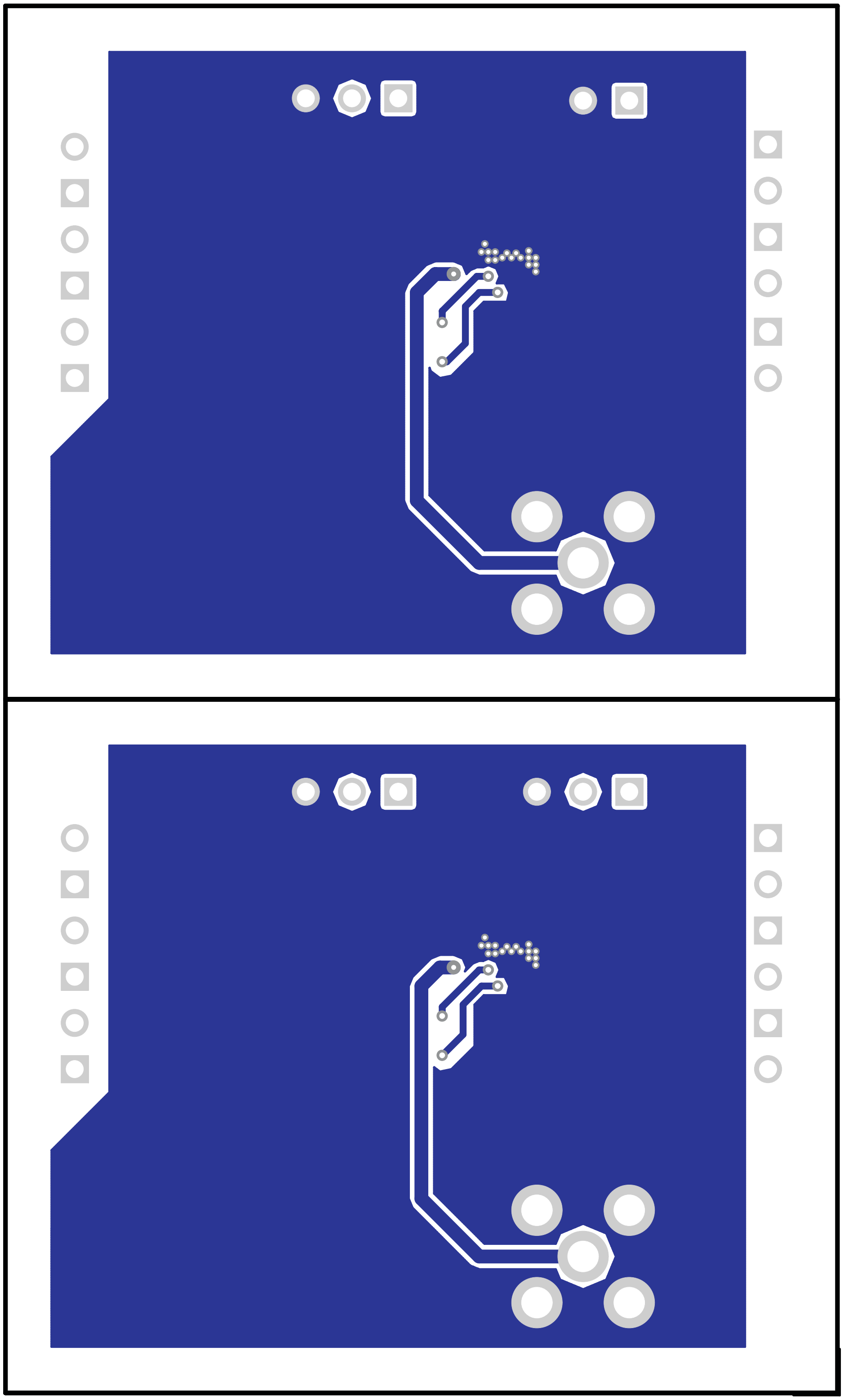


Figure 16. TPS62065/67EVM Bottom-Side Copper (Bottom View)

8 Bill of Materials

Table 2 lists the bill of materials for the TPS62065/67EVM.

Table 2. TPS62065/67EVM Bill of Materials(1)(2)(3)(4)

Count	RefDes	Value	Description	Size	Part Number	MFR
2	C10, C20	22 µF	Capacitor, ceramic, 10 V, X7R, 10%	1210	GRM32ER71A226K	MuRata
2	C11, C21	22 pF	Capacitor, ceramic, 10 V, NGO, 5%	0603	Standard	Standard
4	C12, C13, C22, C23	10 µF	Capacitor, ceramic, 6.3 V, X5R, 20%	0603	GRM188R60J106ME47D	muRata
0	C14, C24	Open	Capacitor, ceramic, 6.3 V, X5R, 20%	0603	GRM188R60J106ME47D	muRata
0	J16, J27	Open	Connector, SMA , straight, PC mount	0.210 in^2	901-144-8RFX	AMP
2	L10, L20	1.0 µH	Inductor, chip coil, ±30%	1515	LQH44PN1R0NP0L	Murata
1	R10	360 kΩ	Resistor, chip, 1/16W, 1%	0603	Standard	Std
2	R11, R21	180 kΩ	Resistor, chip, 1/16W, 1%	0603	Standard	Std
1	R20	820 kΩ	Resistor, chip, 1/16W, 1%	0603	Standard	Std
4	R12, R13, R22, R23	1.00 MΩ	Resistor, chip, 1/16W, 1%	0603	Standard	Std
1	U10	TPS62065DSG	IC, step-down converter, 3 MHz, 1.6 A	SON-8	TPS62065DSG	TI
1	U20	TPS62067DSG	IC, step-down converter, 3 MHz, 1.6 A	SON-8	TPS62067DSG	TI

(1) These assemblies are ESD sensitive. ESD precautions must be observed.
(2) These assemblies must be clean and free from flux and all contaminants. Use of *no-clean* flux is not acceptable.
(3) These assemblies must comply with workmanship standards IPC-A-610 Class 2.
(4) Reference designators marked with an asterisk (**) cannot be substituted. All other components can be substituted with equivalent manufacturing components.

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 3.0 V to 6.0 V and the output voltage range of 0.8 V to 6.0 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +60°C. The EVM is designed to operate properly with certain components above +60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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		Wireless	www.ti.com/wireless-apps

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