TEXAS INSTRUMENTS

THS4130

EVM User's Guide for High-Speed Fully-Differential Amplifier

User's Guide

January 2001

Mixed-Signal Products

SLOU101

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Preface

About This Manual

This manual is written to provide information about the evaluation module of the fully differential amplifier under test. Additionally, this document provides a good example of PCB design for high speed applications. The user should keep in mind the following points.

The design of the high-speed amplifier PCB is an elegant and sensitive process. Therefore, the user must approach the PCB design with care and awareness. It is recommend that the user initially review the datasheet of the device under test. It is also helpful to review the schematic and layout of the THS4130 EVM to determine the design techniques used in the evaluation board. In addition, it is recommended that the user review the application note *Fully-Differential Amplifiers* (literature number SLOA054B) to gain more insight about differential amplifiers. This application note reviews the differential amplifiers and presents calculations for various filters.

How to Use This Manual

- Chapter 1—Introduction and Description
- Chapter 2—Using the THS4130 EVM
- Chapter 3—General High-Speed Amplifier Design Considerations

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

- THS4130 data sheet (literature number SLOS318)
- THS4130 application report (literature number SLOA054A), *Fully-Differential Amplifiers*

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Contents

Figures

Tables

Chapter 1

Introduction and Description

The Texas Instruments THS4130 evaluation module (EVM) helps designers evaluate the performance of the THS4130 operational amplifier. Also, this EVM is a good example of high-speed PCB design.

This document details the Texas Instruments THS4130 high-speed operational amplifier evaluation module (EVM). It includes a list of EVM features, a brief description of the module illustrated with a series of schematic diagrams, EVM specifications, details on connecting and using the EVM, and a discussion of high-speed amplifier design considerations.

This EVM enables the user to implement various circuits to clarify the available configurations presented by the schematic of the EVM. In addition, the schematic of the default circuit has been added to depict the components mounted on the EVM when it is received by the customer. This configuration correlates to the single input/differential output signal.

Other sample circuits are presented to show how the user can implement other circuit configurations such as differential input/differential output signal, transformer utilization on the input and output terminals, VICR level shifter, and Butterworth filter with multiple feedback. The user may be able to create and implement circuit configurations in addition to those presented in this document using the THS4130 EVM.

Topic **Page**

1.1 Description

The THS4130 EVM is a good example of PCB design and layout for high-speed operational amplifier applications. It is a complete circuit for the high-speed operational amplifier. The EVM is made of the THS4130 high-speed operational amplifier, a number of passive components, and various features and footprints that enable the user to experiment, test, and verify various operational amplifier circuit implementations. The board measures 4.5 inches in length by 2.5 inches in width. Initially, this board is populated for a single-ended input amplifier (see Figure 1-2 for populated circuits). The outputs (V_{O+} and $V_{O–}$) can be tested differentially or single ended. Gain is set to one and can be changed by changing the ratios of the feedback and gain resistors (see the device datasheet for recommended resistor values). The user may populate various footprints on the evaluation module board to verify filter designs or perform other experiments. Each input is terminated with a 50-Ω resistor to provide correct line-impedance matching.

1.2 Evaluation Module Features

THS4130 high-speed operational amplifier EVM features include:

- Voltage supply operation range: 5-V to ±15-V operation (see the device data sheet)
- Single and differential input and output capability
- Nominal 50-Ω input and output termination resistors. They can be configured according to the application requirement.
- V_{OCM} direct input control (see schematic and the device data sheet)
- V_{OCM} pin can be controlled via transformer center-tap (see schematic)
- Shutdown pin control, JU1 (if applicable to the device, see the device data sheet)
- Input and output transformer footprints for changing single-ended signals to differential signals
- Footprint for high-precision, balanced feedback and gain resistors (0.01% or better)
- Footprints for low-pass filter implementation (see application note SLOA054A)
- Footprints for antialiasing filter implementation (see application note SLOA054A)
- Differential probe terminals on input and output nodes for differential probe insertion
- Various GND and signal test points on the PCB
- Circuit schematic printed on the back of the EVM
- A good example of high-speed amplifier PCB design and layout

1.3 THS4130 EVM Specifications

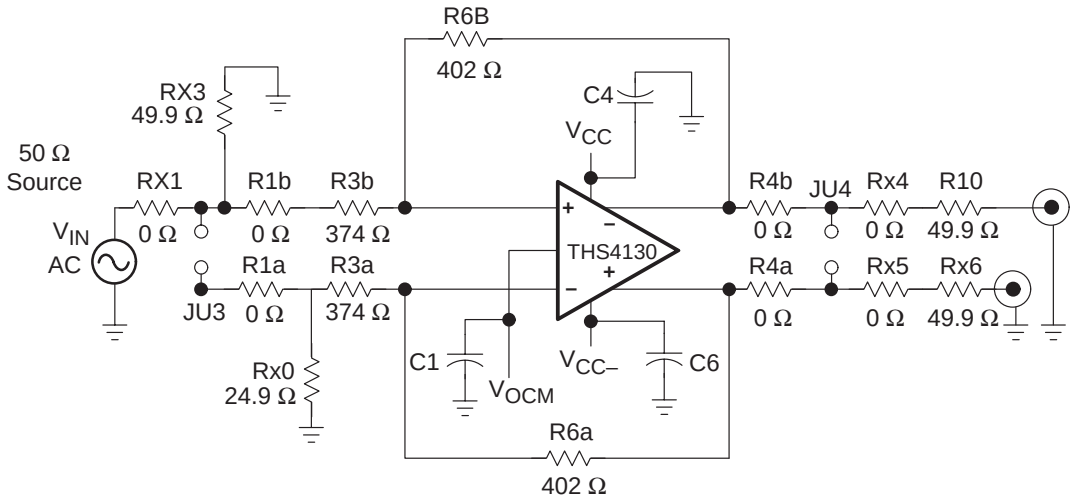
Supply voltage range, $\pm V_{CC}$ . . . . 5 V to ±15 V (see the device data sheet)
Supply current, I_{CC} . . . . . (see the device data sheet)
Output drive, I_O, V_{CC} = ±15 . . . . . (see the device data sheet)

For complete THS4130 amplifier IC specifications, parameter measurement information, and additional application information, see the THS4130 data sheet, TI literature number SLOS318.

1.4 Schematic of the Populated Circuit (Default Configuration)

For verification of jumper locations and other bypass components, see the complete EVM schematic in Figure 1–2.

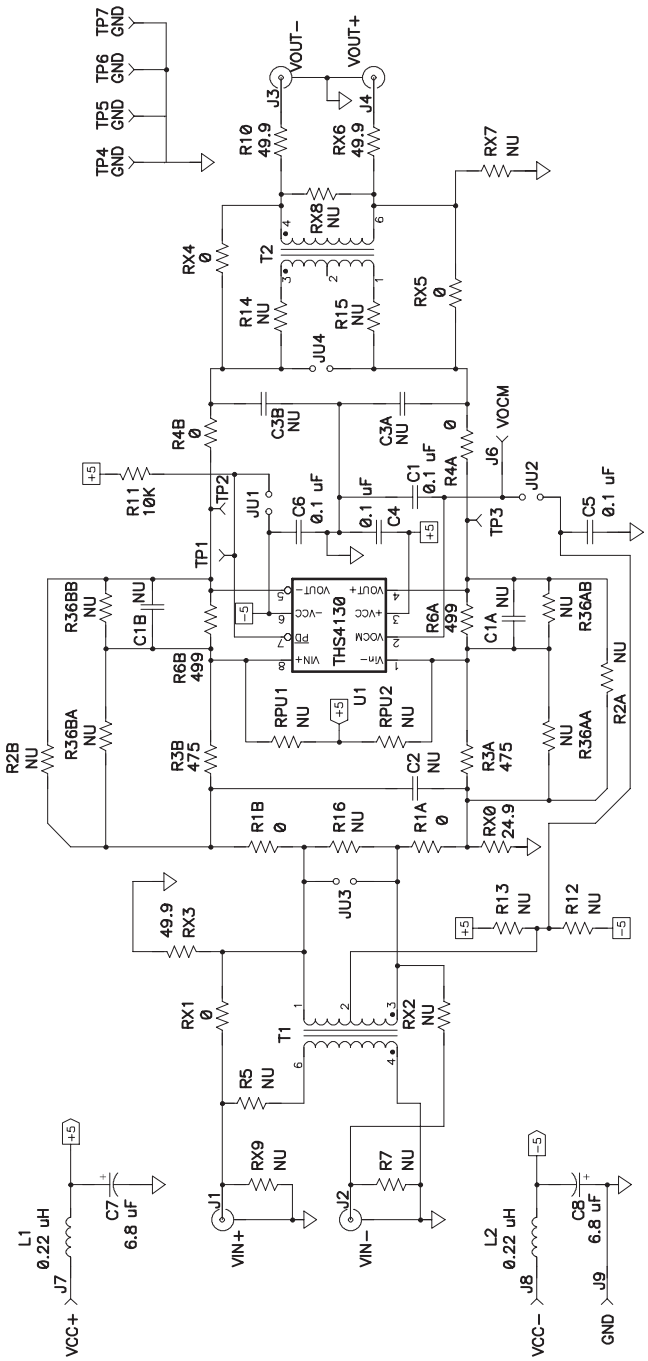
Figure 1–1. Schematic of the Populated Circuit on the EVM (Default Configuration)



NOTE: Default populated footprints on the EVM from the input nodes to the output terminals Gain = 1

1.5 THS4130 EVM Schematic

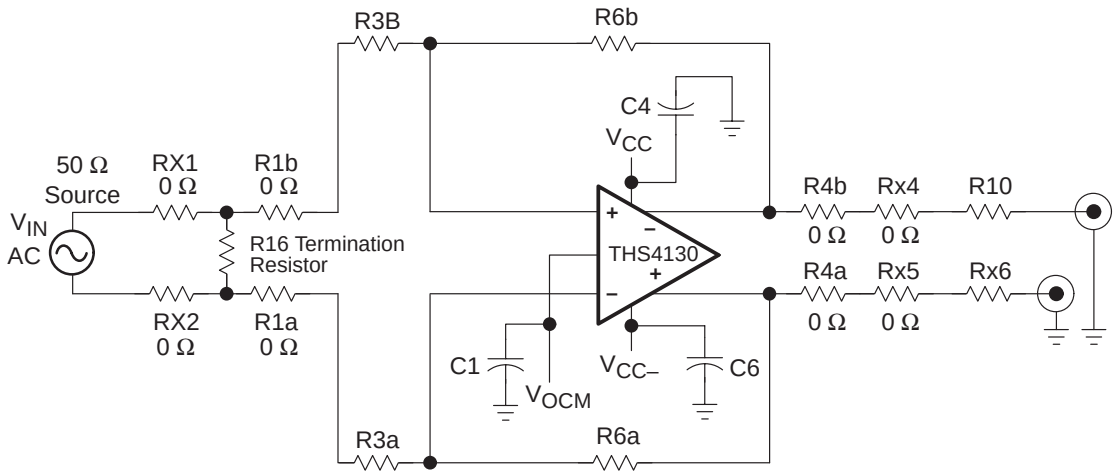
Figure 1–2. Schematic



1.6 Additional Sample Schematics

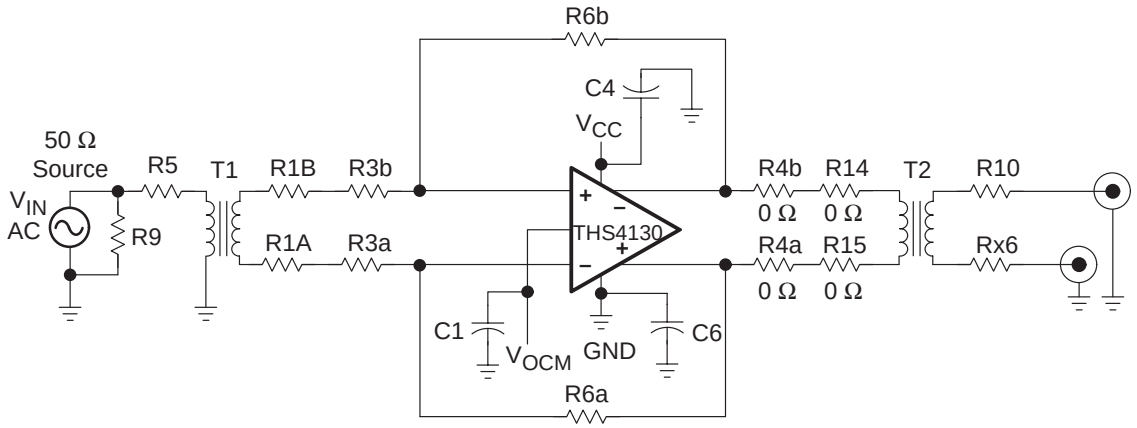
For verification of jumper locations and other bypass components, see the complete EVM schematic in Figure 1–2.

Figure 1–3. Fully-Differential In/Fully-Differential Out, Without Transformer



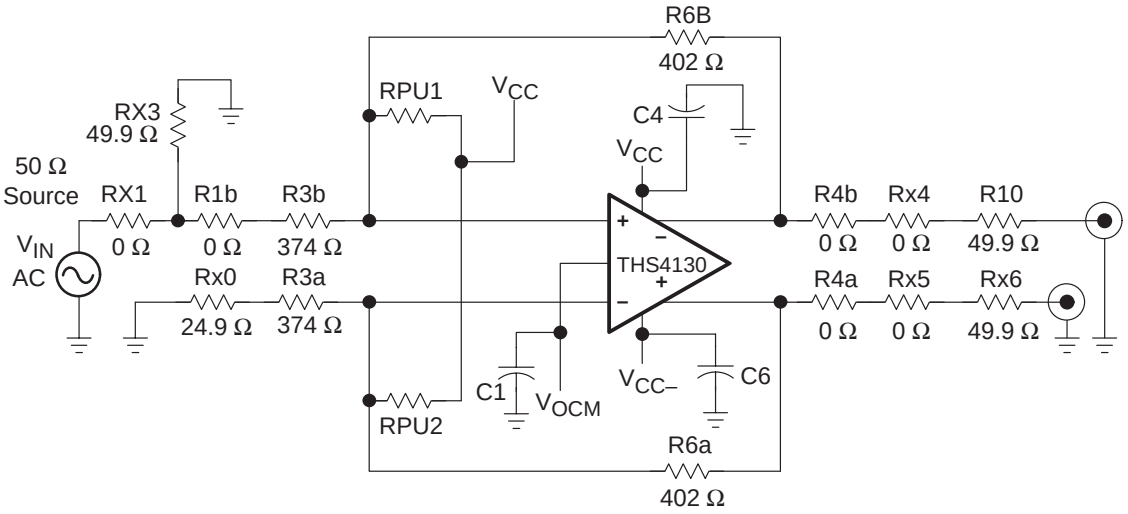
NOTE: Fully-differential in / fully-differential out signal path. *See the Texas Instruments February 2001 Analog Applications Journal for the information on the termination resistors*.

Figure 1–4. Fully-Differential In/Fully-Differential Out, Utilizing Transformer



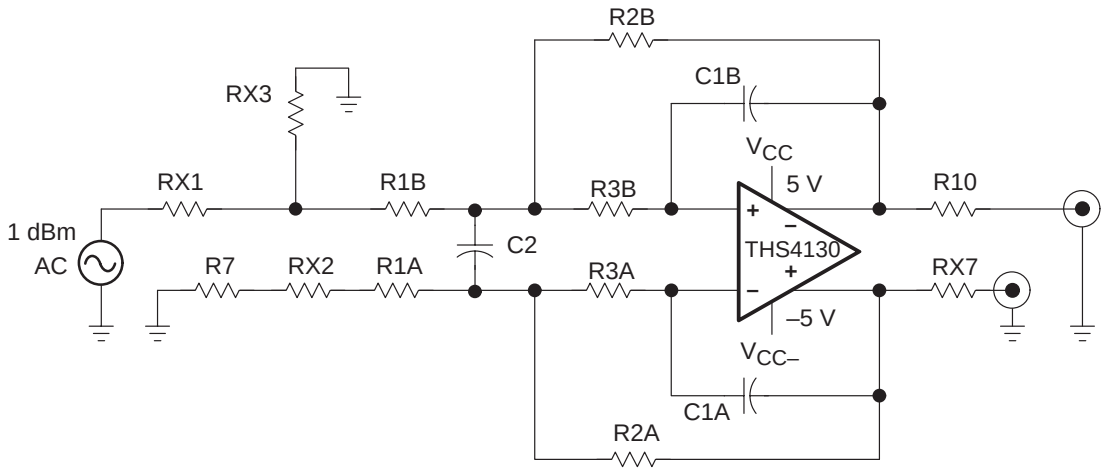
NOTE: Utilizing the input and output transformers to create a fully-differential signal input/ differential or single output and isolate the amplifier from the rest of the front-end and back-end circuits.

Figure 1–5. VICR Level Shifter



NOTE: Shifting the VICR within the specified range in the data sheet via RPU1 and RPU2 if the VICR is out of the specified range. See the Application section of the data sheet for the THS4130 for more information.

Figure 1–6. Butterworth Filter With Multiple Feedback.



NOTE: Butterworth filter implemented with multiple feedback architecture

1.7 THS4130 EVM Layout

Figure 1–7. Top Layer (Silkscreen)

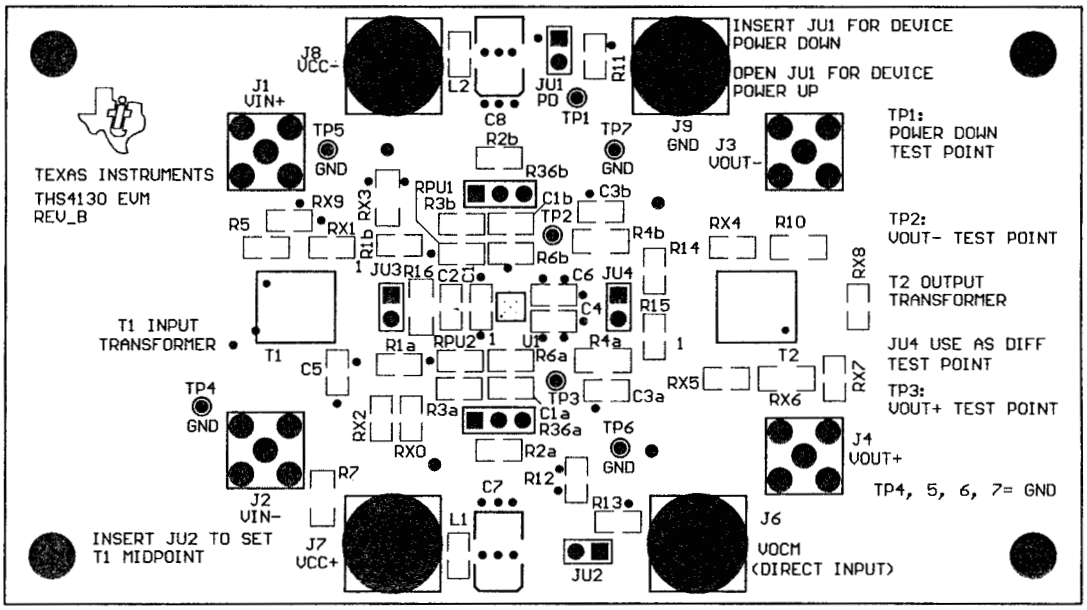


Figure 1–8. Top (Layer 1) (Signals)

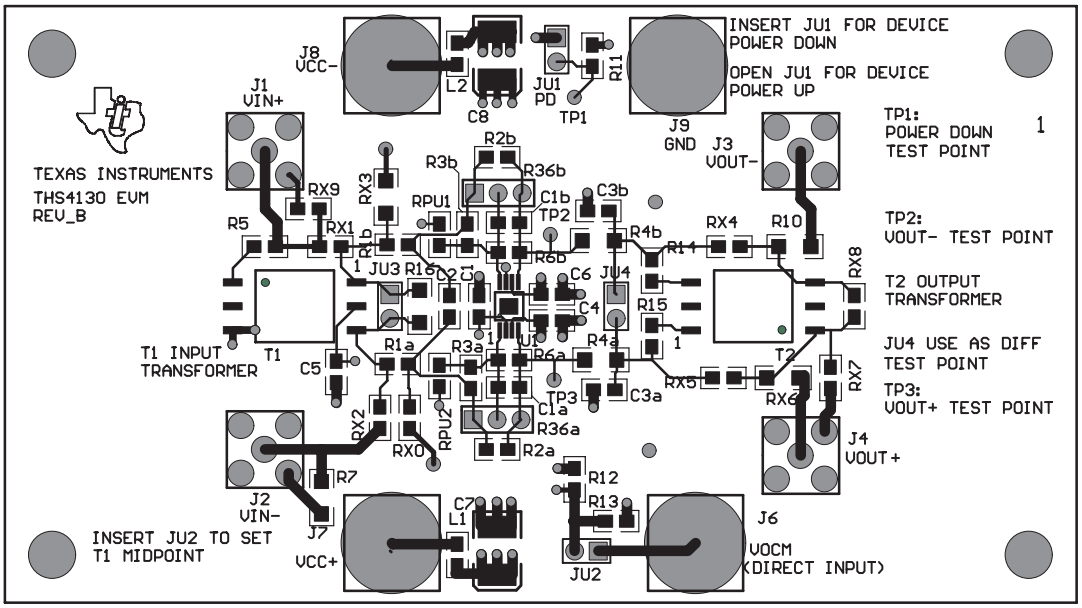


Figure 1–9. Internal Plane (Layer 2) (Ground Plane)

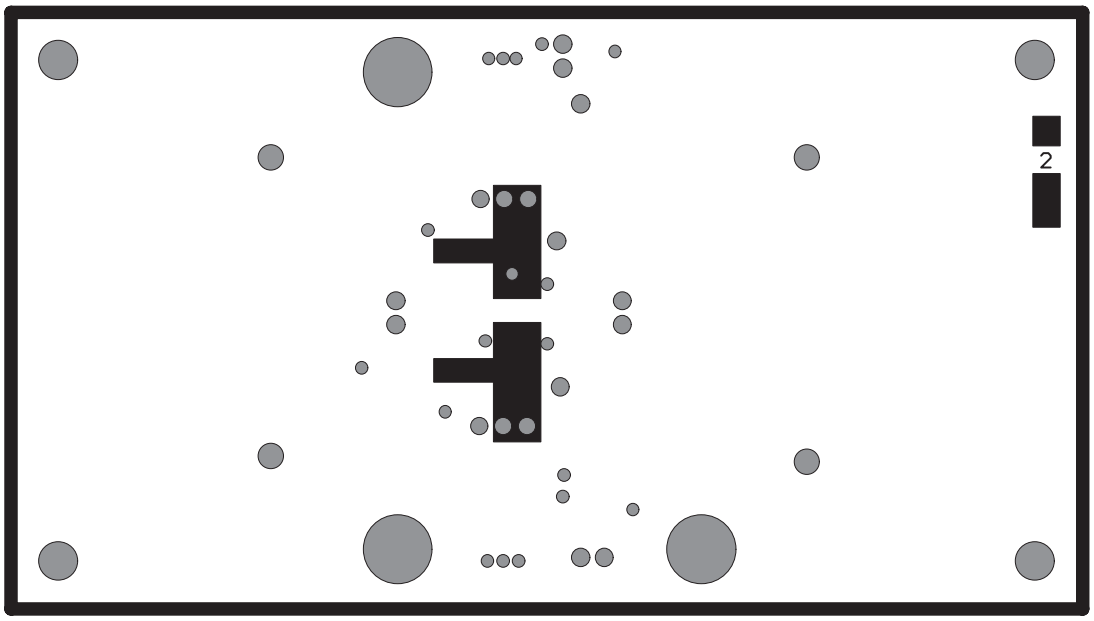


Figure 1–10. Internal Plane (Layer 3) (± V_{CC} Plane)

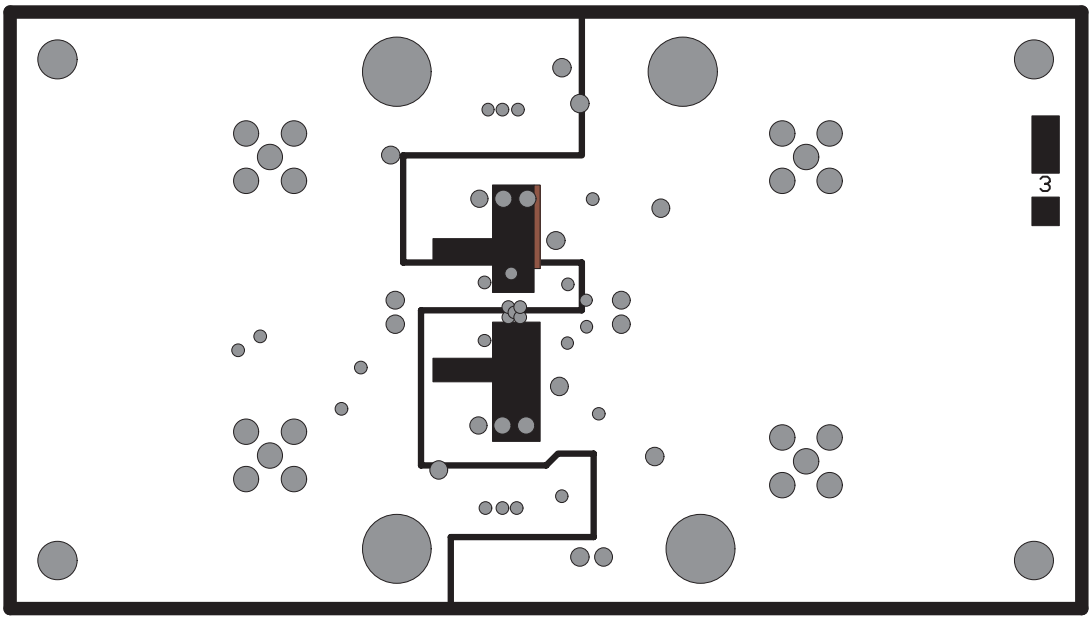
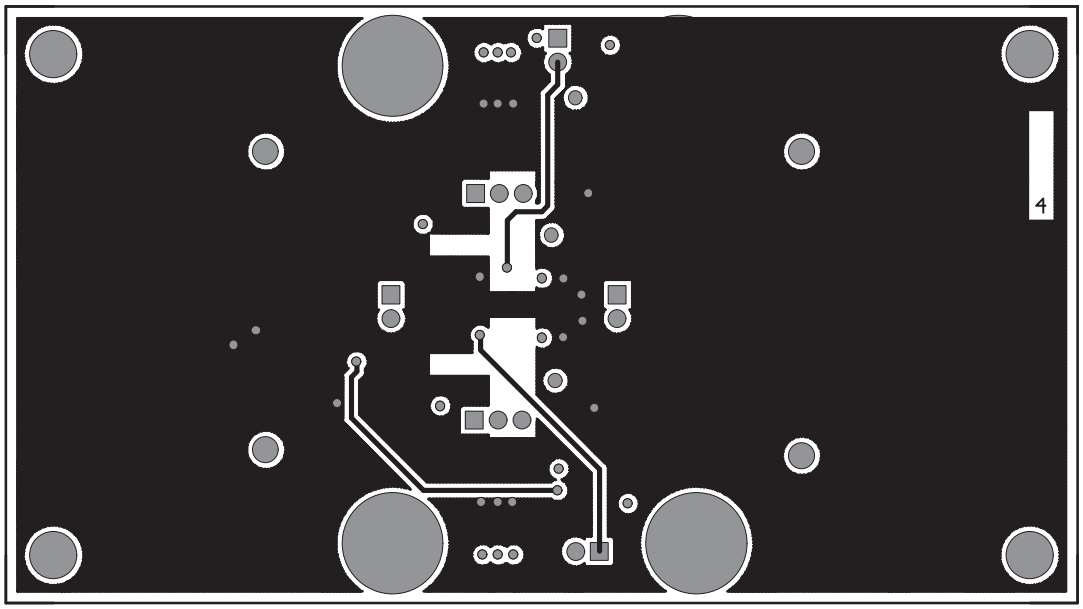


Figure 1–11. Bottom (Layer 4) (Ground and Signal)



Chapter 2

Using the THS4130 EVM

It is recommended that the user perform the following exercises to learn the usage of the EVM. This practice helps the user learn about the various terminals on the EVM and their function. In addition, it suggests the components and equipment needed to operate the EVM.

Topic **Page**

2.1 Required Equipment

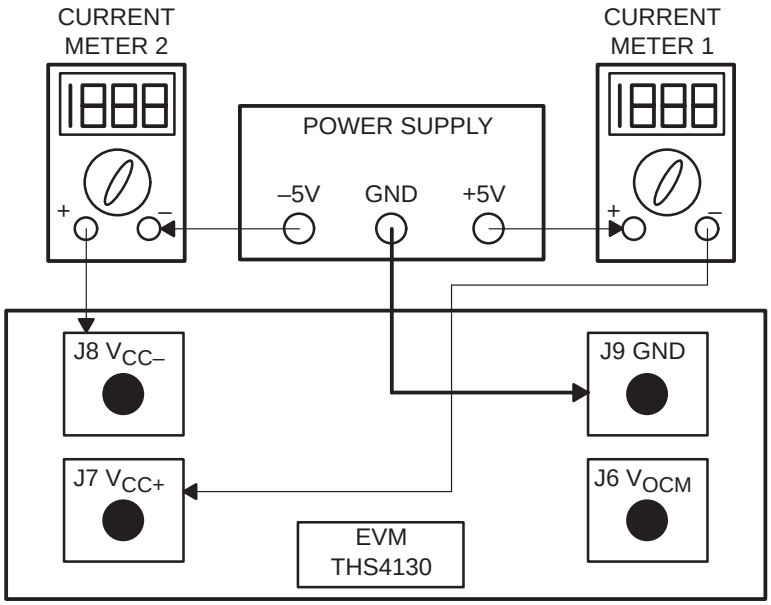
- ❑ One double-output dc power supply (±5 V, 100 mA output minimum)
- ❑ Two dc current meters with resolution to 1 mA and capable of the maximum current the dc power supply can supply. If available, set the current limit on the dc power supply to 100 mA.

  Note: Some power supplies incorporate current meters which may be applicable to this test.
- ❑ 50-Ω source impedance function generator (1 MHz, 10 V_{PP} sine wave)
- ❑ Oscilloscope (50-MHz bandwidth minimum, 50-Ω input impedance).

2.2 Power Supply Setup

1) Set the dc power supply to ±5 V.
2) Make sure the dc power supply is turned off before proceeding to the next step.
3) Connect the positive (+) terminal of the power supply to the positive (+) terminal of the current meter number 1.
4) Connect the negative (–) terminal of the current meter number 1 to the V_{CC+} of the EVM (J7).
5) Connect the common ground terminal of the power supply to the ground GND on the EVM (J9).
6) Connect the negative (–) terminal of the power supply to the negative (–) terminal of the second current meter.
7) Connect the positive (+) terminal of the current meter number 2 to the $V_{CC–}$ of the EVM (J8).

Figure 2–1. Power Supply Connection



Figures are not drawn to scale.

2.3 Input and Output Setup

1) Ensure that JU3, JU4, and JU1 are *not installed* (open circuit).

2) Set the function generator to generate a 1 MHz, ±0.5 V (1 V_{PP}) sine wave with no dc offset.

3) Turn off the function generator before proceeding to the next step.

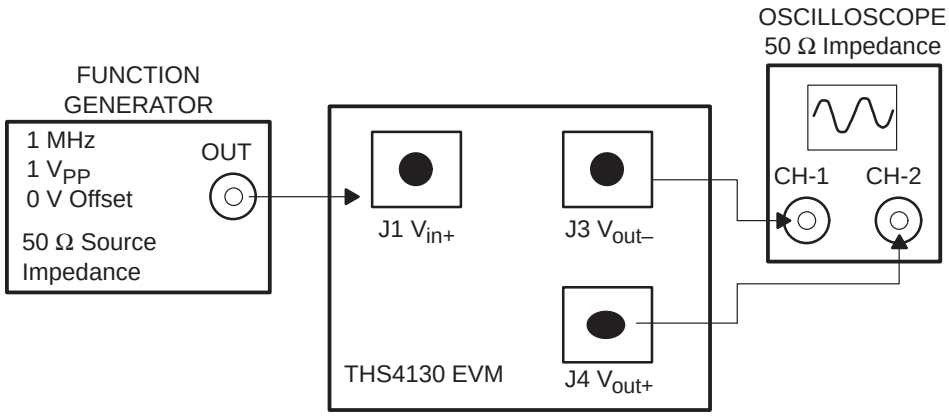
4) Using a BNC-to-SMA cable, connect the function generator to J1 (V_{I+}) on the EVM.

5) Using a BNC-to-SMA cable, connect the oscilloscope to J3 ($V_{O–}$) on the EVM.

6) Using a BNC-to-SMA cable, connect the oscilloscope to J4 (V_{O+}) on the EVM. Set the oscilloscope to 0.5 V/division and a time-base of 0.2 µs/division.

   Note: The oscilloscope must be set to use a 50-Ω input impedance for proper results.

Figure 2–2. Signal Connections



Figures are not drawn to scale.

2.4 Testing the EVM Setup

1) Turn on the dc power supply.

2) Verify that both the +5 V (current meter 1) and the –5 V (current meter 2) currents are below 20 mA.

Caution:

Currents above 20 mA indicate a possible short or a wrong resistor value on the PCB. Do not proceed until this situation is corrected.

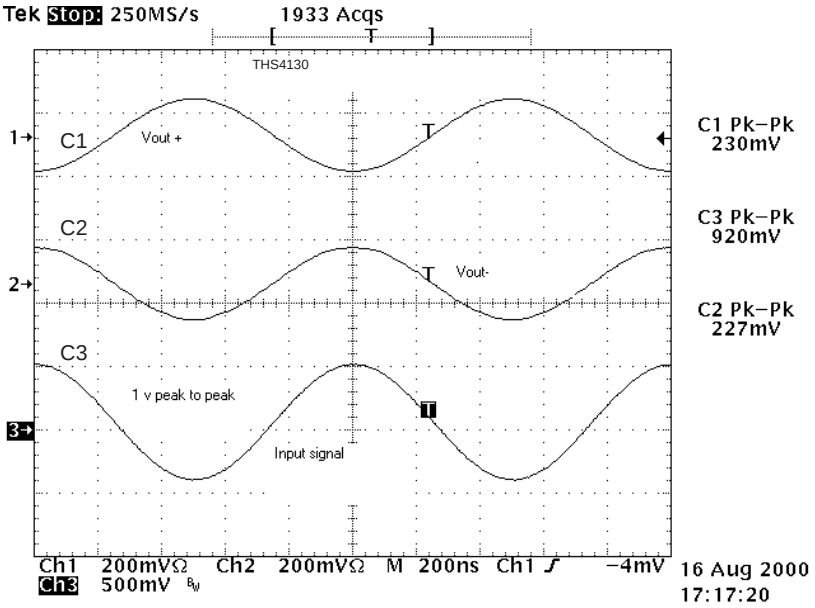
3) Turn on the function generator.

4) Verify the oscilloscope is showing two 1 MHz sine waves with amplitude of ±0.125 V. The dc offset of the signal must be below 50 mV.

   Note: V_{OUT+} and V_{OUT-} should be 180 degrees out of phase. The internal attenuation of the scope should be set to 6 dB for a gain of one. Otherwise, the output will show a *gain of one-half* due to the voltage division occurring at the 50-Ω termination resistor.

Use Figure 3 as a reference for the input and output signals.

Figure 2–3. Driver 1 Output Signal



2.5 Power Down Verification

This EVM is used to evaluate devices with and without the shutdown function. Therefore, this step is only applicable if the device has a shutdown function. Please see the data sheet for power-down verification.

1) Insert the jumper JU1 to power down the device. The current consumption (dc current meters) should drop to less than 1.5 mA. Remember to discount the current flow through the 10-kΩ pullup resistor on the EVM when calculating the device current consumption in the shutdown mode.
2) Turn off the power supply and disconnect the wiring.
3) Turn off the function generator and disconnect the wiring.
4) Basic operation of the operational amplifier and its EVM is complete.

2.6 Measuring the Frequency Response

This EVM is designed to easily interface with network analyzers. Jumpers J3 and J4 facilitate the use and insertion of the differential probes at the input and output nodes. It is important to consider the following steps to ensure optimal performance in terms of bandwidth, phase margin, gain, and peaking

1) Connect the power supply according to the power supply set up (section 2.2)
2) Use proper load values. Loads directly effect the performance of the differential operational amplifier (the suggested value is 200 Ω differentially, 100 Ω on each output node).

Caution:

Incorrect connections cause excessive current flow and may damage the device.

3) Place the GND connection of the probe as close as possible to the output nodes. Use the GND holes on the EVM. The GND holes create a shorter route to the GND plane and output nodes.
4) Place the probe at the input nodes, set the power level of the network analyzer to the proper level (information in the data sheet typically is produced at –20 dBm power level), and calibrate the network analyzer.

Note:

If a differential probe is used, verify that resistors R1a, R1b, R4b, and R4a are in place. The resistors are 0 Ω values providing the path to the differential probe terminals.

5) Place the probe at the output nodes (if a differential probe is used, insert the probe into the provided jumper), and measure the frequency response.

Note:

Transformers are used to change the single ended signals to differential signal or vice versa. On this EVM, they can be populated according to the application or the experiment. The V_{OCM} pin of the device may be connected to the center-tap of the transformer, or maybe set via an external source such as V_{ref} of a data converter. If the V_{OCM} pin is not connected to an external source, it will be set at the center point of the power supply. For example, if ±5 sources are used, the V_{OCM} level will be set to zero.

2.7 Butterworth Filter

An example of a Butterworth filter implemented with multiple feedback architecture is provided. The following circuit is implemented on the EVM board. The following figures represent the circuit configuration and the component values. The corner frequency of the filter (–3dB) is set at 1 MHz.

For verification of jumper locations and other bypass components, see the complete EVM schematic in Figure 1–2.

Figure 2–4. Multiple Feedback Filter Circuit

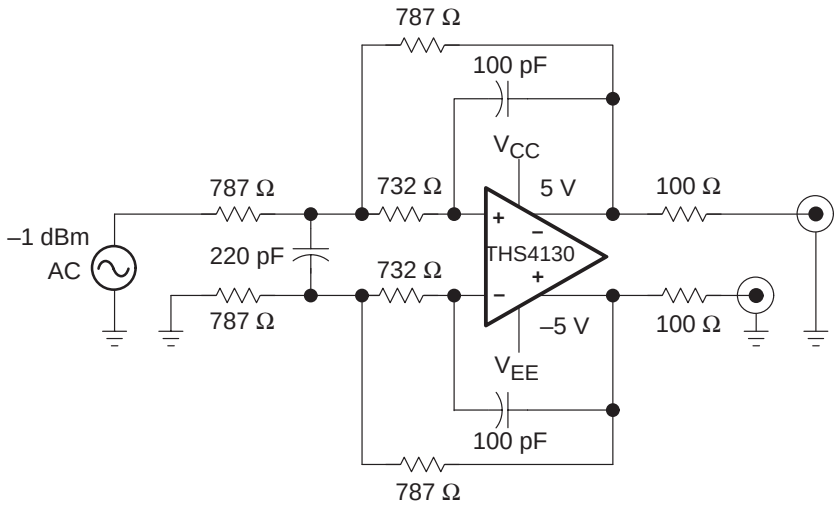
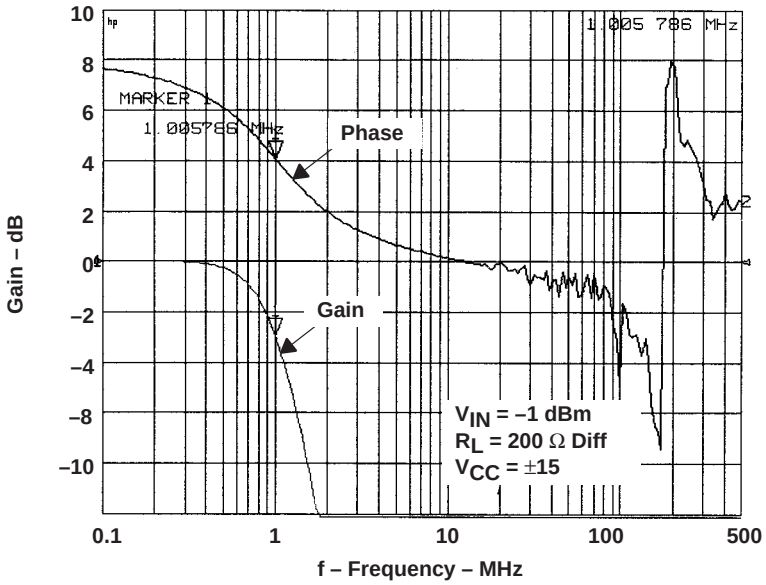


Figure 2–5. Gain vs Phase

Butterworth filter with multiple feedback frequency response.



2.8 THS4130 EVM Bill of Materials

Table 2–1. THS4130 EVM Bill of Materials

Ref.	Description	Size	Qty.	Manufacturer	Part Number
C1, C4, C5, C6	Capacitor, 0.1 μF, ceramic	0805	4	Murata	GRM40–X7R104K25
C7, C8	Capacitor, 6.8 μF, 35 V, 20% tantalum, SM	7343	2	Sprague	293D685X9035D2T
C1A, C1B, C2, C3A, C3B	Open	0805	5		
J1, J2, J3, J4	SMT_PCB_MT	SMA jack	4	Amphenol	901-144-8RFX
J6, J7, J8, J9	Banana jack		4	Newark	35F865
JU1, JU2, JU3, JU4	2 pos jumper header, 0.1 ctrs., 0.025” sq pins	2 pos jump	4		
JU1, JU2	Shorting jumpers header, 0.1 ctrs., 0.025” sq pins		2		
L1, L2	Inductor, 0.22 μH SM	0805	2	Digi–Key	PCD1176CT–ND
R1a, R1b, RX1, RX4, RX5	Resistor, 0 Ω, 1%	0805	5	Digi–Key	P0.0ACT–ND
R2a, R2b, R5, R12, R13, R14, R15, RX2, RX7, RX8, RX9	Open	0805	11		

Table 2–1. THS4130 EVM Bill of Materials (continued)

Ref.	Description	Size	Qty.	Manufacturer	Part Number
R3a, R3b	Resistor, 374 Ω, 1%	0805	2	Digi–Key	P374CTR–ND
R4a, R4b	Resistor, 0 Ω, 1%	1206	2	Digi–Key	P0.0ECT–ND
R6a, R6b	Resistor, 402 Ω, 1%	0805	2	Digi–Key	P402CTR–ND
R11	Resistor, 10 kΩ, 1%	0805	1	Digi–Key	P10.KCTR–ND
R10, RX3, RX6	Resistor, 49.9 Ω, 1%	1206	3	Digi–Key	P49.9FTR–ND
R16, R7	Open	1206	2		
R36aA, R36aB, R36bA, R36bB	High precision resistor		2		
RPU1, RPU2	Open	0805	2		
RX0	Resistor, 24.9 Ω, 1%	0805	1	Digi–Key	P24.9CTR–ND
T1, T2	Open	MC KK81	2		
TP1, TP2, TP3	Test point 2	TP .025	3	Farnell	240-345
TP4, TP5, TP6, TP7	Test point 2	TP .025	4	Farnell	240-333
U1	IC, THS4130	8 Pin DGN	1	Texas Instruments	THS4130CDGN

Chapter 3

General High-Speed Amplifier Design Considerations

The THS4130 EVM layout has been designed for use with high-speed signals and can be used as an example when designing PCBs incorporating the THS4130. Careful attention has been given to component selection, grounding, power supply bypassing, and signal path layout. Disregarding these basic design considerations could result in less than optimum performance of the THS4130 high-speed operational amplifier.

Surface-mount components were selected because of the extremely low lead inductance associated with this technology. This helps minimize both stray inductance and capacitance. Also, because surface-mount components are physically small, the layout can be very compact.

Tantalum power supply bypass capacitors at the power input pads help supply currents needed for rapid, large signal changes at the amplifier output. The 0.1-μF power supply bypass capacitors were placed as close as possible to the IC power input pins in order to minimize the return path impedance. This improves high frequency bypassing and reduces harmonic distortion.

A proper ground plane on both sides of the PCB should be used with high-speed circuit design. This provides low-inductive ground connections for return current paths. In the area of the amplifier input pins, however, the ground plane should be removed to minimize stray capacitance and reduce ground plane noise coupling into these pins. This is especially important for the inverting pin while the amplifier is operating in the noninverting mode. Because the voltage at this pin swings directly with the noninverting input voltage, any stray capacitance would allow currents to flow into the ground plane. This could cause possible gain error and/or oscillation. Capacitance variations at the amplifier input pin of greater than 1 pF can significantly affect the response of the amplifier.

In general, it is best to keep signal lines as short and as straight as possible. Incorporation of microstrip or stripline techniques is also recommended when signal lines are greater than 1 inch in length. These traces must be designed with a characteristic impedance of either 50 Ω or 75 Ω, as required by the application. Such a signal line must also be properly terminated with an appropriate resistor.

Finally, proper termination of all inputs and outputs must be incorporated into the layout. Unterminated lines, such as coaxial cable, can appear to be a reactive load to the amplifier. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears to be purely resistive, and reflections are absorbed at each end of the line. Another advantage of using an output termination resistor is that capacitive loads are isolated from the amplifier output. This isolation helps minimize the reduction in the amplifier's phase-margin and improves the amplifier stability resulting in reduced peaking and settling times.