Xilinx Automotive – Flexible Solutions Beyond Silicon

DRIVING AUTOMOTIVE SOLUTIONS

Solutions Beyond Silicon

Xilinx leads one of the fastest-growing segments of the semiconductor industry—Programmable Logic Devices (PLDs). With over 50 percent market share, Xilinx PLDs are rapidly becoming the solution of choice for automotive applications, offering extreme flexibility, proven reliability, and the freedom to change functionality even after being manufactured. As the automotive electronics market grows in the areas of infotainment, driver assistance and driver information systems, Xilinx devices are at the heart of each new innovation.

The Xilinx Automotive (XA) family of CPLDs and FPGAs allows for integration and platform flexibility in design, lowering costs and eliminating obsolescence concerns, while helping you achieve aggressive BOM cost targets.

To provide the complete solution, Xilinx is committed to develop, support and maintain key automotive IP blocks through our LogiCORE™ system.

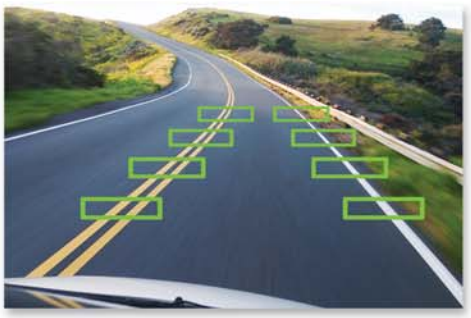
Xilinx is also working with prominent third-party companies to offer further IP modules, as well as the required operating system/software support. In addition, custom development and system integration are offered through expert design services by Xilinx, as well as by proven third-party providers.

Courtesy of Ibeo Automobile Sensor GmbH

Automotive Industry Standards

- ISO/TS16949 Automotive Certification
- AEC-Q100 Device Qualification
- RoHS Compliance
- Pb-Free Packaging
- Extended temperature ranges:
  I-Grade (T_j = -40˚C to + 100˚C)
  Q-Grade (T_j = -40˚C to +125˚C)

IMAGE PROCESSING AND RECOGNITION



Xilinx Automotive FPGAs are being utilized as key components in the deployment of vision-based Driver Assistance Systems:

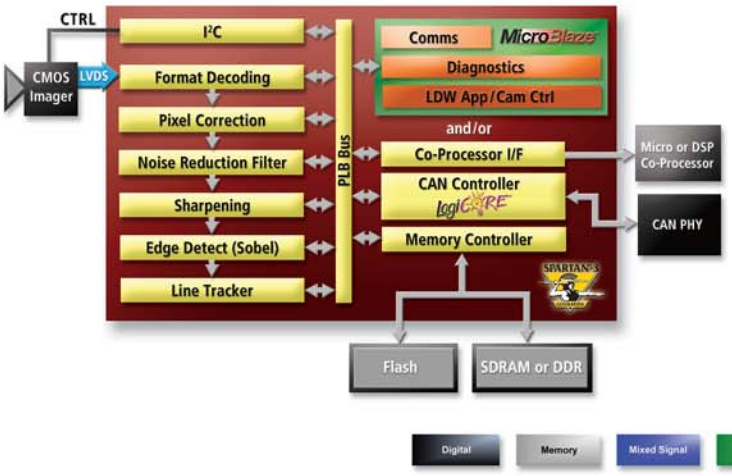
- Superior computational performance to support pixel-level image processing
- Scalability for multiple feature bundling and customization on a single platform
- Flexibility for time-to-market and processing algorithm evolutionary enhancement

Xilinx Automotive and its alliance members offer a combination of image processing IP solutions and design services tailored to automotive market needs:

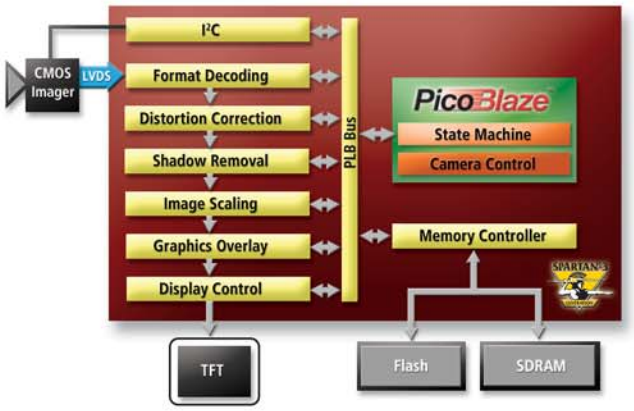
- Productized IP cores provide fundamental image processing functionality and serve as building blocks for customer-implemented designs
- Specialized design services leverage FPGA design experts with image processing experience for efficient design and implementation efforts (turn-key or collaborative)
- Application-specific development boards for proof-of-concept implementation

Vision-based Automotive Applications

Forward-Looking Example: Lane Departure Warning



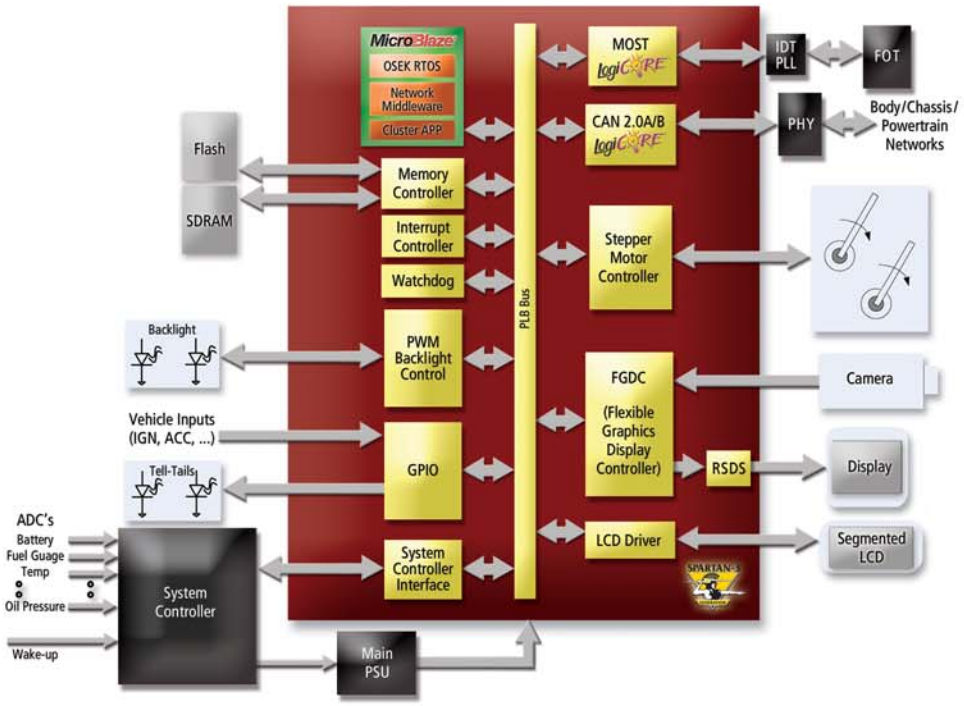
Rear-Looking Example: Back-up/Park Aid



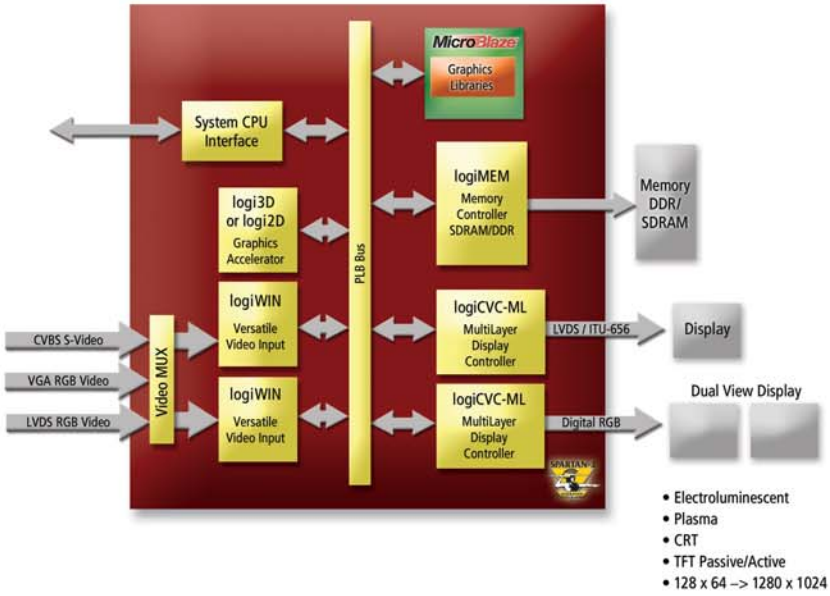
DDC's Automotive VADR module provides an FPGA-based image processing platform with the ability to record raw roadway video data in the field for laboratory evaluation.

VIDEO AND GRAPHICS

Hybrid Instrument Cluster



Flexible Graphics Display Controller System



- Electroluminescent
- Plasma
- CRT
- TFT Passive/Active
- 128 x 64 –> 1280 x 1024

Scalability and Flexibility

The scalability and flexibility of FPGAs can be leveraged by the system architect in multiple ways. For example, in driver information applications, the increased usage of LED background lighting in today's instrument clusters requires sophisticated control of the individual LEDs to match the exact color and brightness in OEM specifications.

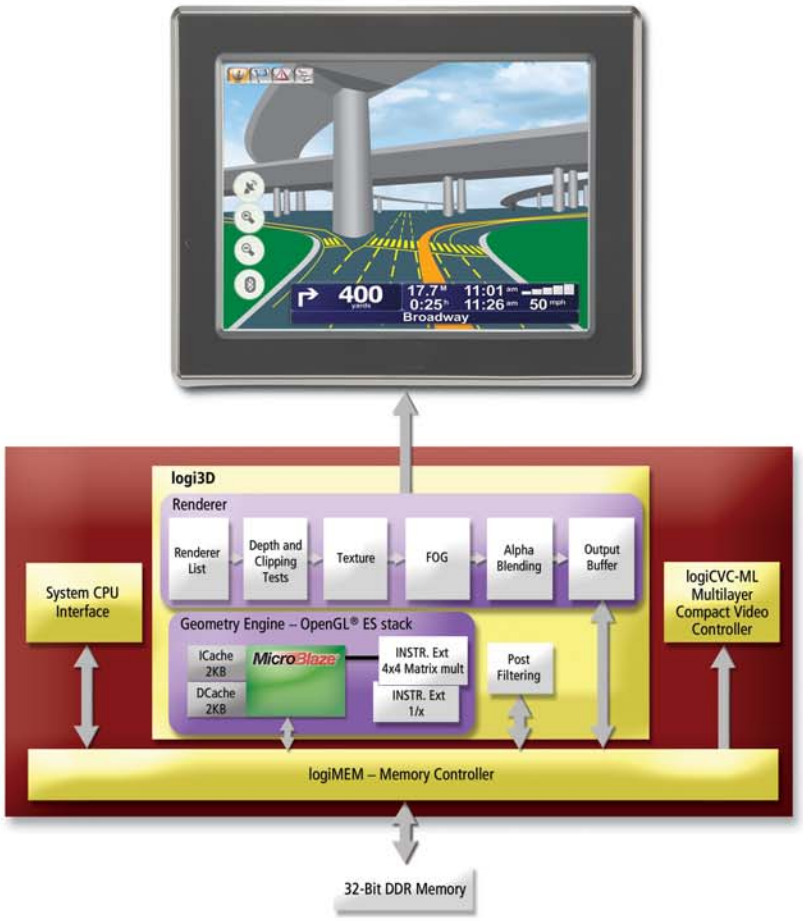
Based on production variances of the LEDs, along with varying numbers and arrangements inside the clusters, achieving high production yields has become difficult and now requires individual end-of-line programmability, easily achievable with FPGA technology.

Easy LCD Interfacing

Deployment of hybrid instrument clusters consisting of various numbers of traditional analog gauges, with the addition of an LCD TFT display, poses further challenges to the developer. Built-in support on Spartan™-3 generation products for low-swing differential I/O standards, such as Reduced Swing Differential Signaling (RSDS), make external terminating resistors obsolete by simultaneously simplifying the physical connection between the FPGA and the display.

Different kinds of display connections, as well as resolutions, can easily be overcome with the highly scalable and flexible FPGA approach, covering a complete range of needs from simple text, to 2D animation, to graphics-intensive 3D representations.

3D Graphics Accelerator



Xylon® Graphics Display Controller Solution

- Xylon Graphics Display Controller solution features a set of configurable IP that is fully compatible with the Xilinx EDK Platform Studio, allowing for complete systems with optional Microblaze™ embedded processor with little, or no, VHDL coding required
- Xylon IP cores combined with a Spartan XA FPGA scale very efficiently, thus making it possible to size the FPGA to a particular end-product configuration, and optimize cost-per-function without changing platform architecture or board design
- Graphics subsystems can be assembled with the appropriate features that are well suited to an entire range of low- to high-performance graphics systems, with or without video support, all at a competitive cost
- Scaling the number of displays to two or more in a system, such as Rear-Seat Entertainment, is now possible on a single FPGA

Supporting a Wide Range of Applications

- Low-end graphics systems, such as message centers or HVAC control, requiring display functions such as blend, fade, scroll, and simple animation of graphic objects through the use of a multilayer alpha blended LCD controller and basic 2D acceleration
- Mid/High-end graphics systems, such as fully reconfigurable LCD instrument clusters or Rear-Seat Entertainment systems, requiring additional operations such as bitmap decompression, anti-aliased scalable fonts, bitmap rotation, and bitmap translation/scaling
- High-end graphics systems, such as navigation or advanced user interfaces, requiring real time manipulation of 3D graphics including texture rendering, shading, or other true 3D effects

logicBRICKS™
Designed by XYLON

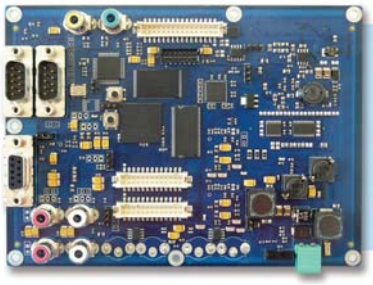
Xylon graphics software support ranges from basic embedded graphic libraries (i.e. Segger emWIN) to complete end-to-end development solutions including GUI development environments (i.e. Altia) and industry standard interfaces (i.e. OpenGL ES).

APPLICATION DEVELOPMENT PLATFORMS

logiCRAFT2

The logiCRAFT2 provides designers with an evaluation and development platform targeted for multi-display automotive infotainment systems, such as rear-seat entertainment products. Using a completely field-configurable platform, it combines the highly popular Xilinx MicroBlaze 32-bit microprocessor core together with a wide range of graphics and display controller IP modules from Xylon's logicBRICKS™ IP core family. Based on a Xilinx Spartan-3 FPGA 1.5 million system gate platform, it is capable of:

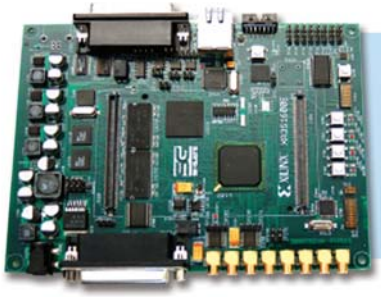
- Driving up to three different displays simultaneously, including configurable power supply voltages for each, with different video streams on each display
- Supporting a wide variety of video input and output standards, including: LVDS, CMOS, digital and analog RGB, COG and CVBS
- Providing complementary audio inputs and outputs, including infrared-based audio transmission for wireless headphone utilization
- Connectivity to automotive bus systems, such as LIN, CAN and MOST® standards, as well as other industry standards such as RS232, USB and Ethernet



logiCRAFT3

The logiCRAFT3 is derived from the logiCRAFT2 platform utilizing a smaller form factor, ideally to fit behind a 7" LCD, targeting single and remote display applications in the automotive environment. It is based on a completely field-configurable platform combining the Xilinx MicroBlaze 32-bit micro-processor core together with the wide range of graphics and display controller IP modules from Xylon's logicBRICKS IP core offerings.

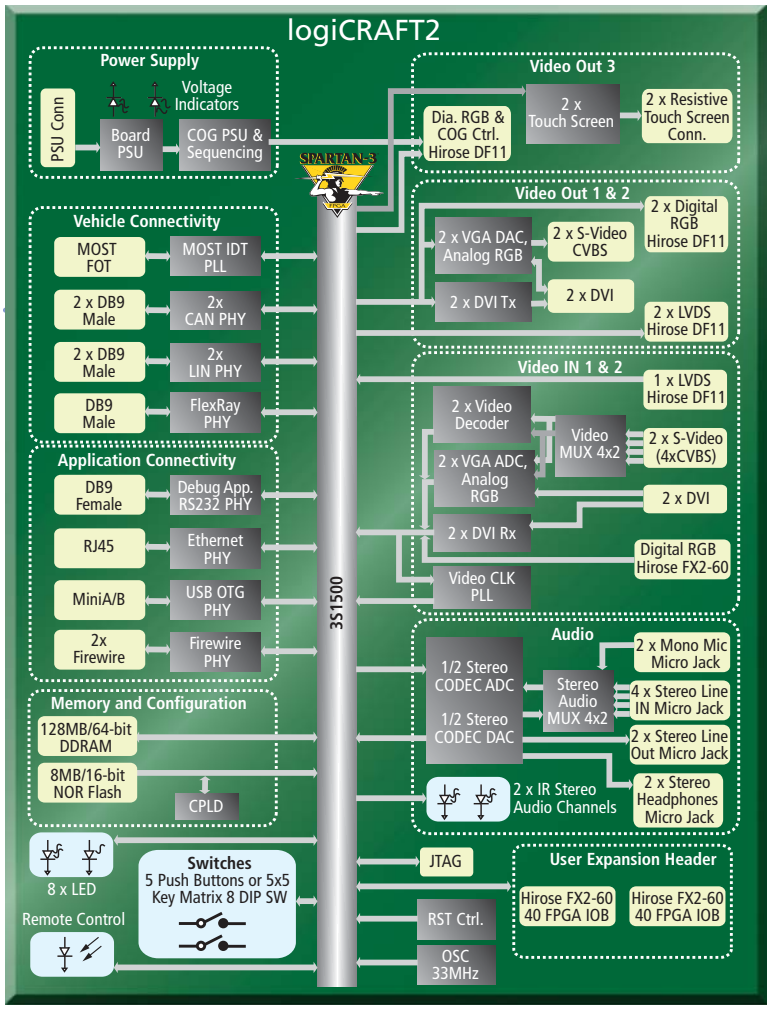
- The platform supports a wide variety of simultaneous video input and output standards, such as CVBS or S-Video supporting PAL/NTSC/SECAM as well as one/two twisted pairs 1-wire LVDS based on APIX by Inova—COG displays as well as different COG power supply requirements are also supported
- Audio input and output capabilities
- Connectivity is provided via CAN and RS232; in addition, it can be optionally extended with an Apple iPod compatible serial interface, as well as a Bluetooth module based on Cambridge Silicon Radio
- Provisions to control a touch screen are also offered

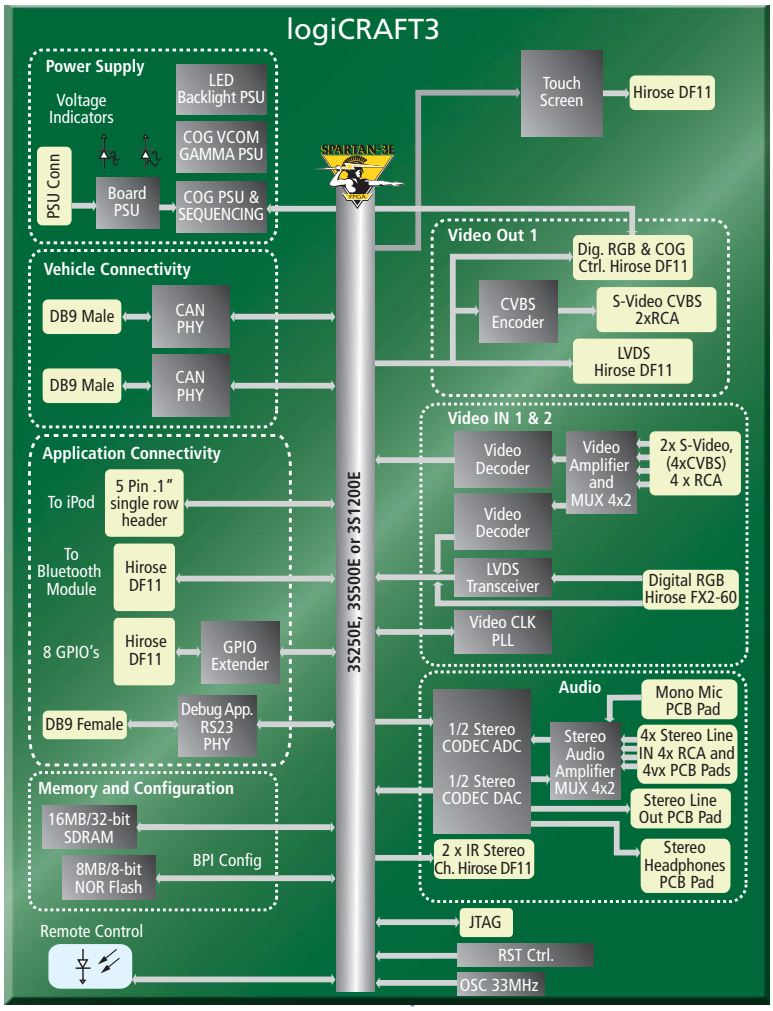


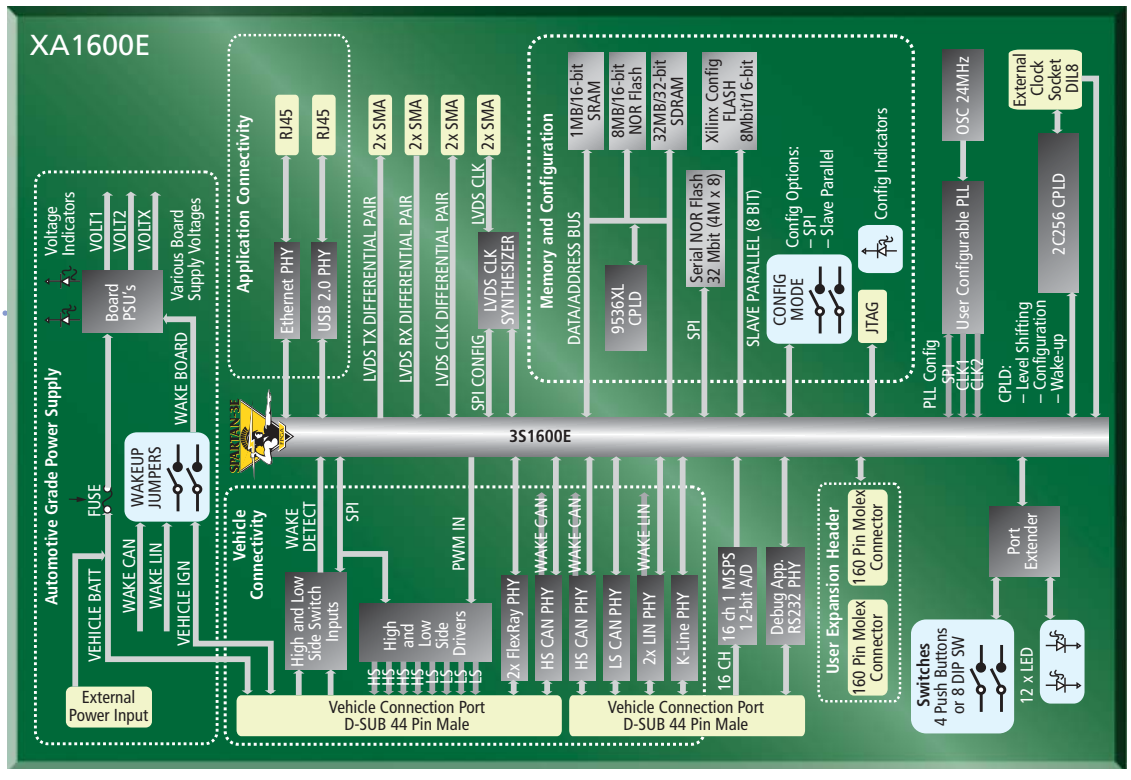
XA1600E Board

The Automotive ECU Development Kit (HW-XA3S1600E-UNI-G) provides designers with a configurable and expandable out-of-the-box platform, suitable for a wide range of Automotive applications. Due to its small form factor, it can easily be placed in a standard metal housing. The board has also been designed to be powered by a 12 volt power supply for in-vehicle prototype use.

- Powered by a completely field-configurable platform running on a Xilinx Spartan-3E FPGA, it combines programmable logic for custom-driven IP applications as well as the popular Xilinx MicroBlaze 32-bit microprocessor core
- Features robust memory subsystem containing on-board Flash and SRAM memory
- Supports standard Automotive and System-on-Chip peripherals including all necessary physical layers on-board the ECU, such as JTAG, 10/100 Ethernet, USB 2.0, 12-bit ADC, High- and Low-Speed CAN, FlexRay™, LIN, K-Line, UART, SPI and over 150 user programmable I/Os







XILINX AUTOMOTIV

Image Processing and Recognition

Xilinx and its alliance members offer solutions beyond silicon by providing IP building blocks and design services in the areas of image processing and recognition. This allows for faster development and product differentiation for driver assistance applications, including:

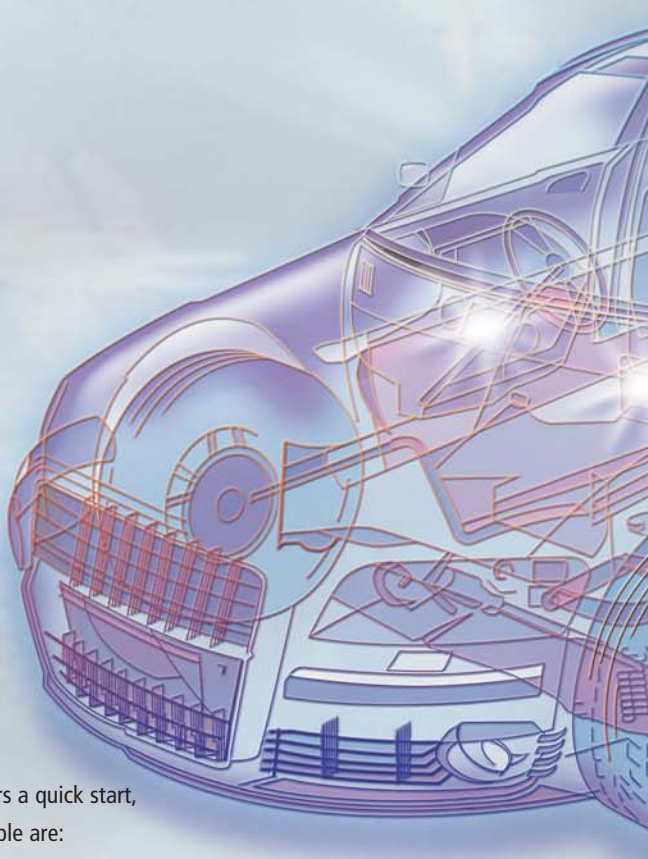
- Night Vision
- Lane Departure Warning
- Park Assist
- Back Guide Monitor
- Adaptive Cruise Control
- Drowsy Driver Detection

Courtesy of Robert Bosch GmbH

Video and Graphics

Offerings of key IP building blocks and design services allow for highly scalable and cost-efficient implementations of infotainment and driver information systems, including:

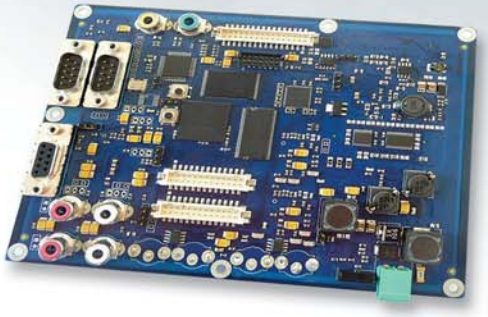
- Head-Unit
- Rear-Seat Entertainment
- TV Tuner
- Audio/Multimedia Systems
- Game Consoles
- Hybrid Instrument Cluster
- Heads-up Display



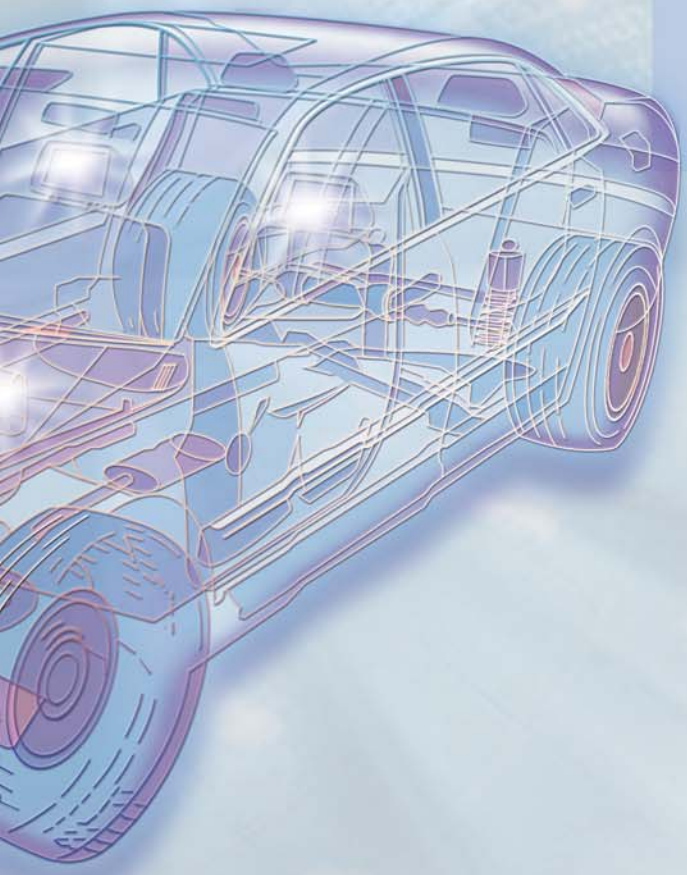
Application Development Platforms

Off-the-shelf, application-specific development platforms are available to provide developers a quick start, and serve as a comprehensive hardware base to satisfy their expectations. Currently available are:

- Automotive ECU Development Kit (HW-XA3S1600E-UNI-G)
- logiCRAFT2—Infotainment Development Platform
- logiCRAFT3—Compact Multimedia Display Development Platform
- VADR—Image Processing Development Platform



E – AT A GLANCE



Xilinx Technology Leadership

Xilinx leads the way in Programmable Logic Devices (PLDs), one of the fastest growing segments of the semiconductor industry.

- Inventing and driving the technology of the Field Programmable Gate Array (FPGA)
- Offering highly scalable and flexible devices, where features and functions can be changed "on the fly," or upgraded in the field
- Supplying more than 50% of the market for these devices today
- Expert design services through Xilinx and third party providers
- Full compliance and certification to ISO-9001, ISO-14001 and ISO/TS16949

Xilinx Automotive Products

Xilinx Automotive solutions are driven by a dedicated automotive product line, based on:

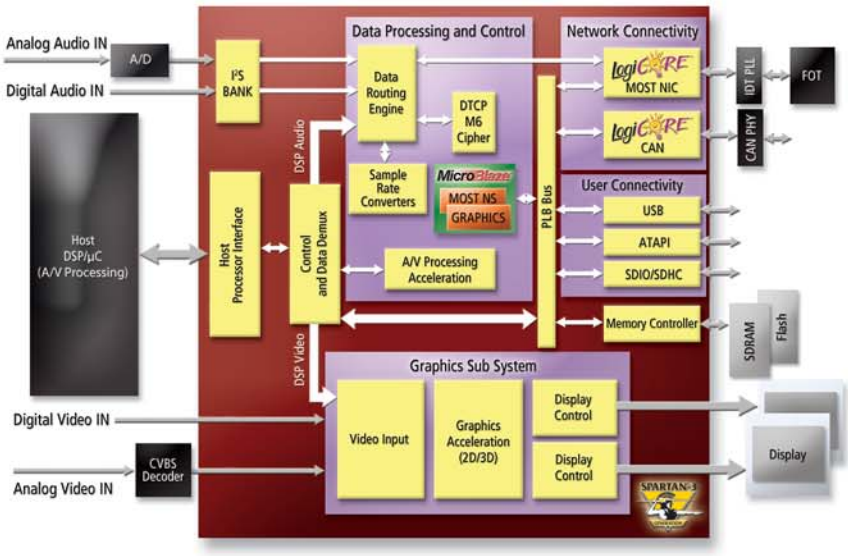
- Pin-compatible products in various densities and packages suited for automotive applications
- AEC-Q100 qualified products
- Production Part Approval Process (PPAP) documentation for all XA products
- A continuous improvement strategy
- Active membership in the Automotive Electronics Council (AEC) Technical Specification Committee
- Associate membership in AUTOSAR, JASPAR, MOST Cooperation and FlexRay Consortium

Vehicle Networking

Xilinx has designed, and is directly supporting, key automotive-specific network interfaces. Xilinx works together with leading industry companies to provide customers access to a comprehensive solution.

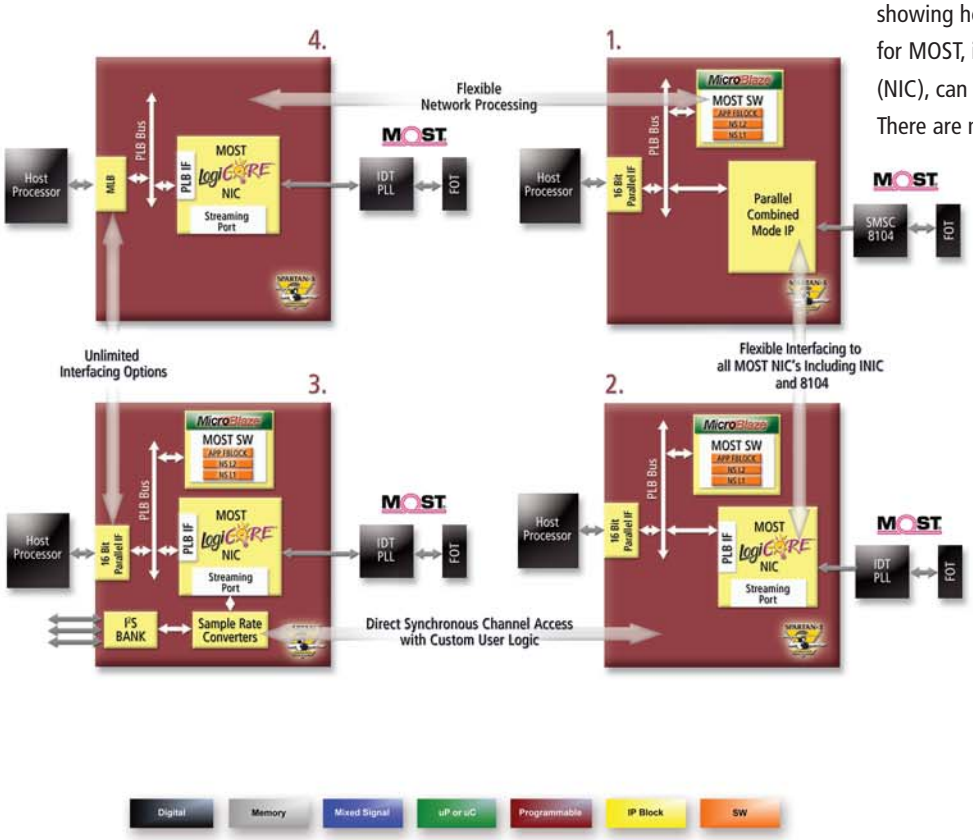
CAN MOST mocean vector FlexRay

VEHICLE NETWORKING



This super-set block diagram of an infotainment rear-seat entertainment application shows a possible set-up based on the combination of a host or digital signal processor (DSP) together with an FPGA. In this example, the FPGA acts as a companion chip to the host, providing multiple functions, such as audio/video processing acceleration, a graphics sub-system, and different user and vehicle networking connections, such as CAN and MOST.

Flexible MOST Architecture – your design, your way



The following overview outlines four architectural options showing how various components within the Xilinx solution for MOST, including the MOST Network Interface Controller (NIC), can be utilized to realize efficient system architectures. There are many possible combinations that are not constrained by fixed or predetermined interfaces, but can be freely defined based on the desired overall system architecture.

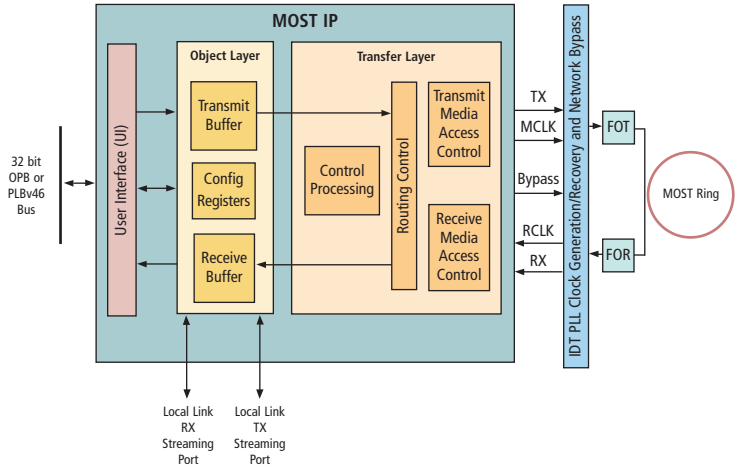
1. Off-loading the host processor by utilizing the MicroBlaze processor to run the full MOST Network Services software stack along with OEM-specific FBlocks and High-Level-Protocols in conjunction with the OS8104 (PCM IP) or OS81050 (MLB IP).

2. Utilization of available LogiCORE IP to completely eliminate the need for an external MOST network controller.

3. Addition of direct access to the synchronous MOST channels to perform pre- or post-processing of incoming or outgoing data in FPGA hardware without the need for any software overhead.

4. Connectivity to a wide range of different host interfaces.

MOST Solution

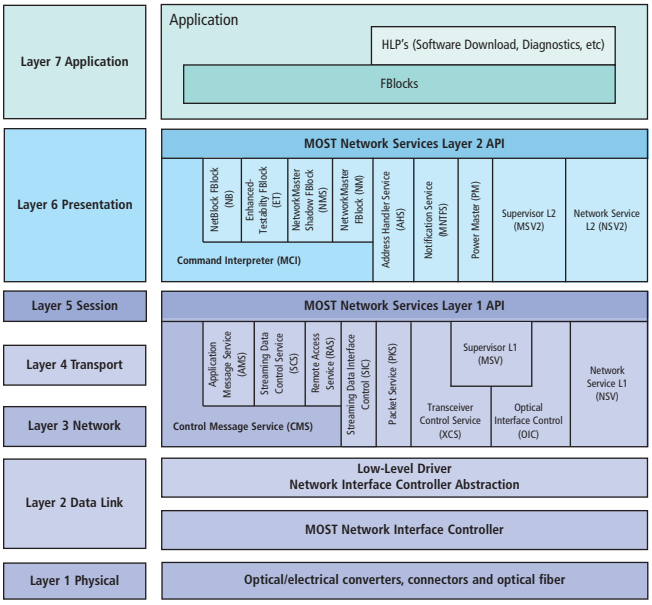


MOST IP Specifics					
Supported XA Device Families	Spartan-3, Spartan-3E, Spartan-3A, Spartan-3A DSP				
	I/O	LUTs	FFs	Block RAMs	Slices*
Resources Used	7	4049-4117	2535-2580	6	2930-2990

* Represent typical slice count for Spartan-3 generation devices. Results will vary on device utilization and ISE options

The LogiCORE IP for the Media Oriented Systems Transport (MOST) is a complete NIC supporting the MOST Specification revision 2.4 or later for the MOST25 network. Capabilities include:

- Compatible with SMSC 8104(A), OS8105x (INIC) and Analog Devices MXVR transceivers
- Direct interface to MOST ring via IDT PLL (IDT5V80001) for clock generation/recovery and the fiber optic transceiver (FOT)
- Operates in both master and slave modes
- Synchronous, asynchronous, and control channels with 4-60 bytes of synchronous data per frame including support of up to full bandwidth sustained transfers (24 Mbps)
- Streaming port allows synchronous data co-processing with low host controller overhead
- Full support of error and status notification including support for ring break diagnosis test
- Supported in CORE Generator™ software for stand alone applications and in EDK for MicroBlaze-based ECU applications

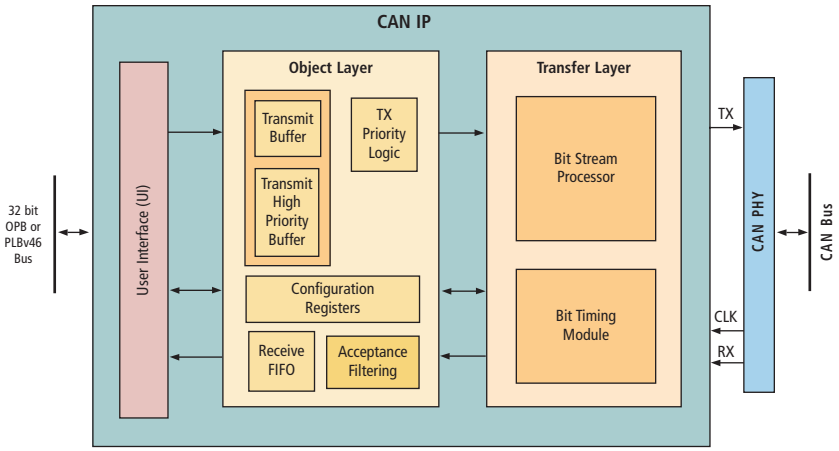


Working closely with Mocean Laboratories AB, and the MOST Cooperation, Xilinx enables a portable and highly modular MOST solution where applications can be moved between NICs without source code modification. The MOST solution is comprised of:

- Full software stack (up to MOST Specification revision 2.5) supporting Xilinx solution for MOST
- Versions also available supporting SMSC OS8104(A) and OS8105x (INIC) for MicroBlaze processor
- All services and protocols standardized in the MOST Cooperation are supported
- MOST Cooperation and several OEM FBlocks and High-level Protocol Modules available including source code
- Fully linked/structured electronic documentation
- ANSI-C Source code with automated documentation generation
- Browse documentation using Service, Module, Function or Variable views
- Application examples library available as source code

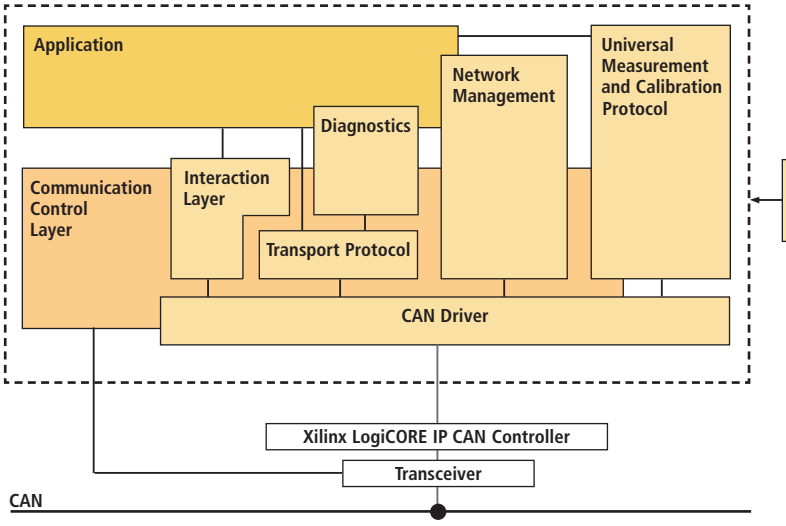
MOCEAN
DRIVEN BY INNOVATION

CAN Solution



CAN IP Specifics					
Supported XA Device Families	Spartan-3, Spartan-3E, Spartan-3A, Spartan-3A DSP				
Resources Used	I/O	LUTs	FFs	BlockRAMs	Slices*
	3	868-1056	411-593	2	569-885

* Represent typical slice count for Spartan-3 generation devices. Results will vary on device utilization and ISE options



Courtesy of Vector Group

The LogiCORE IP for the Controller Area Network (CAN) is a controller compliant to ISO 11898-1, CAN 2.0A and CAN 2.0B standards. It provides characteristics such as:

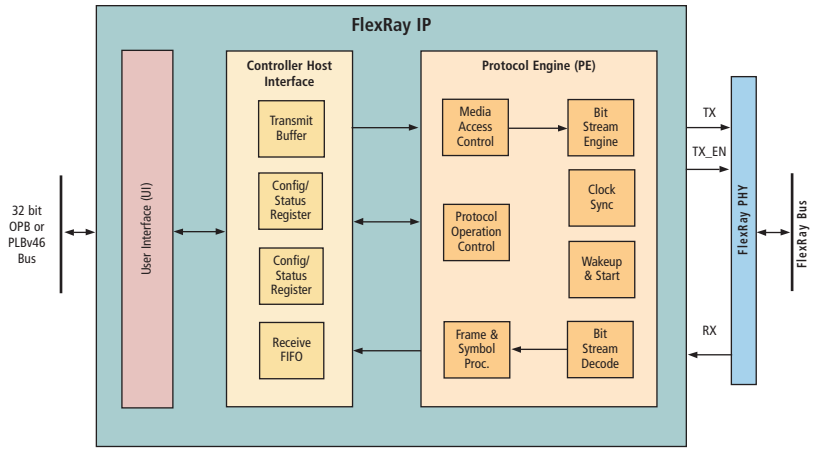
- Validated at C&S group
- Supports bit rates of up to 1 Mbps
- Supports both standard (11-bit identifier) and extended (29-bit identifier) frames
- Transmit and receive message FIFOs with user-configurable depths of up to 64 messages
- Transmit prioritization through one High-Priority Transmit buffer
- Acceptance filtering (user-configurable number) of up to 4 acceptance filters
- Maskable Error and Status Interrupts
- Supported in CORE Generator software for stand alone applications and in EDK for MicroBlaze-based ECU applications

Working closely with Vector, the availability of the CAN Driver for the Xilinx MicroBlaze 32-bit processor, enables easy access to the full suite of Vector's CANbedded Software solution.

- The CAN Driver handles the hardware-specific characteristics of the Xilinx FPGA and provides the initialization, wakeup detection, transmission and reception of messages with data—and functional interface data—and functional notification including indication and confirmation as well as overrun and error handling
- Provision of a standardized application interface to the higher level software modules as the interaction layer, transport protocol, network management, universal measurement and calibration protocol also available through Vector
- Several diagnostics layers available in accordance with ISO14229 (UDS) and ISO14230 (Keyword Protocol 2000)
- Full integration into the Vector tools chain including flash programming, operating system, database and debug tools

vector

FlexRay Solution

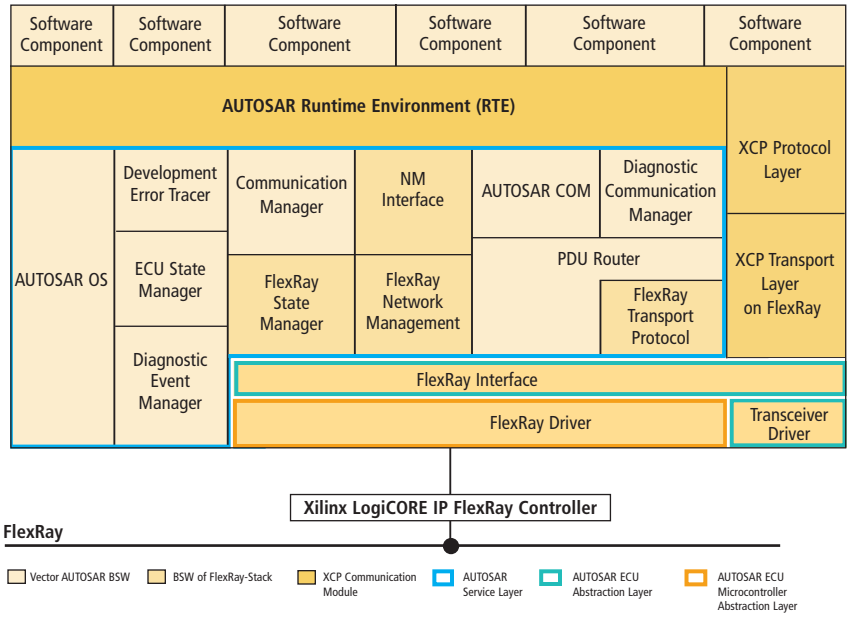


The LogiCORE IP for FlexRay is a controller that implements the FlexRay communication protocol as defined in the FlexRay Protocol Specification v2.1 Rev A. It provides functionalities such as:

- Data rate of up to 10 Mbps
- Single Communication Channel
- Scalable synchronous and asynchronous data transmission
- Configurable payload length up to a maximum of 256 bytes
- Configurable receive and transmit buffers for storage of up to 128 messages each
- Frame ID, cycle counter and message ID based receive filtering
- OPB and PLB interface suitable with single and burst support
- Variable OPB and PLB interface clock
- Supported in CORE Generator software for stand alone applications and in EDK for MicroBlaze-based ECU applications

FlexRay IP Specifics					
Supported XA Device Families	Spartan-3, Spartan-3E, Spartan-3A, Spartan-3A DSP				
Resources Used	I/O	LUTs	FFs	Block RAMs	Slices*
	5	5506-6587	3179-3386	9 to 18	4028-4789

* Represent typical slice count for Spartan-3 generation devices. Results will vary on device utilization and ISE options



Courtesy of Vector Group

Availability of the FlexRay Driver for the Xilinx MicroBlaze 32-bit processor enables easy access to the full suite of Vector's FlexRay software solution developed according to the AUTOSAR specification.

- The FlexRay Driver handles the hardware-specific characteristics of the Xilinx FPGA and acts as an abstraction layer to other software offerings available through Vector, covering the signal, diagnostic and transport layer as well as the network support and node management
- Full support of the FlexRay synchronous layer for the driver as well as support of the FlexRay asynchronous layer for the protocol stack and the application
- Full integration into the Vector tool chain including the DaVinci Network Designer for FlexRay supporting multiple FIBEX revisions, the development & analysis tool with real-time support, as well as measurements and calibrations of ECUs

vector

XILINX AUTOMOTIVE DEVICES

FPGAs

		Spartan-IIE					Spartan-3					Spartan-3E				
	Part Number	XA2S50E	XA2S100E	XA2S150E	XA2S200E	XA2S300E	XA3S50	XA3S200	XA3S400	XA3S1000	XA3S1500	XA3S100E	XA3S250E	XA3S500E	XA3S1200E	XA3S1600E
Logic Resources	System Gates [1]	50K	100K	150K	200K	300K	50K	200K	400K	1000K	1500K	100K	250K	500K	1200K	1600K
	Slices [2]	768	1,200	1,728	2,352	3,072	768	1,920	3,584	7,680	13,312	960	2,448	4,656	8,672	14,752
	Logic Cells	1,728	2,700	3,888	5,292	6,912	1,728	4,320	8,064	17,280	29,952	2,160	5,508	10,476	19,512	33,192
	CLB Flip-Flops	1,536	2,400	3,456	4,704	6,144	1,536	3,840	7,168	15,360	26,624	1,920	4,896	9,312	17,344	29,504
Memory Resources	Maximum Distributed RAM (Kbits)	24	37	54	73	96	12	30	56	120	208	15	38	73	136	231
	Block RAM Blocks	8	10	12	14	16	4	12	16	24	32	4	12	20	28	36
	Total Block RAM (Kbits)	32	40	48	56	64	72	216	288	432	576	72	216	360	504	648
Clock Resources	Digital Clock Managers (DCMs) Spartan-3, (DLLs) Spartan-IIE	4	4	4	4	4	2	4	4	4	4	2	4	4	8	8
I/O Resources	Maximum Single Ended I/Os	102	102	182	182	182	124	173	264	333	487	108	172	190	304	376
	Maximum Differential I/O Pairs	28	28	83	83	83	56	76	116	149	221	40	68	77	124	156
	I/O Standards Supported	LVTTL, LVCMOS25, LVCMOS18, HSTL Class I, HSTL Class III, HSTL Class IV, PCI 3.3V 32 - 33MHz, PCI-X 3.3V, SSTL3 Class I, SSTL3 Class II, SSTL2 Class I, SSTL2 Class II, AGP-2x, CTT, LVDS, Bus LVDS, LVPECL25 & 33					LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, GTL, GTL+, HSTL15 Class I, HSTL15 Class III, HSTL18 Class I, HSTL18 Class II, HSTL18 Class III, PCI 3.3V 32/64bit 33MHz, SSTL2 Class I, SSTL2 Class II, SSTL18 Class I, Bus LVDS, LDT (ULVDS), LVDS_ext, LVDS25 & 33, LVPECL25, RSDS25					LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, HSTL18 Class I, HSTL18 Class III, PCI 3.3V 32/64bit 33MHz, PCI-X 3.3V, SSTL2 Class I, SSTL18 Class I, Bus LVDS, LVDS25, LVPECL25, Mini-LVDS25, RSDS25				
Embedded Hard IP Resources	DSP48A Slices	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Dedicated Multipliers	—	—	—	—	—	4	12	16	24	32	4	12	20	28	36
	Device DNA Security	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Miscellaneous	Temperature Range [4]	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I	I, Q	I, Q	I, Q	I, Q	I, Q
	Speed Grade	-6	-6	-6	-6	-6	-4	-4	-4	-4	-4	-4	-4	-4	-4	-4
	RoHS (Pb-free)	No	No	No	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	XA Released	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Configuration	Configuration Memory Bits (Mbits)	0.6	0.9	1.1	1.4	1.9	0.4	1.0	1.7	3.2	5.2	0.6	1.4	2.3	3.8	6.0

Package	Area	Maximum User I/Os														
VQFP Packages (VQ): very thin QFP (0.5 mm lead spacing)																
VQG100	16 x 16 mm						63	63				66	66			
Chip Scale Packages (CP): wire-bond chip-scale BGA (0.5 mm ball spacing)																
CPG132	8 x 8 mm											83	92	92		
TQFP Packages (TQ): thin QFP (0.5 mm lead spacing)																
TQG144	22 x 22 mm	102	102					97				108	108			
PQFP Packages (PQ): wire-bond plastic QFP (0.5 mm lead spacing)																
PQG208	30.6 x 30.6 mm						124	141	141				158	158		
FGA Packages (FT): wire-bond fine-pitch thin BGA (1.0 mm ball spacing)																
FTG256	17 x 17 mm			182	182	182		173	173	173			172	190	190	
FGA Packages (FG): wire-bond fine-pitch BGA (1.0 mm ball spacing)																
FGG400	21 x 21 mm														304	304
FGG456	23 x 23 mm								264	333	333					
FGG484	23 x 23 mm															376
FGG676	27 x 27 mm										487					

Notes: 1. System Gates include 20%-30% of CLBs used as RAMs. 2. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic. Integrated in the DSP48A slices (Advanced Multiply Accumulate element). 4. Temperature Range Automotive I (T_j = -40°C to +100°C); Automotive Q (T_j = -40°C to +125°C)

FPGAs

		Spartan-3A				Spartan-3A DSP	
	Part Number	XA3S200A	XA3S400A	XA3S700A	XA3S1400A	XA3SD1800A	XA3SD3400A
Logic Resources	System Gates [1]	200K	400K	700K	1400K	1800K	3400K
	Slices [2]	1,792	3,584	5,888	11,264	16,640	23,872
	Logic Cells	4,032	8,064	13,248	25,344	37,440	53,712
	CLB Flip-Flops	3,584	7,168	11,776	22,528	33,280	47,744
Memory Resources	Maximum Distributed RAM (Kbits)	28	56	92	176	260	373
	Block RAM Blocks	16	20	20	32	84	126
	Total Block RAM (Kbits)	288	360	360	576	1,512	2,268
Clock Resources	Digital Clock Managers (DCM)	4	4	8	8	8	8
I/O Resources	Maximum Single Ended I/Os	195	311	372	375	519	469
	Maximum Differential I/O Pairs	90	142	165	165	227	213
	I/O Standards Supported	LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, HSTL15 Class I, HSTL15 Class III, HSTL18 Class I, HSTL18 Class II, HSTL18 Class III, PCI 3.3V 32/64bit 33MHz, PCI-X 3.3V, SSTL3 Class I, SSTL3 Class II, SSTL2 Class I, SSTL2 Class II, SSTL18 Class I, SSTL18 Class II, Bus LVDS, LVDS25 & 33, LVPECL25 & 33, Mini-LVDS25 & 33, RSDS25 & 33, TMDS25 & 33, PPDS25 & 33					
Embedded Hard IP Resources	DSP48A Slices	—	—	—	—	84	126
	Dedicated Multipliers	16	20	20	32	84 [3]	126 [3]
	Device DNA Security	Yes	Yes	Yes	Yes	Yes	Yes
Miscellaneous	Temperature Range [4]	I, Q	I, Q	I, Q	I, Q	I, Q	I
	Speed Grade	-4	-4	-4	-4	-4	-4
	RoHS (Pb-free)	Yes	Yes	Yes	Yes	Yes	Yes
	XA Released	No	No	No	No	No	No
Configuration	Configuration Memory Bits (Mbits)	1.2	1.9	2.7	4.8	8.2	11.7

Package	Area	Maximum User I/Os					
FGA Packages (FT): wire-bond fine-pitch thin BGA (1.0 mm ball spacing)							
FTG256	17 x 17 mm	195	195				
Chip Scale Packages (CS): wire-bond chip-scale BGA (0.8 mm ball spacing)							
CSG484	19 x 19 mm					309	309
FGA Packages (FG): wire-bond fine-pitch BGA (1.0 mm ball spacing)							
FGG400	21 x 21 mm		311	311			
FGG484	23 x 23 mm			372	375		
FGG676	27 x 27 mm					519	469

Notes: 1. System Gates include 20%-30% of CLBs used as RAMs.
2. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic.
3. Integrated in the DSP48A slices (Advanced Multiply Accumulate element).
4. Temperature Range Automotive I (T_j = -40°C to +100°C); Automotive Q (T_j = -40°C to +125°C).

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CPLDs

		XA9500XL Family			CoolRunner-II Family				
	Part Number	XA9536XL	XA9572XL	XA95144XL	XA2C32A	XA2C64A	XA2C128	XA2C256	XA2C384
Logic Resources	System Gates	800	1,600	3,200	750	1,500	3,000	6,000	9,000
	Macrocells	36	72	144	32	64	128	256	384
	Product terms per Macrocell	90	90	90	56	56	56	56	56
Clock Resources	Global Clocks	3	3	3	3	3	3	3	3
	Product Term Clocks per Function Block	18	18	18	16	16	16	16	16
I/O Resources	Maximum I/O	34	72	117	33	64	100	118	118
	Input Voltage Compatible (V)	2.5/3.3/5	2.5/3.3/5	2.5/3.3/5	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3
	Output Voltage Compatible (V)	2.5/3.3	2.5/3.3	2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3
Speed Grades	Min. pin-to-pin Logic Delay (ns)	15.5	15.5	15.5	5.5	6.7	7.0	7.0	9.2
	Automotive I Speed Grades	-15	-15	-15	-6	-7	-7	-7	-10
	Automotive Q Speed Grades	-15	-15	-15	-7	-8	-8	-8	-11
Miscellaneous	Temperature Grades [1]	I, Q	I, Q	I	I, Q	I, Q	I, Q	I, Q	I, Q
	RoHS (Pb-free)	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	XA Released	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Package	Area [2]	Maximum User I/Os							
VQFP Packages (VQ): very thin QFP (0.5 mm lead spacing)									
VQG44	12 x 12 mm	34	34		33	33			
VQG64	12 x 12 mm		52						
VQG100	16 x 16 mm					64	80	80	
TQFP Packages (TQ): thin QFP (0.5 mm lead spacing)									
TQG100	16 x 16 mm		72						
TQG144	22 x 22 mm							118	118
Chip Scale Packages (CP): wire-bond chip-scale BGA (0.5 mm ball spacing)									
CPG132	8 x 8 mm						100		
Chip Scale Packages (CS): wire-bond chip-scale BGA (0.8 mm ball spacing)									
CSG144	12 x 12 mm			117					

Notes: 1. Temperature Range Automotive I (T_a = -40°C to +85°C); Automotive Q (T_a = -40°C to +105°C with T_j maximum = +125°C).
2. Area dimensions for lead-frame products are inclusive of the leads.

Corporate Headquarters

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
USA
Tel: 408-559-7778
Web: www.xilinx.com

Europe

Xilinx Europe
One Logic Drive
Citywest Business Campus
Saggart, County Dublin
Ireland
Tel: +353-1-464-0311
Web: www.xilinx.com

Japan

Xilinx K.K.
Art Village Osaki Central Tower 4F
1-2-2 Osaki, Shinagawa-ku
Tokyo 141-0032 Japan
Tel: +81-3-6744-7777
Web: japan.xilinx.com

Asia Pacific Pte. Ltd.

Xilinx, Asia Pacific
5 Changi Business Park
Singapore 486040
Tel: +65-6407-3000
Web: www.xilinx.com

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Printed in U.S.A. PN 2055