


MC9S12C Family Device User Guide V01.05

Covers also

MC9S12GC Family

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Revision History

| Version Number | Revision Date | Effective Date | Author | Description of Changes |
|----------------|---------------|----------------|--------|---|
| 00.01 | 25.JAN.03 | 25.JAN.03 | | Original Version. Based on C32 user guide version 01.12 |
| 00.02 | 07.FEB.03 | 07.FEB.03 | | Enhanced PortK description Part number table revision in preface |
| 00.03 | 25.FEB.03 | 25.FEB.03 | | QFP112 Emulation pinout correction Enhanced part number explanation in preface Reduced pseudo STOP current spec. for C64,C96,C128 |
| 00.04 | 15.APR.03 | 15.APR.03 | | Enhanced PortAD signal description Corrected VDDR description in 2.4.2 Revised pin leakage in electrical parameters |
| 00.05 | 05.MAY.03 | 05.MAY.03 | | SPI timing parameter table correction Output drive high value reduced in 3V range PE[4:2] Pull-Up spec out of reset changed 3V Expansion bus timing parameters not tested in production Minimum bus frequency specification increased to 0.25MHz. |
| 00.06 | 21.MAY.03 | 21.MAY.03 | | Parameter classification added to Appendix Table C-2. IOH changed to 4mA for 3V range. |
| 01.00 | 15.JUL.03 | 15.JUL.03 | | LVR level defined for C32. Run IDD changed for C32. Block guide reference table updated Added PCB layout guide for Pierce oscillator configuration IOL parameter updated in 3.3V range |
| 01.01 | 12.AUG.03 | 12.AUG.03 | | Updated PARTID listing due to C128 ECO revision |
| 01.02 | 20.NOV.03 | 20.NOV.03 | | Changed DOC number and CPU DOC reference number Included separate C32 LVI levels Changed PortM pull up reset state to enabled. |
| 01.03 | 27.NOV.03 | 27.NOV.03 | | Added References to the CAN-less GC-Family No major revision number increment, since silicon functionality is not changed. Added VDDX connection in PCB layout figures 8-1.to 8-6 Added Part ID for 2L45J mask set to Part ID table |
| 01.04 | 27.JAN.04 | 27.JAN.04 | | Table A-4 VDD/VDDPLL min when supplied externally now 2.35V Reference S12FTS128K1 in Preface (was S12FTS128K) Reference to CPU Guide corrected to Version2 |
| 01.05 | 11.FEB.04 | 11.FEB.04 | | Corrected flash sector sizes for C-Family devices with >64K Flash Corrected Preface Table 0-1 16K part listing to GC16 without CAN Added PPAGE specifications to memory map diagrams Added flash timing parameters for 1024 byte sector size |

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| | \$001A - \$001B Miscellaneous Peripherals (Device User Guide) | 35 |
| | \$001C - \$001D MMC map 3 of 4 (HCS12 Module Mapping Control, 36 Device User Guide) | 36 |
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| | \$001F - \$001F INT map 2 of 2 (HCS12 Interrupt) | 36 |
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Preface

The Device User Guide provides information about the MC9S12C-Family as well the MC9S12GC-Family devices made up of standard HCS12 blocks and the HCS12 processor core. This document is part of the customer documentation. A complete set of device manuals also includes the HCS12 Core User Guide and all the individual Block User Guides of the implemented modules. In an effort to reduce redundancy all module specific information is located only in the respective Block User Guide. If applicable, special implementation details of the module are given in the block description sections of this document.

The C-Family and the GC-Family offer an extensive range of package, temperature and speed options. The members of the GC-Family do not feature a CAN module.

Table 0-1 shows a feature overview of the MC9S12C and MC9S12GC Family members.

Table 0-2 summarizes the package option and size configuration.

Table 0-3 lists the part number coding based on the package, speed and temperature and preliminary die options for the C-Family.

Table 0-4 lists the part number coding based on the package, speed and temperature and preliminary die options for the GC-Family.

Table 0-1 List of MC9S12C and MC9S12GC Family members

| Flash | RAM | Device | CAN | SCI | SPI | A/D | PWM | Timer |
|-------|-----|-------------|-----|-----|-----|-----|-----|-------|
| 128K | 4K | MC9S12C128 | 1 | 1 | 1 | 8ch | 6ch | 8ch |
| | | MC9S12GC128 | — | 1 | 1 | 8ch | 6ch | 8ch |
| 96K | 4K | MC9S12C96 | 1 | 1 | 1 | 8ch | 6ch | 8ch |
| 64K | 4K | MC9S12C64 | 1 | 1 | 1 | 8ch | 6ch | 8ch |
| | | MC9S12GC64 | — | 1 | 1 | 8ch | 6ch | 8ch |
| 32K | 2K | MC9S12C32 | 1 | 1 | 1 | 8ch | 6ch | 8ch |
| | | MC9S12GC32 | — | 1 | 1 | 8ch | 6ch | 8ch |
| 16K | 1K | MC9S12GC16 | — | 1 | 1 | 8ch | 6ch | 8ch |

Table 0-2 MC9S12C-Family Package Option Summary

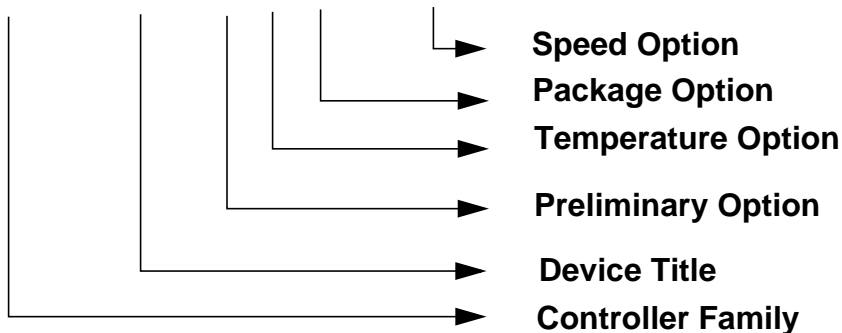
| Package | Device | Part Number | Mask ¹ set | Temp. ² Options | Flash | RAM | I/O ^{3,4} |
|---------|------------|-------------|--------------------------|-------------------------------|-------|-----|--------------------|
| 48LQFP | MC9S12C128 | MC9S12C128 | 0L09S | M, V, C | 128K | 4K | 31 |
| 52LQFP | MC9S12C128 | MC9S12C128 | 0L09S | M, V, C | | | 35 |
| 80QFP | MC9S12C128 | MC9S12C128 | 0L09S | M, V, C | | | 60 |
| 48LQFP | MC9S12C96 | MC9S12C96 | TBD | M, V, C | 96K | 4K | 31 |
| 52LQFP | MC9S12C96 | MC9S12C96 | TBD | M, V, C | | | 35 |
| 80QFP | MC9S12C96 | MC9S12C96 | TBD | M, V, C | | | 60 |

| Package | Device | Part Number | Mask ¹ set | Temp. ² Options | Flash | RAM | I/O ^{3,4} |
|---------|-------------|-------------|-----------------------|----------------------------|-------|-----|--------------------|
| 48LQFP | MC9S12C64 | MC9S12C64 | TBD | M, V, C | 64K | 4K | 31 |
| 52LQFP | MC9S12C64 | MC9S12C64 | TBD | M, V, C | | | 35 |
| 80QFP | MC9S12C64 | MC9S12C64 | TBD | M, V, C | | | 60 |
| 48LQFP | MC9S12C32 | MC9S12C32 | 1L45J | M, V, C | 32K | 2K | 31 |
| 52LQFP | MC9S12C32 | MC9S12C32 | 1L45J | M, V, C | | | 35 |
| 80QFP | MC9S12C32 | MC9S12C32 | 1L45J | M, V, C | | | 60 |
| 48LQFP | MC9S12GC128 | MC9S12GC128 | 0L09S | M, V, C | 128K | 4K | 31 |
| 52LQFP | MC9S12GC128 | MC9S12GC128 | 0L09S | M, V, C | | | 35 |
| 80QFP | MC9S12GC128 | MC9S12GC128 | 0L09S | M, V, C | | | 60 |
| 48LQFP | MC9S12GC128 | MC9S12GC64 | TBD | M, V, C | 64K | 4K | 31 |
| 52LQFP | MC9S12GC128 | MC9S12GC64 | TBD | M, V, C | | | 35 |
| 80QFP | MC9S12GC128 | MC9S12GC64 | TBD | M, V, C | | | 60 |
| 48LQFP | MC9S12GC32 | MC9S12GC32 | 1L45J | M, V, C | 32K | 2K | 31 |
| 52LQFP | MC9S12GC32 | MC9S12GC32 | 1L45J | M, V, C | | | 35 |
| 80QFP | MC9S12GC32 | MC9S12GC32 | 1L45J | M, V, C | | | 60 |
| 48LQFP | MC9S12GC16 | MC9S12GC16 | 1L45J | M, V, C | 16K | 2K | 31 |
| 52LQFP | MC9S12GC16 | MC9S12GC16 | 1L45J | M, V, C | | | 35 |
| 80QFP | MC9S12GC16 | MC9S12GC16 | 1L45J | M, V, C | | | 60 |

NOTES:

1. Maskset dependent errata can be accessed at http://e-www.motorola.com/wbapp/sps/site/prod_summary.jsp
2. C: T_A = 85°C, f = 25MHz. V: T_A = 105°C, f = 25MHz. M: T_A = 125°C, f = 25MHz
3. All C-Family derivatives feature 1 CAN, 1 SCI, 1 SPI, an 8-channel A/D, a 6-channel PWM and an 8 channel timer. The GC-Family members do not have the CAN module
4. I/O is the sum of ports capable to act as digital input or output.

MC9S12 C32 (P)C FU 25



Temperature Options

- C = -40°C to 85°C
- V = -40°C to 105°C
- M = -40°C to 125°C

Package Options

- FU = 80QFP
- PB = 52LQFP
- FA = 48LQFP

- Speed Options**
 25 = 25MHz bus
 16 = 16MHz bus

Figure 0-1 Order Part number Coding

Table 0-3 MC9S12C-Family Part Number Coding

| Part Number | Mask set | Temp. | Package | Speed | Description |
|-----------------|----------|-------------|---------|-------|-------------|
| MC9S12C128CFA16 | TBD | -40°C, 85°C | 48LQFP | 16MHz | C128 die |

| Part Number | Mask set | Temp. | Package | Speed | Description |
|-----------------|----------|--------------|---------|-------|--------------------------------|
| MC9S12C128CPB16 | TBD | -40°C, 85°C | 52LQFP | 16MHz | C128 die |
| MC9S12C128CFU16 | TBD | -40°C, 85°C | 80QFP | 16MHz | C128 die |
| MC9S12C128VFA16 | TBD | -40°C, 105°C | 48LQFP | 16MHz | C128 die |
| MC9S12C128VPB16 | TBD | -40°C, 105°C | 52LQFP | 16MHz | C128 die |
| MC9S12C128VFU16 | TBD | -40°C, 105°C | 80QFP | 16MHz | C128 die |
| MC9S12C128MFA16 | TBD | -40°C, 125°C | 48LQFP | 16MHz | C128 die |
| MC9S12C128MPB16 | TBD | -40°C, 125°C | 52LQFP | 16MHz | C128 die |
| MC9S12C128MFU16 | TBD | -40°C, 125°C | 80QFP | 16MHz | C128 die |
| MC9S12C128CFA25 | TBD | -40°C, 85°C | 48LQFP | 25MHz | C128 die |
| MC9S12C128CPB25 | TBD | -40°C, 85°C | 52LQFP | 25MHz | C128 die |
| MC9S12C128CFU25 | TBD | -40°C, 85°C | 80QFP | 25MHz | C128 die |
| MC9S12C128VFA25 | TBD | -40°C, 105°C | 48LQFP | 25MHz | C128 die |
| MC9S12C128VPB25 | TBD | -40°C, 105°C | 52LQFP | 25MHz | C128 die |
| MC9S12C128VFU25 | TBD | -40°C, 105°C | 80QFP | 25MHz | C128 die |
| MC9S12C128MFA25 | TBD | -40°C, 125°C | 48LQFP | 25MHz | C128 die |
| MC9S12C128MPB25 | TBD | -40°C, 125°C | 52LQFP | 25MHz | C128 die |
| MC9S12C128MFU25 | TBD | -40°C, 125°C | 80QFP | 25MHz | C128 die |
| MC9S12C96PCFA16 | 0L09S | -40°C, 85°C | 48LQFP | 16MHz | Preliminary C96 using C128 die |
| MC9S12C96PCPB16 | 0L09S | -40°C, 85°C | 52LQFP | 16MHz | Preliminary C96 using C128 die |
| MC9S12C96PCFU16 | 0L09S | -40°C, 85°C | 80QFP | 16MHz | Preliminary C96 using C128 die |
| MC9S12C96CFA16 | TBD | -40°C, 85°C | 48LQFP | 16MHz | Final C96 using C96 die |
| MC9S12C96CPB16 | TBD | -40°C, 85°C | 52LQFP | 16MHz | Final C96 using C96 die |
| MC9S12C96CFU16 | TBD | -40°C, 85°C | 80QFP | 16MHz | Final C96 using C96 die |
| MC9S12C96PVFA16 | 0L09S | -40°C, 105°C | 48LQFP | 16MHz | Preliminary C96 using C128 die |
| MC9S12C96PVPB16 | 0L09S | -40°C, 105°C | 52LQFP | 16MHz | Preliminary C96 using C128 die |
| MC9S12C96PVFU16 | 0L09S | -40°C, 105°C | 80QFP | 16MHz | Preliminary C96 using C128 die |
| MC9S12C96VFA16 | TBD | -40°C, 105°C | 48LQFP | 16MHz | Final C96 using C96 die |
| MC9S12C96VPB16 | TBD | -40°C, 105°C | 52LQFP | 16MHz | Final C96 using C96 die |
| MC9S12C96VFU16 | TBD | -40°C, 105°C | 80QFP | 16MHz | Final C96 using C96 die |
| MC9S12C96PMFA16 | 0L09S | -40°C, 125°C | 48LQFP | 16MHz | Preliminary C96 using C128 die |
| MC9S12C96PMPB16 | 0L09S | -40°C, 125°C | 52LQFP | 16MHz | Preliminary C96 using C128 die |
| MC9S12C96PMFU16 | 0L09S | -40°C, 125°C | 80QFP | 16MHz | Preliminary C96 using C128 die |
| MC9S12C96MFA16 | TBD | -40°C, 125°C | 48LQFP | 16MHz | Final C96 using C96 die |
| MC9S12C96MPB16 | TBD | -40°C, 125°C | 52LQFP | 16MHz | Final C96 using C96 die |
| MC9S12C96MFU16 | TBD | -40°C, 125°C | 80QFP | 16MHz | Final C96 using C96 die |
| MC9S12C96PCFA25 | 0L09S | -40°C, 85°C | 48LQFP | 25MHz | Preliminary C96 using C128 die |
| MC9S12C96PCPB25 | 0L09S | -40°C, 85°C | 52LQFP | 25MHz | Preliminary C96 using C128 die |
| MC9S12C96PCFU25 | 0L09S | -40°C, 85°C | 80QFP | 25MHz | Preliminary C96 using C128 die |
| MC9S12C96CFA25 | TBD | -40°C, 85°C | 48LQFP | 25MHz | Final C96 using C96 die |
| MC9S12C96CPB25 | TBD | -40°C, 85°C | 52LQFP | 25MHz | Final C96 using C96 die |
| MC9S12C96CFU25 | TBD | -40°C, 85°C | 80QFP | 25MHz | Final C96 using C96 die |
| MC9S12C96PVFA25 | 0L09S | -40°C, 105°C | 48LQFP | 25MHz | Preliminary C96 using C128 die |
| MC9S12C96PVPB25 | 0L09S | -40°C, 105°C | 52LQFP | 25MHz | Preliminary C96 using C128 die |
| MC9S12C96PVFU25 | 0L09S | -40°C, 105°C | 80QFP | 25MHz | Preliminary C96 using C128 die |

| Part Number | Mask set | Temp. | Package | Speed | Description |
|-----------------|----------|--------------|---------|-------|--------------------------------|
| MC9S12C96VFA25 | TBD | -40°C, 105°C | 48LQFP | 25MHz | Final C96 using C96 die |
| MC9S12C96VPB25 | TBD | -40°C, 105°C | 52LQFP | 25MHz | Final C96 using C96 die |
| MC9S12C96VFU25 | TBD | -40°C, 105°C | 80QFP | 25MHz | Final C96 using C96 die |
| MC9S12C96PMFA25 | 0L09S | -40°C, 125°C | 48LQFP | 25MHz | Preliminary C96 using C128 die |
| MC9S12C96PMPB25 | 0L09S | -40°C, 125°C | 52LQFP | 25MHz | Preliminary C96 using C128 die |
| MC9S12C96PMFU25 | 0L09S | -40°C, 125°C | 80QFP | 25MHz | Preliminary C96 using C128 die |
| MC9S12C96MFA25 | TBD | -40°C, 125°C | 48LQFP | 25MHz | Final C96 using C96 die |
| MC9S12C96MPB25 | TBD | -40°C, 125°C | 52LQFP | 25MHz | Final C96 using C96 die |
| MC9S12C96MFU25 | TBD | -40°C, 125°C | 80QFP | 25MHz | Final C96 using C96 die |
| MC9S12C64PCFA16 | 0L09S | -40°C, 85°C | 48LQFP | 16MHz | Preliminary C64 using C128 die |
| MC9S12C64PCPB16 | 0L09S | -40°C, 85°C | 52LQFP | 16MHz | Preliminary C64 using C128 die |
| MC9S12C64PCFU16 | 0L09S | -40°C, 85°C | 80QFP | 16MHz | Preliminary C64 using C128 die |
| MC9S12C64CFA16 | TBD | -40°C, 85°C | 48LQFP | 16MHz | Final C64 using C64 die |
| MC9S12C64CPB16 | TBD | -40°C, 85°C | 52LQFP | 16MHz | Final C64 using C64 die |
| MC9S12C64CFU16 | TBD | -40°C, 85°C | 80QFP | 16MHz | Final C64 using C64 die |
| MC9S12C64PVFA16 | 0L09S | -40°C, 105°C | 48LQFP | 16MHz | Preliminary C64 using C128 die |
| MC9S12C64PVPB16 | 0L09S | -40°C, 105°C | 52LQFP | 16MHz | Preliminary C64 using C128 die |
| MC9S12C64PVFU16 | 0L09S | -40°C, 105°C | 80QFP | 16MHz | Preliminary C64 using C128 die |
| MC9S12C64VFA16 | TBD | -40°C, 105°C | 48LQFP | 16MHz | Final C64 using C64 die |
| MC9S12C64VPB16 | TBD | -40°C, 105°C | 52LQFP | 16MHz | Final C64 using C64 die |
| MC9S12C64VFU16 | TBD | -40°C, 105°C | 80QFP | 16MHz | Final C64 using C64 die |
| MC9S12C64PMFA16 | 0L09S | -40°C, 125°C | 48LQFP | 16MHz | Preliminary C64 using C128 die |
| MC9S12C64PMPB16 | 0L09S | -40°C, 125°C | 52LQFP | 16MHz | Preliminary C64 using C128 die |
| MC9S12C64PMFU16 | 0L09S | -40°C, 125°C | 80QFP | 16MHz | Preliminary C64 using C128 die |
| MC9S12C64MFA16 | TBD | -40°C, 125°C | 48LQFP | 16MHz | Final C64 using C64 die |
| MC9S12C64MPB16 | TBD | -40°C, 125°C | 52LQFP | 16MHz | Final C64 using C64 die |
| MC9S12C64MFU16 | TBD | -40°C, 125°C | 80QFP | 16MHz | Final C64 using C64 die |
| MC9S12C64PCFA25 | 0L09S | -40°C, 85°C | 48LQFP | 25MHz | Preliminary C64 using C128 die |
| MC9S12C64PCPB25 | 0L09S | -40°C, 85°C | 52LQFP | 25MHz | Preliminary C64 using C128 die |
| MC9S12C64PCFU25 | 0L09S | -40°C, 85°C | 80QFP | 25MHz | Preliminary C64 using C128 die |
| MC9S12C64CFA25 | TBD | -40°C, 85°C | 48LQFP | 25MHz | Final C64 using C64 die |
| MC9S12C64CPB25 | TBD | -40°C, 85°C | 52LQFP | 25MHz | Final C64 using C64 die |
| MC9S12C64CFU25 | TBD | -40°C, 85°C | 80QFP | 25MHz | Final C64 using C64 die |
| MC9S12C64PVFA25 | 0L09S | -40°C, 105°C | 48LQFP | 25MHz | Preliminary C64 using C128 die |
| MC9S12C64PVPB25 | 0L09S | -40°C, 105°C | 52LQFP | 25MHz | Preliminary C64 using C128 die |
| MC9S12C64PVFU25 | 0L09S | -40°C, 105°C | 80QFP | 25MHz | Preliminary C64 using C128 die |
| MC9S12C64VFA25 | TBD | -40°C, 105°C | 48LQFP | 25MHz | Final C64 using C64 die |
| MC9S12C64VPB25 | TBD | -40°C, 105°C | 52LQFP | 25MHz | Final C64 using C64 die |
| MC9S12C64VFU25 | TBD | -40°C, 105°C | 80QFP | 25MHz | Final C64 using C64 die |
| MC9S12C64PMFA25 | 0L09S | -40°C, 125°C | 48LQFP | 25MHz | Preliminary C64 using C128 die |
| MC9S12C64PMPB25 | 0L09S | -40°C, 125°C | 52LQFP | 25MHz | Preliminary C64 using C128 die |
| MC9S12C64PMFU25 | 0L09S | -40°C, 125°C | 80QFP | 25MHz | Preliminary C64 using C128 die |
| MC9S12C64MFA25 | TBD | -40°C, 125°C | 48LQFP | 25MHz | Final C64 using C64 die |
| MC9S12C64MPB25 | TBD | -40°C, 125°C | 52LQFP | 25MHz | Final C64 using C64 die |

| Part Number | Mask set | Temp. | Package | Speed | Description |
|----------------|----------|--------------|---------|-------|-------------------------|
| MC9S12C64MFU25 | TBD | -40°C, 125°C | 80QFP | 25MHz | Final C64 using C64 die |
| MC9S12C32CFA16 | 1L45J | -40°C, 85°C | 48LQFP | 16MHz | C32 die |
| MC9S12C32CPB16 | 1L45J | -40°C, 85°C | 52LQFP | 16MHz | C32 die |
| MC9S12C32CFU16 | 1L45J | -40°C, 85°C | 80QFP | 16MHz | C32 die |
| MC9S12C32VFA16 | 1L45J | -40°C, 105°C | 48LQFP | 16MHz | C32 die |
| MC9S12C32VPB16 | 1L45J | -40°C, 105°C | 52LQFP | 16MHz | C32 die |
| MC9S12C32VFU16 | 1L45J | -40°C, 105°C | 80QFP | 16MHz | C32 die |
| MC9S12C32MFA16 | 1L45J | -40°C, 125°C | 48LQFP | 16MHz | C32 die |
| MC9S12C32MPB16 | 1L45J | -40°C, 125°C | 52LQFP | 16MHz | C32 die |
| MC9S12C32MFU16 | 1L45J | -40°C, 125°C | 80QFP | 16MHz | C32 die |
| MC9S12C32CFA25 | 1L45J | -40°C, 85°C | 48LQFP | 25MHz | C32 die |
| MC9S12C32CPB25 | 1L45J | -40°C, 85°C | 52LQFP | 25MHz | C32 die |
| MC9S12C32CFU25 | 1L45J | -40°C, 85°C | 80QFP | 25MHz | C32 die |
| MC9S12C32VFA25 | 1L45J | -40°C, 105°C | 48LQFP | 25MHz | C32 die |
| MC9S12C32VPB25 | 1L45J | -40°C, 105°C | 52LQFP | 25MHz | C32 die |
| MC9S12C32VFU25 | 1L45J | -40°C, 105°C | 80QFP | 25MHz | C32 die |
| MC9S12C32MFA25 | 1L45J | -40°C, 125°C | 48LQFP | 25MHz | C32 die |
| MC9S12C32MPB25 | 1L45J | -40°C, 125°C | 52LQFP | 25MHz | C32 die |
| MC9S12C32MFU25 | 1L45J | -40°C, 125°C | 80QFP | 25MHz | C32 die |

Table 0-4 MC9S12GC-Family Part Number Coding

| Part Number | Mask set | Temp. | Package | Speed | Description |
|-------------------|----------|--------------|---------|-------|----------------------------------|
| MC9S12GC128PCFA25 | 0L09S | -40°C, 85°C | 48LQFP | 25MHz | Preliminary GC128 using C128 die |
| MC9S12GC128PCPB25 | 0L09S | -40°C, 85°C | 52LQFP | 25MHz | Preliminary GC128 using C128 die |
| MC9S12GC128PCFU25 | 0L09S | -40°C, 85°C | 80QFP | 25MHz | Preliminary GC128 using C128 die |
| MC9S12GC128CFA25 | TBD | -40°C, 85°C | 48LQFP | 25MHz | Final GC128 using GC128 die |
| MC9S12GC128CPB25 | TBD | -40°C, 85°C | 52LQFP | 25MHz | Final GC128 using GC128 die |
| MC9S12GC128CFU25 | TBD | -40°C, 85°C | 80QFP | 25MHz | Final GC128 using GC128 die |
| MC9S12GC128PVFA25 | 0L09S | -40°C, 105°C | 48LQFP | 25MHz | Preliminary GC128 using C128 die |
| MC9S12GC128PVPB25 | 0L09S | -40°C, 105°C | 52LQFP | 25MHz | Preliminary GC128 using C128 die |
| MC9S12GC128PVFU25 | 0L09S | -40°C, 105°C | 80QFP | 25MHz | Preliminary GC128 using C128 die |
| MC9S12GC128VFA25 | TBD | -40°C, 105°C | 48LQFP | 25MHz | Final GC128 using GC128 die |
| MC9S12GC128VPB25 | TBD | -40°C, 105°C | 52LQFP | 25MHz | Final GC128 using GC128 die |
| MC9S12GC128VFU25 | TBD | -40°C, 105°C | 80QFP | 25MHz | Final GC128 using GC128 die |
| MC9S12GC128PMFA25 | 0L09S | -40°C, 125°C | 48LQFP | 25MHz | Preliminary GC128 using C128 die |
| MC9S12GC128PMPB25 | 0L09S | -40°C, 125°C | 52LQFP | 25MHz | Preliminary GC128 using C128 die |
| MC9S12GC128PMFU25 | 0L09S | -40°C, 125°C | 80QFP | 25MHz | Preliminary GC128 using C128 die |
| MC9S12GC128MFA25 | TBD | -40°C, 125°C | 48LQFP | 25MHz | Final GC128 using GC128 die |
| MC9S12GC128MPB25 | TBD | -40°C, 125°C | 52LQFP | 25MHz | Final GC128 using GC128 die |
| MC9S12GC128MFU25 | TBD | -40°C, 125°C | 80QFP | 25MHz | Final GC128 using GC128 die |
| MC9S12GC64PCFA25 | 0L09S | -40°C, 85°C | 48LQFP | 25MHz | Preliminary GC64 using C128 die |
| MC9S12GC64PCPB25 | 0L09S | -40°C, 85°C | 52LQFP | 25MHz | Preliminary GC64 using C128 die |
| MC9S12GC64PCFU25 | 0L09S | -40°C, 85°C | 80QFP | 25MHz | Preliminary GC64 using C128 die |

| Part Number | Mask set | Temp. | Package | Speed | Description |
|------------------|----------|--------------|---------|-------|---------------------------------|
| MC9S12GC64CFA25 | TBD | -40°C, 85°C | 48LQFP | 25MHz | Final GC64 using GC64 die |
| MC9S12GC64CPB25 | TBD | -40°C, 85°C | 52LQFP | 25MHz | Final GC64 using GC64 die |
| MC9S12GC64CFU25 | TBD | -40°C, 85°C | 80QFP | 25MHz | Final GC64 using GC64 die |
| MC9S12GC64PVFA25 | 0L09S | -40°C, 105°C | 48LQFP | 25MHz | Preliminary GC64 using C128 die |
| MC9S12GC64PVPB25 | 0L09S | -40°C, 105°C | 52LQFP | 25MHz | Preliminary GC64 using C128 die |
| MC9S12GC64PVFU25 | 0L09S | -40°C, 105°C | 80QFP | 25MHz | Preliminary GC64 using C128 die |
| MC9S12GC64VFA25 | TBD | -40°C, 105°C | 48LQFP | 25MHz | Final GC64 using GC64 die |
| MC9S12GC64VPB25 | TBD | -40°C, 105°C | 52LQFP | 25MHz | Final GC64 using GC64 die |
| MC9S12GC64VFU25 | TBD | -40°C, 105°C | 80QFP | 25MHz | Final GC64 using GC64 die |
| MC9S12GC64PMFA25 | 0L09S | -40°C, 125°C | 48LQFP | 25MHz | Preliminary GC64 using C128 die |
| MC9S12GC64PMPB25 | 0L09S | -40°C, 125°C | 52LQFP | 25MHz | Preliminary GC64 using C128 die |
| MC9S12GC64PMFU25 | 0L09S | -40°C, 125°C | 80QFP | 25MHz | Preliminary GC64 using C128 die |
| MC9S12GC64MFA25 | TBD | -40°C, 125°C | 48LQFP | 25MHz | Final GC64 using GC64 die |
| MC9S12GC64MPB25 | TBD | -40°C, 125°C | 52LQFP | 25MHz | Final GC64 using GC64 die |
| MC9S12GC64MFU25 | TBD | -40°C, 125°C | 80QFP | 25MHz | Final GC64 using GC64 die |
| MC9S12GC32PCFA25 | 1L45J | -40°C, 85°C | 48LQFP | 25MHz | Preliminary GC32 using C32 die |
| MC9S12GC32PCPB25 | 1L45J | -40°C, 85°C | 52LQFP | 25MHz | Preliminary GC32 using C32 die |
| MC9S12GC32PCFU25 | 1L45J | -40°C, 85°C | 80QFP | 25MHz | Preliminary GC32 using C32 die |
| MC9S12GC32CFA25 | TBD | -40°C, 85°C | 48LQFP | 25MHz | Final GC32 using GC32 die |
| MC9S12GC32CPB25 | TBD | -40°C, 85°C | 52LQFP | 25MHz | Final GC32 using GC32 die |
| MC9S12GC32CFU25 | TBD | -40°C, 85°C | 80QFP | 25MHz | Final GC32 using GC32 die |
| MC9S12GC32PVFA25 | 1L45J | -40°C, 105°C | 48LQFP | 25MHz | Preliminary GC32 using C32 die |
| MC9S12GC32PVPB25 | 1L45J | -40°C, 105°C | 52LQFP | 25MHz | Preliminary GC32 using C32 die |
| MC9S12GC32PVFU25 | 1L45J | -40°C, 105°C | 80QFP | 25MHz | Preliminary GC32 using C32 die |
| MC9S12GC32VFA25 | TBD | -40°C, 105°C | 48LQFP | 25MHz | Final GC32 using GC32 die |
| MC9S12GC32VPB25 | TBD | -40°C, 105°C | 52LQFP | 25MHz | Final GC32 using GC32 die |
| MC9S12GC32VFU25 | TBD | -40°C, 105°C | 80QFP | 25MHz | Final GC32 using GC32 die |
| MC9S12GC32PMFA25 | 1L45J | -40°C, 125°C | 48LQFP | 25MHz | Preliminary GC32 using C32 die |
| MC9S12GC32PMPB25 | 1L45J | -40°C, 125°C | 52LQFP | 25MHz | Preliminary GC32 using C32 die |
| MC9S12GC32PMFU25 | 1L45J | -40°C, 125°C | 80QFP | 25MHz | Preliminary GC32 using C32 die |
| MC9S12GC32MFA25 | TBD | -40°C, 125°C | 48LQFP | 25MHz | Final GC32 using GC32 die |
| MC9S12GC32MPB25 | TBD | -40°C, 125°C | 52LQFP | 25MHz | Final GC32 using GC32 die |
| MC9S12GC32MFU25 | TBD | -40°C, 125°C | 80QFP | 25MHz | Final GC32 using GC32 die |
| MC9S12GC16PCFA25 | 1L45J | -40°C, 85°C | 48LQFP | 25MHz | Preliminary GC16 using C32 die |
| MC9S12GC16PCPB25 | 1L45J | -40°C, 85°C | 52LQFP | 25MHz | Preliminary GC16 using C32 die |
| MC9S12GC16PCFU25 | 1L45J | -40°C, 85°C | 80QFP | 25MHz | Preliminary GC16 using C32 die |
| MC9S12GC16CFA25 | TBD | -40°C, 85°C | 48LQFP | 25MHz | Final GC16 using GC16 die |
| MC9S12GC16CPB25 | TBD | -40°C, 85°C | 52LQFP | 25MHz | Final GC16 using GC16 die |
| MC9S12GC16CFU25 | TBD | -40°C, 85°C | 80QFP | 25MHz | Final GC16 using GC16 die |
| MC9S12GC16PVFA25 | 1L45J | -40°C, 105°C | 48LQFP | 25MHz | Preliminary GC16 using C32 die |
| MC9S12GC16PVPB25 | 1L45J | -40°C, 105°C | 52LQFP | 25MHz | Preliminary GC16 using C32 die |
| MC9S12GC16PVFU25 | 1L45J | -40°C, 105°C | 80QFP | 25MHz | Preliminary GC16 using C32 die |
| MC9S12GC16VFA25 | TBD | -40°C, 105°C | 48LQFP | 25MHz | Final GC16 using GC16 die |
| MC9S12GC16VPB25 | TBD | -40°C, 105°C | 52LQFP | 25MHz | Final GC16 using GC16 die |

| Part Number | Mask set | Temp. | Package | Speed | Description |
|------------------|----------|--------------|---------|-------|--------------------------------|
| MC9S12GC16VFU25 | TBD | -40°C, 105°C | 80QFP | 25MHz | Final GC16 using GC16 die |
| MC9S12GC16PMFA25 | 1L45J | -40°C, 125°C | 48LQFP | 25MHz | Preliminary GC16 using C32 die |
| MC9S12GC16PMPB25 | 1L45J | -40°C, 125°C | 52LQFP | 25MHz | Preliminary GC16 using C32 die |
| MC9S12GC16PMFU25 | 1L45J | -40°C, 125°C | 80QFP | 25MHz | Preliminary GC16 using C32 die |
| MC9S12GC16MFA25 | TBD | -40°C, 125°C | 48LQFP | 25MHz | Final GC16 using GC16 die |
| MC9S12GC16MPB25 | TBD | -40°C, 125°C | 52LQFP | 25MHz | Final GC16 using GC16 die |
| MC9S12GC16MFU25 | TBD | -40°C, 125°C | 80QFP | 25MHz | Final GC16 using GC16 die |

Table 0-5 Document References

| User Guide ¹ | Version | Document Order Number |
|---|---------|-----------------------|
| CPU12 Reference Manual | V02 | S12CPUV2/D |
| HCS12 Debug (DBG) Block Guide | V01 | S12DBGV1/D |
| HCS12 Background Debug (BDM) Block Guide | V04 | S12BDMV4/D |
| HCS12 Module Mapping Control (MMC) Block Guide | V04 | S12MMCV4/D |
| HCS12 Multiplexed External Bus Interface (MEBI) Block Guide | V03 | S12MEBIV3/D |
| HCS12 Interrupt (INT) Block Guide | V01 | S12INTV1/D |
| Analog To Digital Converter: 10 Bit 8 Channel (ATD_10B8C) Block Guide | V02 | S12ATD10B8CV2/D |
| Clock and Reset Generator (CRG) Block Guide | V04 | S12CRGV4/D |
| Serial Communications Interface (SCI) Block Guide | V02 | S12SCIV2/D |
| Serial Peripheral Interface (SPI) Block Guide | V03 | S12SPIV3/D |
| Motorola Scalable CAN (MSCAN) Block Guide ² | V02 | S12MSCANV2/D |
| Pulse Width Modulator: 8 bit, 6 channel (PWM_8B6C) Block Guide | V01 | S12PWM8B6V1/D |
| Timer: 16 bit, 8 channel (TIM_16B8C) Block Guide | V01 | S12TIM16B8CV1/D |
| Voltage Regulator (VREG) Block Guide | V02 | S12VREG3V3V2/D |
| Oscillator (OSC) Block Guide | V02 | S12OSCV2/D |
| Port Integration Module (PIM_9C32) Block Guide | V01 | S12C32PIMV1/D |
| 32Kbyte Flash EEPROM (FTS32K) Block Guide | V01 | S12FTS32KV1/D |
| 64Kbyte Flash EEPROM (FTS64K) Block Guide | V01 | S12FTS64KV1/D |
| 128Kbyte Flash EEPROM (FTS128K1) Block Guide | V01 | S12FTS128K1V1/D |

NOTES:

1. For the GC16 refer to the 16K flash, for the C32 and GC32 refer to the 32K flash, for the C64 and GC64 the 64K flash, for the C96 the 96K flash and C128 the 128K flash document.
2. Not available on the GC-Family members

Terminology

| Acronyms and Abbreviations | |
|---|--|
| | |
| New or invented terms, symbols, and notations | |
| | |

Section 1 Introduction

1.1 Overview

The MC9S12C-Family and the MC9S12GC-Family is a 48/52/80 pin Flash-based Industrial/Automotive network control MCU family. Members of the MC9S12C-Family and the MC9S12GC-Family deliver the power and flexibility of our 16 Bit core (CPU12) family to a whole new range of cost and space sensitive, general purpose Industrial and Automotive network applications. All MC9S12C-Family and MC9S12GC-Family members are comprised of standard on-chip peripherals including a 16-bit central processing unit (CPU12), up to 128K bytes of Flash EEPROM, up to 4K bytes of RAM, an asynchronous serial communications interface (SCI), a serial peripheral interface (SPI), an 8-channel 16-bit timer module (TIM), a 6-channel 8-bit Pulse Width Modulator (PWM), an 8-channel, 10-bit analog-to-digital converter (ADC). The MC9S12C-Family members also feature a CAN 2.0 A, B software compatible module (MSCAN12). The MC9S12C-Family as well as the MC9S12GC-Family has full 16-bit data paths throughout. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. In addition to the I/O ports available in each module, up to 10 dedicated I/O port bits are available with Wake-Up capability from STOP or WAIT mode. The MC9S12C-Family and the MC9S12GC-Family devices are available in 48, 52 and 80 pin QFP packages, with the 80 Pin version pin compatible to the HCS12 A, B and D- Family derivatives.

1.2 Features

- 16-bit HCS12 CORE
 - HCS12 CPU
 - i. Upward compatible with M68HC11 instruction set
 - ii. Interrupt stacking and programmer's model identical to M68HC11
 - iii. Instruction queue
 - iv. Enhanced indexed addressing
 - MMC (memory map and interface)
 - INT (interrupt control)
 - BDM (background debug mode)
 - DBG12 (enhanced debug12 module, including breakpoints and change-of-flow trace buffer)
 - MEBI: Multiplexed Expansion Bus Interface (available only in 80 pin package version)
- Wake-up interrupt inputs
 - Up to 12-port bits available for wake up interrupt function with digital filtering
- Memory options
 - 16K or 32KByte Flash EEPROM (erasable in 512-byte sectors)
 - 64K, 96K or 128KByte Flash EEPROM (erasable in 1024-byte sectors)

- 1K, 2K or 4K Byte RAM
- Analog-to-Digital Converters
 - One 8-channel module with 10-bit resolution.
 - External conversion trigger capability
- Available on MC9S12C-Family:
One 1M bit per second, CAN 2.0 A, B software compatible module
 - Five receive and three transmit buffers
 - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
 - Four separate interrupt channels for Rx, Tx, error and wake-up
 - Low-pass filter wake-up function
 - Loop-back for self test operation
- Timer Module (TIM)
 - 8-Channel Timer
 - Each Channel Configurable as either Input Capture or Output Compare
 - Simple PWM Mode
 - Modulo Reset of Timer Counter
 - 16-Bit Pulse Accumulator
 - External Event Counting
 - Gated Time Accumulation
- 6 PWM channels
 - Programmable period and duty cycle
 - 8-bit 6-channel or 16-bit 3-channel
 - Separate control for each pulse width and duty cycle
 - Center-aligned or left-aligned outputs
 - Programmable clock select logic with a wide range of frequencies
 - Fast emergency shutdown input
- Serial interfaces
 - One asynchronous serial communications interface (SCI)
 - One synchronous serial peripheral interface (SPI)
- CRG (Clock Reset Generator Module)
 - Windowed COP watchdog,
 - Real time interrupt,
 - Clock monitor,

- Pierce or low current Colpitts oscillator
- Phase-locked loop clock frequency multiplier
- Limp home mode in absence of external clock
- Low power 0.5 to 16 MHz crystal oscillator reference clock
- Operating frequency
 - 32MHz equivalent to 16MHz Bus Speed for single chip
 - 32MHz equivalent to 16MHz Bus Speed in expanded bus modes
 - Option of 9S12C-Family: 50MHz equivalent to 25MHz Bus Speed
 - All 9S12GC-Family Members allow a 50MHz operating frequency.
- Internal 2.5V Regulator
 - Supports an input voltage range from 2.97V to 5.5V
 - Low power mode capability
 - Includes low voltage reset (LVR) circuitry
 - Includes low voltage interrupt (LVI) circuitry
- 48-Pin LQFP, 52-Pin LQFP or 80-Pin QFP package
 - Up to 58 I/O lines with 5V input and drive capability (80 pin package)
 - Up to 2 dedicated 5V input only lines (IRQ, XIRQ)
 - 5V 8 A/D converter inputs and 5V I/O
- Development support
 - Single-wire background debug™ mode (BDM)
 - On-chip hardware breakpoints
 - Enhanced DBG12 debug features

1.3 Modes of Operation

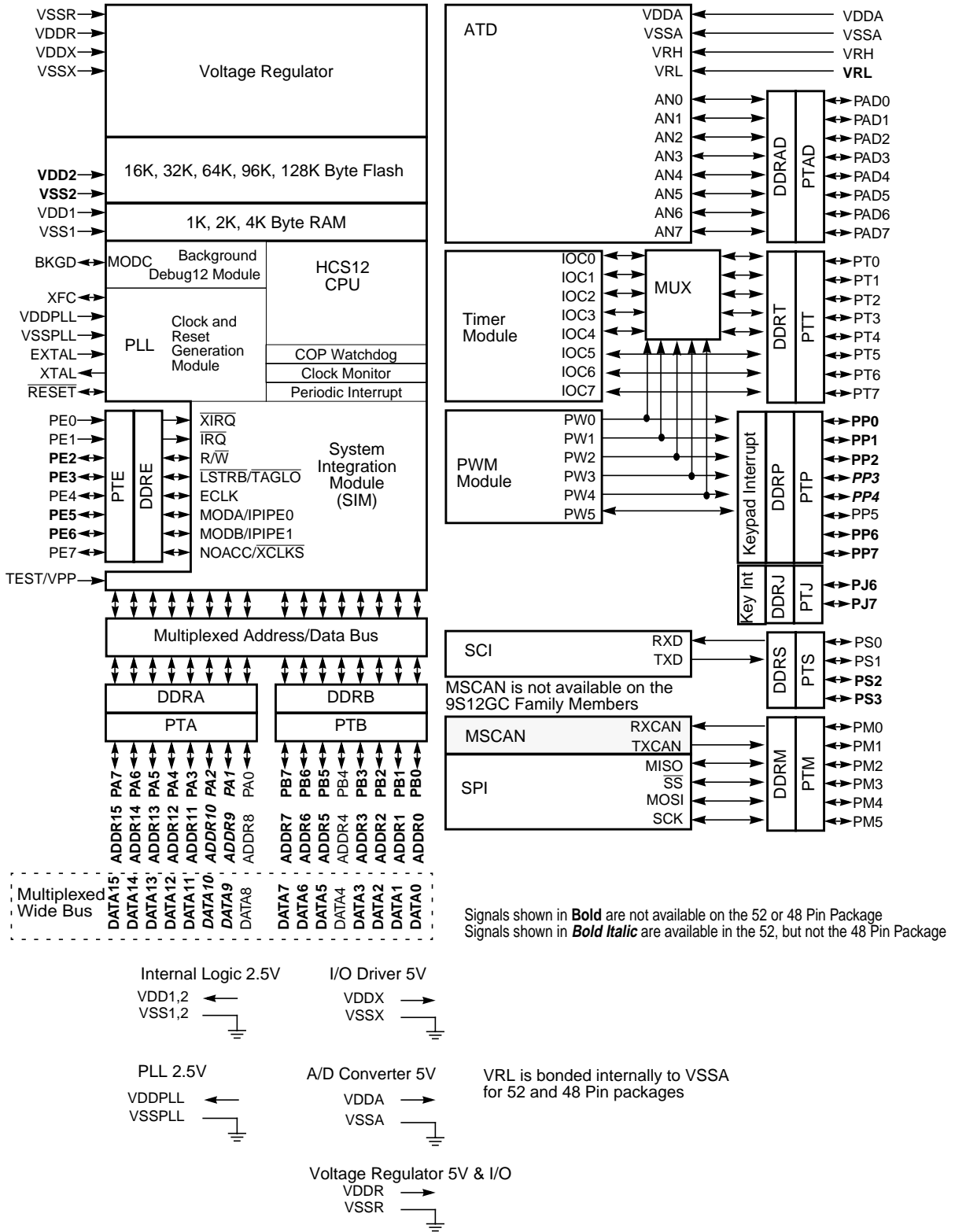
User modes (**Expanded modes are only available in the 80 pin package version**).

- Normal and Emulation Operating Modes
 - Normal Single-Chip Mode
 - Normal Expanded Wide Mode
 - Normal Expanded Narrow Mode
 - Emulation Expanded Wide Mode
 - Emulation Expanded Narrow Mode
- Special Operating Modes

- Special Single-Chip Mode with active Background Debug Mode
- Special Test Mode (**Motorola use only**)
- Special Peripheral Mode (**Motorola use only**)
- Low power modes
 - Stop Mode
 - Pseudo Stop Mode
 - Wait Mode

1.4 Block Diagram

Figure 1-1 MC9S12C-Family Block Diagram



Signals shown in **Bold** are not available on the 52 or 48 Pin Package
 Signals shown in **Bold Italic** are available in the 52, but not the 48 Pin Package

1.5 Device Memory Map

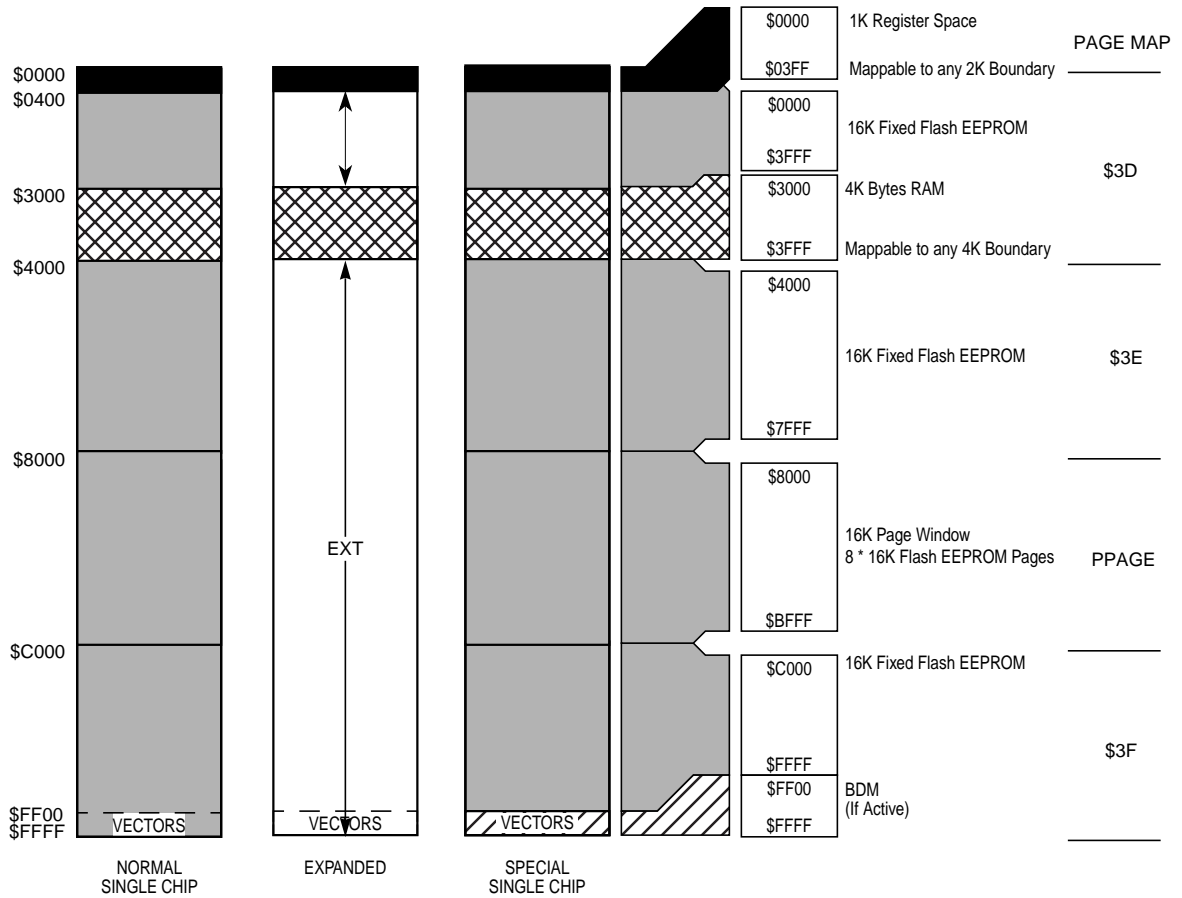
Table 1-1 shows the device register map of the MC9S12C-Family after reset. The following figures (**Figure 1-2**, **Figure 1-2**, **Figure 1-3** and **Figure 1-4**) illustrate the full device memory map with flash and RAM.

Table 1-1 Device Register Map Overview

| Address | Module | Size |
|---------------|---|------|
| \$000 - \$017 | CORE (Ports A, B, E, Modes, Inits, Test) | 24 |
| \$018 | Reserved | 1 |
| \$019 | Voltage Regulator (VREG) | 1 |
| \$01A - \$01B | Device ID register | 2 |
| \$01C - \$01F | CORE (MEMSIZ, IRQ, HPRIO) | 4 |
| \$020 - \$02F | CORE (DBG) | 16 |
| \$030 - \$033 | CORE (PPAGE ¹) | 4 |
| \$034 - \$03F | Clock and Reset Generator (CRG) | 12 |
| \$040 - \$06F | Standard Timer Module 16-bit 8-channels (TIM) | 48 |
| \$070 - \$07F | Reserved | 16 |
| \$080 - \$09F | Analog to Digital Convert (ATD) | 32 |
| \$0A0 - \$0C7 | Reserved | 40 |
| \$0C8 - \$0CF | Serial Communications Interface (SCI) | 8 |
| \$0D0 - \$0D7 | Reserved | 8 |
| \$0D8 - \$0DF | Serial Peripheral Interface (SPI) | 8 |
| \$0E0 - \$0FF | Pulse Width Modulator 8-bit 6 channels (PWM) | 32 |
| \$100 - \$10F | Flash Control Register | 16 |
| \$110 - \$13F | Reserved | 48 |
| \$140 - \$17F | Motorola Scalable CAN (MSCAN) ² | 64 |
| \$180 - \$23F | Reserved | 192 |
| \$240 - \$27F | Port Integration Module (PIM) | 64 |
| \$280 - \$3FF | Reserved | 384 |

NOTES:

1. External memory paging is not supported on this device (**6.1.1 PPAGE**).
2. Not available on MC9S12GC-Family Devices

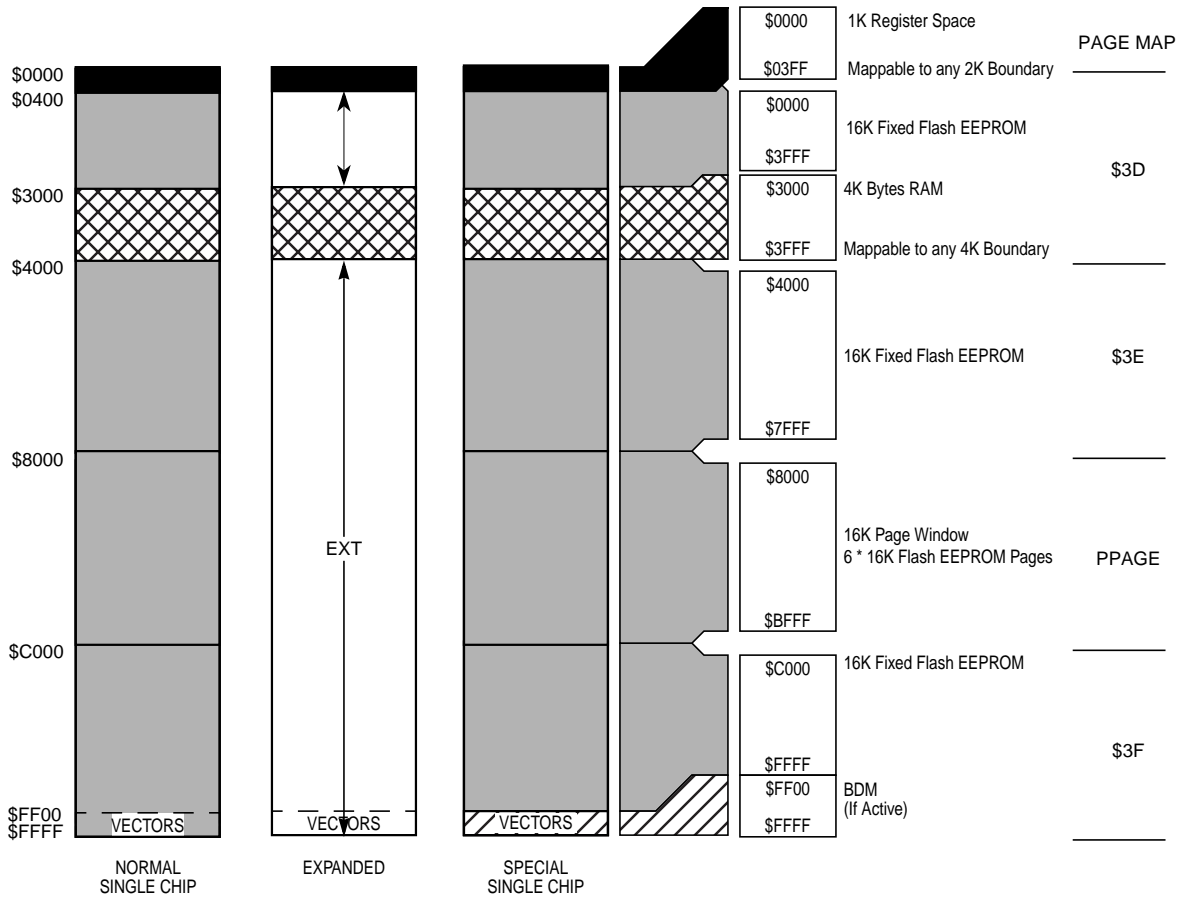


The figure shows a useful map, which is not the map out of reset. After reset the map is:

- \$0000 - \$03FF: Register Space
- \$0000 - \$0FFF: 4K RAM (only 3K visible \$0400 - \$0FFF)

Flash Erase Sector Size is 1024 Bytes

Figure 1-2 MC9S12C128 and MC9S12GC128 User configurable Memory Map

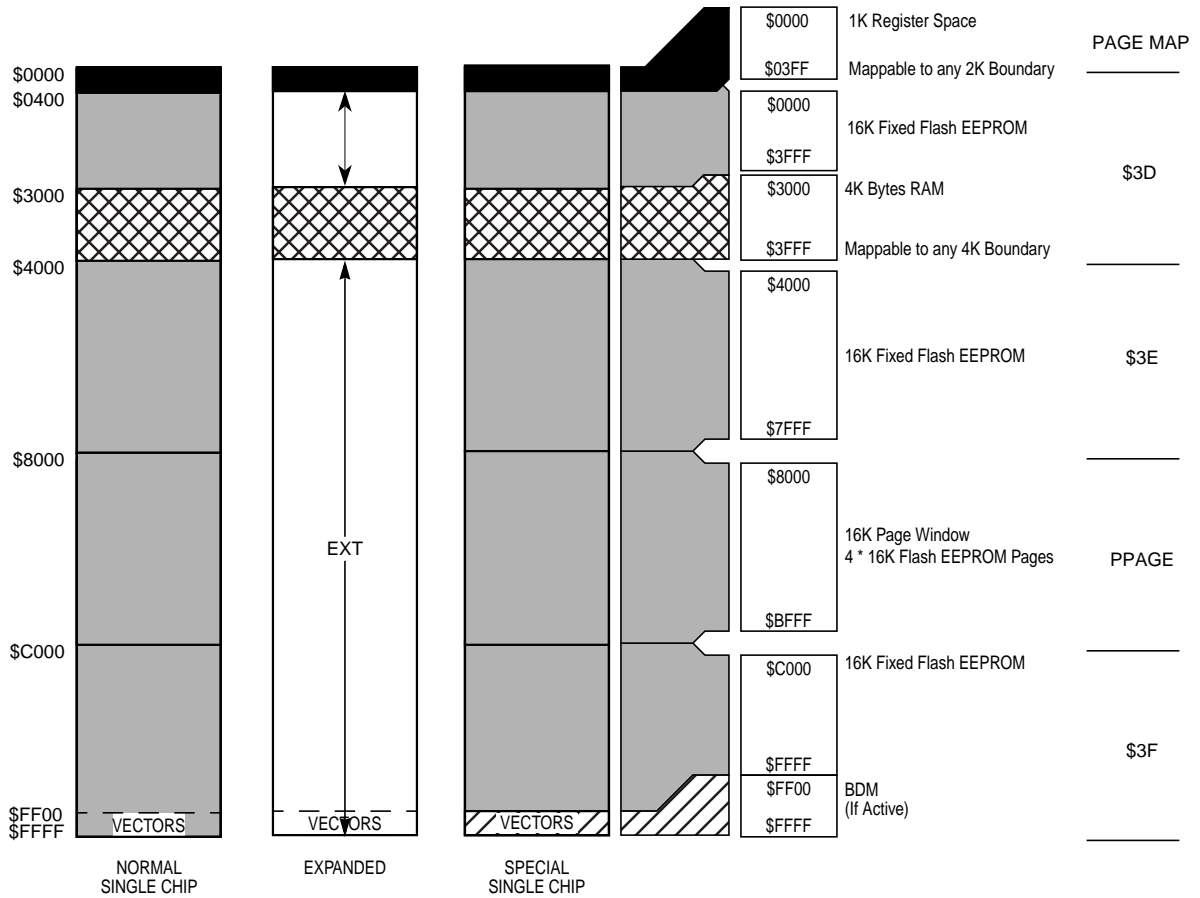


The figure shows a useful map, which is not the map out of reset. After reset the map is:

- \$0000 - \$03FF: Register Space
- \$0000 - \$0FFF: 4K RAM (only 3K visible \$0400 - \$0FFF)

Flash Erase Sector Size is 1024 Bytes

Figure 1-3 MC9S12C96 User Configurable Memory Map

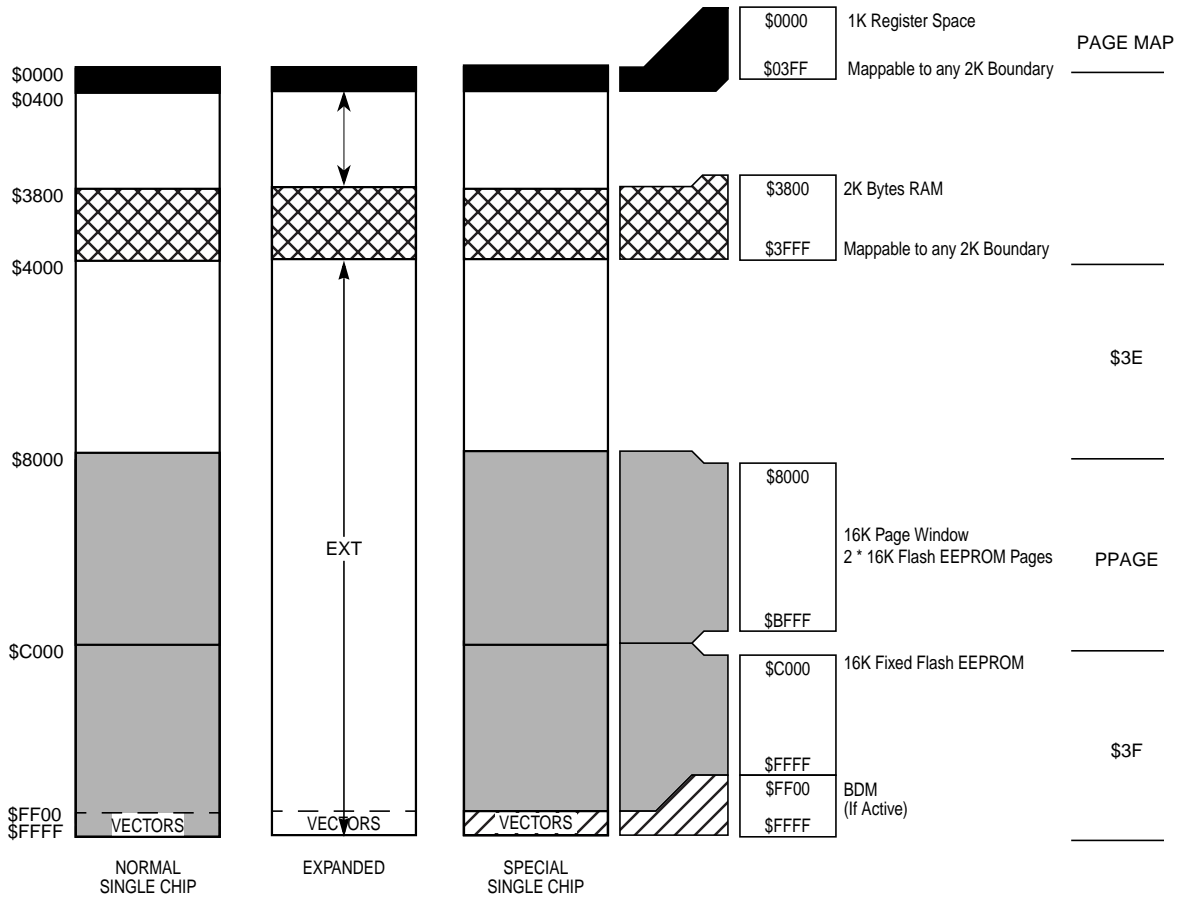


The figure shows a useful map, which is not the map out of reset. After reset the map is:

- \$0000 - \$03FF: Register Space
- \$0000 - \$0FFF: 4K RAM (only 3K visible \$0400 - \$0FFF)

Flash Erase Sector Size is 1024 Bytes

Figure 1-4 MC9S12C64 and MC9S12GC64 User Configurable Memory Map

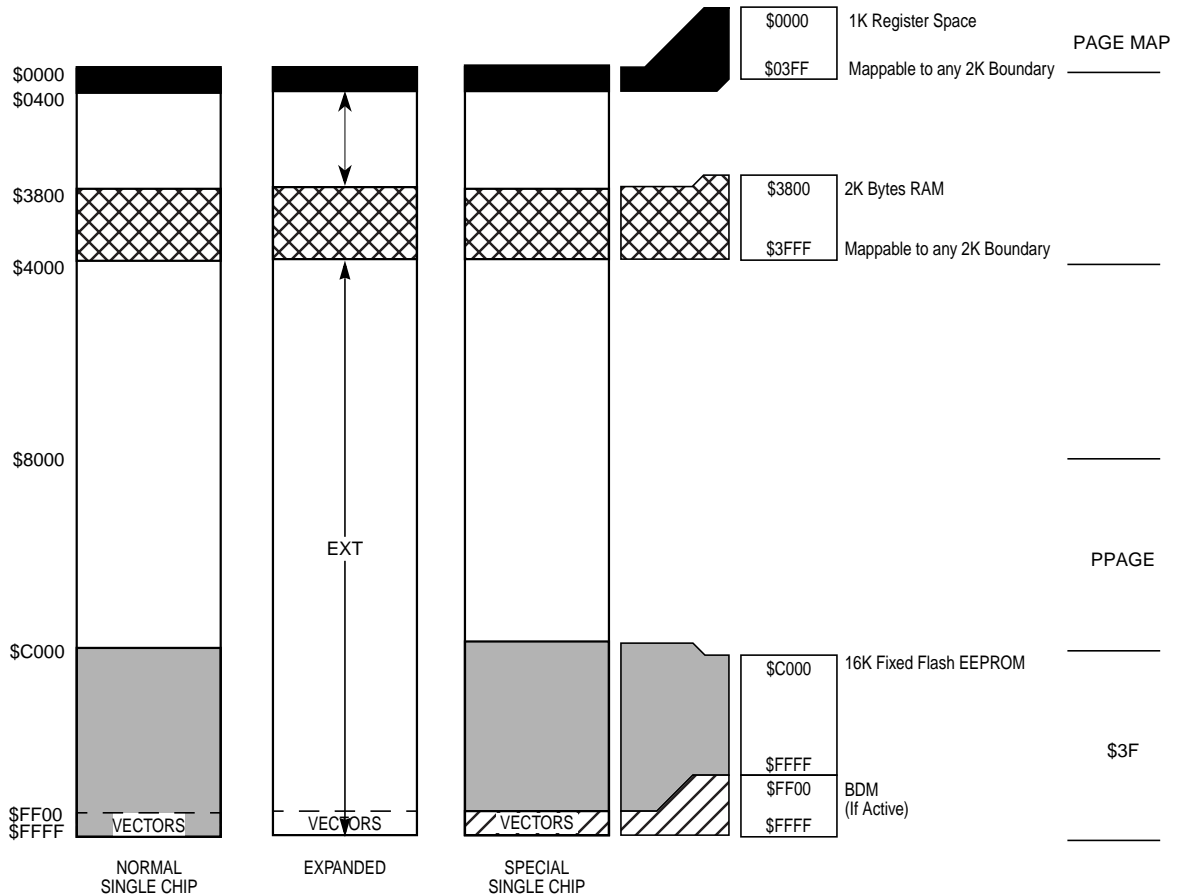


The figure shows a useful map, which is not the map out of reset. After reset the map is:

\$0000 - \$03FF: Register Space
 \$0800 - \$0FFF: 2K RAM

Flash Erase Sector Size is 512 Bytes

Figure 1-5 MC9S12C32 and MC9S12GC32 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

\$0000 - \$03FF: Register Space
 \$0800 - \$0FFF: 2K RAM

Flash Erase Sector Size is 512 Bytes

Figure 1-6 MC9S12GC16 User Configurable Memory Map

1.6 Detailed Register Map

The detailed register map of the MC9S12C Family is listed in address order below.

\$0000 - \$000F

MEBI map 1 of 3 (HCS12 Multiplexed External Bus Interface)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|--------|-------|-------|-------|-------|-------|-------|-------|
| \$0000 | PORTA | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0001 | PORTB | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0002 | DDRA | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0003 | DDRB | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0004 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0005 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0006 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0007 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0008 | PORTE | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | Bit 1 | Bit 0 |
| | | Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | | |
| \$0009 | DDRE | Read: | Bit 7 | 6 | 5 | 4 | 3 | Bit 2 | 0 | 0 |
| | | Write: | Bit 7 | 6 | 5 | 4 | 3 | Bit 2 | | |
| \$000A | PEAR | Read: | NOACCE | 0 | PIPOE | NECLK | LSTRE | RDWE | 0 | 0 |
| | | Write: | | | | | | | | |
| \$000B | MODE | Read: | MODC | MODB | MODA | 0 | IVIS | 0 | EMK | EME |
| | | Write: | | | | | | | | |
| \$000C | PUCR | Read: | PUPKE | 0 | 0 | PUPEE | 0 | 0 | PUPBE | PUPAE |
| | | Write: | | | | | | | | |
| \$000D | RDRIV | Read: | RDPK | 0 | 0 | RDPE | 0 | 0 | RDPB | RDPA |
| | | Write: | | | | | | | | |
| \$000E | EBICTL | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ESTR |
| | | Write: | | | | | | | | |
| \$000F | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$0010 - \$0014

MMC map 1 of 4 (HCS12 Module Mapping Control)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|--------|--------|-------|-------|-------|-------|-------|-------|-------|--------|
| \$0010 | INITRM | Read: | RAM15 | RAM14 | RAM13 | RAM12 | RAM11 | 0 | 0 | RAMHAL |
| | | Write: | | | | | | | | |
| \$0011 | INITRG | Read: | 0 | REG14 | REG13 | REG12 | REG11 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

\$0010 - \$0014

MMC map 1 of 4 (HCS12 Module Mapping Control)

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|------------|-------|-------|-------|--------|--------|-------|-------|
| \$0012 | INITEE | Read: EE15 | EE14 | EE13 | EE12 | EE11 | 0 | 0 | EEON |
| | | Write: | | | | | | | |
| \$0013 | MISC | Read: 0 | 0 | 0 | 0 | EXSTR1 | EXSTR0 | ROMHM | ROMON |
| | | Write: | | | | | | | |
| \$0014 | Reserved | Read: 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | |

\$0015 - \$0016

INT map 1 of 2 (HCS12 Interrupt)

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|------------|-------|-------|-------|-------|-------|-------|-------|
| \$0015 | ITCR | Read: 0 | 0 | 0 | WRINT | ADR3 | ADR2 | ADR1 | ADR0 |
| | | Write: | | | | | | | |
| \$0016 | ITEST | Read: INTE | INTC | INTA | INT8 | INT6 | INT4 | INT2 | INT0 |
| | | Write: | | | | | | | |

\$0017 - \$0017

MMC map 2 of 4 (HCS12 Module Mapping Control)

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|---------|-------|-------|-------|-------|-------|-------|-------|
| \$0017 | Reserved | Read: 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | |

\$0018 - \$0018

Miscellaneous Peripherals (Device User Guide)

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|---------|-------|-------|-------|-------|-------|-------|-------|
| \$0018 | Reserved | Read: 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | |

\$0019 - \$0019

VREG3V3 (Voltage Regulator)

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|---------|-------|-------|-------|-------|-------|-------|-------|
| \$0019 | VREGCTRL | Read: 0 | 0 | 0 | 0 | 0 | LVDS | LVIE | LVIF |
| | | Write: | | | | | | | |

\$001A - \$001B

Miscellaneous Peripherals (Device User Guide)

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------|------------|-------|-------|-------|-------|-------|-------|-------|
| \$001A | PARTIDH | Read: ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | ID9 | ID8 |
| | | Write: | | | | | | | |
| \$001B | PARTIDL | Read: ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| | | Write: | | | | | | | |

\$001C - \$001D

MMC map 3 of 4 (HCS12 Module Mapping Control, Device User Guide)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------|--------|---------|---------|---------|---------|-------|---------|---------|---------|
| \$001C | MEMSIZ0 | Read: | reg_sw0 | 0 | eep_sw1 | eep_sw0 | 0 | ram_sw2 | ram_sw1 | ram_sw0 |
| | | Write: | | | | | | | | |
| \$001D | MEMSIZ1 | Read: | rom_sw1 | rom_sw0 | 0 | 0 | 0 | 0 | pag_sw1 | pag_sw0 |
| | | Write: | | | | | | | | |

\$001E - \$001E

MEBI map 2 of 3 (HCS12 Multiplexed External Bus Interface)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$001E | INTCR | Read: | IRQE | IRQEN | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$001F - \$001F

INT map 2 of 2 (HCS12 Interrupt)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$001F | HPRIO | Read: | PSEL7 | PSEL6 | PSEL5 | PSEL4 | PSEL3 | PSEL2 | PSEL1 | 0 |
| | | Write: | | | | | | | | |

\$0020 - \$002F

DBG (including BKP) map 1 of 1 (HCS12 Debug)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------------|-------|--------|--------|--------|--------|--------|--------|--------|-------|
| \$0020 | DBGC1 - | read | DBGEN | ARM | TRGSEL | BEGIN | DBGBRK | 0 | CAPMOD | |
| | | write | | | | | | | | |
| \$0021 | DBGSC - | read | AF | BF | CF | 0 | TRG | | | |
| | | write | | | | | | | | |
| \$0022 | DBGTBH - | read | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 |
| | | write | | | | | | | | |
| \$0023 | DBGTBL - | read | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | write | | | | | | | | |
| \$0024 | DBGCNT - | read | TBF | 0 | CNT | | | | | |
| | | write | | | | | | | | |
| \$0025 | DBGCCX - | read | PAGSEL | | | EXTCMP | | | | |
| | | write | | | | | | | | |
| \$0026 | DBGCCH | read | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | write | | | | | | | | |
| \$0027 | DBGCCL - | read | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | write | | | | | | | | |
| \$0028 | DBGC2 BKPCT0 | read | BKABEN | FULL | BDM | TAGAB | BKGEN | TAGC | RWCEN | RWC |
| | | write | | | | | | | | |
| \$0029 | DBGC3 BKPCT1 | read | BKAMBH | BKAMBL | BKBMBH | BKBMBL | RWAEN | RWA | RWBEN | RWB |
| | | write | | | | | | | | |
| \$002A | DBGCAH BKPOX | read | PAGSEL | | | EXTCMP | | | | |
| | | write | | | | | | | | |
| \$002B | DBGCAH BKPOH | read | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | write | | | | | | | | |

\$0020 - \$002F

DBG (including BKP) map 1 of 1 (HCS12 Debug)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|--------|-------|--------|-------|-------|--------|-------|-------|-------|-------|
| \$002C | DBGCAL | read | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | BKP0L | write | | | | | | | | |
| \$002D | DBGCBX | read | PAGSEL | | | EXTCMP | | | | |
| | BKP1X | write | | | | | | | | |
| \$002E | DBGCBH | read | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | BKP1H | write | | | | | | | | |
| \$002F | DBGCBL | read | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | BKP1L | write | | | | | | | | |

\$0030 - \$0031

MMC map 4 of 4 (HCS12 Module Mapping Control)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$0030 | PPAGE | Read: | 0 | 0 | PIX5 | PIX4 | PIX3 | PIX2 | PIX1 | PIX0 |
| | | Write: | | | | | | | | |
| \$0031 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$0032 - \$0033

MEBI map 3 of 3 (HCS12 Multiplexed External Bus Interface)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$0032 | PORTK ¹ | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$0033 | DDRK ⁽¹⁾ | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |

NOTES:

1. Only applicable in special emulation-only bond outs, for emulation of extended memory map.

\$0034 - \$003F

CRG (Clock and Reset Generator)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|--------|--------|-------|--------|--------|--------|--------|--------|--------|
| \$0034 | SYNR | Read: | 0 | 0 | SYN5 | SYN4 | SYN3 | SYN2 | SYN1 | SYN0 |
| | | Write: | | | | | | | | |
| \$0035 | REFDV | Read: | 0 | 0 | 0 | 0 | REFDV3 | REFDV2 | REFDV1 | REFDV0 |
| | | Write: | | | | | | | | |
| \$0036 | CTFLG | Read: | TOUT7 | TOUT6 | TOUT5 | TOUT4 | TOUT3 | TOUT2 | TOUT1 | TOUT0 |
| | TEST ONLY | Write: | | | | | | | | |
| \$0037 | CRGFLG | Read: | RTIF | PROF | 0 | LOCKIF | LOCK | TRACK | SCMIF | SCM |
| | | Write: | | | | | | | | |
| \$0038 | CRGINT | Read: | RTIE | 0 | 0 | LOCKIE | 0 | 0 | SCMIE | 0 |
| | | Write: | | | | | | | | |
| \$0039 | CLKSEL | Read: | PLLSEL | PSTP | SYSWAI | ROAWAI | PLLWAI | CWAI | RTIWAI | COPWAI |
| | | Write: | | | | | | | | |
| \$003A | PLLCTL | Read: | CME | PLLON | AUTO | ACQ | 0 | PRE | PCE | SCME |
| | | Write: | | | | | | | | |

\$0034 - \$003F

CRG (Clock and Reset Generator)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------------|--------|--------|--------|-------|--------|-------|-------|-------|-------|
| \$003B | RTICTL | Read: | 0 | RTR6 | RTR5 | RTR4 | RTR3 | RTR2 | RTR1 | RTR0 |
| | | Write: | | | | | | | | |
| \$003C | COPCTL | Read: | WCOP | RSBCK | 0 | 0 | 0 | CR2 | CR1 | CR0 |
| | | Write: | | | | | | | | |
| \$003D | FORBYP TEST ONLY | Read: | RTIBYP | COPBYP | 0 | PLLBYP | 0 | 0 | FCM | 0 |
| | | Write: | | | | | | | | |
| \$003E | CTCTL TEST ONLY | Read: | TCTL7 | TCTL6 | TCTL5 | TCTL4 | TCLT3 | TCTL2 | TCTL1 | TCTL0 |
| | | Write: | | | | | | | | |
| \$003F | ARMCOP | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |

\$0040 - \$006F

TIM (Timer 16 Bit 8 Channels)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|--------|--------|-------|-------|-------|-------|-------|-------|-------|
| \$0040 | TIOS | Read: | IOS7 | IOS6 | IOS5 | IOS4 | IOS3 | IOS2 | IOS1 | IOS0 |
| | | Write: | | | | | | | | |
| \$0041 | CFORC | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | FOC7 | FOC6 | FOC5 | FOC4 | FOC3 | FOC2 | FOC1 | FOC0 |
| \$0042 | OC7M | Read: | OC7M7 | OC7M6 | OC7M5 | OC7M4 | OC7M3 | OC7M2 | OC7M1 | OC7M0 |
| | | Write: | | | | | | | | |
| \$0043 | OC7D | Read: | OC7D7 | OC7D6 | OC7D5 | OC7D4 | OC7D3 | OC7D2 | OC7D1 | OC7D0 |
| | | Write: | | | | | | | | |
| \$0044 | TCNT (hi) | Read: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | Write: | | | | | | | | |
| \$0045 | TCNT (lo) | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$0046 | TSCR1 | Read: | TEN | TSWAI | TSFRZ | TFFCA | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0047 | TTOV | Read: | TOV7 | TOV6 | TOV5 | TOV4 | TOV3 | TOV2 | TOV1 | TOV0 |
| | | Write: | | | | | | | | |
| \$0048 | TCTL1 | Read: | OM7 | OL7 | OM6 | OL6 | OM5 | OL5 | OM4 | OL4 |
| | | Write: | | | | | | | | |
| \$0049 | TCTL2 | Read: | OM3 | OL3 | OM2 | OL2 | OM1 | OL1 | OM0 | OL0 |
| | | Write: | | | | | | | | |
| \$004A | TCTL3 | Read: | EDG7B | EDG7A | EDG6B | EDG6A | EDG5B | EDG5A | EDG4B | EDG4A |
| | | Write: | | | | | | | | |
| \$004B | TCTL4 | Read: | EDG3B | EDG3A | EDG2B | EDG2A | EDG1B | EDG1A | EDG0B | EDG0A |
| | | Write: | | | | | | | | |
| \$004C | TIE | Read: | C7I | C6I | C5I | C4I | C3I | C2I | C1I | C0I |
| | | Write: | | | | | | | | |
| \$004D | TSCR2 | Read: | TOI | 0 | 0 | 0 | TCRE | PR2 | PR1 | PR0 |
| | | Write: | | | | | | | | |
| \$004E | TFLG1 | Read: | C7F | C6F | C5F | C4F | C3F | C2F | C1F | C0F |
| | | Write: | | | | | | | | |
| \$004F | TFLG2 | Read: | TOF | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------|-----------------|--------|-------|-------|-------|-------|-------|-------|-------|
| \$0050 | TC0 (hi) | Read: Write: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| \$0051 | TC0 (lo) | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0052 | TC1 (hi) | Read: Write: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| \$0053 | TC1 (lo) | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0054 | TC2 (hi) | Read: Write: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| \$0055 | TC2 (lo) | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0056 | TC3 (hi) | Read: Write: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| \$0057 | TC3 (lo) | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0058 | TC4 (hi) | Read: Write: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| \$0059 | TC4 (lo) | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$005A | TC5 (hi) | Read: Write: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| \$005B | TC5 (lo) | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$005C | TC6 (hi) | Read: Write: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| \$005D | TC6 (lo) | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$005E | TC7 (hi) | Read: Write: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| \$005F | TC7 (lo) | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0060 | PACTL | Read: Write: | 0 | PAEN | PAMOD | PEDGE | CLK1 | CLK0 | PAOVI | PAI |
| \$0061 | PAFLG | Read: Write: | 0 | 0 | 0 | 0 | 0 | 0 | PAOVF | PAIF |
| \$0062 | PACNT (hi) | Read: Write: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| \$0063 | PACNT (lo) | Read: Write: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| \$0064 | Reserved | Read: Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$0065 | Reserved | Read: Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$0066 | Reserved | Read: Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$0067 | Reserved | Read: Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$0068 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0069 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$006A | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$006B | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$006C | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$006D | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$006E | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$006F | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$0070 - \$007F

Reserved

| | | | | | | | | | | |
|----------|----------|--------|---|---|---|---|---|---|---|---|
| \$0070 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| - \$007F | | Write: | | | | | | | | |

\$0080 - \$009F

ATD (Analog to Digital Converter 10 Bit 8 Channel)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|-------|-------|-------|---------|--------|-------|-------|-------|
| \$0080 | ATDCTL0 | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0081 | ATDCTL1 | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0082 | ATDCTL2 | Read: | ADPU | AFFC | AWAI | ETRIGLE | ETRIGP | ETRIG | ASCIE | ASCIF |
| | | Write: | | | | | | | | |
| \$0083 | ATDCTL3 | Read: | 0 | S8C | S4C | S2C | S1C | FIFO | FRZ1 | FRZ0 |
| | | Write: | | | | | | | | |
| \$0084 | ATDCTL4 | Read: | SRES8 | SMP1 | SMP0 | PRS4 | PRS3 | PRS2 | PRS1 | PRS0 |
| | | Write: | | | | | | | | |
| \$0085 | ATDCTL5 | Read: | DJM | DSGN | SCAN | MULT | 0 | CC | CB | CA |
| | | Write: | | | | | | | | |
| \$0086 | ATDSTAT0 | Read: | SCF | 0 | ETORF | FIFOR | 0 | CC2 | CC1 | CC0 |
| | | Write: | | | | | | | | |
| \$0087 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0088 | ATDTEST0 | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0089 | ATDTEST1 | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SC |
| | | Write: | | | | | | | | |
| \$008A | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$0080 - \$009F

ATD (Analog to Digital Converter 10 Bit 8 Channel)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$008B | ATDSTAT1 | Read: | CCF7 | CCF6 | CCF5 | CCF4 | CCF3 | CCF2 | CCF1 | CCF0 |
| | | Write: | | | | | | | | |
| \$008C | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$008D | ATDDIEN | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$008E | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$008F | PORTAD0 | Read: | Bit7 | 6 | 5 | 4 | 3 | 2 | 1 | BIT 0 |
| | | Write: | | | | | | | | |
| \$0090 | ATDDR0H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$0091 | ATDDR0L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0092 | ATDDR1H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$0093 | ATDDR1L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0094 | ATDDR2H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$0095 | ATDDR2L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0096 | ATDDR3H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$0097 | ATDDR3L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0098 | ATDDR4H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$0099 | ATDDR4L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$009A | ATDDR5H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$009B | ATDDR5L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$009C | ATDDR6H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$009D | ATDDR6L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$009E | ATDDR7H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| \$009F | ATDDR7L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$00A0 - \$00C7

Reserved

| | | | | | | | | | | |
|-----------------|----------|--------|---|---|---|---|---|---|---|---|
| \$00A0 - \$00C7 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$00C8 - \$00CF

SCI (Asynchronous Serial Interface)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|--------|--------|-------|---------|-------|-------|-------|-------|-------|-------|
| \$00C8 | SCIBDH | Read: | 0 | 0 | 0 | SBR12 | SBR11 | SBR10 | SBR9 | SBR8 |
| | | Write: | | | | | | | | |
| \$00C9 | SCIBDL | Read: | SBR7 | SBR6 | SBR5 | SBR4 | SBR3 | SBR2 | SBR1 | SBR0 |
| | | Write: | | | | | | | | |
| \$00CA | SCICR1 | Read: | LOOPS | SCISWAI | RSRC | M | WAKE | ILT | PE | PT |
| | | Write: | | | | | | | | |
| \$00CB | SCICR2 | Read: | TIE | TCIE | RIE | ILIE | TE | RE | RWU | SBK |
| | | Write: | | | | | | | | |
| \$00CC | SCISR1 | Read: | TDRE | TC | RDRF | IDLE | OR | NF | FE | PF |
| | | Write: | | | | | | | | |
| \$00CD | SCISR2 | Read: | 0 | 0 | 0 | 0 | 0 | BRK13 | TXDIR | RAF |
| | | Write: | | | | | | | | |
| \$00CE | SCIDRH | Read: | R8 | T8 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00CF | SCIDRL | Read: | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 |
| | | Write: | T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 |

\$00D0 - \$00D7

Reserved

| | | | | | | | | | | |
|---------|----------|--------|---|---|---|---|---|---|---|---|
| \$00D0 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| -\$00D7 | | Write: | | | | | | | | |

\$00D8 - \$00DF

SPI (Serial Peripheral Interface)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|-------|-------|-------|--------|---------|-------|---------|-------|
| \$00D8 | SPICR1 | Read: | SPIE | SPE | SPTIE | MSTR | CPOL | CPHA | SSOE | LSBFE |
| | | Write: | | | | | | | | |
| \$00D9 | SPICR2 | Read: | 0 | 0 | 0 | MODFEN | BIDIROE | 0 | SPISWAI | SPC0 |
| | | Write: | | | | | | | | |
| \$00DA | SPIBR | Read: | 0 | SPPR2 | SPPR1 | SPPR0 | 0 | SPR2 | SPR1 | SPR0 |
| | | Write: | | | | | | | | |
| \$00DB | SPISR | Read: | SPIF | 0 | SPTEF | MODF | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00DC | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00DD | SPIDR | Read: | Bit7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit0 |
| | | Write: | | | | | | | | |
| \$00DE | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00DF | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$00E0 - \$00FF

PWM (Pulse Width Modulator)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$00E0 | PWME | Read: | 0 | 0 | PWME5 | PWME4 | PWME3 | PWME2 | PWME1 | PWME0 |
| | | Write: | | | | | | | | |
| \$00E1 | PWMPOL | Read: | 0 | 0 | PPOL5 | PPOL4 | PPOL3 | PPOL2 | PPOL1 | PPOL0 |
| | | Write: | | | | | | | | |
| \$00E2 | PWMCLK | Read: | 0 | 0 | PCLK5 | PCLK4 | PCLK3 | PCLK2 | PCLK1 | PCLK0 |
| | | Write: | | | | | | | | |
| \$00E3 | PWMPRCLK | Read: | 0 | PCKB2 | PCKB1 | PCKB0 | 0 | PCKA2 | PCKA1 | PCKA0 |
| | | Write: | | | | | | | | |
| \$00E4 | PWMCAE | Read: | 0 | 0 | CAE5 | CAE4 | CAE3 | CAE2 | CAE1 | CAE0 |
| | | Write: | | | | | | | | |
| \$00E5 | PWMCTL | Read: | 0 | CON45 | CON23 | CON01 | PSWAI | PFRZ | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00E6 | PWMTST Test Only | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00E7 | PWMPRSC | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00E8 | PWMSCLA | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00E9 | PWMSCLB | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00EA | PWMSCNTA | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00EB | PWMSCNTB | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00EC | PWMCNT0 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$00ED | PWMCNT1 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$00EE | PWMCNT2 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$00EF | PWMCNT3 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$00F0 | PWMCNT4 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$00F1 | PWMCNT5 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| \$00F2 | PWMPER0 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00F3 | PWMPER1 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00F4 | PWMPER2 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00F5 | PWMPER3 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00F6 | PWMPER4 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$00F7 | PWMPER5 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00F8 | PWMDTY0 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00F9 | PWMDTY1 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00FA | PWMDTY2 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00FB | PWMDTY3 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00FC | PWMDTY4 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00FD | PWMDTY5 | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| \$00FE | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$00FF | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$0100 - \$010F

Flash Control Register

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------------------|--------|--------|--------|--------|--------|-------|--------|--------|--------|
| \$0100 | FCLKDIV | Read: | FDIVLD | PRDIV8 | FDIV5 | FDIV4 | FDIV3 | FDIV2 | FDIV1 | FDIV0 |
| | | Write: | | | | | | | | |
| \$0101 | FSEC | Read: | KEYEN1 | KEYEN0 | NV5 | NV4 | NV3 | NV2 | SEC1 | SEC0 |
| | | Write: | | | | | | | | |
| \$0102 | FTSTMOD | Read: | 0 | 0 | 0 | WRALL | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0103 | FCNFG | Read: | CBEIE | CCIE | KEYACC | 0 | 0 | 0 | BKSEL1 | BKSEL0 |
| | | Write: | | | | | | | | |
| \$0104 | FPROT | Read: | FPOPEN | NV6 | FPHDIS | FPHS1 | FPHS0 | FPLDIS | FPLS1 | FPLS0 |
| | | Write: | | | | | | | | |
| \$0105 | FSTAT | Read: | CBEIF | CCIF | PVIOL | ACCERR | 0 | BLANK | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0106 | FCMD | Read: | 0 | CMDB6 | CMDB5 | 0 | 0 | CMDB2 | 0 | CMDB0 |
| | | Write: | | | | | | | | |
| \$0107 | Reserved for Factory Test | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0108 | Reserved for Factory Test | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0109 | Reserved for Factory Test | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$010A | Reserved for Factory Test | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$010B | Reserved for Factory Test | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$0100 - \$010F

Flash Control Register

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$010C | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$010D | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$010E | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$010F | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$0110 - \$013F

Reserved

| | | | | | | | | | | |
|-----------------|----------|--------|---|---|---|---|---|---|---|---|
| \$0110 - \$003F | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$0140 - \$017F

CAN (Motorola Scalable CAN - MSCAN)¹

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|--------|-------|--------|---------|---------|---------|---------|--------|--------|
| \$0140 | CANCTL0 | Read: | RXFRM | RXACT | CSWAI | SYNCH | TIME | WUPE | SLPRQ | INITRQ |
| | | Write: | | | | | | | | |
| \$0141 | CANCTL1 | Read: | CANE | CLKSRC | LOOPB | LISTEN | 0 | WUPM | SLPAK | INITAK |
| | | Write: | | | | | | | | |
| \$0142 | CANBTR0 | Read: | SJW1 | SJW0 | BRP5 | BRP4 | BRP3 | BRP2 | BRP1 | BRP0 |
| | | Write: | | | | | | | | |
| \$0143 | CANBTR1 | Read: | SAMP | TSEG22 | TSEG21 | TSEG20 | TSEG13 | TSEG12 | TSEG11 | TSEG10 |
| | | Write: | | | | | | | | |
| \$0144 | CANRFLG | Read: | WUPIF | CSCIF | RSTAT1 | RSTAT0 | TSTAT1 | TSTAT0 | OVRIF | RXF |
| | | Write: | | | | | | | | |
| \$0145 | CANRIER | Read: | WUPIE | CSCIE | RSTATE1 | RSTATE0 | TSTATE1 | TSTATE0 | OVRIE | RXFIE |
| | | Write: | | | | | | | | |
| \$0146 | CANTFLG | Read: | 0 | 0 | 0 | 0 | 0 | TXE2 | TXE1 | TXE0 |
| | | Write: | | | | | | | | |
| \$0147 | CANTIER | Read: | 0 | 0 | 0 | 0 | 0 | TXEIE2 | TXEIE1 | TXEIE0 |
| | | Write: | | | | | | | | |
| \$0148 | CANTARQ | Read: | 0 | 0 | 0 | 0 | 0 | ABTRQ2 | ABTRQ1 | ABTRQ0 |
| | | Write: | | | | | | | | |
| \$0149 | CANTAAK | Read: | 0 | 0 | 0 | 0 | 0 | ABTAK2 | ABTAK1 | ABTAK0 |
| | | Write: | | | | | | | | |
| \$014A | CANTBSEL | Read: | 0 | 0 | 0 | 0 | 0 | TX2 | TX1 | TX0 |
| | | Write: | | | | | | | | |
| \$014B | CANIDAC | Read: | 0 | 0 | IDAM1 | IDAM0 | 0 | IDHIT2 | IDHIT1 | IDHIT0 |
| | | Write: | | | | | | | | |
| \$014C | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$014D | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

\$0140 - \$017F

CAN (Motorola Scalable CAN - MSCAN)¹

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------|---------------------|--------|---|--------|--------|--------|--------|--------|--------|--------|
| \$014E | CANRXERR | Read: | RXERR7 | RXERR6 | RXERR5 | RXERR4 | RXERR3 | RXERR2 | RXERR1 | RXERR0 |
| | | Write: | | | | | | | | |
| \$014F | CANTXERR | Read: | TXERR7 | TXERR6 | TXERR5 | TXERR4 | TXERR3 | TXERR2 | TXERR1 | TXERR0 |
| | | Write: | | | | | | | | |
| \$0150 - \$0153 | CANIDAR0 - CANIDAR3 | Read: | AC7 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |
| | | Write: | | | | | | | | |
| \$0154 - \$0157 | CANIDMR0 - CANIDMR3 | Read: | AM7 | AM6 | AM5 | AM4 | AM3 | AM2 | AM1 | AM0 |
| | | Write: | | | | | | | | |
| \$0158 - \$015B | CANIDAR4 - CANIDAR7 | Read: | AC7 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |
| | | Write: | | | | | | | | |
| \$015C - \$015F | CANIDMR4 - CANIDMR7 | Read: | AM7 | AM6 | AM5 | AM4 | AM3 | AM2 | AM1 | AM0 |
| | | Write: | | | | | | | | |
| \$0160 - \$016F | CANRXFG | Read: | FOREGROUND RECEIVE BUFFER see Table 1-2 | | | | | | | |
| | | Write: | | | | | | | | |
| \$0170 - \$017F | CANTXFG | Read: | FOREGROUND TRANSMIT BUFFER see Table 1-2 | | | | | | | |
| | | Write: | | | | | | | | |

NOTES:

1. Not available on the MC9S12GC-Family members. Those memory locations should not be accessed.

Table 1-2 Detailed MSCAN Foreground Receive and Transmit Buffer Layout

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------------|-----------------------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$xxx0 | Extended ID | Read: | ID28 | ID27 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 |
| | | Write: | | | | | | | | |
| \$xxx1 | Standard ID | Read: | ID10 | ID9 | ID8 | ID7 | ID6 | ID5 | ID4 | ID3 |
| | | Write: | | | | | | | | |
| \$xxx1 | Extended ID | Read: | ID20 | ID19 | ID18 | SRR=1 | IDE=1 | ID17 | ID16 | ID15 |
| | | Write: | | | | | | | | |
| \$xxx2 | Standard ID | Read: | ID2 | ID1 | ID0 | RTR | IDE=0 | | | |
| | | Write: | | | | | | | | |
| \$xxx2 | Extended ID | Read: | ID14 | ID13 | ID12 | ID11 | ID10 | ID9 | ID8 | ID7 |
| | | Write: | | | | | | | | |
| \$xxx3 | Standard ID | Read: | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 | RTR |
| | | Write: | | | | | | | | |
| \$xxx4- \$xxxB | CANxRDSR0 - CANxRDSR7 | Read: | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| | | Write: | | | | | | | | |
| \$xxxC | CANRxDLR | Read: | | | | | DLC3 | DLC2 | DLC1 | DLC0 |
| | | Write: | | | | | | | | |
| \$xxxD | Reserved | Read: | | | | | | | | |
| | | Write: | | | | | | | | |
| \$xxxE | CANxRTSRH | Read: | TSR15 | TSR14 | TSR13 | TSR12 | TSR11 | TSR10 | TSR9 | TSR8 |
| | | Write: | | | | | | | | |
| \$xxxF | CANxRTSRL | Read: | TSR7 | TSR6 | TSR5 | TSR4 | TSR3 | TSR2 | TSR1 | TSR0 |
| | | Write: | | | | | | | | |
| \$xx10 | Extended ID | Read: | ID28 | ID27 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 |
| | | Write: | | | | | | | | |
| | Standard ID | Read: | ID10 | ID9 | ID8 | ID7 | ID6 | ID5 | ID4 | ID3 |
| | | Write: | | | | | | | | |

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------|--------------------------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$xx11 | Extended ID CANxTIDR1 | Read: | ID20 | ID19 | ID18 | SRR=1 | IDE=1 | ID17 | ID16 | ID15 |
| | | Write: | | | | | | | | |
| | Standard ID | Read: | ID2 | ID1 | ID0 | RTR | IDE=0 | | | |
| | | Write: | | | | | | | | |
| \$xx12 | Extended ID CANxTIDR2 | Read: | ID14 | ID13 | ID12 | ID11 | ID10 | ID9 | ID8 | ID7 |
| | | Write: | | | | | | | | |
| | Standard ID | Read: | | | | | | | | |
| | | Write: | | | | | | | | |
| \$xx13 | Extended ID CANxTIDR3 | Read: | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 | RTR |
| | | Write: | | | | | | | | |
| | Standard ID | Read: | | | | | | | | |
| | | Write: | | | | | | | | |
| \$xx14- \$xx1B | CANxTDSR0 - CANxTDSR7 | Read: | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| | | Write: | | | | | | | | |
| \$xx1C | CANxTDLR | Read: | | | | | DLC3 | DLC2 | DLC1 | DLC0 |
| | | Write: | | | | | | | | |
| \$xx1D | CONxTTBPR | Read: | PRI07 | PRI06 | PRI05 | PRI04 | PRI03 | PRI02 | PRI01 | PRI00 |
| | | Write: | | | | | | | | |
| \$xx1E | CANxTTSRH | Read: | TSR15 | TSR14 | TSR13 | TSR12 | TSR11 | TSR10 | TSR9 | TSR8 |
| | | Write: | | | | | | | | |
| \$xx1F | CANxTTSRL | Read: | TSR7 | TSR6 | TSR5 | TSR4 | TSR3 | TSR2 | TSR1 | TSR0 |
| | | Write: | | | | | | | | |

\$0180 - \$023F

\$0180
- \$023F Reserved

Reserved

| | | | | | | | | |
|--------|---|---|---|---|---|---|---|---|
| Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Write: | | | | | | | | |

\$0240 - \$027F

PIM (Port Interface Module)

| | | | | | | | | | | |
|--------|----------|--------|-------|-------|-------|--------|--------|--------|--------|--------|
| \$0240 | PTT | Read: | PTT7 | PTT6 | PTT5 | PTT4 | PTT3 | PTT2 | PTT1 | PTT0 |
| | | Write: | | | | | | | | |
| \$0241 | PTIT | Read: | PTIT7 | PTIT6 | PTIT5 | PTIT4 | PTIT3 | PTIT2 | PTIT1 | PTIT0 |
| | | Write: | | | | | | | | |
| \$0242 | DDRT | Read: | DDRT7 | DDRT6 | DDRT5 | DDRT4 | DDRT3 | DDRT2 | DDRT1 | DDRT0 |
| | | Write: | | | | | | | | |
| \$0243 | RDRT | Read: | RDRT7 | RDRT6 | RDRT5 | RDRT4 | RDRT3 | RDRT2 | RDRT1 | RDRT0 |
| | | Write: | | | | | | | | |
| \$0244 | PERT | Read: | PERT7 | PERT6 | PERT5 | PERT4 | PERT3 | PERT2 | PERT1 | PERT0 |
| | | Write: | | | | | | | | |
| \$0245 | PPST | Read: | PPST7 | PPST6 | PPST5 | PPST4 | PPST3 | PPST2 | PPST1 | PPST0 |
| | | Write: | | | | | | | | |
| \$0246 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0247 | MODRR | Read: | 0 | 0 | 0 | MODRR4 | MODRR3 | MODRR2 | MODRR1 | MODRR0 |
| | | Write: | | | | | | | | |
| \$0248 | PTS | Read: | 0 | 0 | 0 | 0 | PTS3 | PTS2 | PTS1 | PTS0 |
| | | Write: | | | | | | | | |

| | | | | | | | | | | |
|--------|----------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$0249 | PTIS | Read: | 0 | 0 | 0 | 0 | PTIS3 | PTIS2 | PTIS1 | PTIS0 |
| | | Write: | | | | | | | | |
| \$024A | DDRS | Read: | 0 | 0 | 0 | 0 | DDRS3 | DDRS2 | DDRS1 | DDRS0 |
| | | Write: | | | | | | | | |
| \$024B | RDRS | Read: | 0 | 0 | 0 | 0 | RDRS3 | RDRS2 | RDRS1 | RDRS0 |
| | | Write: | | | | | | | | |
| \$024C | PERS | Read: | 0 | 0 | 0 | 0 | PERS3 | PERS2 | PERS1 | PERS0 |
| | | Write: | | | | | | | | |
| \$024D | PPSS | Read: | 0 | 0 | 0 | 0 | PPSS3 | PPSS2 | PPSS1 | PPSS0 |
| | | Write: | | | | | | | | |
| \$024E | WOMS | Read: | 0 | 0 | 0 | 0 | WOMS3 | WOMS2 | WOMS1 | WOMS0 |
| | | Write: | | | | | | | | |
| \$024F | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0250 | PTM | Read: | 0 | 0 | PTM5 | PTM4 | PTM3 | PTM2 | PTM1 | PTM0 |
| | | Write: | | | | | | | | |
| \$0251 | PTIM | Read: | 0 | 0 | PTIM5 | PTIM4 | PTIM3 | PTIM2 | PTIM1 | PTIM0 |
| | | Write: | | | | | | | | |
| \$0252 | DDRM | Read: | 0 | 0 | DDRM5 | DDRM4 | DDRM3 | DDRM2 | DDRM1 | DDRM0 |
| | | Write: | | | | | | | | |
| \$0253 | RDRM | Read: | 0 | 0 | RDRM5 | RDRM4 | RDRM3 | RDRM2 | RDRM1 | RDRM0 |
| | | Write: | | | | | | | | |
| \$0254 | PERM | Read: | 0 | 0 | PERM5 | PERM4 | PERM3 | PERM2 | PERM1 | PERM0 |
| | | Write: | | | | | | | | |
| \$0255 | PPSM | Read: | 0 | 0 | PPSM5 | PPSM4 | PPSM3 | PPSM2 | PPSM1 | PPSM0 |
| | | Write: | | | | | | | | |
| \$0256 | WOMM | Read: | 0 | 0 | WOMM5 | WOMM4 | WOMM3 | WOMM2 | WOMM1 | WOMM0 |
| | | Write: | | | | | | | | |
| \$0257 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0258 | PTP | Read: | PTP7 | PTP6 | PTP5 | PTP4 | PTP3 | PTP2 | PTP1 | PTP0 |
| | | Write: | | | | | | | | |
| \$0259 | PTIP | Read: | PTIP7 | PTIP6 | PTIP5 | PTIP4 | PTIP3 | PTIP2 | PTIP1 | PTIP0 |
| | | Write: | | | | | | | | |
| \$025A | DDRP | Read: | DDRP7 | DDRP6 | DDRP5 | DDRP4 | DDRP3 | DDRP2 | DDRP1 | DDRP0 |
| | | Write: | | | | | | | | |
| \$025B | RDRP | Read: | RDRP7 | RDRP6 | RDRP5 | RDRP4 | RDRP3 | RDRP2 | RDRP1 | RDRP0 |
| | | Write: | | | | | | | | |
| \$025C | PERP | Read: | PERP7 | PERP6 | PERP5 | PERP4 | PERP3 | PERP2 | PERP1 | PERP0 |
| | | Write: | | | | | | | | |
| \$025D | PPSP | Read: | PPSP7 | PPSP6 | PPSP5 | PPSP4 | PPSP3 | PPSP2 | PPSP1 | PPSP0 |
| | | Write: | | | | | | | | |
| \$025E | PIEP | Read: | PIEP7 | PIEP6 | PIEP5 | PIEP4 | PIEP3 | PIEP2 | PIEP1 | PIEP0 |
| | | Write: | | | | | | | | |
| \$025F | PIFP | Read: | PIFP7 | PIFP6 | PIFP5 | PIFP4 | PIFP3 | PIFP2 | PIFP1 | PIFP0 |
| | | Write: | | | | | | | | |
| \$0260 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

| | | | | | | | | | | |
|-------------------|----------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| \$0261 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | Write: | | | | | | | | |
| \$0262 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | Write: | | | | | | | | |
| \$0263 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | Write: | | | | | | | | |
| \$0264 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | Write: | | | | | | | | |
| \$0265 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | Write: | | | | | | | | |
| \$0266 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | Write: | | | | | | | | |
| \$0267 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | Write: | | | | | | | | |
| \$0268 | PTJ | Read: | PTJ7 | PTJ6 | 0 | 0 | 0 | 0 | 0 | |
| | | Write: | | | | | | | | |
| \$0269 | PTIJ | Read: | PTIJ7 | PTIJ6 | 0 | 0 | 0 | 0 | 0 | |
| | | Write: | | | | | | | | |
| \$026A | DDRJ | Read: | DDRJ7 | DDRJ7 | 0 | 0 | 0 | 0 | 0 | |
| | | Write: | | | | | | | | |
| \$026B | RDRJ | Read: | RDRJ7 | RDRJ6 | 0 | 0 | 0 | 0 | 0 | |
| | | Write: | | | | | | | | |
| \$026C | PERJ | Read: | PERJ7 | PERJ6 | 0 | 0 | 0 | 0 | 0 | |
| | | Write: | | | | | | | | |
| \$026D | PPSJ | Read: | PPSJ7 | PPSJ6 | 0 | 0 | 0 | 0 | 0 | |
| | | Write: | | | | | | | | |
| \$026E | PIEJ | Read: | PIEJ7 | PIEJ6 | 0 | 0 | 0 | 0 | 0 | |
| | | Write: | | | | | | | | |
| \$026F | PIFJ | Read: | PIFJ7 | PIFJ6 | 0 | 0 | 0 | 0 | 0 | |
| | | Write: | | | | | | | | |
| \$0270 | PTAD | Read: | PTAD7 | PTAD6 | PTAD5 | PTAD4 | PTAD3 | PTAD2 | PTAD1 | PTAD0 |
| | | Write: | | | | | | | | |
| \$0271 | PTIAD | Read: | PTIAD7 | PTIAD6 | PTIAD5 | PTIAD4 | PTIAD3 | PTIAD2 | PTIAD1 | PTIJ7 |
| | | Write: | | | | | | | | |
| \$0272 | DDRAD | Read: | DDRAD7 | DDRAD6 | DDRAD5 | DDRAD4 | DDRAD3 | DDRAD2 | DDRAD1 | DDRAD0 |
| | | Write: | | | | | | | | |
| \$0273 | RDRAD | Read: | RDRAD7 | RDRAD6 | RDRAD5 | RDRAD4 | RDRAD3 | RDRAD2 | RDRAD1 | RDRAD0 |
| | | Write: | | | | | | | | |
| \$0274 | PERAD | Read: | PERAD7 | PERAD6 | PERAD5 | PERAD4 | PERAD3 | PERAD2 | PERAD1 | PERAD0 |
| | | Write: | | | | | | | | |
| \$0275 | PPSAD | Read: | PPSAD7 | PPSAD6 | PPSAD5 | PPSAD4 | PPSAD3 | PPSAD2 | PPSAD1 | PPSAD0 |
| | | Write: | | | | | | | | |
| \$0276- \$027F | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | Write: | | | | | | | | |

\$0280 - \$03FF

Reserved space

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------|---------------|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| \$0280 - \$2FF | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| \$0300 - \$03FF | Unimplemented | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

1.7 Part ID Assignments

The part ID is located in two 8-bit registers PARTIDH and PARTIDL (addresses \$001A and \$001B after reset). The read-only value is a unique part ID for each revision of the chip. Table 1-3 shows the assigned part ID numbers.

Table 1-3 Assigned Part ID Numbers

| Device | Mask Set Number | Part ID ¹ |
|-------------|-----------------|----------------------|
| MC9S12C32 | 0L45J | \$3300 |
| MC9S12C32 | 1L45J | \$3300 |
| MC9S12C32 | 2L45J | \$3302 |
| MC9S12C64 | TBD | TBD |
| MC9S12C96 | TBD | TBD |
| MC9S12C128 | 0L09S | \$3100 |
| MC9S12C128 | 1L09S | \$3101 |
| MC9S12GC16 | TBD | TBD |
| MC9S12GC32 | TBD | TBD |
| MC9S12GC64 | TBD | TBD |
| MC9S12GC128 | TBD | TBD |

NOTES:

- The coding is as follows:
 Bit 15-12: Major family identifier
 Bit 11-8: Minor family identifier
 Bit 7-4: Major mask set revision number including FAB transfers
 Bit 3-0: Minor - non full - mask set revision

The device memory sizes are located in two 8-bit registers MEMSIZ0 and MEMSIZ1 (addresses \$001C and \$001D after reset). **Table 1-4** shows the read-only values of these registers. Refer to Module Mapping and Control (MMC) Block Guide for further details.

Table 1-4 Memory size registers

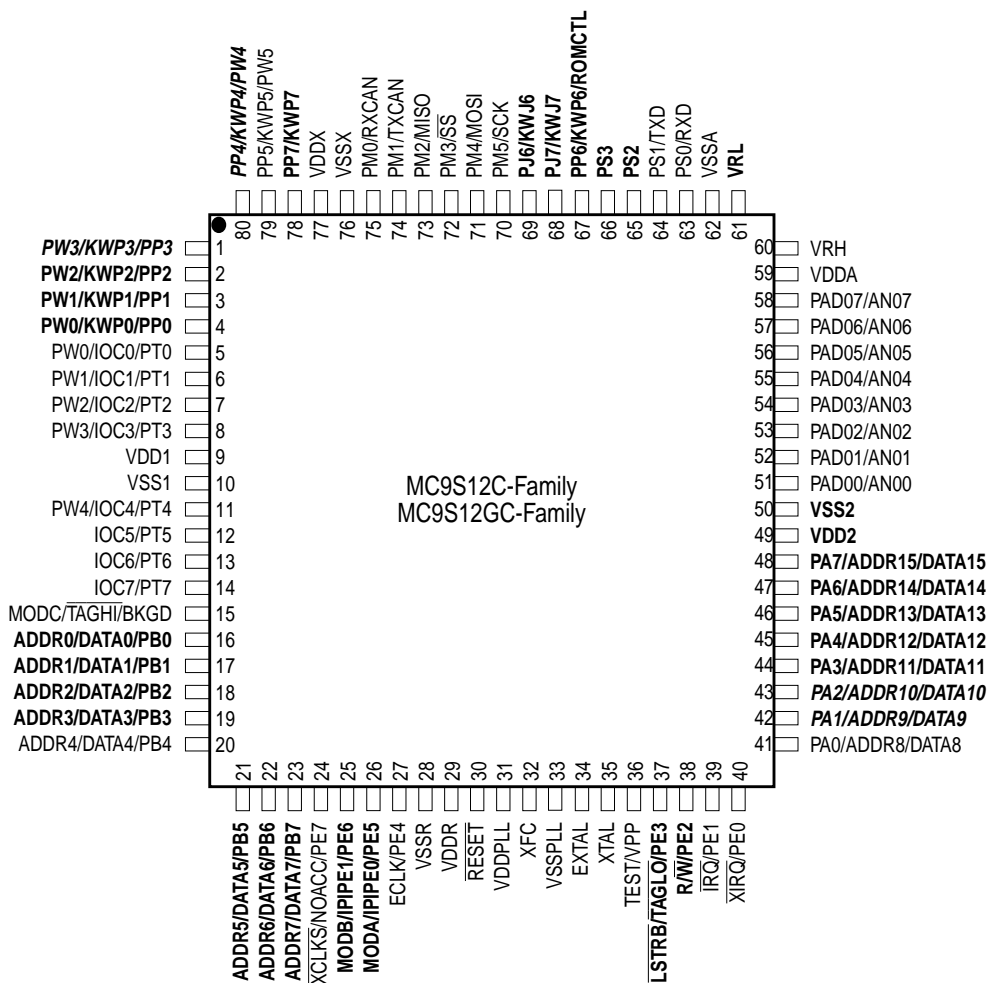
| Device | Register name | Value |
|------------|---------------|-------|
| MC9S12GC16 | MEMSIZ0 | \$00 |
| | MEMSIZ1 | \$80 |

Table 1-4 Memory size registers

| Device | Register name | Value |
|-------------------------|---------------|-------|
| MC9S12C32, MC9S12GC32 | MEMSIZ0 | \$00 |
| | MEMSIZ1 | \$80 |
| MC9S12C64, MC9S12GC64 | MEMSIZ0 | \$01 |
| | MEMSIZ1 | \$C0 |
| MC9S12C96 | MEMSIZ0 | \$01 |
| | MEMSIZ1 | \$C0 |
| MC9S12C128, MC9S12GC128 | MEMSIZ0 | \$01 |
| | MEMSIZ1 | \$C0 |

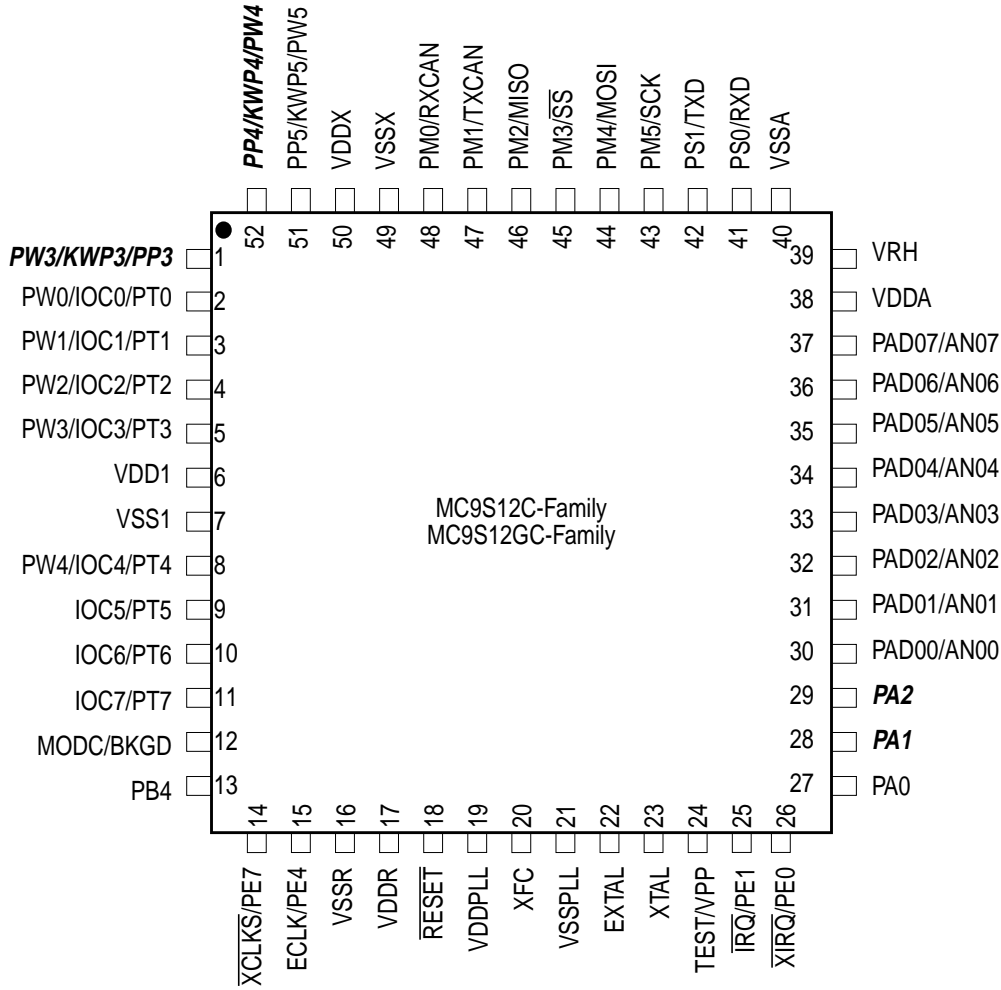
Section 2 Signal Description

2.1 Device Pinout



Signals shown in **Bold** are not available on the 52 or 48 Pin Package
 Signals shown in **Bold Italic** are available in the 52, but not the 48 Pin Package

Figure 2-1 Pin Assignments in 80 QFP for MC9S12C-Family



* Signals shown in ***Bold italic*** are not available on the 48 Pin Package

Figure 2-2 Pin assignments in 52 LQFP for MC9S12C-Family

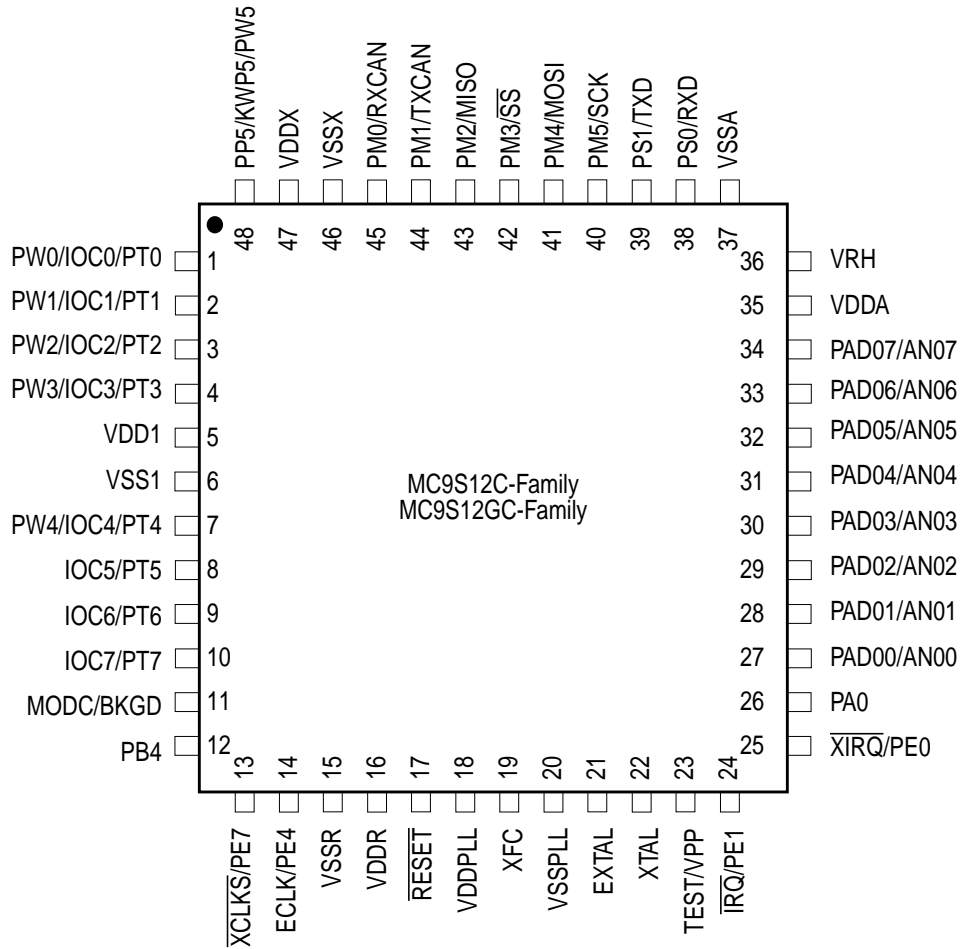


Figure 2-3 Pin Assignments in 48 LQFP for MC9S12C-Family

2.2 Signal Properties Summary

Table 2-1 Signal Properties

| Pin Name Function 1 | Pin Name Function 2 | Pin Name Function 3 | Power Domain | Internal Pull Resistor | | Description |
|------------------------|--------------------------|------------------------|-----------------|------------------------------|-------------------------|---|
| | | | | CTRL | Reset State | |
| EXTAL | — | — | VDDPLL | NA | NA | Oscillator pins |
| XTAL | — | — | VDDPLL | NA | NA | |
| RESET | — | — | VDDX | None | None | External reset pin |
| XFC | — | — | VDDPLL | NA | NA | PLL loop filter pin |
| TEST | VPP | — | VSSX | NA | NA | Test pin only |
| BKGD | MODC | TAGHI | VDDX | Up | Up | Background debug, mode pin, tag signal high |
| PE7 | NOACC | XCLKS | VDDX | PUCR | Up | Port E I/O pin, access, clock select |
| PE6 | IPIPE1 | MODB | VDDX | While RESET pin is low: Down | | Port E I/O pin and pipe status |
| PE5 | IPIPE0 | MODA | VDDX | While RESET pin is low: Down | | Port E I/O pin and pipe status |
| PE4 | ECLK | — | VDDX | PUCR | Mode Dep ¹ | Port E I/O pin, bus clock output |
| PE3 | LSTRB | TAGLO | VDDX | PUCR | Mode Dep ⁽¹⁾ | Port E I/O pin, low strobe, tag signal low |
| PE2 | R/W | — | VDDX | PUCR | Mode Dep ⁽¹⁾ | Port E I/O pin, R/W in expanded modes |
| PE1 | IRQ | — | VDDX | PUCR | Up | Port E input, external interrupt pin |
| PE0 | XIRQ | — | VDDX | PUCR | Up | Port E input, non-maskable interrupt pin |
| PA[7:3] | ADDR[15:1/ DATA[15:1] | — | VDDX | PUCR | Disabled | Port A I/O pin & multiplexed address/data |
| PA[2:1] | ADDR[10:9/ DATA[10:9] | — | VDDX | PUCR | Disabled | Port A I/O pin & multiplexed address/data |
| PA[0] | ADDR[8]/ DATA[8] | — | VDDX | PUCR | Disabled | Port A I/O pin & multiplexed address/data |
| PB[7:5] | ADDR[7:5]/ DATA[7:5] | — | VDDX | PUCR | Disabled | Port B I/O pin & multiplexed address/data |
| PB[4] | ADDR[4]/ DATA[4] | — | VDDX | PUCR | Disabled | Port B I/O pin & multiplexed address/data |
| PB[3:0] | ADDR[3:0]/ DATA[3:0] | — | VDDX | PUCR | Disabled | Port B I/O pin & multiplexed address/data |
| PAD[7:0] | AN[7:0] | — | VDDA | PERAD/P PSAD | Disabled | Port AD I/O pins and ATD inputs |
| PP[7] | KWP[7] | — | VDDX | PERP/ PPSP | Disabled | Port P I/O Pins and keypad wake-up |
| PP[6] | KWP[6] | ROMCTL | VDDX | PERP/ PPSP | Disabled | Port P I/O Pins, keypad wake-up and ROMON enable. |
| PP[5] | KWP[5] | PW5 | VDDX | PERP/ PPSP | Disabled | Port P I/O Pin, keypad wake-up, PW5 output |
| PP[4:3] | KWP[4:3] | PW[4:3] | VDDX | PERP/ PPSP | Disabled | Port P I/O Pin, keypad wake-up, PWM output |

| Pin Name Function 1 | Pin Name Function 2 | Pin Name Function 3 | Power Domain | Internal Pull Resistor | | Description |
|------------------------|------------------------|------------------------|-----------------|---------------------------|----------------|---|
| | | | | CTRL | Reset State | |
| PP[2:0] | KWP[2:0] | PW[2:0] | VDDX | PERP/ PPSP | Disabled | Port P I/O Pins, keypad wake-up, PWM outputs |
| PJ[7:6] | KWJ[7:6] | — | VDDX | PERJ/ PPSJ | Disabled | Port J I/O Pins and keypad wake-up |
| PM5 | SCK | — | VDDX | PERM/ PPSM | Up | Port M I/O Pin and SPI SCK signal |
| PM4 | MOSI | — | VDDX | PERM/ PPSM | Up | Port M I/O Pin and SPI MOSI signal |
| PM3 | \overline{SS} | — | VDDX | PERM/ PPSM | Up | Port M I/O Pin and SPI \overline{SS} signal |
| PM2 | MISO | — | VDDX | PERM/ PPSM | Up | Port M I/O Pin and SPI MISO signal |
| PM1 | TXCAN | — | VDDX | PERM/ PPSM | Up | Port M I/O Pin and CAN transmit signal ² |
| PM0 | RXCAN | — | VDDX | PERM/ PPSM | Up | Port M I/O Pin and CAN receive signal ² |
| PS[3:2] | — | — | VDDX | PERS/ PPSS | Up | Port S I/O Pins |
| PS1 | TXD | — | VDDX | PERS/ PPSS | Up | Port S I/O Pin and SCI transmit signal |
| PS0 | RXD | — | VDDX | PERS/ PPSS | Up | Port S I/O Pin and SCI receive signal |
| PT[7:5] | IOC[7:5] | — | VDDX | PERT/ PPST | Disabled | Port T I/O Pins shared with timer (TIM) |
| PT[4:0] | IOC[4:0] | PW[4:0] | VDDX | PERT/ PPST | Disabled | Port T I/O Pins shared with timer and PWM |

NOTES:

1. The PortE output buffer enable signal control at reset is determined by the PEAR register and is mode dependent. E.g. in special test mode RDWE=LSTRE=1 which enables the PE[3:2] output buffers and disables the pull-ups. Refer to S12_MEBI user guide for PEAR register details.
2. CAN functionality is not available on the MC9S12GC-Family members

2.2.1 Pin Initialization for 48 & 52 Pin LQFP bond-out versions

Not Bonded Pins If the port pins are not bonded out in the chosen package the user should initialize the registers to be inputs with enabled pull resistance to avoid excess current consumption. This applies to the following pins:

(48LQFP): Port A[7:1], Port B[7:5], Port B[3:0], PortE[6,5,3,2], Port P[7:6], PortP[4:0], Port J[7:6], PortS[3:2]

(52LQFP): Port A[7:3], Port B[7:5], Port B[3:0], PortE[6,5,3,2], Port P[7:6], PortP[2:0], Port J[7:6], PortS[3:2]

2.3 Detailed Signal Descriptions

2.3.1 EXTAL, XTAL — Oscillator Pins

EXTAL and XTAL are the crystal driver and external clock pins. On reset all the device clocks are derived from the EXTAL input frequency. XTAL is the crystal output.

2.3.2 $\overline{\text{RESET}}$ — External Reset Pin

RESET is an active low bidirectional control signal that acts as an input to initialize the MCU to a known start-up state. It also acts as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or COP watchdog circuit. External circuitry connected to the RESET pin should not include a large capacitance that would interfere with the ability of this signal to rise to a valid logic one within 32 ECLK cycles after the low drive is released. Upon detection of any reset, an internal circuit drives the RESET pin low and a clocked reset sequence controls when the MCU can begin normal processing.

2.3.3 TEST / VPP — Test Pin

This pin is reserved for test and must be tied to VSS in all applications.

2.3.4 XFC — PLL Loop Filter Pin

Dedicated pin used to create the PLL loop filter. See CRG BUG for more detailed information. PLL loop filter. Please ask your Motorola representative for the interactive application note to compute PLL loop filter elements. Any current leakage on this pin must be avoided.

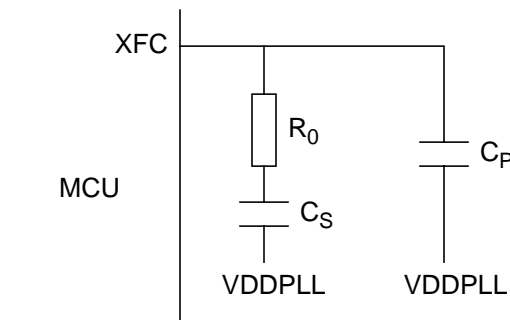


Figure 2-4 PLL Loop Filter Connections

2.3.5 BKGD / $\overline{\text{TAGHI}}$ / MODC — Background Debug, Tag High & Mode Pin

The BKGD / $\overline{\text{TAGHI}}$ / MODC pin is used as a pseudo-open-drain pin for the background debug communication. In MCU expanded modes of operation when instruction tagging is on, an input low on this pin during the falling edge of E-clock tags the high half of the instruction word being read into the instruction queue. It is also used as a MCU operating mode select pin at the rising edge during reset, when the state of this pin is latched to the MODC bit.

2.3.6 PA[7:0] / ADDR[15:8] / DATA[15:8] — Port A I/O Pins

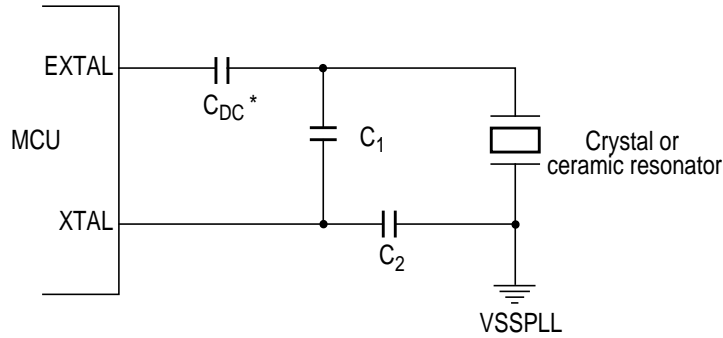
PA7-PA0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus. PA[7:1] pins are not available in the 48 package version. PA[7:3] are not available in the 52 pin package version.

2.3.7 PB[7:0] / ADDR[7:0] / DATA[7:0] — Port B I/O Pins

PB7-PB0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus. PB[7:5] and PB[3:0] pins are not available in the 48 nor 52 pin package version.

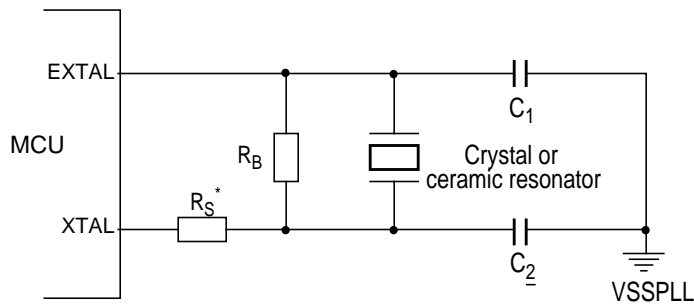
2.3.8 PE7 / NOACC / $\overline{\text{XCLKS}}$ — Port E I/O Pin 7

PE7 is a general purpose input or output pin. During MCU expanded modes of operation, the NOACC signal, when enabled, is used to indicate that the current bus cycle is an unused or “free” cycle. This signal will assert when the CPU is not using the bus. The XCLKS is an input signal which controls whether a crystal in combination with the internal Colpitts (low power) oscillator is used or whether Pierce oscillator/external clock circuitry is used. The state of this pin is latched at the rising edge of RESET. If the input is a logic low the EXTAL pin is configured for an external clock drive or a Pierce Oscillator. If input is a logic high a Colpitts oscillator circuit is configured on EXTAL and XTAL. Since this pin is an input with a pull-up device during reset, if the pin is left floating, the default configuration is a Colpitts oscillator circuit on EXTAL and XTAL.



* Due to the nature of a translated ground Colpitts oscillator a DC voltage bias is applied to the crystal
 .Please contact the crystal manufacturer for crystal DC

Figure 2-5 Colpitts Oscillator Connections (PE7=1)



* R_s can be zero (shorted) when use with higher frequency crystals.
 Refer to manufacturer's data.

Figure 2-6 Pierce Oscillator Connections (PE7=0)

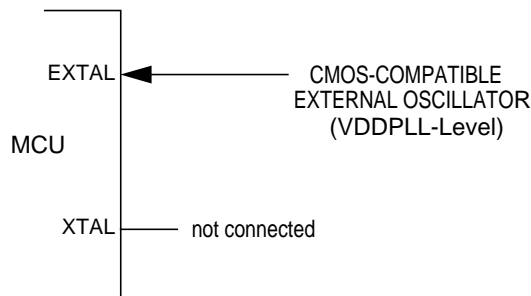


Figure 2-7 External Clock Connections (PE7=0)

2.3.9 PE6 / MODB / IPIPE1 — Port E I/O Pin 6

PE6 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODB bit at the rising edge of RESET. This pin is shared with the instruction queue tracking signal IPIPE1}. This pin is an input with a pull-down device which is only active when RESET is low. PE[6] is not available in the 48 / 52 pin package versions.

2.3.10 PE5 / MODA / IPIPE0 — Port E I/O Pin 5

PE5 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODA bit at the rising edge of RESET. This pin is shared with the instruction queue tracking signal IPIPE0}. This pin is an input with a pull-down device which is only active when RESET is low. This pin is not available in the 48 / 52 pin package versions.

2.3.11 PE4 / ECLK— Port E I/O Pin [4] / E-Clock Output

ECLK is the output connection for the internal bus clock. It is used to demultiplex the address and data in expanded modes and is used as a timing reference. ECLK frequency is equal to 1/2 the crystal frequency out of reset. The ECLK pin is initially configured as ECLK output with stretch in all expanded modes. The E clock output function depends upon the settings of the NECLK bit in the PEAR register, the IVIS bit in the MODE register and the ESTR bit in the EBICTL register. All clocks, including the E clock, are halted when the MCU is in STOP mode. It is possible to configure the MCU to interface to slow external memory. ECLK can be stretched for such accesses. Reference the MISC register (EXSTR[1:0] bits) for more information. In normal expanded narrow mode, the E clock is available for use in external select decode logic or as a constant speed clock for use in the external application system. Alternatively PE4 can be used as a general purpose input or output pin.

2.3.12 PE3 / $\overline{\text{LSTRB}}$ — Port E I/O Pin [3] / Low-Byte Strobe ($\overline{\text{LSTRB}}$)

In all modes this pin can be used as a general-purpose I/O and is an input with an active pull-up out of reset. If the strobe function is required, it should be enabled by setting the LSTRE bit in the PEAR register. This signal is used in write operations. Therefore external low byte writes will not be possible until this function is enabled. This pin is also used as $\overline{\text{TAGLO}}$ in Special Expanded modes and is multiplexed with the $\overline{\text{LSTRB}}$ function. This pin is not available in the 48 / 52 pin package versions.

2.3.13 PE2 / $\overline{\text{R/W}}$ — Port E I/O Pin [2] / Read/Write

In all modes this pin can be used as a general-purpose I/O and is an input with an active pull-up out of reset. If the read/write function is required it should be enabled by setting the RDWE bit in the PEAR register. External writes will not be possible until enabled. This pin is not available in the 48 / 52 pin package versions.

2.3.14 PE1 / $\overline{\text{IRQ}}$ — Port E input Pin [1] / Maskable Interrupt Pin

The $\overline{\text{IRQ}}$ input provides a means of applying asynchronous interrupt requests to the MCU. Either falling edge-sensitive triggering or level-sensitive triggering is program selectable (INTCR register). $\overline{\text{IRQ}}$ is always enabled and configured to level-sensitive triggering out of reset. It can be disabled by clearing IRQEN bit (INTCR register). When the MCU is reset the $\overline{\text{IRQ}}$ function is masked in the condition code register. This pin is always an input and can always be read. There is an active pull-up on this pin while in reset and immediately out of reset. The pull-up can be turned off by clearing PUPPEE in the PUCR register.

2.3.15 PE0 / $\overline{\text{XIRQ}}$ — Port E input Pin [0] / Non Maskable Interrupt Pin

The $\overline{\text{XIRQ}}$ input provides a means of requesting a non maskable interrupt after reset initialization. During reset, the X bit in the condition code register (CCR) is set and any interrupt is masked until MCU software enables it. Because the $\overline{\text{XIRQ}}$ input is level sensitive, it can be connected to a multiple-source wired-OR network. This pin is always an input and can always be read. There is an active pull-up on this pin while in reset and immediately out of reset. The pull-up can be turned off by clearing PUPPEE in the PUCR register.

2.3.16 PAD[7:0] / AN[7:0] — Port AD I/O Pins [7:0]

PAD7-PAD0 are general purpose I/O pins and also analog inputs for the analog to digital converter. In order to use a PAD pin as a standard I/O, the corresponding ATDDIEN register bit must be set. These bits are cleared out of reset to configure the PAD pins for A/D operation.

When the A/D converter is active in multi-channel mode, port inputs are scanned and converted irrespective of PortAD configuration. Thus PortAD pins that are configured as digital inputs or digital outputs are also converted in the A/D conversion sequence.

2.3.17 PP[7] / KWP[7] — Port P I/O Pin [7]

PP7 is a general purpose input or output pin, shared with the keypad interrupt function. When configured as an input, it can generate interrupts causing the MCU to exit STOP or WAIT mode. This pin is not available in the 48 / 52 pin package versions.

2.3.18 PP[6] / KWP[6]/ROMCTL — Port P I/O Pin [6]

PP6 is a general purpose input or output pin, shared with the keypad interrupt function. When configured as an input, it can generate interrupts causing the MCU to exit STOP or WAIT mode. This pin is not available in the 48 / 52 pin package versions. During MCU expanded modes of operation, this pin is used to enable the Flash EEPROM memory in the memory map (ROMCTL). At the rising edge of RESET, the state of this pin is latched to the ROMON bit.

PP6=1 in emulation modes equates to ROMON =0 (ROM space externally mapped)

PP6=0 in expanded modes equates to ROMON =0 (ROM space externally mapped)

2.3.19 PP[5:0] / KWP[5:0] / PW[5:0] — Port P I/O Pins [5:0]

PP[5:0] are general purpose input or output pins, shared with the keypad interrupt function. When configured as inputs, they can generate interrupts causing the MCU to exit STOP or WAIT mode. PP[5:0] are also shared with the PWM output signals, PW[5:0]. Pins PP[2:0] are only available in the 80 pin package version. Pins PP[4:3] are not available in the 48 pin package version.

2.3.20 PJ[7:6] / KWJ[7:6] — Port J I/O Pins [7:6]

PJ[7:6] are general purpose input or output pins, shared with the keypad interrupt function. When configured as inputs, they can generate interrupts causing the MCU to exit STOP or WAIT mode. These pins are not available in the 48 pin package version nor in the 52 pin package version.

2.3.21 PM5 / SCK — Port M I/O Pin 5

PM5 is a general purpose input or output pin and also the serial clock pin SCK for the Serial Peripheral Interface (SPI).

2.3.22 PM4 / MOSI — Port M I/O Pin 4

PM4 is a general purpose input or output pin and also the master output (during master mode) or slave input (during slave mode) pin for the Serial Peripheral Interface (SPI).

2.3.23 PM3 / \overline{SS} — Port M I/O Pin 3

PM3 is a general purpose input or output pin and also the slave select pin \overline{SS} for the Serial Peripheral Interface (SPI).

2.3.24 PM2 / MISO — Port M I/O Pin 2

PM2 is a general purpose input or output pin and also the master input (during master mode) or slave output (during slave mode) pin for the Serial Peripheral Interface (SPI).

2.3.25 PM1 / TXCAN — Port M I/O Pin 1

PM1 is a general purpose input or output pin and the transmit pin, TXCAN, of the CAN module if available.

2.3.26 PM0 / RXCAN — Port M I/O Pin 0

PM0 is a general purpose input or output pin and the receive pin, RXCAN, of the CAN module if available.

2.3.27 PS[3:2] — Port S I/O Pins [3:2]

PS3 and PS2 are general purpose input or output pins. These pins are not available in the 48 / 52 pin package versions.

2.3.28 PS1 / TXD — Port S I/O Pin 1

PS1 is a general purpose input or output pin and the transmit pin, TXD, of Serial Communication Interface (SCI).

2.3.29 PS0 / RXD — Port S I/O Pin 0

PS0 is a general purpose input or output pin and the receive pin, RXD, of Serial Communication Interface (SCI).

2.3.30 PPT[7:5] / IOC[7:5] — Port T I/O Pins [7:5]

PT7-PT5 are general purpose input or output pins. They can also be configured as the timer system input capture or output compare pins IOC7-IOC5.

2.3.31 PT[4:0] / IOC[4:0] / PW[4:0]— Port T I/O Pins [4:0]

PT4-PT0 are general purpose input or output pins. They can also be configured as the timer system input capture or output compare pins IOC4-IOC0 or as the PWM outputs PW[4:0].

2.4 Power Supply Pins

2.4.1 VDDX, VSSX — Power & Ground Pins for I/O Drivers

External power and ground for I/O drivers. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.2 VDDR, VSSR — Power & Ground Pins for I/O Drivers & for Internal Voltage Regulator

External power and ground for the internal voltage regulator. Connecting VDDR to ground disables the internal voltage regulator.

2.4.3 VDD1, VDD2, VSS1, VSS2 — Internal Logic Power Pins

Power is supplied to the MCU through VDD and VSS. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if VDDR is tied to ground.

2.4.4 VDDA, VSSA — Power Supply Pins for ATD and VREG

VDDA, VSSA are the power supply and ground input pins for the voltage regulator reference and the analog to digital converter.

2.4.5 VRH, VRL — ATD Reference Voltage Input Pins

VRH and VRL are the reference voltage input pins for the analog to digital converter.

2.4.6 VDDPLL, VSSPLL — Power Supply Pins for PLL

Provides operating voltage and ground for the Oscillator and the Phased-Locked Loop. This allows the supply voltage to the Oscillator and PLL to be bypassed independently. This 2.5V voltage is generated by the internal voltage regulator.

Table 2-2 MC9S12C-Family Power and Ground Connection Summary

| Mnemonic | Nominal Voltage | Description |
|--------------|-----------------|--|
| VDD1 VDD2 | 2.5 V | Internal power and ground generated by internal regulator. These also allow an external source to supply the core VDD/VSS voltages and bypass the internal voltage regulator. In the 48 and 52 LQFP packages VDD2 and VSS2 are not available. |
| VSS1 VSS2 | 0V | |
| VDDR | 5.0 V | External power and ground, supply to internal voltage regulator. |
| VSSR | 0 V | |
| VDDX | 5.0 V | External power and ground, supply to pin drivers. |
| VSSX | 0 V | |
| VDDA | 5.0 V | Operating voltage and ground for the analog-to-digital converters and the reference for the internal voltage regulator, allows the supply voltage to the A/D to be bypassed independently. |
| VSSA | 0 V | |
| VRH | 5.0 V | Reference voltage low for the ATD converter. In the 48 and 52 LQFP packages VRL is bonded to VSSA. |
| VRL | 0 V | |
| VDDPLL | 2.5 V | Provides operating voltage and ground for the Phased-Locked Loop. This allows the supply voltage to the PLL to be bypassed independently. Internal power and ground generated by internal regulator. |
| VSSPLL | 0 V | |

NOTE: All VSS pins must be connected together in the application. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on MCU pin load.

Section 3 System Clock Description

The Clock and Reset Generator provides the internal clock signals for the core and all peripheral modules. **Figure 3-1** shows the clock connections from the CRG to all modules. Consult the CRG Block User Guide for details on clock generation.

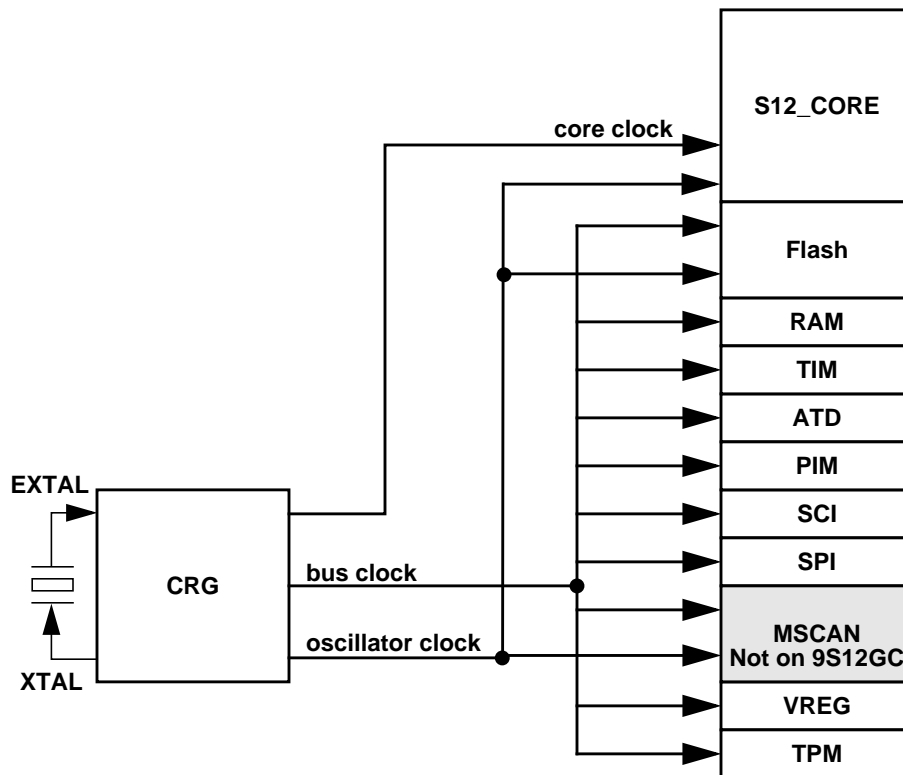


Figure 3-1 Clock Connections

Section 4 Modes of Operation

4.1 Overview

Eight possible modes determine the operating configuration of the MC9S12C Family. Each mode has an associated default memory map and external bus configuration controlled by a further pin.

Three low power modes exist for the device.

4.2 Chip Configuration Summary

The operating mode out of reset is determined by the states of the MODC, MODB, and MODA pins during reset. The MODC, MODB, and MODA bits in the MODE register show the current operating mode and provide limited mode switching during operation. The states of the MODC, MODB, and MODA pins are

latched into these bits on the rising edge of the reset signal. The ROMCTL signal allows the setting of the ROMON bit in the MISC register thus controlling whether the internal Flash is visible in the memory map. ROMON = 1 mean the Flash is visible in the memory map. The state of the ROMCTL pin is latched into the ROMON bit in the MISC register on the rising edge of the reset signal.

Table 4-1 Mode Selection

| BKGD = MODC | PE6 = MODB | PE5 = MODA | PP6 = ROMCTL | ROMON Bit | Mode Description |
|-------------|------------|------------|--------------|-----------|---|
| 0 | 0 | 0 | X | 1 | Special Single Chip, BDM allowed and ACTIVE. BDM is allowed in all other modes but a serial command is required to make BDM active. |
| 0 | 0 | 1 | 0 | 1 | Emulation Expanded Narrow, BDM allowed |
| | | | 1 | 0 | |
| 0 | 1 | 0 | X | 0 | Special Test (Expanded Wide), BDM allowed |
| 0 | 1 | 1 | 0 | 1 | Emulation Expanded Wide, BDM allowed |
| | | | 1 | 0 | |
| 1 | 0 | 0 | X | 1 | Normal Single Chip, BDM allowed |
| 1 | 0 | 1 | 0 | 0 | Normal Expanded Narrow, BDM allowed |
| | | | 1 | 1 | |
| 1 | 1 | 0 | X | 1 | Peripheral; BDM allowed but bus operations would cause bus conflicts (must not be used) |
| 1 | 1 | 1 | 0 | 0 | Normal Expanded Wide, BDM allowed |
| | | | 1 | 1 | |

For further explanation on the modes refer to the S12_MEBI block guide.

Table 4-2 Clock Selection Based on PE7

| PE7 = XCLKS | Description |
|-------------|---|
| 1 | Colpitts Oscillator selected |
| 0 | Pierce Oscillator/external clock selected |

4.3 Security

The device will make available a security feature preventing the unauthorized read and write of the memory contents. This feature allows:

- Protection of the contents of FLASH,
- Operation in single-chip mode,
- Operation from external memory with internal FLASH disabled.

The user must be reminded that part of the security must lie with the user’s code. An extreme example would be user’s code that dumps the contents of the internal program. This code would defeat the purpose of security. At the same time the user may also wish to put a back door in the user’s program. An example

of this is the user downloads a key through the SCI which allows access to a programming routine that updates parameters.

4.3.1 Securing the Microcontroller

Once the user has programmed the FLASH, the part can be secured by programming the security bits located in the FLASH module. These non-volatile bits will keep the part secured through resetting the part and through powering down the part.

The security byte resides in a portion of the Flash array.

Check the Flash Block User Guide for more details on the security configuration.

4.3.2 Operation of the Secured Microcontroller

4.3.2.1 Normal Single Chip Mode

This will be the most common usage of the secured part. Everything will appear the same as if the part was not secured with the exception of BDM operation. The BDM operation will be blocked.

4.3.2.2 Executing from External Memory

The user may wish to execute from external space with a secured microcontroller. This is accomplished by resetting directly into expanded mode. The internal FLASH will be disabled. BDM operations will be blocked.

4.3.3 Unsecuring the Microcontroller

In order to unsecure the microcontroller, the internal FLASH must be erased. This can be done through an external program in expanded mode or via a sequence of BDM commands. Unsecuring is also possible via the Backdoor Key Access. Refer to Flash Block Guide for details.

Once the user has erased the FLASH, the part can be reset into special single chip mode. This invokes a program that verifies the erasure of the internal FLASH. Once this program completes, the user can erase and program the FLASH security bits to the unsecured state. This is generally done through the BDM, but the user could also change to expanded mode (by writing the mode bits through the BDM) and jumping to an external program (again through BDM commands). Note that if the part goes through a reset before the security bits are reprogrammed to the unsecure state, the part will be secured again.

4.4 Low Power Modes

The microcontroller features three main low power modes. Consult the respective Block User Guide for information on the module behavior in Stop, Pseudo Stop, and Wait Mode. An important source of information about the clock system is the Clock and Reset Generator User Guide (CRG).

4.4.1 Stop

Executing the CPU STOP instruction stops all clocks and the oscillator thus putting the chip in fully static mode. Wake up from this mode can be done via reset or external interrupts.

4.4.2 Pseudo Stop

This mode is entered by executing the CPU STOP instruction. In this mode the oscillator is still running and the Real Time Interrupt (RTI) or Watchdog (COP) sub module can stay active. Other peripherals are turned off. This mode consumes more current than the full STOP mode, but the wake up time from this mode is significantly shorter.

4.4.3 Wait

This mode is entered by executing the CPU WAI instruction. In this mode the CPU will not execute instructions. The internal CPU signals (address and databus) will be fully static. All peripherals stay active. For further power consumption reduction the peripherals can individually turn off their local clocks.

4.4.4 Run

Although this is not a low power mode, unused peripheral modules should not be enabled in order to save power.

Section 5 Resets and Interrupts

5.1 Overview

Consult the Exception Processing section of the CPU12 Reference Manual for information.

5.2 Vectors

5.2.1 Vector Table

Table 5-1 lists interrupt sources and vectors in default order of priority.

Table 5-1 Interrupt Vector Locations

| Vector Address | Interrupt Source | CCR Mask | Local Enable | HPRIO Value to Elevate |
|----------------|--|----------|--------------------|------------------------|
| \$FFFE, \$FFFF | External Reset, Power On Reset or Low Voltage Reset (see CRG Flags Register to determine reset source) | None | None | – |
| \$FFFC, \$FFFD | Clock Monitor fail reset | None | COPCTL (CME, FCME) | – |
| \$FFFA, \$FFFB | COP failure reset | None | COP rate select | – |
| \$FFF8, \$FFF9 | Unimplemented instruction trap | None | None | – |

| | | | | |
|------------------|------------------------------|-------|----------------------------------|------|
| \$FFF6, \$FFF7 | SWI | None | None | – |
| \$FFF4, \$FFF5 | XIRQ | X-Bit | None | – |
| \$FFF2, \$FFF3 | IRQ | I-Bit | INTCR (IRQEN) | \$F2 |
| \$FFF0, \$FFF1 | Real Time Interrupt | I-Bit | CRGINT (RTIE) | \$F0 |
| \$FFEE, \$FFEF | Standard Timer channel 0 | I-Bit | TIE (C0I) | \$EE |
| \$FFEC, \$FFED | Standard Timer channel 1 | I-Bit | TIE (C1I) | \$EC |
| \$FFEA, \$FFEB | Standard Timer channel 2 | I-Bit | TIE (C2I) | \$EA |
| \$FFE8, \$FFE9 | Standard Timer channel 3 | I-Bit | TIE (C3I) | \$E8 |
| \$FFE6, \$FFE7 | Standard Timer channel 4 | I-Bit | TIE (C4I) | \$E6 |
| \$FFE4, \$FFE5 | Standard Timer channel 5 | I-Bit | TIE (C5I) | \$E4 |
| \$FFE2, \$FFE3 | Standard Timer channel 6 | I-Bit | TIE (C6I) | \$E2 |
| \$FFE0, \$FFE1 | Standard Timer channel 7 | I-Bit | TIE (C7I) | \$E0 |
| \$FFDE, \$FFDF | Standard Timer overflow | I-Bit | TMSK2 (TOI) | \$DE |
| \$FFDC, \$FFDD | Pulse accumulator A overflow | I-Bit | PACTL (PAOVI) | \$DC |
| \$FFDA, \$FFDB | Pulse accumulator input edge | I-Bit | PACTL (PAI) | \$DA |
| \$FFD8, \$FFD9 | SPI | I-Bit | SPICR1 (SPIE, SPTIE) | \$D8 |
| \$FFD6, \$FFD7 | SCI | I-Bit | SCICR2 (TIE, TCIE, RIE, ILIE) | \$D6 |
| \$FFD4, \$FFD5 | Reserved | | | |
| \$FFD2, \$FFD3 | ATD | I-Bit | ATDCTL2 (ASCIE) | \$D2 |
| \$FFD0, \$FFD1 | Reserved | | | |
| \$FFCE, \$FFCF | Port J | I-Bit | PIEP (PIEP7-6) | \$CE |
| \$FFCC, \$FFCD | Reserved | | | |
| \$FFCA, \$FFCB | Reserved | | | |
| \$FFC8, \$FFC9 | Reserved | | | |
| \$FFC6, \$FFC7 | CRG PLL lock | I-Bit | PLLCR (LOCKIE) | \$C6 |
| \$FFC4, \$FFC5 | CRG Self Clock Mode | I-Bit | PLLCR (SCMIE) | \$C4 |
| \$FFBA to \$FFC3 | Reserved | | | |
| \$FFB8, \$FFB9 | FLASH | I-Bit | FCNFG (CCIE, CBEIE) | \$B8 |
| \$FFB6, \$FFB7 | CAN wake-up ¹ | I-Bit | CANRIER (WUPIE) | \$B6 |
| \$FFB4, \$FFB5 | CAN errors ¹ | I-Bit | CANRIER (CSCIE, OVRIE) | \$B4 |
| \$FFB2, \$FFB3 | CAN receive ¹ | I-Bit | CANRIER (RXFIE) | \$B2 |
| \$FFB0, \$FFB1 | CAN transmit ¹ | I-Bit | CANTIER (TXEIE[2:0]) | \$B0 |
| \$FF90 to \$FFAF | Reserved | | | |
| \$FF8E, \$FF8F | Port P | I-Bit | PIEP (PIEP7-0) | \$8E |
| \$FF8C, \$FF8D | PWM Emergency Shutdown | I-Bit | PWMSDN(PWMIE) | \$8C |
| \$FF8A, \$FF8B | VREG LVI | I-Bit | CTRL0 (LVIE) | \$8A |
| \$FF80 to \$FF89 | Reserved | | | |

NOTES:

1. Not available on MC9S12GC-Family members

5.3 Resets

Resets are a subset of the interrupts featured in **Table 5-1**. The different sources capable of generating a system reset are summarized in **Table 5-2**. When a reset occurs, MCU registers and control bits are

changed to known start-up states. Refer to the respective module Block User Guides for register reset states.

5.3.1 Reset Summary Table

Table 5-2 Reset Summary

| Reset | Priority | Source | Vector |
|---------------------|----------|-------------|----------------|
| Power-on Reset | 1 | CRG Module | \$FFFE, \$FFFF |
| External Reset | 1 | RESET pin | \$FFFE, \$FFFF |
| Low Voltage Reset | 1 | VREG Module | \$FFFE, \$FFFF |
| Clock Monitor Reset | 2 | CRG Module | \$FFFC, \$FFFD |
| COP Watchdog Reset | 3 | CRG Module | \$FFFA, \$FFFB |

5.3.2 Effects of Reset

When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective module Block User Guides for register reset states. Refer to the HCS12 Multiplexed External Bus Interface (MEBI) Block Guide for mode dependent pin configuration of port A, B and E out of reset.

Refer to the PIM Block User Guide for reset configurations of all peripheral module ports.

Refer to **Figure 1-2** to **Figure 1-5** footnotes for locations of the memories depending on the operating mode after reset.

The RAM array is not automatically initialized out of reset.

NOTE: For devices assembled in 48-pin or 52-pin LQFP packages all non-bonded out pins should be configured as outputs after reset in order to avoid current drawn from floating inputs. Refer to **Table 2-1** for affected pins.

Section 6 HCS12 Core Block Description

Consult the individual block guides for information about the HCS12 core modules, i.e. central processing unit (CPU), interrupt module (INT), module mapping control module (MMC), multiplexed external bus interface (MEBI), debug12 module (DBG12) and background debug mode module (BDM).

Where the CPU12 Reference Manual refers to cycles this is equivalent to device bus clock periods.

6.1 Device-specific information

6.1.1 PPAGE

External paging is not supported on these devices. In order to access the 16K flash blocks in the address range \$8000-\$BFFF the PPAGE register must be loaded with the corresponding value for this range. Refer to **Table 6-1** for device specific page mapping.

For all devices Flash Page 3F is visible in the \$C000-\$FFFF range if ROMON is set. For all devices (except 9S12GC16) Page 3E is also visible in the \$4000-\$7FFF range if ROMHM is cleared and ROMON is set. For all devices apart from MC9S12C32 Flash Page 3D is visible in the \$0000-\$3FFF range if ROMON is set...

Table 6-1 Device Specific Flash PAGE Mapping

| Device | PAGE | PAGE visible with PPAGE contents |
|---------------------------|------|---|
| MC9S12GC16 | 3F | \$00,\$01,\$02,\$03,\$04,\$05,\$06,\$07,\$08,\$09.....\$36,\$37,\$38,\$39,\$3A,\$3B,\$3C,\$3D,\$3E,\$3F |
| MC9S12C32 | 3E | \$00,\$02,\$04,\$06,\$08,\$0A,\$0C,\$0E,\$10,\$12.....\$2C,\$2E,\$30,\$32,\$34,\$36,\$38,\$3A,\$3C,\$3E |
| MC9S12C32 | 3F | \$01,\$03,\$05,\$07,\$09,\$0B,\$0D,\$0F,\$11,\$13.....\$2D,\$2F,\$31,\$33,\$35,\$37,\$39,\$3B,\$3D,\$3F |
| MC9S12C64 MC9S12GC64 | 3C | \$00,\$04,\$08,\$0C,\$10,\$14,\$18,\$1C,\$20,\$24,\$28,\$2C,\$30,\$34,\$38,\$3C |
| | 3D | \$01,\$05,\$09,\$0D,\$11,\$15,\$19,\$1D,\$21,\$25,\$29,\$2D,\$31,\$35,\$39,\$3D |
| | 3E | \$02,\$06,\$0A,\$0E,\$12,\$16,\$1A,\$1E,\$22,\$26,\$2A,\$2E,\$32,\$36,\$3A,\$3E |
| | 3F | \$03,\$07,\$0B,\$0F,\$13,\$17,\$1B,\$1F,\$23,\$27,\$2B,\$2F,\$33,\$37,\$3B,\$3F |
| MC9S12C96 | 3A | \$00,\$02,\$08,\$0A,\$10,\$12,\$18,\$1A,\$20,\$22,\$28,\$2A,\$30,\$32,\$38,\$3A |
| | 3B | \$01,\$03,\$09,\$0B,\$11,\$13,\$19,\$1B,\$21,\$23,\$29,\$2B,\$31,\$33,\$39,\$3B |
| | 3C | \$04,\$0C,\$14,\$1C,\$24,\$2C,\$34,\$3C |
| | 3D | \$05,\$0D,\$15,\$1D,\$25,\$2D,\$35,\$3D |
| | 3E | \$06,\$0E,\$16,\$1E,\$26,\$2E,\$36,\$3E |
| | 3F | \$07,\$0F,\$17,\$1F,\$27,\$2F,\$37,\$3F |
| MC9S12C128 MC9S12GC128 | 38 | \$00,\$08,\$10,\$18,\$20,\$28,\$30,\$38 |
| | 39 | \$01,\$09,\$11,\$19,\$21,\$29,\$31,\$39 |
| | 3A | \$02,\$0A,\$12,\$1A,\$22,\$2A,\$32,\$3A |
| | 3B | \$03,\$0B,\$13,\$1B,\$23,\$2B,\$33,\$3B |
| | 3C | \$04,\$0C,\$14,\$1C,\$24,\$2C,\$34,\$3C |
| | 3D | \$05,\$0D,\$15,\$1D,\$25,\$2D,\$35,\$3D |
| | 3E | \$06,\$0E,\$16,\$1E,\$26,\$2E,\$36,\$3E |
| | 3F | \$07,\$0F,\$17,\$1F,\$27,\$2F,\$37,\$3F |

6.1.2 BDM alternate clock

The BDM section of S12 Core User Guide reference to alternate clock is equivalent to oscillator clock.

6.1.3 Extended Address Range Emulation Implications

In order to emulate the MC9S12GC or MC9S12C-Family devices, external addressing of a 128K memory map is required. This is provided in a 112 LQFP package version which includes the 3 necessary extra external address bus signals via PortK[2:0]. This package version is for emulation only and not provided as a general production package.

The reset state of DDRK is \$00, configuring the pins as inputs.

The reset state of PUPKE in the PUCR register is “1” enabling the internal PortK pullups.

In this reset state the pull-ups provide a defined state and prevent a floating input, thereby preventing unnecessary current flow at the input stage.

To prevent unnecessary current flow in production package options, the states of DDRK and PUPKE should not be changed by software.

Section 7 Voltage Regulator (VREG) Block Description

Consult the VREG Block User Guide for information about the dual output linear voltage regulator.

7.1 Device-specific information

The VREG is part of the IPBus domain.

7.1.1 VREGEN

VREGEN is connected internally to VDDR.

7.1.2 VDD1, VDD2, VSS1, VSS2

In the 80 pin QFP package versions, both internal VDD and VSS of the 2.5V domain are bonded out on 2 sides of the device as two pin pairs (VDD1, VSS1 & VDD2, VSS2). VDD1 and VDD2 are connected together internally. VSS1 and VSS2 are connected together internally.

The extra pin pair enables systems using the 80 pin package to employ better supply routing and further decoupling.

Section 8 Recommended Printed Circuit Board Layout

The PCB must be carefully laid out to ensure proper operation of the voltage regulator as well as of the MCU itself. The following rules must be observed:

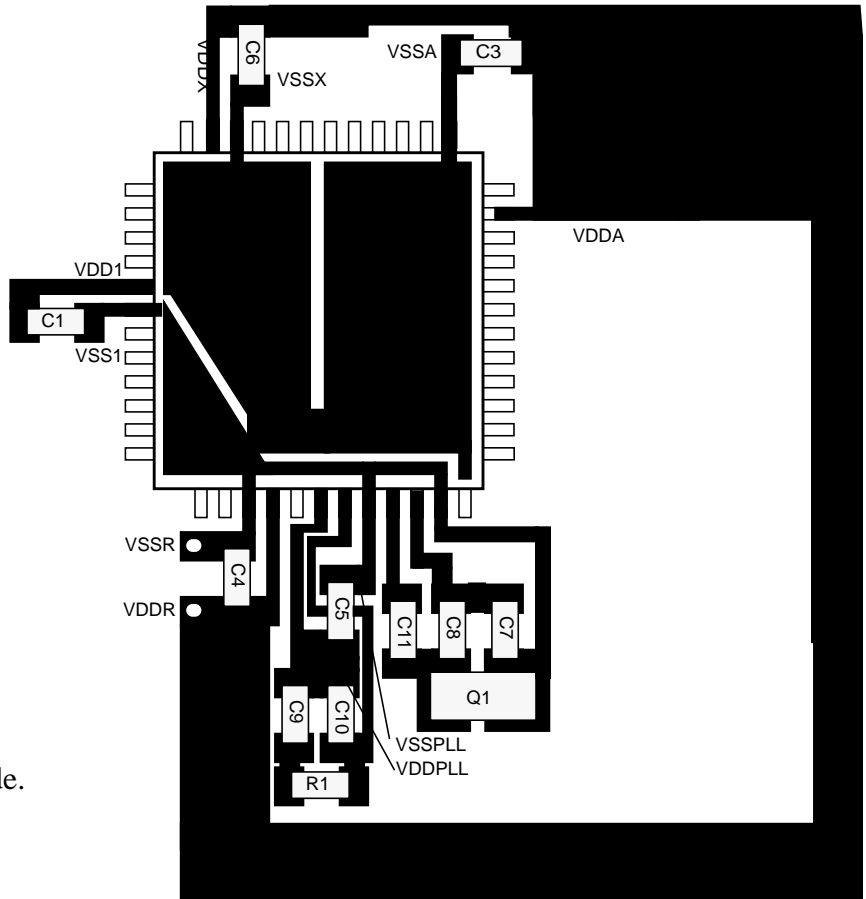
- Every supply pair must be decoupled by a ceramic capacitor connected as near as possible to the corresponding pins (C1 - C6).
- Central point of the ground star should be the VSSR pin.
- Use low ohmic low inductance connections between VSS1, VSS2 and VSSR.
- VSSPLL must be directly connected to VSSR.
- Keep traces of VSSPLL, EXTAL and XTAL as short as possible and occupied board area for C7, C8, C11 and Q1 as small as possible.
- Do not place other signals or supplies underneath area occupied by C7, C8, C10 and Q1 and the connection area to the MCU.
- Central power input should be fed in at the VDDA/VSSA pins.

Table 8-1 Recommended External Component Values

| Component | Purpose | Type | Value |
|---------------------|-------------------------------------|---|---------------------------|
| C1 | VDD1 filter capacitor | ceramic X7R | 220nF, 470nF ¹ |
| C2 | VDD2 filter capacitor (80 QFP only) | ceramic X7R | 220nF |
| C3 | VDDA filter capacitor | ceramic X7R | 100nF |
| C4 | VDDR filter capacitor | X7R/tantalum | >=100nF |
| C5 | VDDPLL filter capacitor | ceramic X7R | 100nF |
| C6 | VDDX filter capacitor | X7R/tantalum | >=100nF |
| C7 | OSC load capacitor | See PLL specification chapter | |
| C8 | OSC load capacitor | | |
| C9 | PLL loop filter capacitor | See PLL specification chapter | |
| C10 | PLL loop filter capacitor | | |
| C11 | DC cutoff capacitor | Colpitts mode only, if recommended by quartz manufacturer | |
| R1 | PLL loop filter resistor | See PLL Specification chapter | |
| R2 / R _B | PLL loop filter resistor | Pierce mode only | |
| R3 / R _S | PLL loop filter resistor | | |
| Q1 | Quartz | | |

NOTES:

1. In 48LQFP and 52LQFP package versions, VDD2 is not available. Thus 470nF must be connected to VDD1.



Note:
Oscillator in
Colpitts mode.

Figure 8-1 Recommended PCB Layout (48 LQFP)

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NOTE: Oscillator in Colpitts mode.

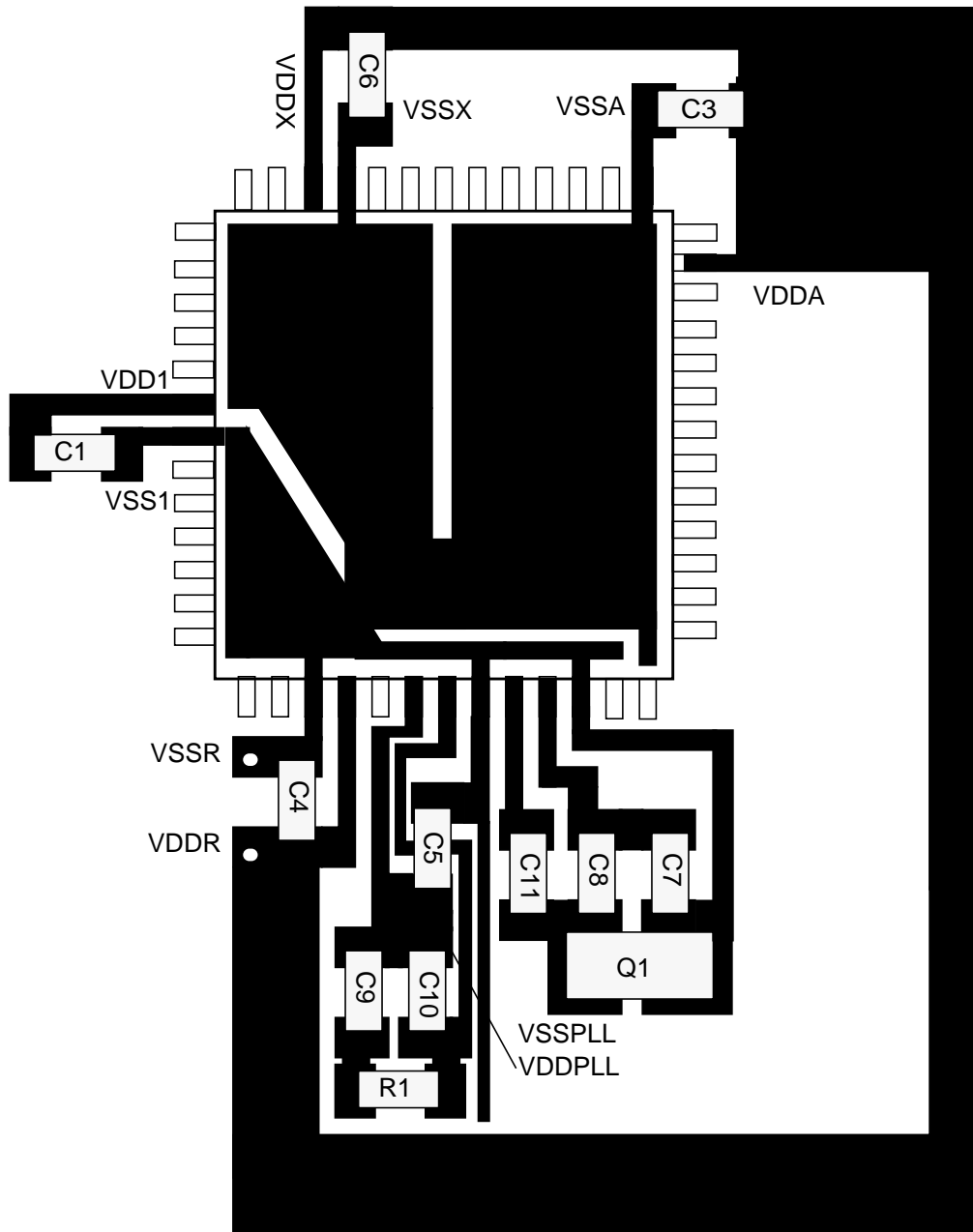


Figure 8-2 Recommended PCB Layout (52 LQFP)

)
 NOTE: Oscillator in Colpitts mode.

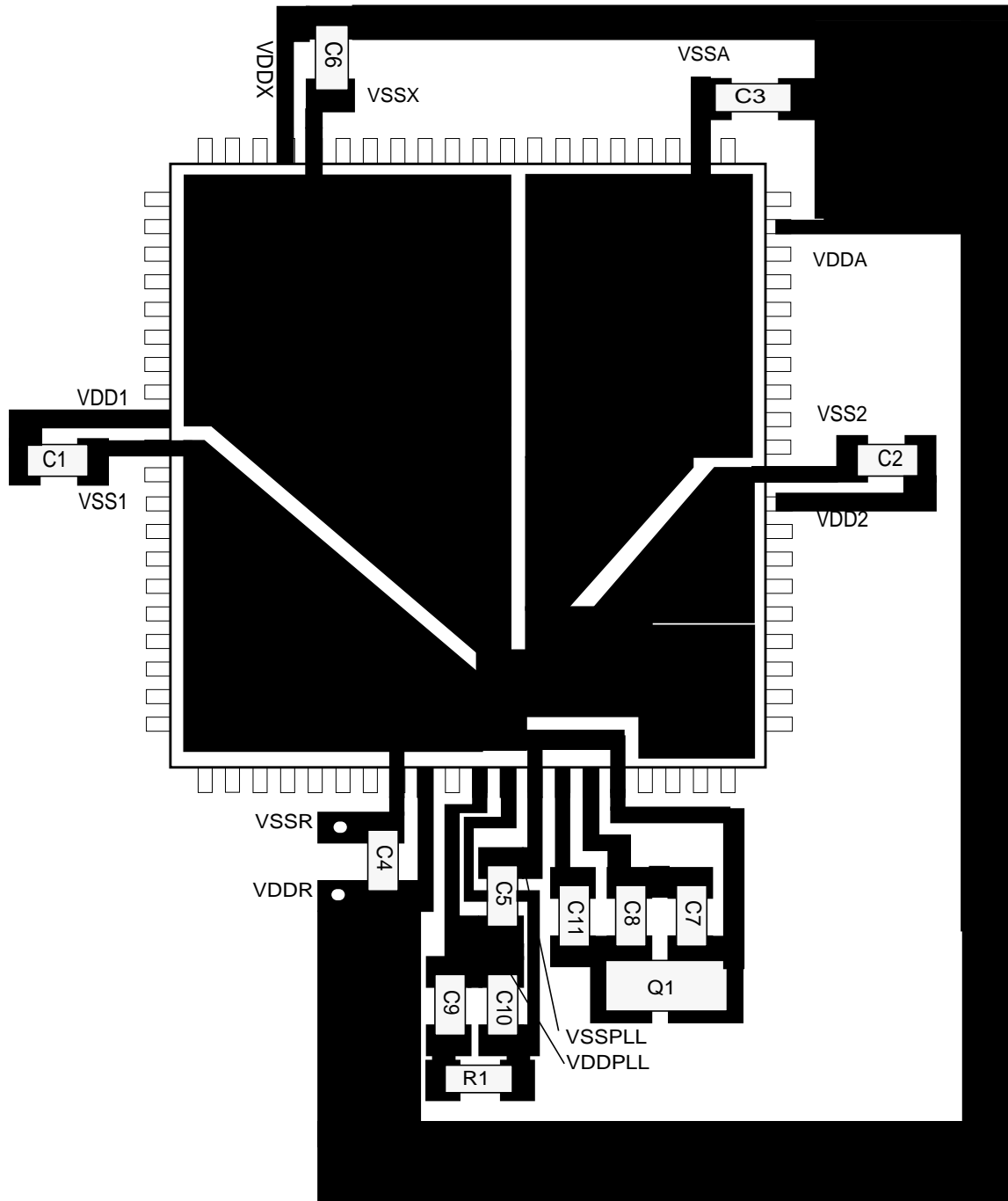


Figure 8-3 Recommended PCB Layout (80 QFP)

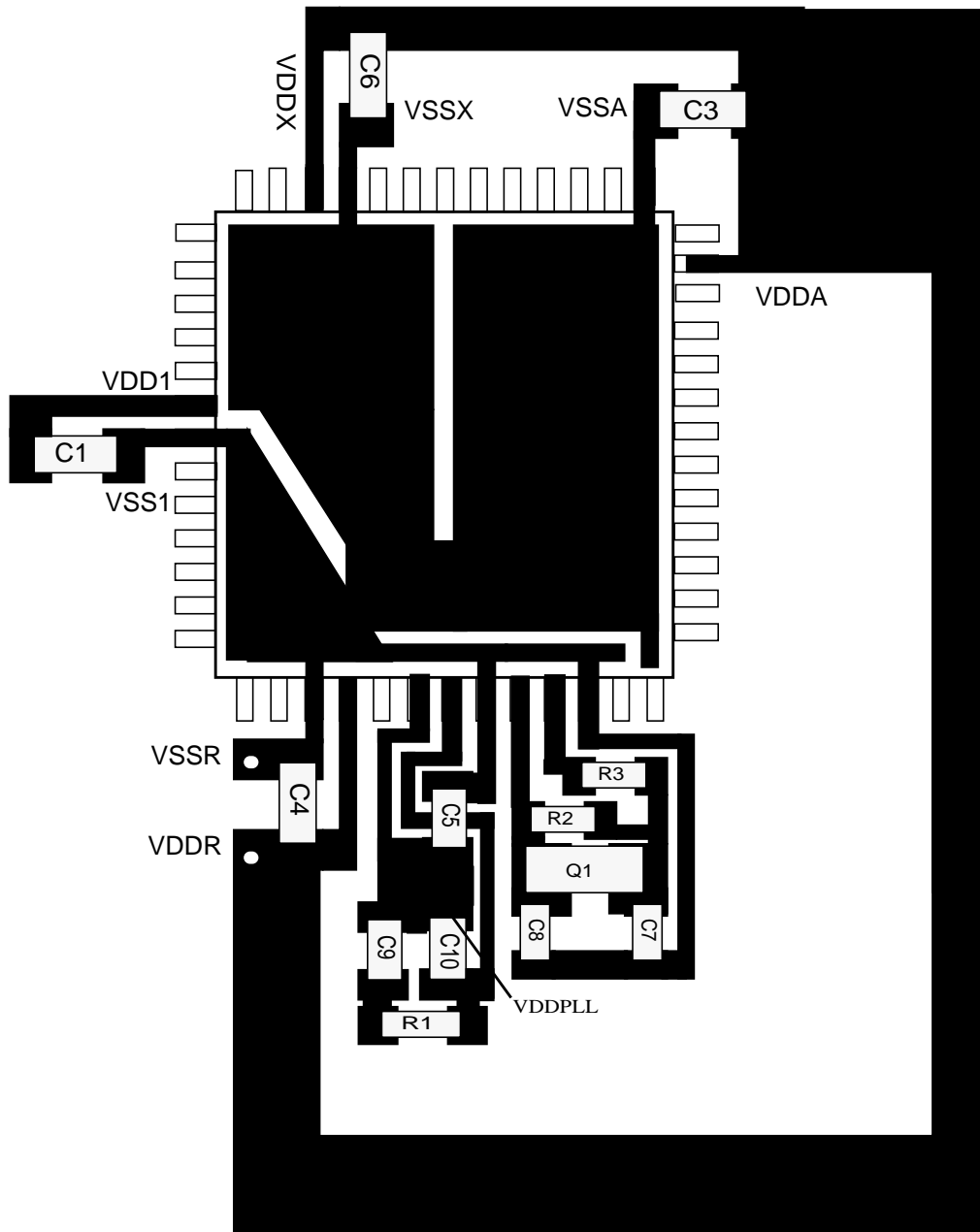


Figure 8-4 Recommended PCB Layout for 48 LQFP Pierce Oscillator

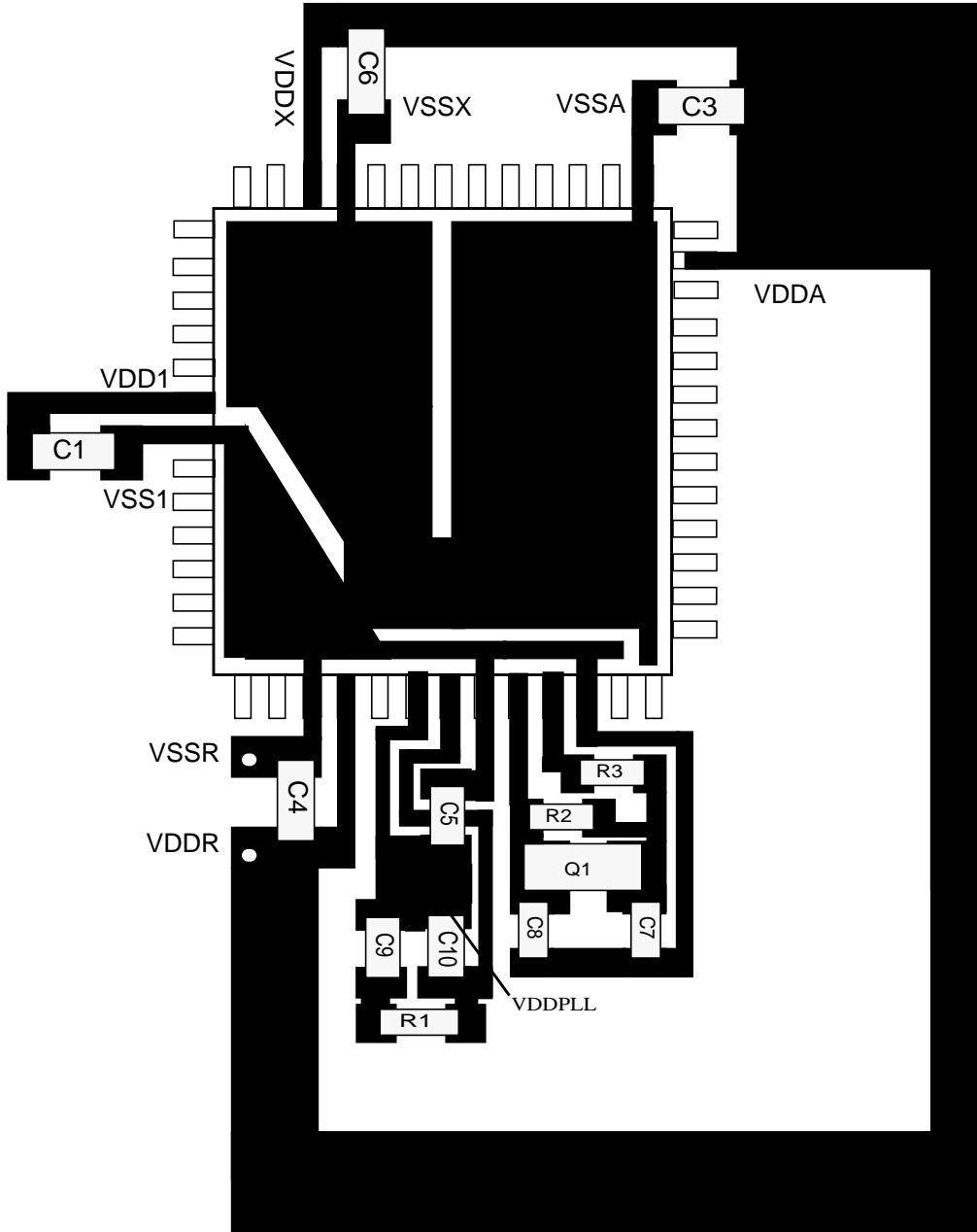


Figure 8-5 Recommended PCB Layout for 52 LQFP Pierce Oscillator

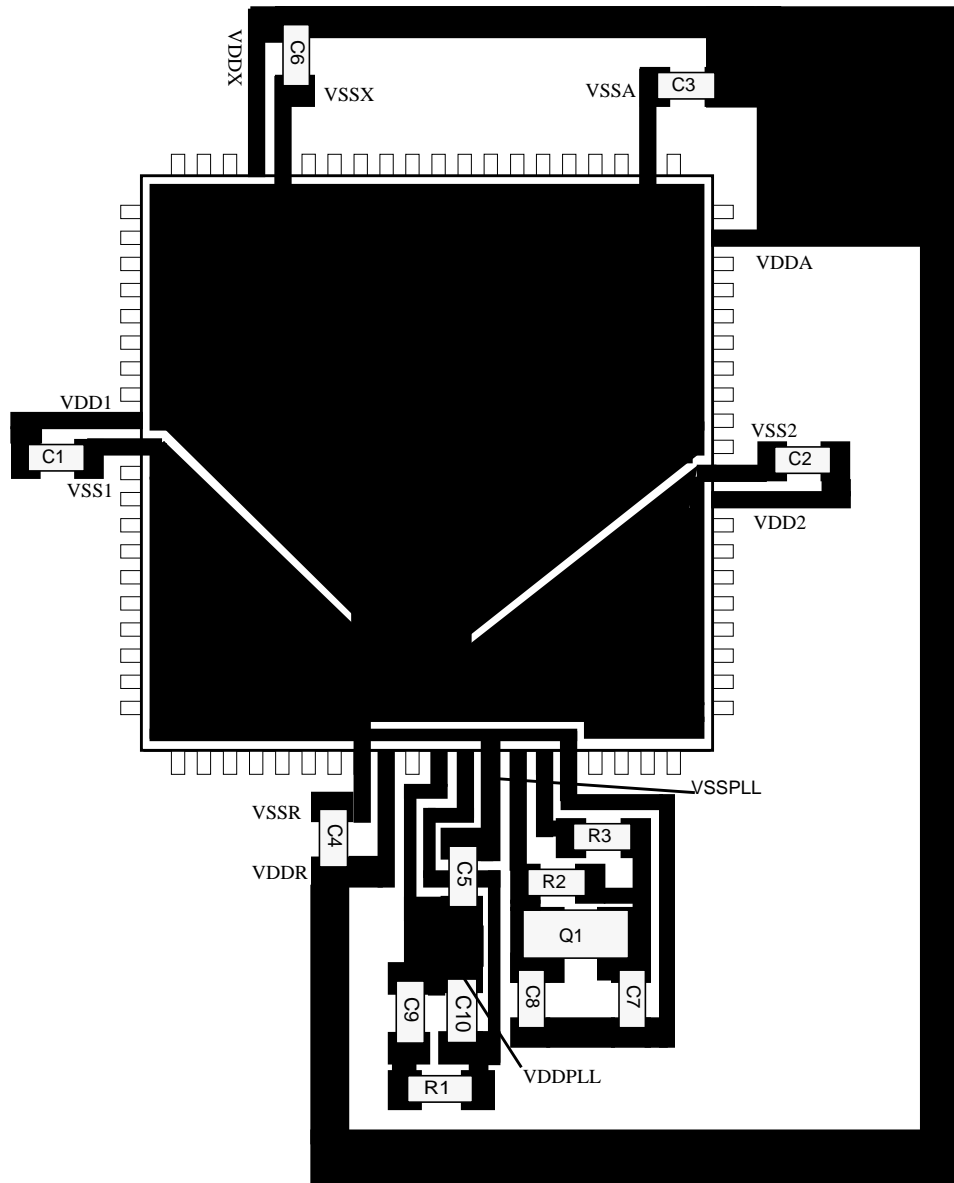


Figure 8-6 Recommended PCB Layout for 80QFP Pierce Oscillator

Section 9 Clock Reset Generator (CRG) Block Description

Consult the CRG Block User Guide for information about the Clock and Reset Generator module.

9.1 Device-specific information

The CRG is part of the IPBus domain.

The Low Voltage Reset feature uses the low voltage reset signal from the VREG module as an input to the CRG module. When the regulator output voltage supply to the internal chip logic falls below a specified threshold the LVR signal from the VREG module causes the CRG module to generate a reset. Consult the VREG Block User Guide for voltage level specifications.

9.1.1 $\overline{\text{XCLKS}}$

The $\overline{\text{XCLKS}}$ input signal is active low (see **2.3.8 PE7 / NOACC / XCLKS — Port E I/O Pin 7**).

Section 10 Oscillator (OSC) Block Description

Consult the OSC Block User Guide for information about the Oscillator module.

Section 11 Timer (TIM) Block Description

Consult the TIM_16B8C Block User Guide for information about the Timer module.

Section 12 Analog to Digital Converter (ATD) Block Description

12.1 Device-specific information

12.1.1 VRL (voltage reference low)

In the 48 and 52 pin package versions, the VRL pad is bonded internally to the VSSA pin.

Consult the ATD_10B8C Block User Guide for further information about the A/D Converter module.

Section 13 Serial Communications Interface (SCI) Block Description

Consult the SCI Block User Guide for information about the Asynchronous Serial Communications Interface module.

Section 14 Serial Peripheral Interface (SPI) Block Description

Consult the SPI Block User Guide for information about the Serial Peripheral Interface module.

Consult the SPI Block User Guide for information about the Synchronous Serial Communications Interface module.

Section 15 Flash Block Description

Consult the FTS16K Block User Guide for information about the Flash module for the MC9S12GC16.

Consult the FTS32K Block User Guide for information about the Flash module for the MC9S12C32 or MC9S12GC32.

Consult the FTS64K Block User Guide for information about the Flash module for the MC9S12C64 or MC9S12GC64.

Consult the FTS96K Block User Guide for information about the Flash module for the MC9S12C96.

Consult the FTS128K Block User Guide for information about the Flash module for the MC9S12C128 or MC9S12GC128.

Section 16 RAM Block Description

This module supports single-cycle misaligned word accesses without wait states.

The MC912GC16 features a single 1K byte RAM module.

The MC9S12C32 and MC9S12GC32 feature a 2K byte RAM module.

The MC9S12C64, MC9S12GC64, MC9S12C96, MC9S12C128 and MC9S12GC128 versions feature a 4K byte RAM module.

Section 17 Pulse Width Modulator (PWM) Block Description

Consult the PWM_8B6C Block User Guide for information about the Pulse Width Modulator Module.

Section 18 MSCAN Block Description

Consult the MSCAN Block User Guide for information about the Motorola Scalable CAN Module. This module is not available on the MC9GC-Family Members.

Section 19 Port Integration Module (PIM) Block Description

Consult the PIM_9C32 Block User Guide for information about the Port Integration Module for all versions of the MC9DS12GC and MC9S12C-Family.

The MODRR register within the PIM allows for mapping of PWM channels to PortT in the absence of PortP pins for the low pin count packages. For the 80QFP package option it is recommended not to use MODRR since this is intended to support PWM channel availability in low pin count packages. Note that when mapping PWM channels to PortT in an 80QFP option, the associated PWM channels are then mapped to both PortP and PortT.

Appendix A Electrical Characteristics

A.1 General

NOTE: *The electrical characteristics given in this section are preliminary and should be used as a guide only. Values cannot be guaranteed by Motorola and are subject to change without notice.*

NOTE: *The parts are specified and tested over the 5V and 3.3V ranges. For the intermediate range, generally the electrical specifications for the 3.3V range apply, but the parts are not tested in production test in the intermediate range.*

This supplement contains the most accurate electrical information for the MC9S12C-Family microcontrollers available at the time of publication. The information should be considered **PRELIMINARY** and is subject to change.

This introduction is intended to give an overview on several common topics like power supply, current injection etc.

A.1.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate.

NOTE: *This classification will be added at a later release of the specification*

P: Those parameters are guaranteed during production testing on each individual device.

C: Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. They are regularly verified by production monitors.

T: Those parameters are achieved by design characterization on a small sample size from typical devices. All values shown in the typical column are within this category.

D: Those parameters are derived mainly from simulations.

A.1.2 Power Supply

The MC9S12C-Family and MC9S12GC-Family members utilize several pins to supply power to the I/O ports, A/D converter, oscillator and PLL as well as the internal logic.

The VDDA, VSSA pair supplies the A/D converter.

The VDDX, VSSX pair supplies the I/O pins

The VDDR, VSSR pair supplies the internal voltage regulator.

VDD1, VSS1, VDD2 and VSS2 are the supply pins for the digital logic.

VDDPLL, VSSPLL supply the oscillator and the PLL.

VSS1 and VSS2 are internally connected by metal.

VDD1 and VDD2 are internally connected by metal.

VDDA, VDDX, VDDR as well as VSSA, VSSX, VSSR are connected by anti-parallel diodes for ESD protection.

NOTE: *In the following context VDD5 is used for either VDDA, VDDR and VDDX; VSS5 is used for either VSSA, VSSR and VSSX unless otherwise noted. IDD5 denotes the sum of the currents flowing into the VDDA, VDDX and VDDR pins. VDD is used for VDD1, VDD2 and VDDPLL, VSS is used for VSS1, VSS2 and VSSPLL. IDD is used for the sum of the currents flowing into VDD1 and VDD2.*

A.1.3 Pins

There are four groups of functional pins.

A.1.3.1 5V I/O pins

Those I/O pins have a nominal level of 5V. This class of pins is comprised of all port I/O pins, the analog inputs, BKGD pin and the RESET inputs. The internal structure of all those pins is identical, however some of the functionality may be disabled. E.g. pull-up and pull-down resistors may be disabled permanently.

A.1.3.2 Analog Reference

This class is made up by the two VRH and VRL pins. In 48 and 52 pin package versions the VRL pad is bonded to the VSSA pin.

A.1.3.3 Oscillator

The pins XFC, EXTAL, XTAL dedicated to the oscillator have a nominal 2.5V level. They are supplied by VDDPLL.

A.1.3.4 TEST

This pin is used for production testing only.

A.1.4 Current Injection

Power supply must maintain regulation within operating V_{DD5} or V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD5}$) is greater than I_{DD5} , the injection current may flow out of VDD5 and could result in external power supply going out of regulation. Insure external VDD5 load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power; e.g. if no system clock is present, or if clock rate is very low which would reduce overall power consumption.

A.1.5 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation under or outside those maxima is not guaranteed. Stress beyond those limits may affect the reliability or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS5} or V_{DD5}).

Table A-1 Absolute Maximum Ratings

| Num | Rating | Symbol | Min | Max | Unit |
|-----|---|------------------|-------|------|------|
| 1 | I/O, Regulator and Analog Supply Voltage | V_{DD5} | -0.3 | 6.5 | V |
| 2 | Digital Logic Supply Voltage ¹ | V_{DD} | -0.3 | 3.0 | V |
| 3 | PLL Supply Voltage ⁽¹⁾ | V_{DDPLL} | -0.3 | 3.0 | V |
| 4 | Voltage difference VDDX to VDDR and VDDA | ΔV_{DDX} | -0.3 | 0.3 | V |
| 5 | Voltage difference VSSX to VSSR and VSSA | ΔV_{SSX} | -0.3 | 0.3 | V |
| 6 | Digital I/O Input Voltage | V_{IN} | -0.3 | 6.5 | V |
| 7 | Analog Reference | V_{RH}, V_{RL} | -0.3 | 6.5 | V |
| 8 | XFC, EXTAL, XTAL inputs | V_{ILV} | -0.3 | 3.0 | V |
| 9 | TEST input | V_{TEST} | -0.3 | 10.0 | V |
| 10 | Instantaneous Maximum Current Single pin limit for all digital I/O pins ² | I_D | -25 | +25 | mA |
| 11 | Instantaneous Maximum Current Single pin limit for XFC, EXTAL, XTAL ³ | I_{DL} | -25 | +25 | mA |
| 12 | Instantaneous Maximum Current Single pin limit for TEST ⁴ | I_{DT} | -0.25 | 0 | mA |
| 13 | Operating Temperature Range (packaged) | T_A | -40 | 125 | °C |
| 14 | Operating Temperature Range (junction) | T_J | -40 | 140 | °C |
| 15 | Storage Temperature Range | T_{stg} | -65 | 155 | °C |

NOTES:

- The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when the device is powered from an external source.
- All digital I/O pins are internally clamped to V_{SSX} and V_{DDX} , V_{SSR} and V_{DDR} or V_{SSA} and V_{DDA} .
- These pins are internally clamped to V_{SSPLL} and V_{DDPLL} .
- This pin is clamped low to V_{SSX} , but not clamped high. This pin must be tied low in applications.

A.1.6 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 Stress test qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table A-2 ESD and Latch-up Test Conditions

| Model | Description | Symbol | Value | Unit |
|------------|---|--------|-------------|------|
| Human Body | Series Resistance | R1 | 1500 | Ohm |
| | Storage Capacitance | C | 100 | pF |
| | Number of Pulse per pin positive negative | - | - 3 3 | |
| Machine | Series Resistance | R1 | 0 | Ohm |
| | Storage Capacitance | C | 200 | pF |
| | Number of Pulse per pin positive negative | - | - 3 3 | |
| Latch-up | Minimum input voltage limit | | -2.5 | V |
| | Maximum input voltage limit | | 7.5 | V |

Table A-3 ESD and Latch-Up Protection Characteristics

| Num | C | Rating | Symbol | Min | Max | Unit |
|-----|---|---|-----------|--------------|-----|------|
| 1 | C | Human Body Model (HBM) | V_{HBM} | 2000 | - | V |
| 2 | C | Machine Model (MM) | V_{MM} | 200 | - | V |
| 3 | C | Charge Device Model (CDM) | V_{CDM} | 500 | - | V |
| 4 | C | Latch-up Current at 125°C positive negative | I_{LAT} | +100 -100 | - | mA |
| 5 | C | Latch-up Current at 27°C positive negative | I_{LAT} | +200 -200 | - | mA |

A.1.7 Operating Conditions

This chapter describes the operating conditions of the devices. Unless otherwise noted those conditions apply to all the following data.

NOTE: *Instead of specifying ambient temperature all parameters are specified for the more meaningful silicon junction temperature. For power dissipation calculations refer to Section A.1.8 Power Dissipation and Thermal Characteristics.*

Table A-4 Operating Conditions

| Rating | Symbol | Min | Typ | Max | Unit |
|---|------------------|------|-----|------|------|
| I/O, Regulator and Analog Supply Voltage | V_{DD5} | 2.97 | 5 | 5.5 | V |
| Digital Logic Supply Voltage ¹ | V_{DD} | 2.35 | 2.5 | 2.75 | V |
| PLL Supply Voltage ⁽¹⁾ | V_{DDPLL} | 2.35 | 2.5 | 2.75 | V |
| Voltage Difference VDDX to VDDA | ΔV_{DDX} | -0.1 | 0 | 0.1 | V |
| Voltage Difference VSSX to VSSR and VSSA | ΔV_{SSX} | -0.1 | 0 | 0.1 | V |
| Oscillator | f_{osc} | 0.5 | - | 16 | MHz |
| Bus Frequency | f_{bus}^2 | 0.25 | - | 25 | MHz |
| Operating Junction Temperature Range | T_J | -40 | - | 140 | °C |

NOTES:

1. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when this regulator is disabled and the device is powered from an external source.
2. Some blocks e.g. ATD (conversion) and NVMs (program/erase) require higher bus frequencies for proper operation.

A.1.8 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded. The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \Theta_{JA})$$

T_J = Junction Temperature, [°C]

T_A = Ambient Temperature, [°C]

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [°C/W]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

P_{INT} = Chip Internal Power Dissipation, [W]

Two cases with internal voltage regulator enabled and disabled must be considered:

1. Internal Voltage Regulator disabled

$$P_{INT} = I_{DD} \cdot V_{DD} + I_{DDPLL} \cdot V_{DDPLL} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

Which is the sum of all output currents on I/O ports associated with VDDX and VDDM.

For R_{DSON} is valid:

$$R_{DSON} = \frac{V_{OL}}{I_{OL}}; \text{for outputs driven low}$$

respectively

$$R_{DSON} = \frac{V_{DD5} - V_{OH}}{I_{OH}}; \text{for outputs driven high}$$

2. Internal voltage regulator enabled

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

I_{DDR} is the current shown in Table A-8 and not the overall current flowing into VDDR, which additionally contains the current flowing into the external loads with output high.

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

Which is the sum of all output currents on I/O ports associated with VDDX and VDDR.

Table A-5 Thermal Package Characteristics¹

| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
|-----|---|---|---------------|-----|-----|-----|------|
| 1 | T | Thermal Resistance LQFP48, single layer PCB ² | θ_{JA} | - | - | 69 | °C/W |
| 2 | T | Thermal Resistance LQFP48, double sided PCB with 2 internal planes ³ | θ_{JA} | - | - | 53 | °C/W |
| 3 | T | Junction to Board LQFP48 | θ_{JB} | | | 30 | °C/W |
| 4 | T | Junction to Case LQFP48 | θ_{JC} | | | 20 | °C/W |
| 5 | T | Junction to Package Top LQFP48 | Ψ_{JT} | | | 4 | °C/W |
| 6 | T | Thermal Resistance LQFP52, single sided PCB | θ_{JA} | - | - | 65 | °C/W |
| 7 | T | Thermal Resistance LQFP52, double sided PCB with 2 internal planes | θ_{JA} | - | - | 49 | °C/W |
| 8 | T | Junction to Board LQFP52 | θ_{JB} | | | 31 | °C/W |
| 9 | T | Junction to Case LQFP52 | θ_{JC} | | | 17 | °C/W |
| 10 | T | Junction to Package Top LQFP52 | Ψ_{JT} | | | 3 | °C/W |
| 11 | T | Thermal Resistance QFP 80, single sided PCB | θ_{JA} | - | - | 52 | °C/W |
| 12 | T | Thermal Resistance QFP 80, double sided PCB with 2 internal planes | θ_{JA} | - | - | 42 | °C/W |
| 13 | T | Junction to Board QFP80 | θ_{JB} | | | 28 | °C/W |
| 14 | T | Junction to Case QFP80 | θ_{JC} | | | 18 | °C/W |
| 15 | T | Junction to Package Top QFP80 | Ψ_{JT} | | | 4 | °C/W |

NOTES:

1. The values for thermal resistance are achieved by package simulations
2. PC Board according to EIA/JEDEC Standard 51-2
3. PC Board according to EIA/JEDEC Standard 51-7

A.1.9 I/O Characteristics

This section describes the characteristics of all I/O pins. All parameters are not always applicable, e.g. not all pins feature pull up/down resistances.

Table A-6 5V I/O Characteristics

| Conditions are 4.5 < VDDX < 5.5V Temperature from -40°C to +140°C, unless otherwise noted | | | | | | | |
|---|---|--|------------------------|----------------------|-----|----------------------|---------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | P | Input High Voltage | V_{IH} | $0.65 \cdot V_{DD5}$ | - | - | V |
| | T | Input High Voltage | V_{IH} | - | - | $V_{DD5} + 0.3$ | V |
| 2 | P | Input Low Voltage | V_{IL} | - | - | $0.35 \cdot V_{DD5}$ | V |
| | T | Input Low Voltage | V_{IL} | $V_{SS5} - 0.3$ | - | - | V |
| 3 | C | Input Hysteresis | V_{HYS} | | 250 | | mV |
| 4 | P | Input Leakage Current (pins in high ohmic input mode) ¹ $V_{in} = V_{DD5}$ or V_{SS5} | I_{in} | -1 | - | 1 | μA |
| 5 | C | Output High Voltage (pins in output mode) Partial Drive $I_{OH} = -2mA$ | V_{OH} | $V_{DD5} - 0.8$ | - | - | V |
| 6 | P | Output High Voltage (pins in output mode) Full Drive $I_{OH} = -10mA$ | V_{OH} | $V_{DD5} - 0.8$ | - | - | V |
| 7 | C | Output Low Voltage (pins in output mode) Partial Drive $I_{OL} = +2mA$ | V_{OL} | - | - | 0.8 | V |
| 8 | P | Output Low Voltage (pins in output mode) Full Drive $I_{OL} = +10mA$ | V_{OL} | - | - | 0.8 | V |
| 9 | P | Internal Pull Up Device Current, tested at V_{IL} Max. | I_{PUL} | - | - | -130 | μA |
| 10 | C | Internal Pull Up Device Current, tested at V_{IH} Min. | I_{PUH} | -10 | - | - | μA |
| 11 | P | Internal Pull Down Device Current, tested at V_{IH} Min. | I_{PDH} | - | - | 130 | μA |
| 12 | C | Internal Pull Down Device Current, tested at V_{IL} Max. | I_{PDL} | 10 | - | - | μA |
| 13 | D | Input Capacitance | C_{in} | | 7 | - | pF |
| 14 | T | Injection current ² Single Pin limit Total Device Limit. Sum of all injected currents | I_{ICS} I_{ICP} | -2.5 -25 | - | 2.5 25 | mA |
| 15 | P | Port P, J Interrupt Input Pulse filtered ³ | t_{PIGN} | | | 3 | μs |
| 16 | P | Port P, J Interrupt Input Pulse passed ³ | t_{PVAL} | 10 | | | μs |

NOTES:

1. Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8 C to 12 C in the temperature range from 50 C to 125 C.
2. Refer to **Section A.1.4 Current Injection**, for more details
3. Parameter only applies in STOP or Pseudo STOP mode.

Table A-7 3.3V I/O Characteristics

| Conditions are VDDX=3.3V +/-10%, Temperature from -40°C to +140°C, unless otherwise noted | | | | | | | |
|---|---|--|------------------------|----------------------|-----|----------------------|---------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | P | Input High Voltage | V_{IH} | $0.65 \cdot V_{DD5}$ | - | - | V |
| | T | Input High Voltage | V_{IH} | - | - | $V_{DD5} + 0.3$ | V |
| 2 | P | Input Low Voltage | V_{IL} | - | - | $0.35 \cdot V_{DD5}$ | V |
| | T | Input Low Voltage | V_{IL} | $V_{SS5} - 0.3$ | - | - | V |
| 3 | C | Input Hysteresis | V_{HYS} | | 250 | | mV |
| 4 | P | Input Leakage Current (pins in high ohmic input mode) ¹ $V_{in} = V_{DD5}$ or V_{SS5} | I_{in} | -1 | - | 1 | μA |
| 5 | C | Output High Voltage (pins in output mode) Partial Drive $I_{OH} = -0.75mA$ | V_{OH} | $V_{DD5} - 0.4$ | - | - | V |
| 6 | P | Output High Voltage (pins in output mode) Full Drive $I_{OH} = -4mA$ | V_{OH} | $V_{DD5} - 0.4$ | - | - | V |
| 7 | C | Output Low Voltage (pins in output mode) Partial Drive $I_{OL} = +0.9mA$ | V_{OL} | - | - | 0.4 | V |
| 8 | P | Output Low Voltage (pins in output mode) Full Drive $I_{OL} = +4.75mA$ | V_{OL} | - | - | 0.4 | V |
| 9 | P | Internal Pull Up Device Current, tested at V_{IL} Max. | I_{PUL} | - | - | -60 | μA |
| 10 | C | Internal Pull Up Device Current, tested at V_{IH} Min. | I_{PUH} | -6 | - | - | μA |
| 11 | P | Internal Pull Down Device Current, tested at V_{IH} Min. | I_{PDH} | - | - | 60 | μA |
| 12 | C | Internal Pull Down Device Current, tested at V_{IL} Max. | I_{PDL} | 6 | - | - | μA |
| 11 | D | Input Capacitance | C_{in} | | 7 | - | pF |
| 12 | T | Injection current ² Single Pin limit Total Device Limit. Sum of all injected currents | I_{ICS} I_{ICP} | -2.5 -25 | - | 2.5 25 | mA |
| 13 | P | Port P, J Interrupt Input Pulse filtered ³ | t_{PIGN} | | | 3 | μs |
| 14 | P | Port P, J Interrupt Input Pulse passed ³ | t_{PVAL} | 10 | | | μs |

NOTES:

- Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8 C to 12 C in the temperature range from 50 C to 125 C.
- Refer to **Section A.1.4 Current Injection**, for more details
- Parameter only applies in STOP or Pseudo STOP mode.

A.1.10 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

A.1.10.1 Measurement Conditions

All measurements are without output loads. Unless otherwise noted the currents are measured in single chip mode, internal voltage regulator enabled and at 25MHz bus frequency using a 4MHz oscillator.

A.1.10.2 Additional Remarks

In expanded modes the currents flowing in the system are highly dependent on the load at the address, data and control signals as well as on the duty cycle of those signals. No generally applicable numbers can be given. A very good estimate is to take the single chip currents and add the currents due to the external loads.

Table A-8 Supply Current Characteristics for MC9S12C32

| Conditions are shown in Table A-4 with internal regulator enabled unless otherwise noted | | | | | | | |
|--|--------------------------------------|--|-----------------|-----|---|-----------------------------|------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | P | Run Supply Current Single Chip | I_{DD5} | | | 35 | mA |
| 2 | P P C | Wait Supply current All modules enabled VDDR<4.9V, only RTI enabled ⁽²⁾ VDDR>4.9V, only RTI enabled | I_{DDW} | | 3.5 2.5 | 30 8 | mA |
| 3 | C P C P C P C P | Pseudo Stop Current (RTI and COP disabled) ⁽²⁾⁽³⁾ -40°C 27°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C | I_{DDPS}^1 | | 340 360 500 550 590 720 780 1100 | 450 1450 1900 4500 | μA |
| 4 | C C C C C | Pseudo Stop Current (RTI and COP enabled) ^{2 3} -40°C 27°C 85°C 105°C 125°C | I_{DDPS}^1 | | 540 700 750 880 1300 | | μA |
| 5 | C P C P C P C P | Stop Current ⁽³⁾ -40°C 27°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C | $I_{DDS}^{(1)}$ | | 10 20 100 140 170 300 350 520 | 80 1000 1400 4000 | μA |

NOTES:

- STOP current measured in production test at increased junction temperature, hence for Temp Option "C" the test is carried out at 100°C although the Temperature specification is 85°C. Similarly for "v" and "M" options the temperature used in test lies 15°C above the temperature option specification.
- PLL off
- At those low power dissipation levels $T_J = T_A$ can be assumed

Table A-9 Supply Current Characteristics for MC9S12C64,MC9S12C96,MC9S12C128

| Conditions are shown in Table A-4 with internal regulator enabled unless otherwise noted | | | | | | | |
|--|--------------------------------------|--|-----------------|-----|---|-----------------------------|------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | P | Run Supply Current Single Chip, | I_{DD5} | | | 45 | mA |
| 2 | P P C | Wait Supply current All modules enabled VDDR<4.9V, only RTI enabled ⁽²⁾ VDDR>4.9V, only RTI enabled | I_{DDW} | | 2.5 3.5 | 33 8 | mA |
| 6 | C P C P C P C P | Pseudo Stop Current (RTI and COP disabled) ⁽²⁾⁽³⁾ -40°C 27°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C | I_{DDPS}^1 | | 190 200 300 400 450 600 650 1000 | 250 1400 1900 4800 | μA |
| 4 | C C C C C | Pseudo Stop Current (RTI and COP enabled) ^{2 3} -40°C 27°C 85°C 105°C 125°C | I_{DDPS}^1 | | 370 500 590 780 1200 | | μA |
| 5 | C P C P C P C P | Stop Current ⁽³⁾ -40°C 27°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C | $I_{DDS}^{(1)}$ | | 12 25 130 160 200 350 400 600 | 100 1200 1700 4500 | μA |

NOTES:

1. STOP current measured in production test at increased junction temperature, hence for Temp Option "C" the test is carried out at 100°C although the Temperature specification is 85°C. Similarly for "v" and "M" options the temperature used in test lies 15°C above the temperature option specification.
2. PLL off
3. At those low power dissipation levels $T_J = T_A$ can be assumed

Appendix B Electrical Specifications

B.1 Voltage Regulator Operating Conditions

Table B-1 Voltage Regulator Electrical Parameters

| Num | C | Characteristic | Symbol | Min | Typical | Max | Unit |
|-----|---|--|--|------------------------------|------------------------------|------------------------------|--------------------|
| 1 | P | Input Voltages | $V_{VDDR, A}$ | 2.97 | — | 5.5 | V |
| 2 | C | Regulator Current Reduced Power Mode Shutdown Mode | I_{REG} | — — | 20 12 | 50 40 | μA μA |
| 3 | P | Output Voltage Core Full Performance Mode | V_{DD} | 2.35 | 2.5 | 2.75 | V |
| 4 | P | Low Voltage Interrupt ¹ Assert Level C32, GC32 Assert Level C64, C96, C128 GC64, GC128 Deassert Level C32, GC32 Deassert Level C64, C96, C128 GC64, GC128 | V_{LVIA} V_{LVIA} V_{LVID} V_{LVID} | 4.30 4.10 4.42 4.25 | 4.53 4.37 4.65 4.52 | 4.77 4.66 4.89 4.77 | V V V V |
| 5 | P | Low Voltage Reset ² Assert Level C32, GC32 Assert Level C64, C96, C128 GC64, GC128 | V_{LVRA} | 2.25 2.25 | 2.3 2.35 | — | V |
| 6 | P | Low Voltage Reset ⁽²⁾ Deassert Level | V_{LVRD} | — | — | 2.55 | V |
| 7 | C | Power-on Reset ³ Assert Level Deassert Level | V_{PORA} V_{PORD} | 0.97 — | — — | — 2.05 | V V |

NOTES:

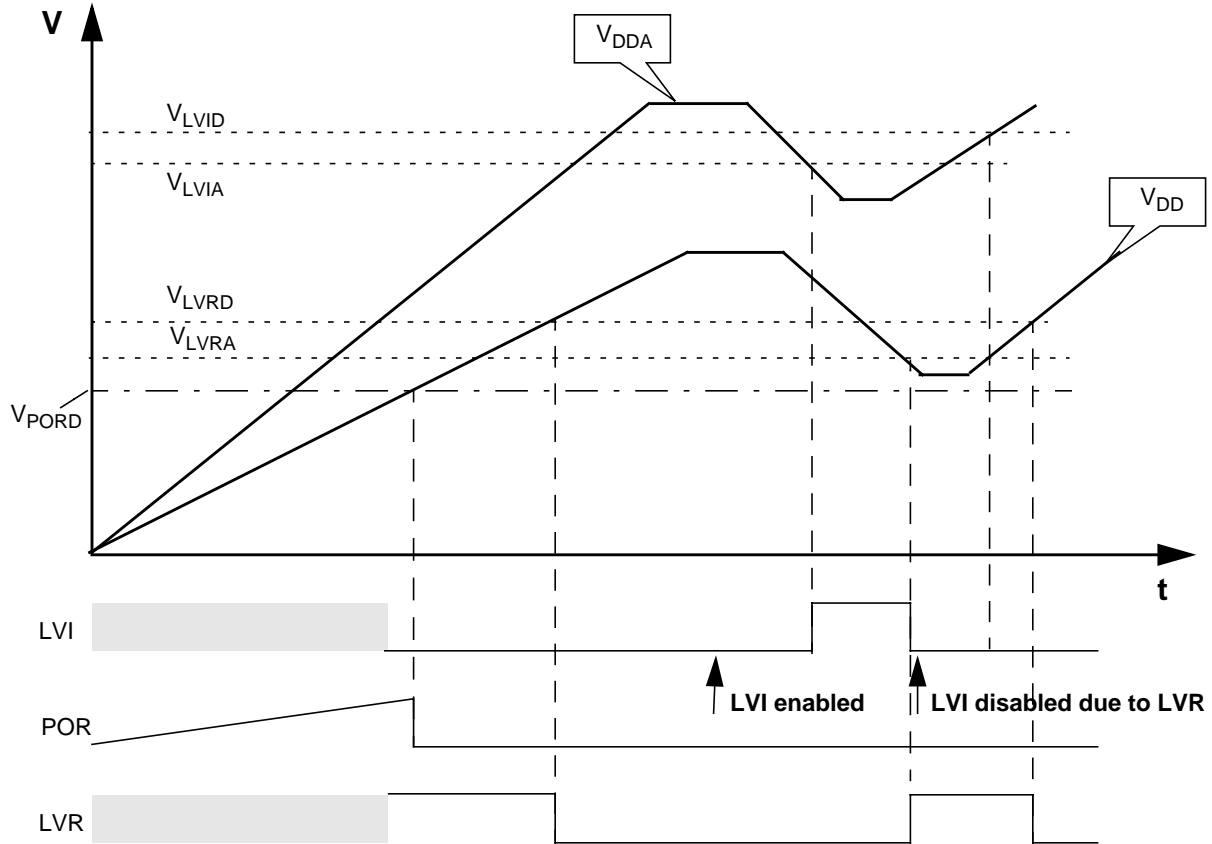
1. Monitors V_{DDA} , active only in Full Performance Mode. Indicates I/O & ADC performance degradation due to low supply voltage.
2. Monitors V_{DD} , active only in Full Performance Mode. MCU is monitored by the POR in RPM (see **Figure B-1**)
3. Monitors V_{DD} . Active in all modes.

NOTE: *The electrical characteristics given in this section are preliminary and should be used as a guide only. Values in this section cannot be guaranteed by Motorola and are subject to change without notice.*

B.2 Chip Power-up and LVI/LVR graphical explanation

Voltage regulator sub modules LVI (low voltage interrupt), POR (power-on reset) and LVR (low voltage reset) handle chip power-up or drops of the supply voltage. Their function is described in **Figure B-1**.

Figure B-1 Voltage Regulator - Chip Power-up and Voltage Drops (not scaled)



B.3 Output Loads

B.3.1 Resistive Loads

The on-chip voltage regulator is intended to supply the internal logic and oscillator circuits allows no external DC loads.

B.3.2 Capacitive Loads

The capacitive loads are specified in **Table B-2**. Ceramic capacitors with X7R dielectricum are required.

Table B-2 Voltage Regulator - Capacitive Loads

| Num | Characteristic | Symbol | Min | Typical | Max | Unit |
|-----|---------------------------------|----------------|-----|---------|-------|------|
| 1 | VDD external capacitive load | C_{DDext} | 400 | 440 | 12000 | nF |
| 2 | VDDPLL external capacitive load | $C_{DDPLLext}$ | 90 | 220 | 5000 | nF |

B.4 ATD Characteristics

This section describes the characteristics of the analog to digital converter.

VRL is not available as a separate pin in the 48 and 52 pin versions. In this case the internal VRL pad is bonded to the VSSA pin.

The ATD is specified and tested for both the 3.3V and 5V range. For ranges between 3.3V and 5V the ATD accuracy is generally the same as in the 3.3V range but is not tested in this range in production test.

B.4.1 ATD Operating Characteristics In 5V Range

The Table B-3 shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:

$V_{SSA} \leq V_{RL} \leq V_{IN} \leq V_{RH} \leq V_{DDA}$. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table B-3 ATD Operating Characteristics

| Conditions are shown in Table A-4 unless otherwise noted. Supply Voltage $5V-10\% \leq V_{DDA} \leq 5V+10\%$ | | | | | | | |
|--|---|--|------------------------------|----------------|-----|----------------|-------------------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | D | Reference Potential Low High | VRL VRH | VSSA VDDA/2 | | VDDA/2 VDDA | V V |
| 2 | C | Differential Reference Voltage ¹ | VRH-VRL | 4.75 | 5.0 | 5.25 | V |
| 3 | D | ATD Clock Frequency | f_{ATDCLK} | 0.5 | | 2.0 | MHz |
| 4 | D | ATD 10-Bit Conversion Period Clock Cycles ² Conv, Time at 2.0MHz ATD Clock f_{ATDCLK} | N_{CONV10} T_{CONV10} | 14 7 | | 28 14 | Cycles μs |
| 5 | D | ATD 8-Bit Conversion Period Clock Cycles ² Conv, Time at 2.0MHz ATD Clock f_{ATDCLK} | N_{CONV10} T_{CONV10} | 12 6 | | 26 13 | Cycles μs |
| 5 | D | Recovery Time ($V_{DDA}=5.0$ Volts) | t_{REC} | | | 20 | μs |
| 6 | P | Reference Supply current | I_{REF} | | | 0.375 | mA |

NOTES:

1. Full accuracy is not guaranteed when differential voltage is less than 4.75V
2. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

B.4.2 ATD Operating Characteristics In 3.3V Range

The Table B-3 shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:

$V_{SSA} \leq V_{RL} \leq V_{IN} \leq V_{RH} \leq V_{DDA}$. This constraint exists since the sample buffer amplifier can not drive

beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped

Table B-4 ATD Operating Characteristics

| Conditions are shown in Table A-4 unless otherwise noted; Supply Voltage $3.3V-10\% \leq V_{DDA} \leq 3.3V+10\%$ | | | | | | | |
|--|---|---|------------------------------|--------------------------|-----|--------------------------|-------------------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | D | Reference Potential Low High | V_{RL} V_{RH} | V_{SSA} $V_{DDA}/2$ | | $V_{DDA}/2$ V_{DDA} | V V |
| 2 | C | Differential Reference Voltage | $V_{RH}-V_{RL}$ | 3.0 | 3.3 | 3.6 | V |
| 3 | D | ATD Clock Frequency | f_{ATDCLK} | 0.5 | | 2.0 | MHz |
| 4 | D | ATD 10-Bit Conversion Period Clock Cycles ¹ Conv, Time at 2.0MHz ATD Clock f_{ATDCLK} | N_{CONV10} T_{CONV10} | 14 7 | | 28 14 | Cycles μs |
| 5 | D | ATD 8-Bit Conversion Period Clock Cycles ⁽¹⁾ Conv, Time at 2.0MHz ATD Clock f_{ATDCLK} | N_{CONV8} T_{CONV8} | 12 6 | | 26 13 | Cycles μs |
| 6 | D | Recovery Time ($V_{DDA}=3.3$ Volts) | t_{REC} | | | 20 | μs |
| 7 | P | Reference Supply current | I_{REF} | | | 0.250 | mA |

NOTES:

1. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

B.4.3 Factors influencing accuracy

Three factors - source resistance, source capacitance and current injection - have an influence on the accuracy of the ATD.

B.4.3.1 Source Resistance:

Due to the input pin leakage current as specified in Table A-6 in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum source resistance R_S specifies results in an error of less than 1/2 LSB (2.5mV) at the maximum leakage current. If device or operating conditions are less than worst case or leakage-induced error is acceptable, larger values of source resistance is allowable.

B.4.3.2 Source capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage $\leq 1LSB$, then the external filter capacitor, $C_f \geq 1024 * (C_{INS} - C_{INN})$.

B.4.3.3 Current injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion values of \$3FF (\$FF in 8-bit mode) for analog inputs greater than VRH and \$000 for values less than VRL unless the current is higher than specified as disruptive conditions.
2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.

The additional input voltage error on the converted channel can be calculated as $V_{ERR} = K * R_S * I_{INJ}$, with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

Table B-5 ATD Electrical Characteristics

| Conditions are shown in Table A-4 unless otherwise noted | | | | | | | |
|--|---|---|------------------------|------|-----|-----------|------------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | C | Max input Source Resistance | R_S | - | - | 1 | K Ω |
| 2 | T | Total Input Capacitance Non Sampling Sampling | C_{INN} C_{INS} | | | 10 15 | pF |
| 3 | C | Disruptive Analog Input Current | I_{NA} | -2.5 | | 2.5 | mA |
| 4 | C | Coupling Ratio positive current injection | K_p | | | 10^{-4} | A/A |
| 5 | C | Coupling Ratio negative current injection | K_n | | | 10^{-2} | A/A |

B.4.4 ATD accuracy (5V Range)

Table B-6 specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table B-6 ATD Conversion Performance

| Conditions are shown in Table A-4 unless otherwise noted $V_{REF} = V_{RH} - V_{RL} = 5.12V$. Resulting to one 8 bit count = 20mV and one 10 bit count = 5mV $f_{ATDCLK} = 2.0MHz$ | | | | | | | |
|---|---|-------------------------------------|--------|------|------|-----|--------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | P | 10-Bit Resolution | LSB | | 5 | | mV |
| 2 | P | 10-Bit Differential Nonlinearity | DNL | -1 | | 1 | Counts |
| 3 | P | 10-Bit Integral Nonlinearity | INL | -2 | | 2 | Counts |
| 4 | P | 10-Bit Absolute Error ¹ | AE | -2.5 | | 2.5 | Counts |
| 5 | P | 8-Bit Resolution | LSB | | 20 | | mV |
| 6 | P | 8-Bit Differential Nonlinearity | DNL | -0.5 | | 0.5 | Counts |
| 7 | P | 8-Bit Integral Nonlinearity | INL | -1.0 | ±0.5 | 1.0 | Counts |
| 8 | P | 8-Bit Absolute Error ⁽¹⁾ | AE | -1.5 | ±1 | 1.5 | Counts |

NOTES:

1. These values include quantization error which is inherently 1/2 count for any A/D converter.

B.4.5 ATD accuracy (3.3V Range)

Table B-6 specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table B-7 ATD Conversion Performance

| Conditions are shown in Table A-4 unless otherwise noted $V_{REF} = V_{RH} - V_{RL} = 3.328V$. Resulting to one 8 bit count = 13mV and one 10 bit count = 3.25mV $f_{ATDCLK} = 2.0MHz$ | | | | | | | |
|---|---|-------------------------------------|--------|------|------|-----|--------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | P | 10-Bit Resolution | LSB | | 3.25 | | mV |
| 2 | P | 10-Bit Differential Nonlinearity | DNL | -1.5 | | 1.5 | Counts |
| 3 | P | 10-Bit Integral Nonlinearity | INL | -3.5 | ±1.5 | 3.5 | Counts |
| 4 | P | 10-Bit Absolute Error ¹ | AE | -5 | ±2.5 | 5 | Counts |
| 5 | P | 8-Bit Resolution | LSB | | 13 | | mV |
| 6 | P | 8-Bit Differential Nonlinearity | DNL | -0.5 | | 0.5 | Counts |
| 7 | P | 8-Bit Integral Nonlinearity | INL | -1.5 | ±1 | 1.5 | Counts |
| 8 | P | 8-Bit Absolute Error ⁽¹⁾ | AE | -2.0 | ±1.5 | 2.0 | Counts |

NOTES:

1. These values include the quantization error which is inherently 1/2 count for any A/D converter.

For the following definitions see also **Figure B-2**.

Differential Non-Linearity (DNL) is defined as the difference between two adjacent switching steps.

$$\text{DNL}(i) = \frac{V_i - V_{i-1}}{1\text{LSB}} - 1$$

The Integral Non-Linearity (INL) is defined as the sum of all DNLs:

$$\text{INL}(n) = \sum_{i=1}^n \text{DNL}(i) = \frac{V_n - V_0}{1\text{LSB}} - n$$

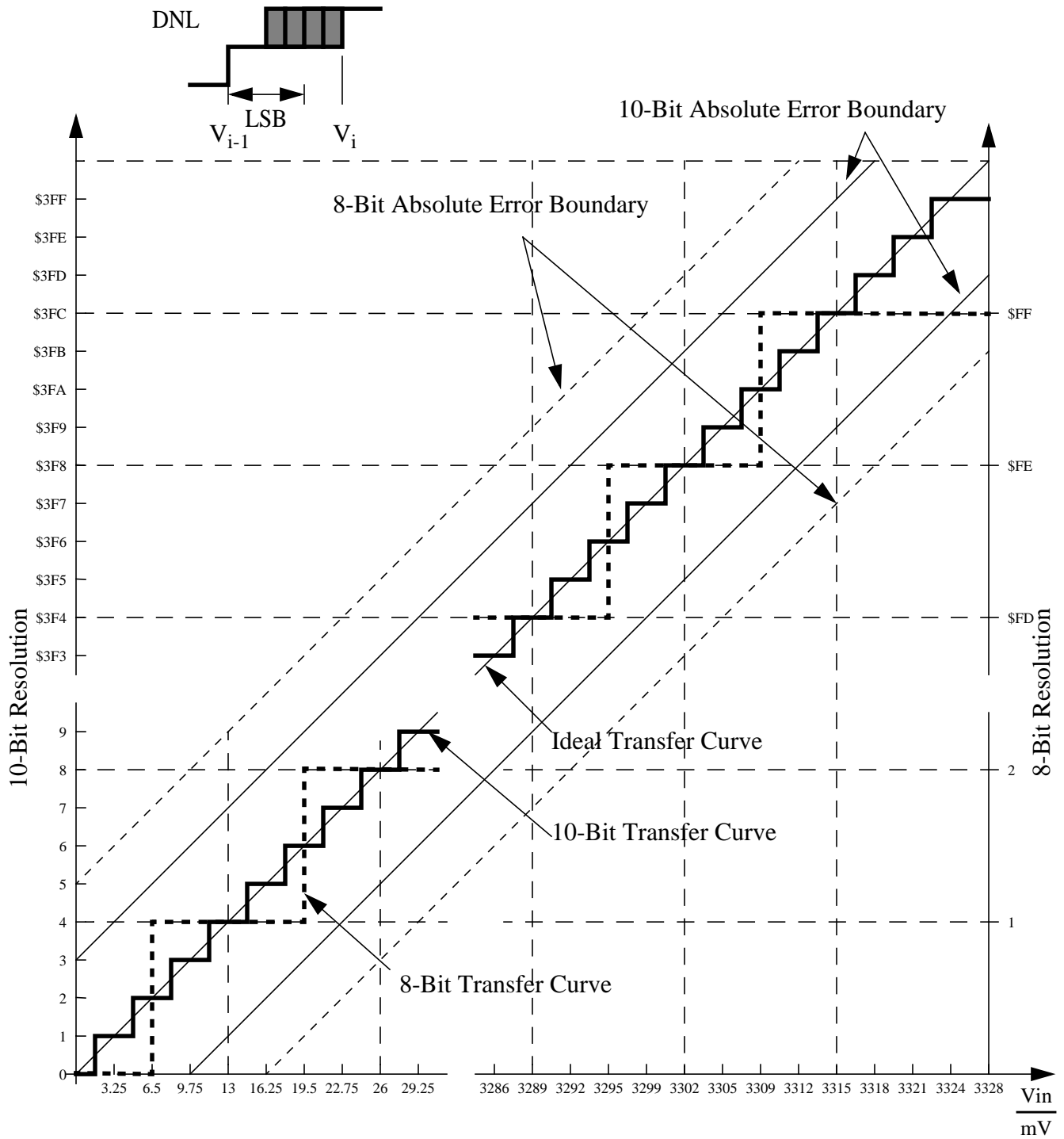


Figure B-2 ATD Accuracy Definitions

NOTE: Figure B-2 shows only definitions, for specification values refer to Table B-6.

B.5 NVM, Flash and EEPROM

B.5.1 NVM timing

The time base for all NVM program or erase operations is derived from the oscillator. A minimum oscillator frequency f_{NVMOSC} is required for performing program or erase operations. The NVM modules do not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. Attempting to program or erase the NVM modules at a lower frequency a full program or erase transition is not assured.

The Flash program and erase operations are timed using a clock derived from the oscillator using the FCLKDIV and ECLKDIV registers respectively. The frequency of this clock must be set within the limits specified as f_{NVMOP} .

The minimum program and erase times shown in Table B-8 are calculated for maximum f_{NVMOP} and maximum f_{bus} . The maximum times are calculated for minimum f_{NVMOP} and a f_{bus} of 2MHz.

B.5.1.1 Single Word Programming

The programming time for single word programming is dependant on the bus frequency as a well as on the frequency f_{NVMOP} and can be calculated according to the following formula.

$$t_{\text{swpgm}} = 9 \cdot \frac{1}{f_{\text{NVMOP}}} + 25 \cdot \frac{1}{f_{\text{bus}}}$$

B.5.1.2 Row Programming

Generally the time to program a consecutive word can be calculated as:

$$t_{\text{bwpgm}} = 4 \cdot \frac{1}{f_{\text{NVMOP}}} + 9 \cdot \frac{1}{f_{\text{bus}}}$$

For the C16, GC16, C32 and GC32 device flash arrays, where up to 32 words in a row can be programmed consecutively by keeping the command pipeline filled, the time to program a whole row is:

$$t_{\text{brpgm}} = t_{\text{swpgm}} + 31 \cdot t_{\text{bwpgm}}$$

For the C64, GC64, C96, C128 and GC128 device flash arrays, where up to 64 words in a row can be programmed consecutively by keeping the command pipeline filled, the time to program a whole row is:

$$t_{\text{brpgm}} = t_{\text{swpgm}} + 63 \cdot t_{\text{bwpgm}}$$

Row programming is more than 2 times faster than single word programming.

B.5.1.3 Sector Erase

Erasing either a 512 byte or 1024 byte Flash sector takes:

$$t_{era} \approx 4000 \cdot \frac{1}{f_{NVMOP}}$$

The setup times can be ignored for this operation.

B.5.1.4 Mass Erase

Erasing a NVM block takes:

$$t_{mass} \approx 20000 \cdot \frac{1}{f_{NVMOP}}$$

This is independent of sector size.

The setup times can be ignored for this operation.

Table B-8 NVM Timing Characteristics

| Conditions are shown in Table A-4 unless otherwise noted | | | | | | | |
|--|---|---|--------------|---------------------|-----|---------------------|------------------------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | D | External Oscillator Clock | f_{NVMOSC} | 0.5 | | 50 ¹ | MHz |
| 2 | D | Bus frequency for Programming or Erase Operations | f_{NVMBUS} | 1 | | | MHz |
| 3 | D | Operating Frequency | f_{NVMOP} | 150 | | 200 | kHz |
| 4 | P | Single Word Programming Time | t_{swpgm} | 46 ² | | 74.5 ³ | μs |
| 5 | D | Flash Burst Programming consecutive word | t_{bwpgm} | 20.4 ² | | 31 ³ | μs |
| 6 | D | Flash Burst Programming Time for 32 Word row | t_{brpgm} | 678.4 ² | | 1035.5 ³ | μs |
| 6 | D | Flash Burst Programming Time for 64 Word row | t_{brpgm} | 1331.2 ² | | 2027.5 ³ | μs |
| 7 | P | Sector Erase Time | t_{era} | 20 ⁴ | | 26.7 ³ | ms |
| 8 | P | Mass Erase Time | t_{mass} | 100 ⁴ | | 133 ³ | ms |
| 9 | D | Blank Check Time Flash per block | t_{check} | 11 ⁵ | | 32778 ⁶ | ⁷ t_{cyc} |
| 9 | D | Blank Check Time Flash per block | t_{check} | 11 ⁸ | | 65546 ⁹ | ⁷ t_{cyc} |

NOTES:

1. Restrictions for oscillator in crystal mode apply!
2. Minimum Programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{bus} .
3. Maximum Erase and Programming times are achieved under particular combinations of f_{NVMOP} and bus frequency f_{bus} . Refer to formulae in Sections A.3.1.1 - A.3.1.4 for guidance.
4. Minimum Erase times are achieved under maximum NVM operating frequency f_{NVMOP} .
5. Minimum time, if first word in the array is not blank (512 byte sector size).
6. Maximum time to complete check on an erased block (512 byte sector size)
7. Where t_{cyc} is the system bus clock period.
8. Minimum time, if first word in the array is not blank (1024 byte sector size)
9. Maximum time to complete check on an erased block (1024 byte sector size).

B.5.2 NVM Reliability

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures.

The failure rates for data retention and program/erase cycling are specified at <2ppm defects over lifetime at the operating conditions noted.

A program/erase cycle is specified as two transitions of the cell value from erased → programmed → erased, 1 → 0 → 1.

NOTE: All values shown in Table B-9 are target values and subject to further extensive characterization.

Table B-9 NVM Reliability Characteristics

| Conditions are shown in Table A-4 unless otherwise noted | | | | | | | |
|--|---|--|--------------|--------|-----|-----|--------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | C | Data Retention at an average junction temperature of $T_{Javg} = 85^{\circ}\text{C}$ | t_{NVMRET} | 15 | | | Years |
| 2 | C | Flash number of Program/Erase cycles | n_{FLPE} | 10,000 | | | Cycles |

B.6 Reset, Oscillator and PLL

This section summarizes the electrical characteristics of the various startup scenarios for Oscillator and Phase-Locked-Loop (PLL).

B.6.1 Startup

Table B-10 summarizes several startup characteristics explained in this section. Detailed description of the startup behavior can be found in the Clock and Reset Generator (CRG) Block User Guide.

Table B-10 Startup Characteristics

| Conditions are shown in Table A-4 unless otherwise noted | | | | | | | |
|--|---|---|-------------|------|-----|------|-----------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | T | POR release level | V_{PORR} | | | 2.07 | V |
| 2 | T | POR assert level | V_{PORA} | 0.97 | | | V |
| 3 | D | Reset input pulse width, minimum input time | PW_{RSTL} | 2 | | | t_{osc} |
| 4 | D | Startup from Reset | n_{RST} | 192 | | 196 | n_{osc} |
| 5 | D | Interrupt pulse width, \overline{IRQ} edge-sensitive mode | PW_{IRQ} | 20 | | | ns |
| 6 | D | Wait recovery startup time | t_{WRS} | | | 14 | t_{cyc} |

B.6.1.1 POR

The release level V_{PORR} and the assert level V_{PORA} are derived from the V_{DD} Supply. They are also valid if the device is powered externally. After releasing the POR reset the oscillator and the clock quality check are started. If after a time t_{CQOUT} no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by n_{uposc} .

B.6.1.2 LVR

The release level V_{LVRR} and the assert level V_{LVRA} are derived from the V_{DD} Supply. They are also valid if the device is powered externally. After releasing the LVR reset the oscillator and the clock quality check are started. If after a time t_{CQOUT} no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by n_{uposc} .

B.6.1.3 SRAM Data Retention

Provided an appropriate external reset signal is applied to the MCU, preventing the CPU from executing code when V_{DD5} is out of specification limits, the SRAM contents integrity is guaranteed if after the reset the PORF bit in the CRG Flags Register has not been set.

B.6.1.4 External Reset

When external reset is asserted for a time greater than PW_{RSTL} the CRG module generates an internal reset, and the CPU starts fetching the reset vector without doing a clock quality check, if there was an oscillation before reset.

B.6.1.5 Stop Recovery

Out of STOP the controller can be woken up by an external interrupt. A clock quality check as after POR is performed before releasing the clocks to the system.

B.6.1.6 Pseudo Stop and Wait Recovery

The recovery from Pseudo STOP and Wait are essentially the same since the oscillator was not stopped in both modes. The controller can be woken up by internal or external interrupts. After t_{wrs} the CPU starts fetching the interrupt vector.

B.6.2 Oscillator

The device features an internal Colpitts oscillator. By asserting the \overline{XCLKS} input during reset this oscillator can be bypassed allowing the input of a square wave. Before asserting the oscillator to the internal system clocks the quality of the oscillation is checked for each start from either power-on, STOP or oscillator fail. t_{CQOUT} specifies the maximum time before switching to the internal self clock mode in case no proper oscillation is detected. The quality monitor also determines the minimum oscillator start-up

time t_{UPOSC} . The device features a clock monitor. A time-out is asserted if the frequency of the incoming clock signal is below the Clock Monitor Failure Assert Frequency f_{CMFA} .

Table B-11 Oscillator Characteristics

| Conditions are shown in Table A-4 unless otherwise noted | | | | | | | |
|--|---|--|--------------|------|-------|---------|---------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1a | C | Crystal oscillator range (Colpitts) | f_{OSC} | 0.5 | | 16 | MHz |
| 1b | C | Crystal oscillator range (Pierce) ¹⁽⁴⁾ | f_{OSC} | 0.5 | | 40 | MHz |
| 2 | P | Startup Current | i_{OSC} | 100 | | | μA |
| 3 | C | Oscillator start-up time (Colpitts) | t_{UPOSC} | | g^2 | 100^3 | ms |
| 4 | D | Clock Quality check time-out | t_{CQOUT} | 0.45 | | 2.5 | s |
| 5 | P | Clock Monitor Failure Assert Frequency | f_{CMFA} | 50 | 100 | 200 | KHz |
| 6 | P | External square wave input frequency ⁴ | f_{EXT} | 0.5 | | 50 | MHz |
| 7 | D | External square wave pulse width low | t_{EXTL} | 9.5 | | | ns |
| 8 | D | External square wave pulse width high | t_{EXTH} | 9.5 | | | ns |
| 9 | D | External square wave rise time | t_{EXTR} | | | 1 | ns |
| 10 | D | External square wave fall time | t_{EXTF} | | | 1 | ns |
| 11 | D | Input Capacitance (EXTAL, XTAL pins) | C_{IN} | | 7 | | pF |
| 12 | C | DC Operating Bias in Colpitts Configuration on EXTAL Pin | V_{DCBIAS} | | 1.1 | | V |

NOTES:

1. Depending on the crystal a damping series resistor might be necessary
2. $f_{osc} = 4\text{MHz}$, $C = 22\text{pF}$.
3. Maximum value is for extreme cases using high Q, low frequency crystals
4. $XCLKS = 0$ during reset

B.6.3 Phase Locked Loop

The oscillator provides the reference clock for the PLL. The PLL's Voltage Controlled Oscillator (VCO) is also the system clock source in self clock mode.

B.6.3.1 XFC Component Selection

This section describes the selection of the XFC components to achieve a good filter characteristics.

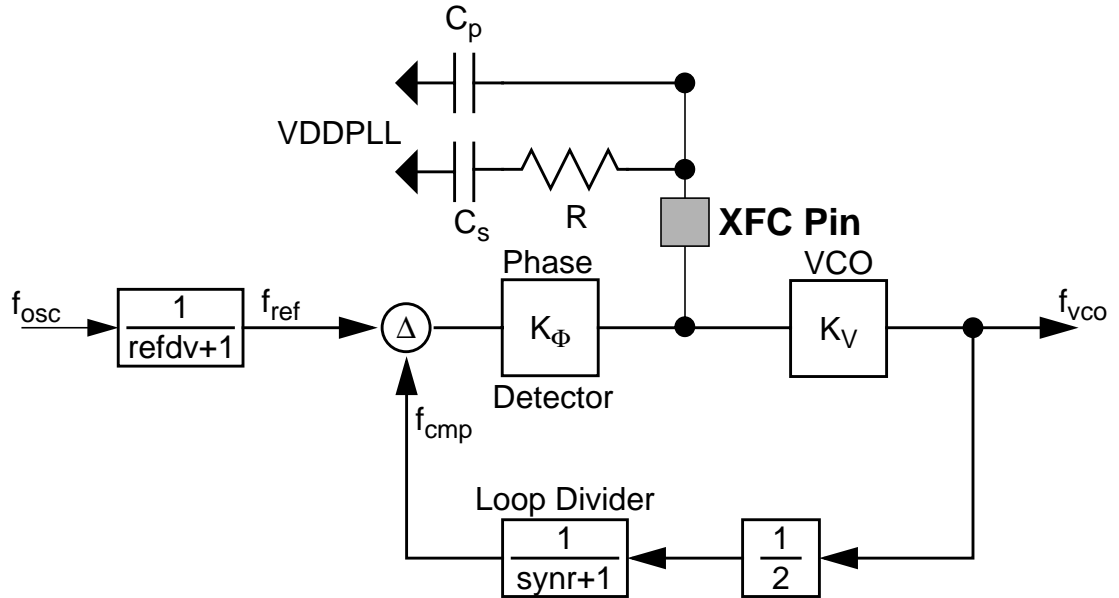


Figure B-3 Basic PLL functional diagram

The following procedure can be used to calculate the resistance and capacitance values using typical values for K_1 , f_1 and i_{ch} from Table B-12.

The grey boxes show the calculation for $f_{VCO} = 50\text{MHz}$ and $f_{ref} = 1\text{MHz}$. E.g., these frequencies are used for $f_{OSC} = 4\text{MHz}$ and a 25MHz bus clock.

The VCO Gain at the desired VCO frequency is approximated by:

$$K_V = K_1 \cdot e^{\frac{(f_1 - f_{VCO})}{K_1 \cdot 1V}} = -100 \cdot e^{\frac{(60 - 50)}{-100}} = -90.48\text{MHz/V}$$

The phase detector relationship is given by:

$$K_{\Phi} = -|i_{ch}| \cdot K_V = 316.7\text{Hz}/\Omega$$

i_{ch} is the current in tracking mode.

The loop bandwidth f_C should be chosen to fulfill the Gardner's stability criteria by at least a factor of 10, typical values are 50. $\zeta = 0.9$ ensures a good transient response.

$$f_C < \frac{2 \cdot \zeta \cdot f_{ref}}{\pi \cdot (\zeta + \sqrt{1 + \zeta^2})} \cdot \frac{1}{10} \rightarrow f_C < \frac{f_{ref}}{4 \cdot 10}; (\zeta = 0.9)$$

$$f_C < 25\text{kHz}$$

And finally the frequency relationship is defined as

$$n = \frac{f_{VCO}}{f_{ref}} = 2 \cdot (\text{synr} + 1) = 50$$

With the above values the resistance can be calculated. The example is shown for a loop bandwidth $f_C=10\text{kHz}$:

$$R = \frac{2 \cdot \pi \cdot n \cdot f_C}{K_\Phi} = 2 \cdot \pi \cdot 50 \cdot 10\text{kHz} / (316.7\text{Hz}/\Omega) = 9.9\text{k}\Omega \approx 10\text{k}\Omega$$

The capacitance C_s can now be calculated as:

$$C_s = \frac{2 \cdot \zeta^2}{\pi \cdot f_C \cdot R} \approx \frac{0.516}{f_C \cdot R}; (\zeta = 0.9) = 5.19\text{nF} \approx 4.7\text{nF}$$

The capacitance C_p should be chosen in the range of:

$$C_s/20 \leq C_p \leq C_s/10 \quad C_p = 470\text{pF}$$

B.6.3.2 Jitter Information

The basic functionality of the PLL is shown in **Figure B-3**. With each transition of the clock f_{cmp} , the deviation from the reference clock f_{ref} is measured and input voltage to the VCO is adjusted accordingly. The adjustment is done continuously with no abrupt changes in the clock output frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in **Figure B-4**.

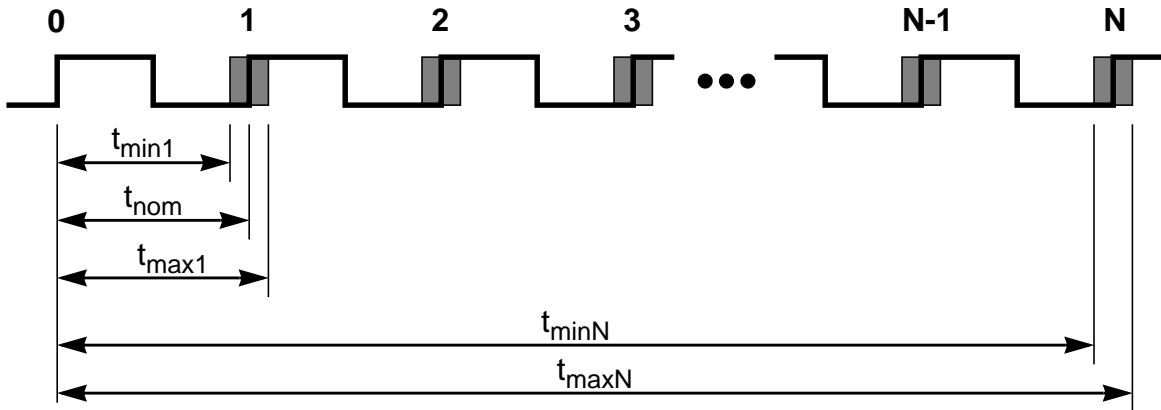


Figure B-4 Jitter Definitions

The relative deviation of t_{nom} is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N).

Defining the jitter as:

$$J(N) = \max\left(\left|1 - \frac{t_{max}(N)}{N \cdot t_{nom}}\right|, \left|1 - \frac{t_{min}(N)}{N \cdot t_{nom}}\right|\right)$$

For $N < 100$, the following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N}} + j_2$$

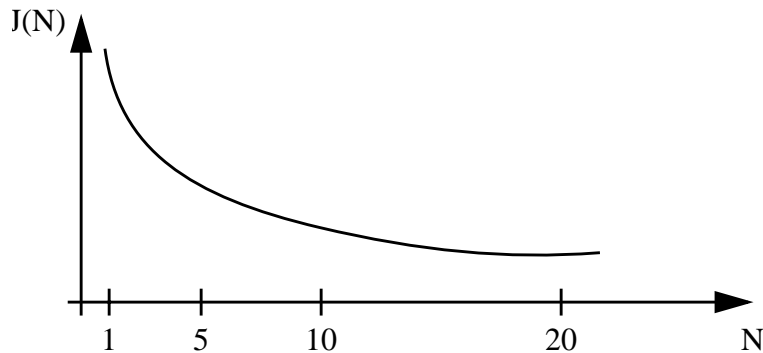


Figure B-5 Maximum bus clock jitter approximation

This is very important to notice with respect to timers, serial modules where a pre-scaler will eliminate the effect of the jitter to a large extent.

Table B-12 PLL Characteristics

| Conditions are shown in Table A-4 unless otherwise noted | | | | | | | |
|--|---|--|-------------------|-----|------|------|------------------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | P | Self Clock Mode frequency | f_{SCM} | 1 | | 5.5 | MHz |
| 2 | D | VCO locking range | f_{VCO} | 8 | | 50 | MHz |
| 3 | D | Lock Detector transition from Acquisition to Tracking mode | $ \Delta_{trk} $ | 3 | | 4 | % ¹ |
| 4 | D | Lock Detection | $ \Delta_{Lock} $ | 0 | | 1.5 | % ⁽¹⁾ |
| 5 | D | Un-Lock Detection | $ \Delta_{unt} $ | 0.5 | | 2.5 | % ⁽¹⁾ |
| 6 | D | Lock Detector transition from Tracking to Acquisition mode | $ \Delta_{unt} $ | 6 | | 8 | % ⁽¹⁾ |
| 7 | C | PLLON Total Stabilization delay (Auto Mode) ² | t_{stab} | | 0.5 | | ms |
| 8 | D | PLLON Acquisition mode stabilization delay ⁽²⁾ | t_{acq} | | 0.3 | | ms |
| 9 | D | PLLON Tracking mode stabilization delay ⁽²⁾ | t_{al} | | 0.2 | | ms |
| 10 | D | Fitting parameter VCO loop gain | K_1 | | -100 | | MHz/V |
| 11 | D | Fitting parameter VCO loop frequency | f_1 | | 60 | | MHz |
| 12 | D | Charge pump current acquisition mode | $ i_{ch} $ | | 38.5 | | μA |
| 13 | D | Charge pump current tracking mode | $ i_{ch} $ | | 3.5 | | μA |
| 14 | C | Jitter fit parameter 1 ⁽²⁾ | j_1 | | | 1.1 | % |
| 15 | C | Jitter fit parameter 2 ⁽²⁾ | j_2 | | | 0.13 | % |

NOTES:

1. % deviation from target frequency

2. $f_{OSC} = 4\text{MHz}$, $f_{BUS} = 25\text{MHz}$ equivalent $f_{VCO} = 50\text{MHz}$: REFDV = #03, SYNRR = #018, Cs = 4.7nF, Cp = 470pF, Rs = 10K Ω .

B.7 MSCAN

Table B-13 MSCAN Wake-up Pulse Characteristics

| Conditions are shown in Table A-4 unless otherwise noted | | | | | | |
|--|---|---------------------------------------|-----------|-----|-----|-----|
| Num | C | Rating | Symbol | Min | Typ | Max |
| 1 | P | MSCAN Wake-up dominant pulse filtered | t_{WUP} | | | 2 |
| 2 | P | MSCAN Wake-up dominant pulse pass | t_{WUP} | 5 | | |

B.8 SPI

Appendix C Electrical Specifications

This section provides electrical parametrics and ratings for the SPI.

In **Table C-1** the measurement conditions are listed.

Table C-1 Measurement Conditions

| Description | Value | Unit |
|--|------------------|------|
| Drive mode | full drive mode | — |
| Load capacitance C_{LOAD} , on all outputs | 50 | pF |
| Thresholds for delay measurement points | (20% / 80%) VDDX | V |

C.1 Master Mode

In **Figure C-1** the timing diagram for master mode with transmission format CPHA=0 is depicted.

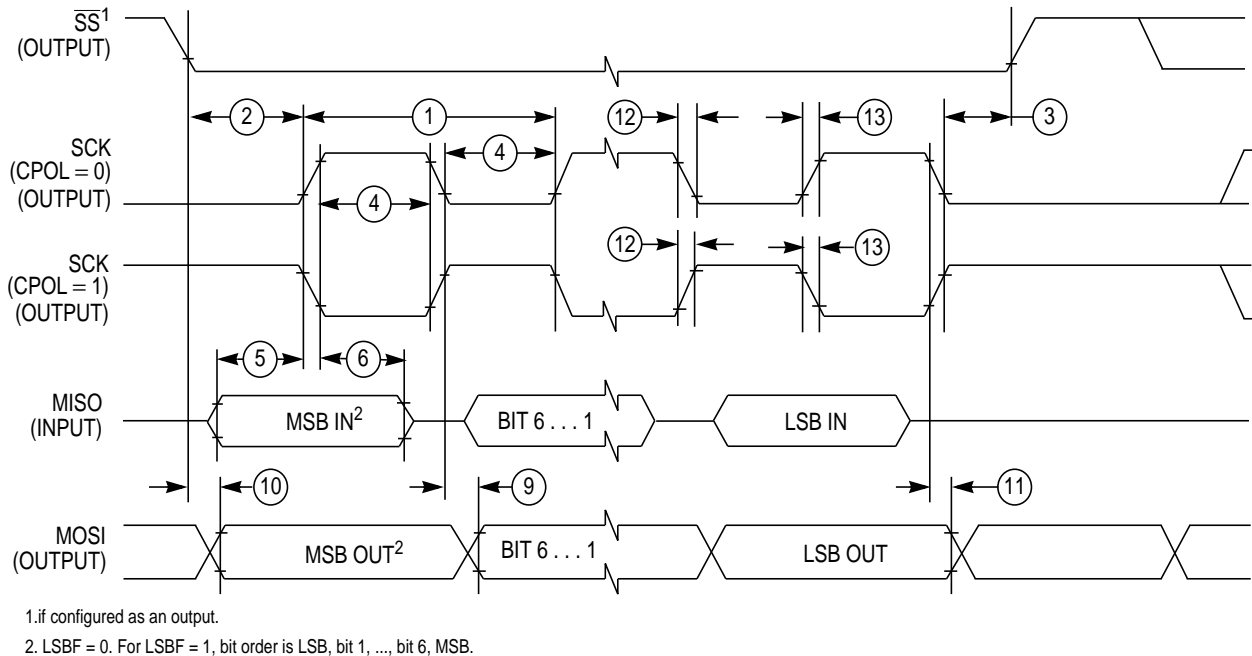


Figure C-1 SPI Master Timing (CPHA=0)

In **Figure C-2** the timing diagram for master mode with transmission format CPHA=1 is depicted.

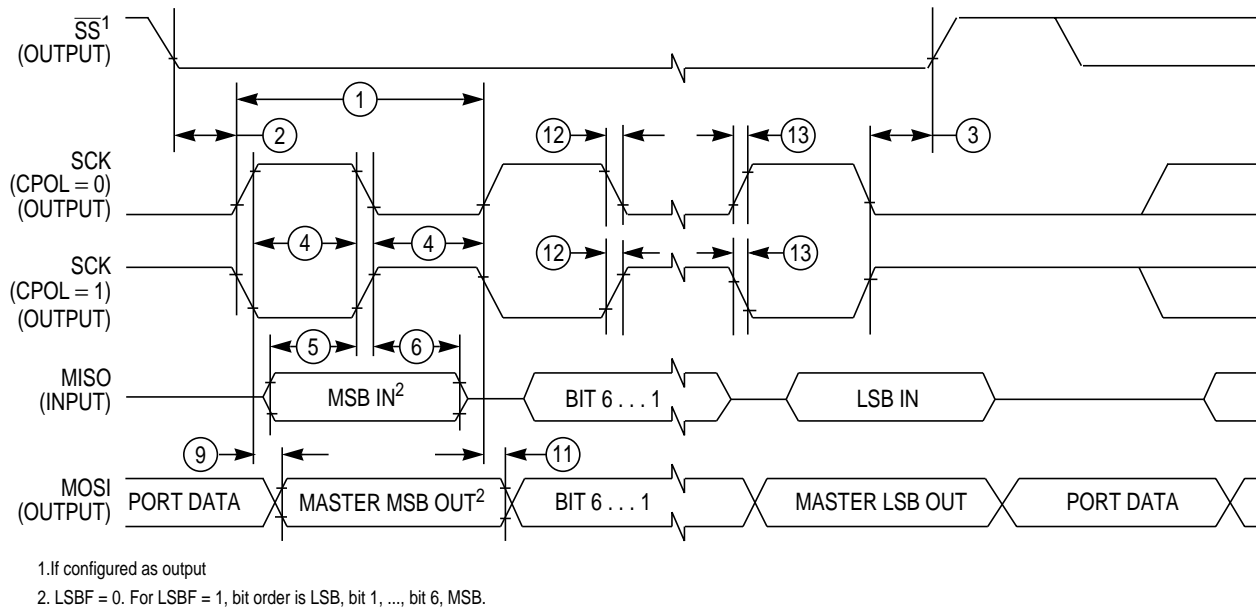


Figure C-2 SPI Master Timing (CPHA=1)

In Table C-2 the timing characteristics for master mode are listed.

Table C-2 SPI Master Mode Timing Characteristics

| Num | C | Characteristic | Symbol | Min | Typ | Max | Unit |
|-----|---|--|------------|--------|-----|------|-----------|
| | | | | | | | |
| 1 | P | SCK Frequency | f_{sck} | 1/2048 | — | 1/2 | f_{bus} |
| 1 | P | SCK Period | t_{sck} | 2 | — | 2048 | t_{bus} |
| 2 | D | Enable Lead Time | t_{lead} | — | 1/2 | — | t_{sck} |
| 3 | D | Enable Lag Time | t_{lag} | — | 1/2 | — | t_{sck} |
| 4 | D | Clock (SCK) High or Low Time | t_{wsck} | — | 1/2 | — | t_{sck} |
| 5 | D | Data Setup Time (Inputs) | t_{su} | 8 | — | — | ns |
| 6 | D | Data Hold Time (Inputs) | t_{hi} | 8 | — | — | ns |
| 9 | D | Data Valid after SCK Edge | t_{vsck} | — | — | 30 | ns |
| 10 | D | Data Valid after \overline{SS} fall (CPHA=0) | t_{vss} | — | — | 15 | ns |
| 11 | D | Data Hold Time (Outputs) | t_{ho} | 20 | — | — | ns |
| 12 | D | Rise and Fall Time Inputs | t_{rfi} | — | — | 8 | ns |
| 13 | D | Rise and Fall Time Outputs | t_{rfo} | — | — | 8 | ns |

C.2 Slave Mode

In **Figure C-3** the timing diagram for slave mode with transmission format CPHA=0 is depicted.

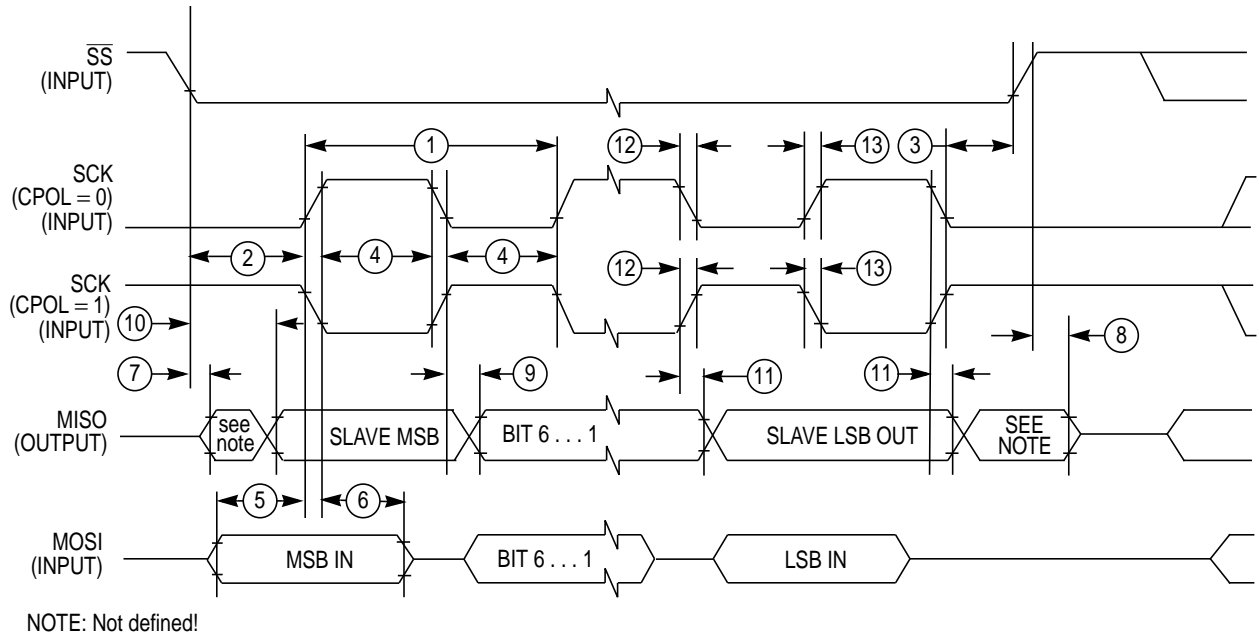


Figure C-3 SPI Slave Timing (CPHA=0)

In **Figure C-4** the timing diagram for slave mode with transmission format CPHA=1 is depicted.

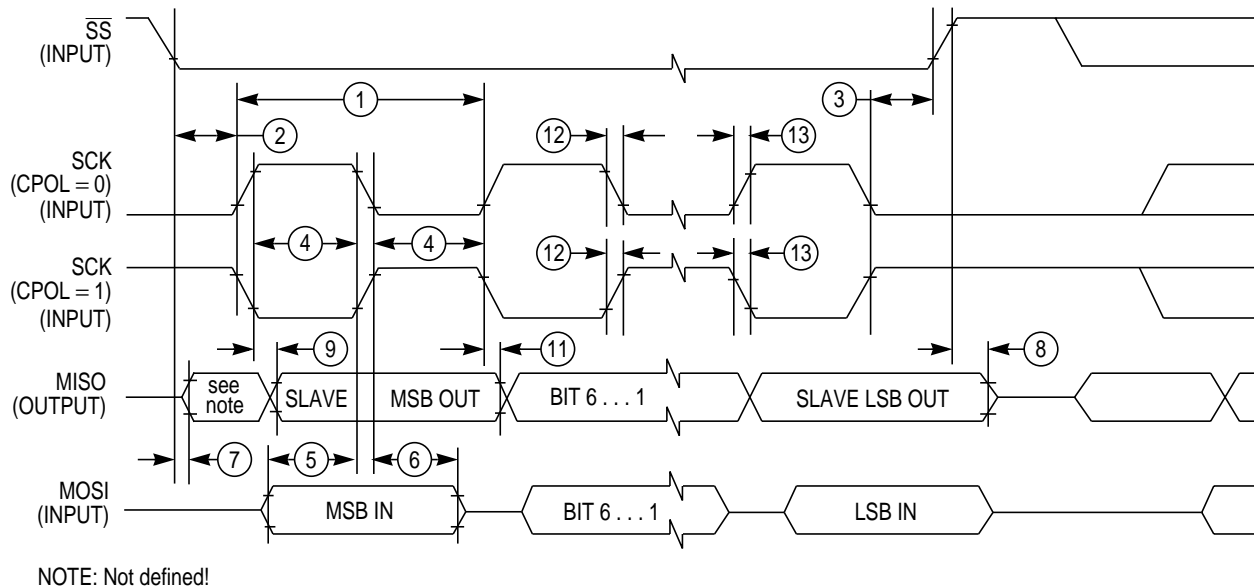


Figure C-4 SPI Slave Timing (CPHA=1)

In Table C-3 the timing characteristics for slave mode are listed.

Table C-3 SPI Slave Mode Timing Characteristics

| Num | C | Characteristic | Symbol | Min | Typ | Max | Unit |
|-----|---|---|------------|-----|-----|------------------|-----------|
| | | | | | | | |
| 1 | D | SCK Frequency | f_{sck} | DC | — | 1/4 | f_{bus} |
| 1 | P | SCK Period | t_{sck} | 4 | — | ∞ | t_{bus} |
| 2 | D | Enable Lead Time | t_{lead} | 4 | — | — | t_{bus} |
| 3 | D | Enable Lag Time | t_{lag} | 4 | — | — | t_{bus} |
| 4 | D | Clock (SCK) High or Low Time | t_{wsck} | 4 | — | — | t_{bus} |
| 5 | D | Data Setup Time (Inputs) | t_{su} | 8 | — | — | ns |
| 6 | D | Data Hold Time (Inputs) | t_{hi} | 8 | — | — | ns |
| 7 | D | Slave Access Time (time to data active) | t_a | — | — | 20 | ns |
| 8 | D | Slave MISO Disable Time | t_{dis} | — | — | 22 | ns |
| 9 | D | Data Valid after SCK Edge | t_{vsck} | — | — | $30 + t_{bus}^1$ | ns |
| 10 | D | Data Valid after \overline{SS} fall | t_{vss} | — | — | $30 + t_{bus}^1$ | ns |
| 11 | D | Data Hold Time (Outputs) | t_{ho} | 20 | — | — | ns |
| 12 | D | Rise and Fall Time Inputs | t_{rfi} | — | — | 8 | ns |
| 13 | D | Rise and Fall Time Outputs | t_{rfo} | — | — | 8 | ns |

NOTES:

- 1. t_{bus} added due to internal synchronization delay

C.3 External Bus Timing

A timing diagram of the external multiplexed-bus is illustrated in **Figure C-5** with the actual timing values shown on table Table C-4. All major bus signals are included in the diagram. While both a data write and data read cycle are shown, only one or the other would occur on a particular bus cycle.

C.3.1 General Muxed Bus Timing

The expanded bus timings are highly dependent on the load conditions. The timing parameters shown assume a balanced load across all outputs.

Figure C-5 General External Bus Timing

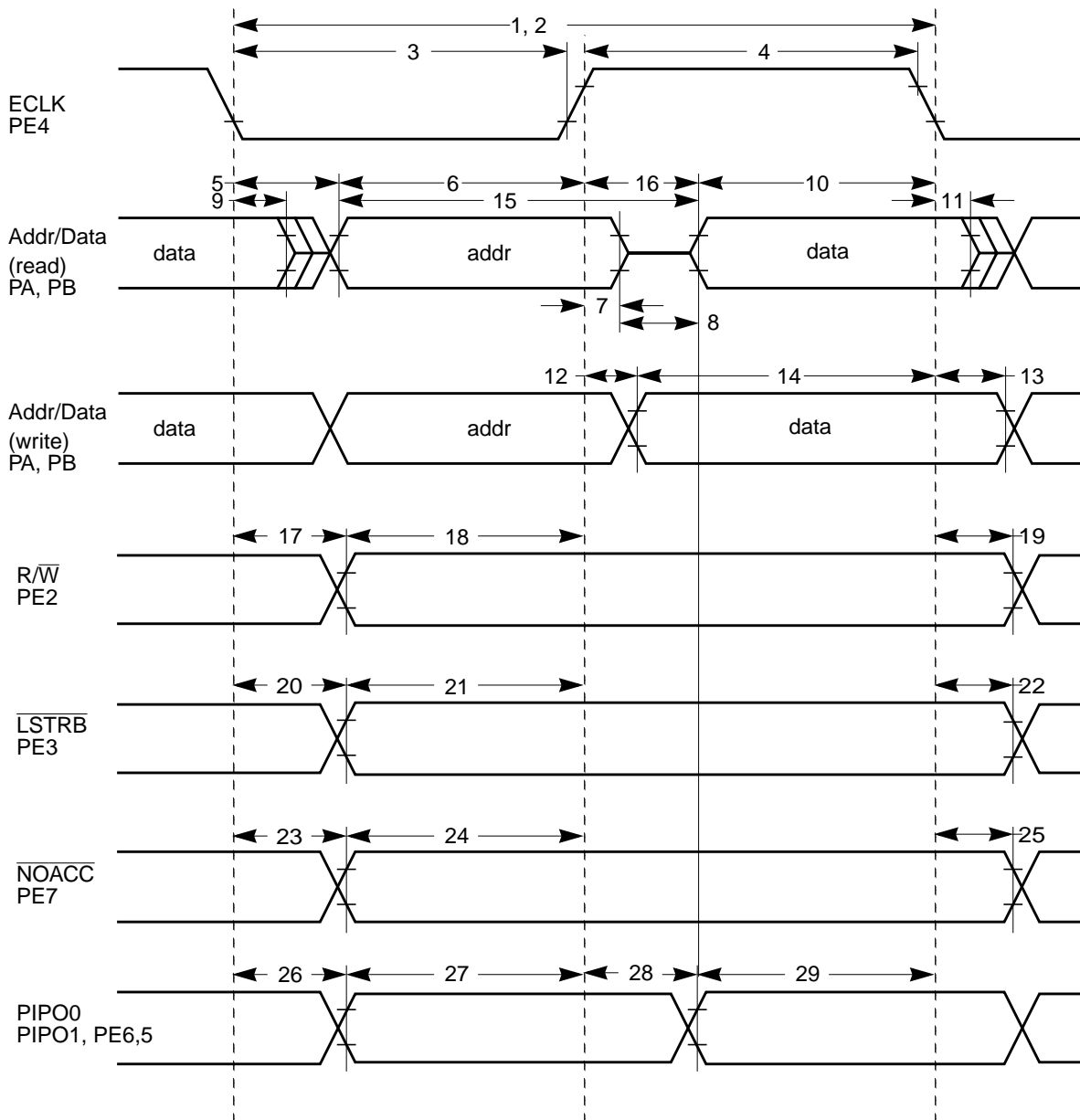


Table C-4 Expanded Bus Timing Characteristics (5V Range)

| Conditions are 4.75V < VDDX < 5.25V, Junction Temperature -40°C to +140°C, C _{LOAD} = 50pF | | | | | | | |
|---|---|---|-------------------|-----|-----|------|------|
| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
| 1 | P | Frequency of operation (E-clock) | f _o | 0 | | 25.0 | MHz |
| 2 | P | Cycle time | t _{cyc} | 40 | | | ns |
| 3 | D | Pulse width, E low | PW _{EL} | 19 | | | ns |
| 4 | D | Pulse width, E high ¹ | PW _{EH} | 19 | | | ns |
| 5 | D | Address delay time | t _{AD} | | | 8 | ns |
| 6 | D | Address valid time to E rise (PW _{EL} -t _{AD}) | t _{AV} | 11 | | | ns |
| 7 | D | Muxed address hold time | t _{MAH} | 2 | | | ns |
| 8 | D | Address hold to data valid | t _{AHDS} | 7 | | | ns |
| 9 | D | Data hold to address | t _{DHA} | 2 | | | ns |
| 10 | D | Read data setup time | t _{DSR} | 13 | | | ns |
| 11 | D | Read data hold time | t _{DHR} | 0 | | | ns |
| 12 | D | Write data delay time | t _{DDW} | | | 7 | ns |
| 13 | D | Write data hold time | t _{DHW} | 2 | | | ns |
| 14 | D | Write data setup time ⁽¹⁾ (PW _{EH} -t _{DDW}) | t _{DSW} | 12 | | | ns |
| 15 | D | Address access time ⁽¹⁾ (t _{cyc} -t _{AD} -t _{DSR}) | t _{ACCA} | 19 | | | ns |
| 16 | D | E high access time ⁽¹⁾ (PW _{EH} -t _{DSR}) | t _{ACCE} | 6 | | | ns |
| 17 | D | Read/write delay time | t _{RWD} | | | 7 | ns |
| 18 | D | Read/write valid time to E rise (PW _{EL} -t _{RWD}) | t _{RWV} | 14 | | | ns |
| 19 | D | Read/write hold time | t _{RWH} | 2 | | | ns |
| 20 | D | Low strobe delay time | t _{LSD} | | | 7 | ns |
| 21 | D | Low strobe valid time to E rise (PW _{EL} -t _{LSD}) | t _{LSV} | 14 | | | ns |
| 22 | D | Low strobe hold time | t _{LSH} | 2 | | | ns |
| 23 | D | NOACC strobe delay time | t _{NOD} | | | 7 | ns |
| 24 | D | NOACC valid time to E rise (PW _{EL} -t _{LSD}) | t _{NOV} | 14 | | | ns |
| 25 | D | NOACC hold time | t _{NOH} | 2 | | | ns |
| 26 | D | IPIPO[1:0] delay time | t _{P0D} | 2 | | 7 | ns |
| 27 | D | IPIPO[1:0] valid time to E rise (PW _{EL} -t _{P0D}) | t _{P0V} | 11 | | | ns |
| 28 | D | IPIPO[1:0] delay time ⁽¹⁾ (PW _{EH} -t _{P1V}) | t _{P1D} | 2 | | 25 | ns |
| 29 | D | IPIPO[1:0] valid time to E fall | t _{P1V} | 11 | | | ns |

NOTES:

1. Affected by clock stretch: add N x t_{cyc} where N=0,1,2 or 3, depending on the number of clock stretches.

Table C-5 Expanded Bus Timing Characteristics (3.3V Range)Conditions are VDDX=3.3V+/-10%, Junction Temperature -40°C to +140°C, C_{LOAD} = 50pF

| Num | C | Rating | Symbol | Min | Typ | Max | Unit |
|-----|---|--|------------------|------|-----|------|------|
| 1 | D | Frequency of operation (E-clock) | f_o | 0 | | 16.0 | MHz |
| 2 | D | Cycle time | t_{cyc} | 62.5 | | | ns |
| 3 | D | Pulse width, E low | PW _{EL} | 30 | | | ns |
| 4 | D | Pulse width, E high ¹ | PW _{EH} | 30 | | | ns |
| 5 | D | Address delay time | t_{AD} | | | 16 | ns |
| 6 | D | Address valid time to E rise (PW _{EL} - t_{AD}) | t_{AV} | 16 | | | ns |
| 7 | D | Muxed address hold time | t_{MAH} | 2 | | | ns |
| 8 | D | Address hold to data valid | t_{AHDS} | 7 | | | ns |
| 9 | D | Data hold to address | t_{DHA} | 2 | | | ns |
| 10 | D | Read data setup time | t_{DSR} | 15 | | | ns |
| 11 | D | Read data hold time | t_{DHR} | 0 | | | ns |
| 12 | D | Write data delay time | t_{DDW} | | | 15 | ns |
| 13 | D | Write data hold time | t_{DHW} | 2 | | | ns |
| 14 | D | Write data setup time ⁽¹⁾ (PW _{EH} - t_{DDW}) | t_{DSW} | 15 | | | ns |
| 15 | D | Address access time ⁽¹⁾ | t_{ACCA} | 29 | | | ns |
| 16 | D | E high access time ⁽¹⁾ (PW _{EH} - t_{DSR}) | t_{ACCE} | 15 | | | ns |
| 17 | D | Read/write delay time | t_{RWD} | | | 14 | ns |
| 18 | D | Read/write valid time to E rise (PW _{EL} - t_{RWD}) | t_{RWV} | 16 | | | ns |
| 19 | D | Read/write hold time | t_{RWH} | 2 | | | ns |
| 20 | D | Low strobe delay time | t_{LSD} | | | 14 | ns |
| 21 | D | Low strobe valid time to E rise (PW _{EL} - t_{LSD}) | t_{LSV} | 16 | | | ns |
| 22 | D | Low strobe hold time | t_{LSH} | 2 | | | ns |
| 23 | D | NOACC strobe delay time | t_{NOD} | | | 14 | ns |
| 24 | D | NOACC valid time to E rise (PW _{EL} - t_{LSD}) | t_{NOV} | 16 | | | ns |
| 25 | D | NOACC hold time | t_{NOH} | 2 | | | ns |
| 26 | D | IPIPO[1:0] delay time | t_{POD} | 2 | | 14 | ns |
| 27 | D | IPIPO[1:0] valid time to E rise (PW _{EL} - t_{POD}) | t_{POV} | 16 | | | ns |
| 28 | D | IPIPO[1:0] delay time ⁽¹⁾ | t_{P1D} | 2 | | 25 | ns |
| 29 | D | IPIPO[1:0] valid time to E fall | t_{P1V} | 11 | | | ns |

NOTES:

1. Affected by clock stretch: add $N \times t_{cyc}$ where $N=0,1,2$ or 3 , depending on the number of clock stretches.

Appendix D Package Information

D.1 General

This section provides the physical dimensions of the MC9S12C Family and MC9S12GC Family packages 48LQFP, 52LQFP, 80QFP.

D.2 80-pin QFP package

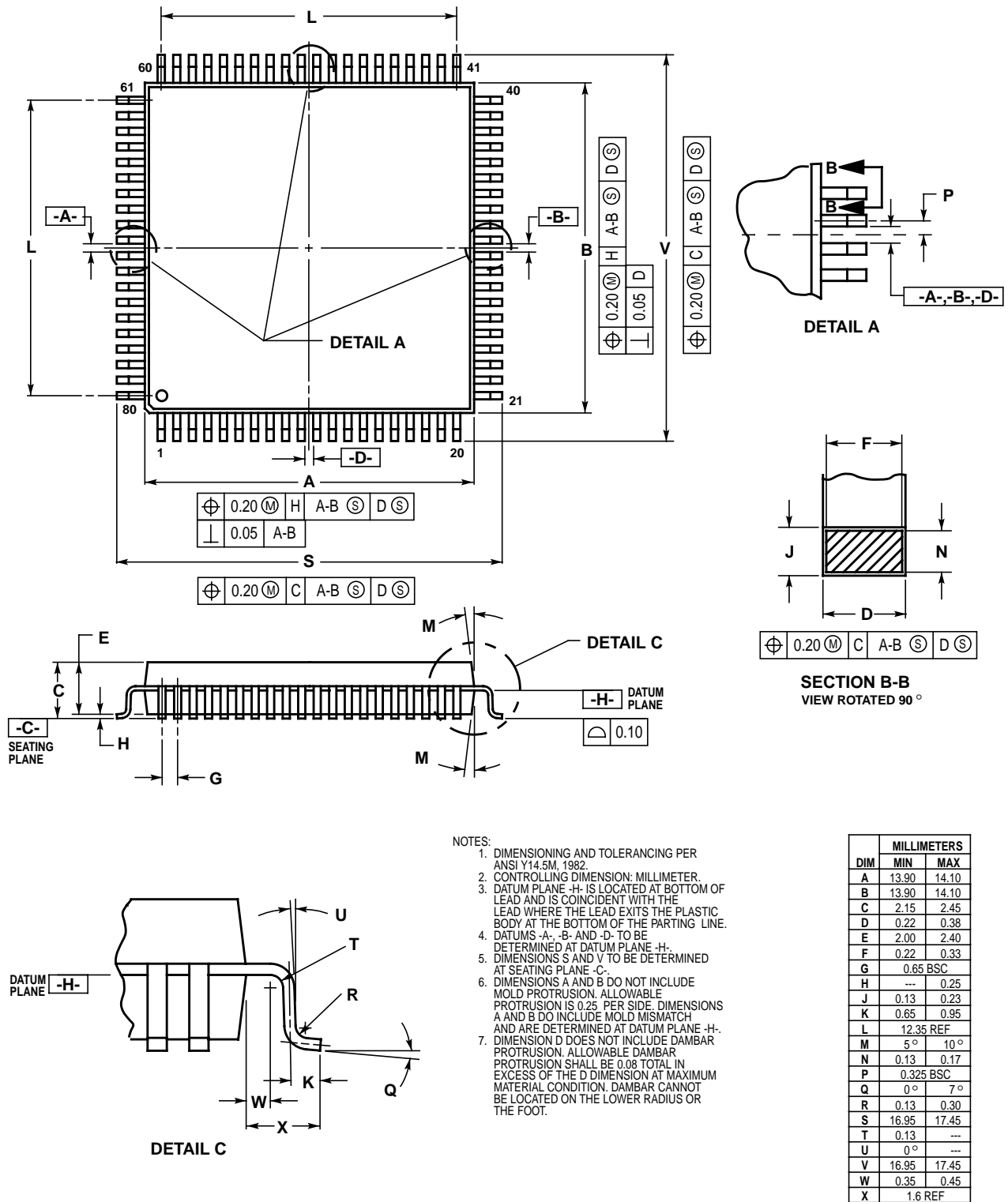


Figure D-1 80-pin QFP Mechanical Dimensions (case no. 841B)

D.3 52-pin LQFP package

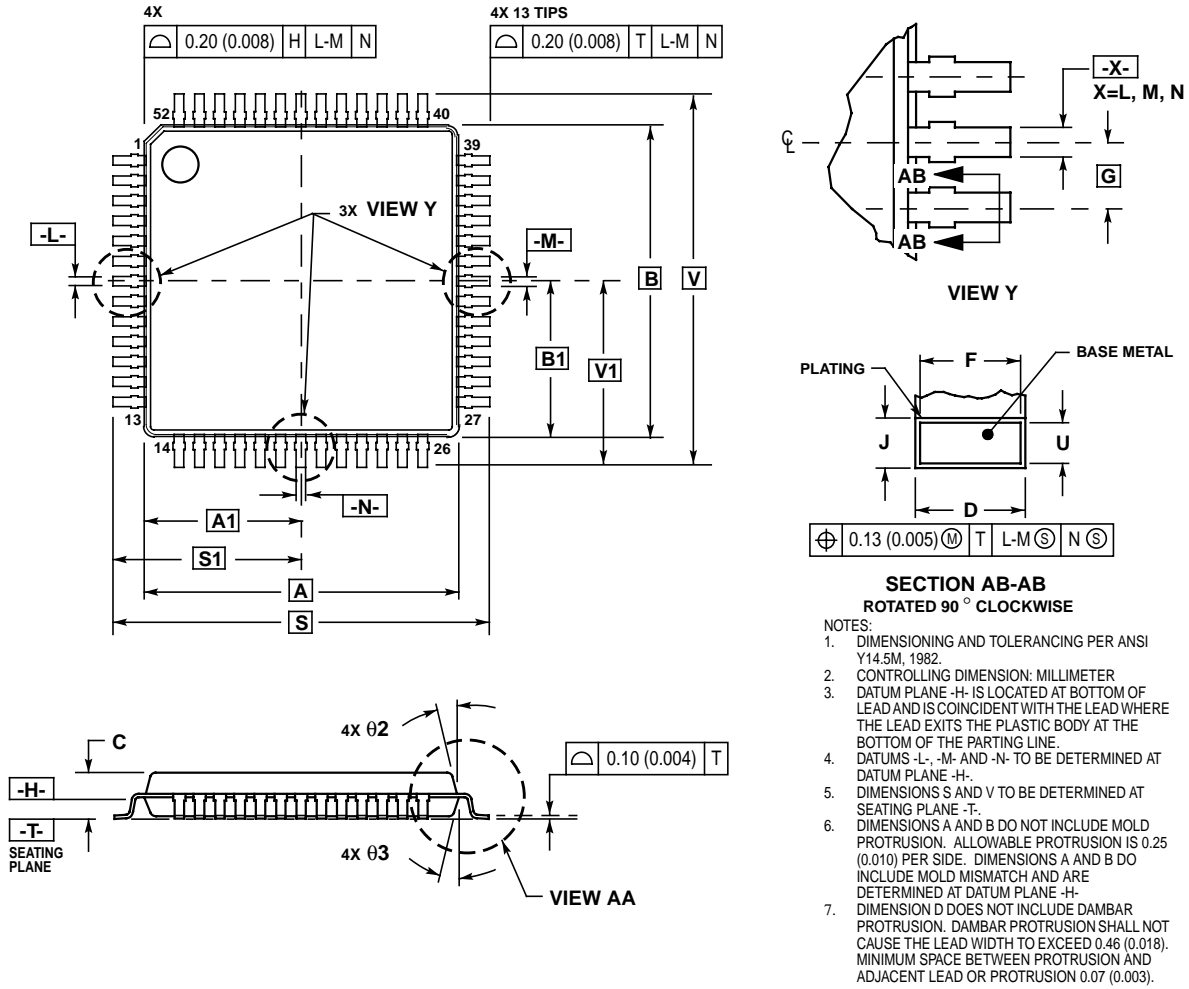


Figure D-2 52-pin LQFP Mechanical Dimensions (case no. 848D-03)

D.4 48-pin LQFP package

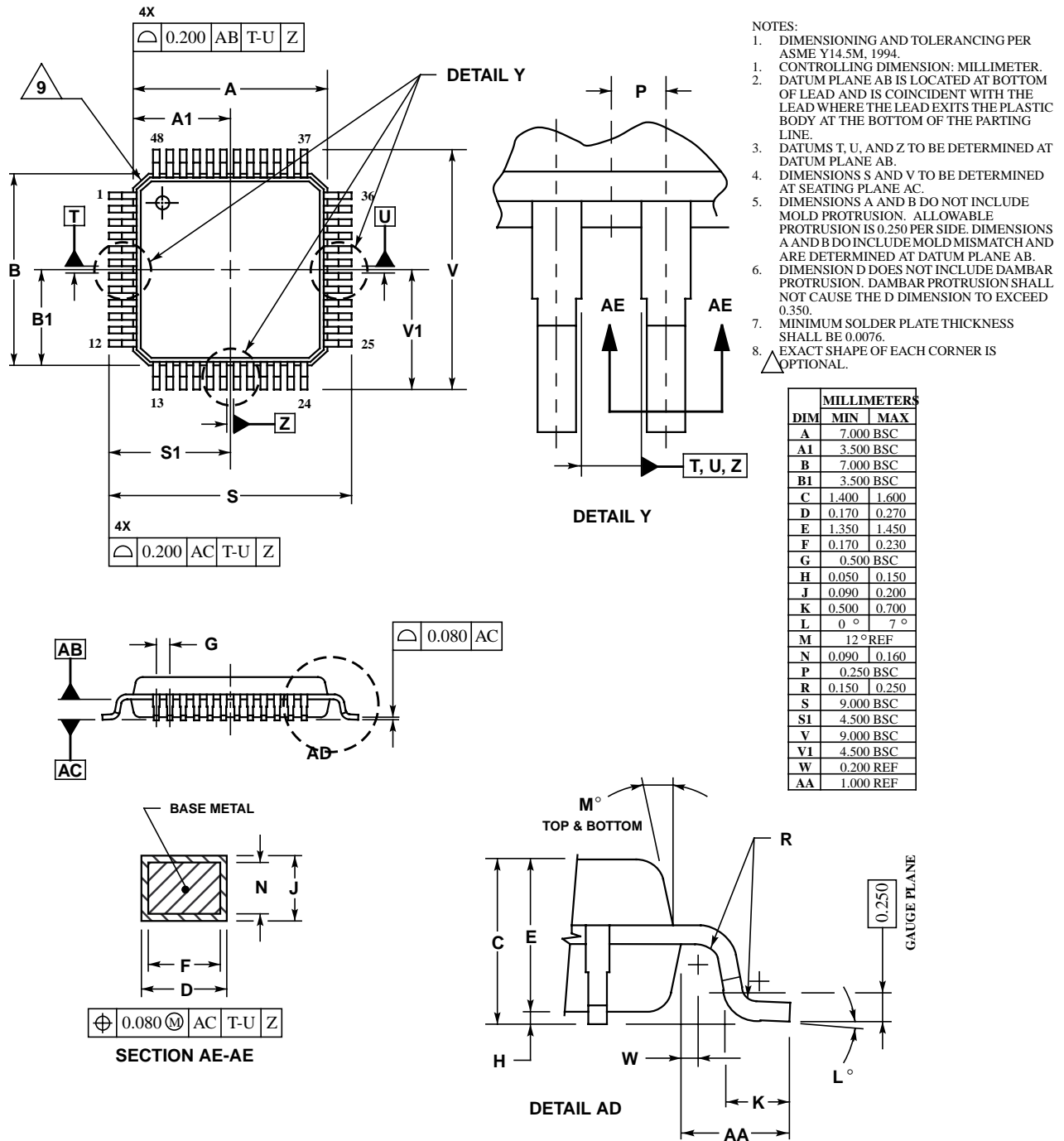


Figure D-3 48-pin LQFP Mechanical Dimensions (case no.932-03 ISSUE F)

E.1.1 PK[2:0] / XADDR[16:14]

PK2-PK0 provide the expanded address XADDR[16:14] for the external bus.

Refer to the S12 Core user guide for detailed information about external address page access.

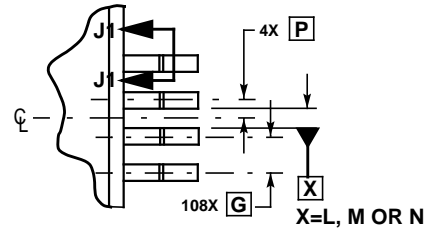
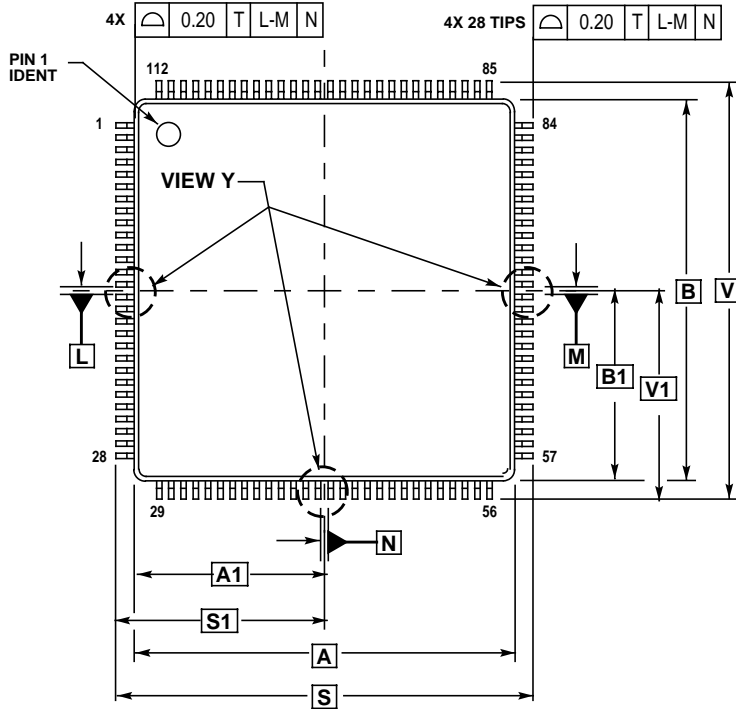
| Pin Name Function 1 | Pin Name Function 2 | Power Domain | Internal Pull Resistor | | Description |
|---------------------|---------------------|--------------|------------------------|-------------|-----------------|
| | | | CTRL | Reset State | |
| PK[2:0] | XADDR[16:14] | VDDX | PUPKE | Up | Port K I/O Pins |

The reset state of DDRK in the S12_CORE is \$00, configuring the pins as inputs.

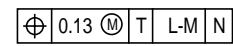
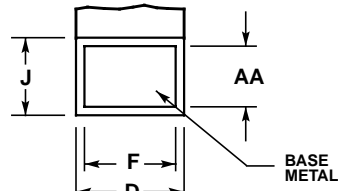
The reset state of PUPKE in the PUCR register of the S12_CORE is "1" enabling the internal pullup resistors at PortK[2:0].

In this reset state the pull-up resistors provide a defined state and prevent a floating input, thereby preventing unnecessary current consumption at the input stage.

E.2 112-pin LQFP package



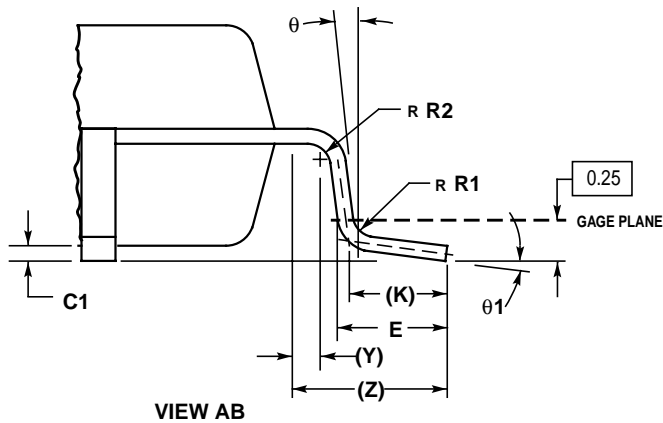
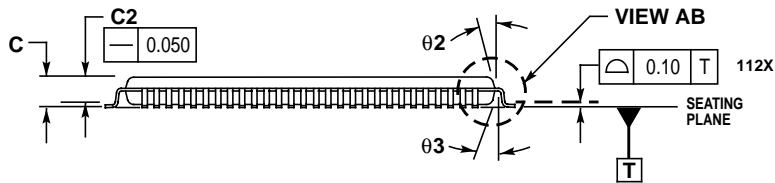
VIEW Y



SECTION J1-J1
ROTATED 90° COUNTERCLOCKWISE

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.46.



| DIM | MILLIMETERS | |
|---------|-------------|-------|
| | MIN | MAX |
| A | 20.000 | BSC |
| A1 | 10.000 | BSC |
| B | 20.000 | BSC |
| B1 | 10.000 | BSC |
| C | --- | 1.600 |
| C1 | 0.050 | 0.150 |
| C2 | 1.350 | 1.450 |
| D | 0.270 | 0.370 |
| E | 0.450 | 0.750 |
| F | 0.270 | 0.330 |
| G | 0.650 | BSC |
| J | 0.090 | 0.170 |
| K | 0.500 | REF |
| P | 0.325 | BSC |
| R1 | 0.100 | 0.200 |
| R2 | 0.100 | 0.200 |
| S | 22.000 | BSC |
| S1 | 11.000 | BSC |
| V | 22.000 | BSC |
| V1 | 11.000 | BSC |
| Y | 0.250 | REF |
| Z | 1.000 | REF |
| AA | 0.090 | 0.160 |
| theta | 0° | 8° |
| theta 1 | 3° | 7° |
| theta 2 | 11° | 13° |
| theta 3 | 11° | 13° |

Figure 19-2 112-pin LQFP mechanical dimensions (case no. 987)80-pin QFP Mechanical Dimensions (case no. 841B)

Device User Guide End Sheet

**FINAL PAGE OF
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