PNX2000

Audio video input processor

Rev. 03 – 23 August 2004 Product data

1. General description

The PNX2000 is a companion IC for use with the Nexperia™ [1] digital video home entertainment engines such as PNX8526 and PNX8550.

The PNX2000 is always used in combination with the PNX3000.

PNX2000 is intended for mid to high-end analog and hybrid TV sets, performing input decoding of single stream analog audio and single stream analog video signals. In addition, the PNX2000 is used for decoding and presentation of all audio output streams in the system. Figure 1 shows a block diagram of the device.

2. Features

- Detection of PAL, NTSC or SECAM, and various $1f_H$ and $2f_H$ component video input sources.
- Full support for $1f_H$ and $2f_H$ video sources; progressive and interlaced.
- Decoding for global VBI Standards (WST, WSS, VPS, CC, VITC).
- ITU-656 output interface.
- Global multi-standard audio demodulation and decoding.
- Dolby Pro Logic II™ [2] multi-channel audio decoding and post-processing.
- Advanced fully programmable audio post-processing functions, including psychoacoustic spatial algorithms for optimal loudspeaker matching.

3. Applications

- Analog TV receivers.
- Hybrid TV receivers.
- DVD recorders.
- VCRs.

1. Nexperia is a trademark of Koninklijke Philips Electronics N.V.
2. Dolby is a trademark of Dolby Laboratories

PHILIPS

4. Ordering information

Table 1: Ordering information

Type number	Package name	Description	Version
PNX2000HL	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

5. Block diagram

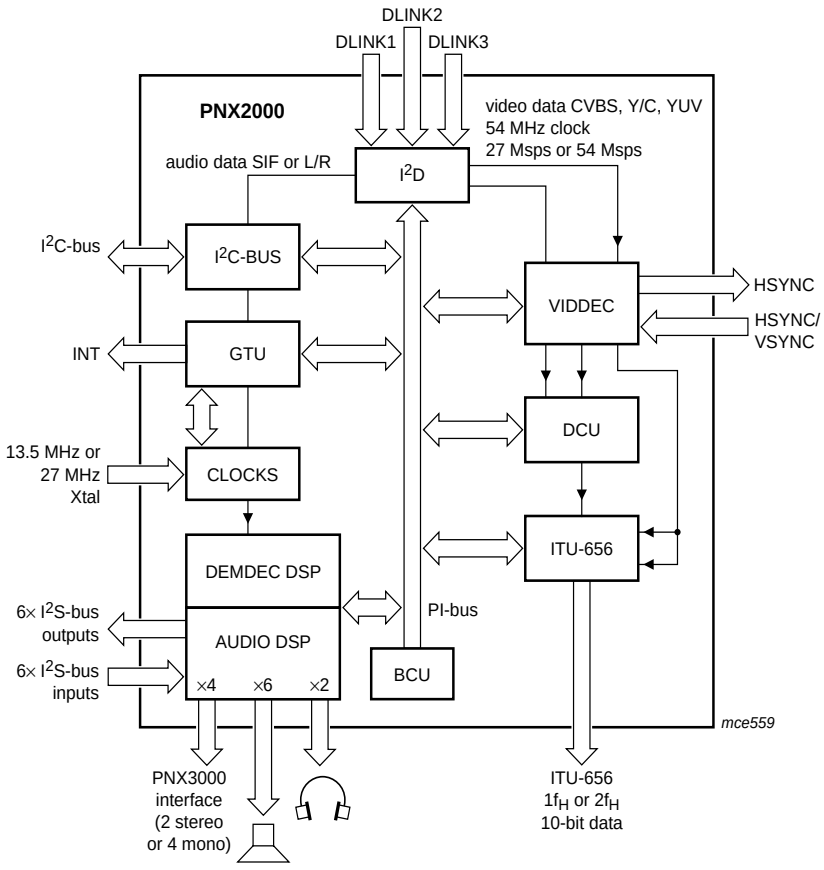


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

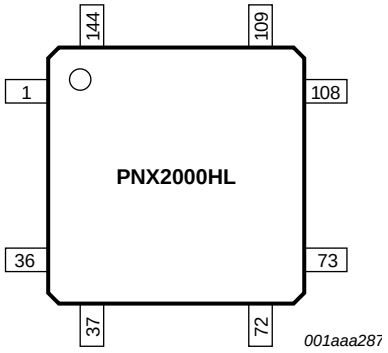


Fig 2. Pin configuration

6.1.1 Pin description

Table 2 describes acronyms used in the pin tables:

Table 2: Acronym description

Acronym	Description
3V	3.3 V LVCMOS
5VT	5 V tolerant inputs
Z	3-state
TTL	TTL logic
TTL-H	TTL with hysteresis
CMOS	CMOS logic
IA	Input Analog
ID	Input Digital
OD	Output Digital
OA	Output Analog
IOA	I/O Analog
IOD	I/O Digital
GA	Ground Analog
SA	Supply Analog
SD	Supply Digital
OSCIN	Crystal Oscillator Input
OSCOUT	Crystal Oscillator Output
OSCGND	Crystal Oscillator Ground

Table 3: Pins in numerical sequence

Pin	Symbol	Type	Description
1	$V_{SSD(I2D)}$	GD	I^2D digital ground
2	DLINK1DP	IA	analog differential data link 1 positive termination
3	DLINK1DN	IA	analog differential data link 1 negative termination
4	DLINK1SP	IA	analog differential strobe link 1 positive termination
5	DLINK1SN	IA	analog differential strobe link 1 negative termination
7	DLINK2DP	IA	analog differential data link 2 positive termination
8	DLINK2DN	IA	analog differential data link 2 negative termination
9	DLINK2SP	IA	analog differential strobe link 2 positive termination
10	DLINK2SN	IA	analog differential strobe link 2 negative termination
12	DLINK3DP	IA	analog differential data link 3 positive termination
13	DLINK3DN	IA	analog differential data link 3 negative termination
14	DLINK3SP	IA	analog differential strobe link 3 positive termination
15	DLINK3SN	IA	analog differential strobe link 3 negative termination
16	$V_{DDD(I2D)}$	SD	I^2D digital 1.8 V supply voltage
17	I2C_ADR	ID	I^2C-bus address select (internal pull-down); TTL; 5VT
18	HSYNCFBL1	IA	horizontal sync (external); fastblanking signal from SCART
19	HSYNCFBL2	IA	horizontal sync (external); fastblanking signal from SCART
20	HVINFO	OD	horizontal and vertical sync information to PNX3000; CMOS
21	VSYNC1	ID	vertical sync (external); TTL; 5VT
22	VSYNC2	ID	vertical sync (external); TTL; 5VT
23	$V_{DD3(DTC)}$	SD	DTC 3.3 V supply voltage
24	$V_{DDD(DTC)}$	SD	DTC 1.8 V supply voltage
25	$V_{SS(DTC)}$	GA	DTC analog ground
26	I2C_SCL	IOD	I^2C-bus clock; TTL; Z; 5VT
27	I2C_SDA	IOD	I^2C-bus data; TTL; Z; 5VT
28	V_{SSE}	-	3.3 V ground
29	V_{SS}	-	1.8 V ground
30	V_{DDI}	-	1.8 V supply voltage
31	MPIFCLK	OD	13.5 MHz or 27 MHz to PNX3000; CMOS
32	V_{DDE}	-	3.3 V supply voltage
33	$V_{DDA(PLL)}$	-	phase locked loop 1.8 V supply voltage
34	-	n.c.	not connected
35	V_{DDI}	-	1.8 V supply voltage
36	V_{SS}	-	1.8 V ground
37	$V_{DDA(XTAL)}$	OSCVDD	1.8 V crystal oscillator supply voltage
38	XIN	OSCIN	crystal oscillator input
39	XOUT	OSCOUT	crystal oscillator output
40	XGND	OSCGND	crystal oscillator ground

Table 3: Pins in numerical sequence...*continued*

Pin	Symbol	Type	Description
41	V_{SSE}	-	3.3 V ground
42	V_{DDI}	-	1.8 V supply voltage
43	V_{SS}	-	1.8 V ground
44	V_{DDM}	-	1.8 V supply voltage for KSFRAMs and KROMs
45	RESET_N	IA	external reset input
46	RESET_SEL	ID	selects between using an external reset input or using internal POR; TTL; 5VT
47	DCLK	OD	reserved; CMOS
48	INTOUT	OD	interrupt line output; Z; 5VT
49	V_{DDE}	-	3.3 V supply voltage
50	LL_CLK	ID	reserved; TTL; 5VT
51	DVO_CLK	OD	digital video output clock; CMOS; Z
52	DVO_VALID	OD	digital video data valid; CMOS; Z
53	V_{DDI}	-	1.8 V supply voltage
54	V_{SS}	-	1.8 V ground
55	DVO_DATA_0	OD	digital video output state 0; CMOS; Z
56	DVO_DATA_1	OD	digital video output state 1; CMOS; Z
57	DVO_DATA_2	OD	digital video output state 2; CMOS; Z
58	DVO_DATA_3	OD	digital video output state 3; CMOS; Z
59	V_{SSE}	-	3.3 V ground
60	DVO_DATA_4	OD	digital video output state 4; CMOS; Z
61	DVO_DATA_5	OD	digital video output state 5; CMOS; Z
62	DVO_DATA_6	OD	digital video output state 6; CMOS; Z
63	DVO_DATA_7	OD	digital video output state 7; CMOS; Z
64	DVO_DATA_8	OD	digital video output state 8; CMOS; Z
65	DVO_DATA_9	OD	digital video output state 9; CMOS; Z
66	V_{DDE}	-	3.3 V supply voltage
67	V_{DDI}	-	1.8 V supply voltage
68	V_{SS}	-	1.8 V ground
69	I2S_OUT_SD3	OD	I^2S-bus data-out channel 3; CMOS
70	I2S_OUT_SD3_WS	OD	I^2S-bus word select channel 3; CMOS
71	I2S_OUT_SD3_SCK	OD	I^2S-bus bit clock channel 3; CMOS
72	V_{SSE}	-	3.3 V ground
73	I2S_OUT_SD6	OD	I^2S-bus data out channel 6; CMOS
74	I2S_OUT_SD5	OD	I^2S-bus data out channel 5; CMOS
75	I2S_OUT_SD4	OD	I^2S-bus data out channel 4; CMOS
76	I2S_OUT_SD2	OD	I^2S-bus data out channel 2; CMOS
77	I2S_OUT_SD1	OD	I^2S-bus data out channel 1; CMOS
78	I2S_WS_SYS	IOD	I^2S-bus system word select; TTL-H; CMOS
79	I2S_SCK_SYS	IOD	I^2S-bus system bit clock; TTL-H; CMOS
80	V_{DDI}	-	1.8 V supply voltage

Table 3: Pins in numerical sequence...*continued*

Pin	Symbol	Type	Description
81	V_{SS}	-	1.8 V ground
82	V_{DDE}	-	3.3 V supply voltage
83	I2S_IN_SD6	ID	I^2S-bus data in channel 6; TTL; 5VT
84	I2S_IN_SD5	ID	I^2S-bus data in channel 5; TTL; 5VT
85	I2S_IN_SD4	ID	I^2S-bus data in channel 4; TTL; 5VT
86	I2S_IN_SD3	ID	I^2S-bus data in channel 3; TTL; 5VT
87	I2S_IN_SD2	ID	I^2S-bus data in channel 2; TTL; 5VT
88	I2S_IN_SD1	ID	I^2S-bus data in channel 1; TTL; 5VT
89	ADAC_CLK	OD	Used for 128 f_s or 256 f_s clock output to external audio DAC; CMOS.
90	-	n.c.	not connected
91	V_{DDE}	-	3.3 V supply voltage
92	TDI	ID	JTAG test data in; TTL-H; 5VT
93	TDO	OD	JTAG test data out; CMOS
94	TCK	ID	JTAG test clock; TTL-H; 5VT
95	TMS	ID	JTAG test mode select; TTL-H; 5VT
96	TRST_N	ID	JTAG reset (active low); TTL-H; 5VT
97	V_{DDI}	-	1.8 V supply voltage
98	V_{SS}	-	1.8 V ground
99	V_{SSE}	-	3.3 V ground
100	$V_{SS(ADAC)}$	GD	audio DAC 1.8 V digital ground
101	$V_{DDD(ADAC)}$	SD	audio DAC 1.8 V digital supply voltage
102	$V_{DDA(ADAC)}$	SA	audio DAC 3.3 V supply voltage
103	ADAC1_P	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
104	ADAC1	OA	analog audio output 1
105	ADAC1_N	GA	Negative analog reference star connected at PNX3000.
106	ADAC2_N	GA	Negative analog reference star connected at PNX3000.
107	ADAC2	OA	analog audio output 2
108	ADAC2_P	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
109	ADAC3_P	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
110	ADAC3	OA	analog audio output 3
111	ADAC3_N	GA	Negative analog reference star connected at PNX3000.
112	ADAC4_N	GA	Negative analog reference star connected at PNX3000.
113	ADAC4	OA	analog audio output 4
114	ADAC4_P	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.

Table 3: Pins in numerical sequence...*continued*

Pin	Symbol	Type	Description
115	ADAC5_P	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
116	ADAC5	OA	analog audio output 5
117	ADAC5_N	GA	Negative analog reference star connected at PNX3000.
118	ADAC6_N	GA	Negative analog reference star connected at PNX3000.
119	ADAC6	OA	analog audio output 6
120	ADAC6_P	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
121	ADAC7_P	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
122	ADAC7	OA	analog audio output 7
123	ADAC7_N	GA	Negative analog reference star connected at PNX3000.
124	ADAC8_N	GA	Negative analog reference star connected at PNX3000.
125	ADAC8	OA	analog audio output 8
126	ADAC8_P	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
127	ADAC9_P	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
128	ADAC9	OA	analog audio output 9
129	ADAC9_N	GA	Negative analog reference star connected at PNX3000.
130	ADAC10_N	GA	Negative analog reference star connected at PNX3000.
131	ADAC10	OA	analog audio output 10
132	ADAC10_P	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
133	ADAC11_P	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
134	ADAC11	OA	analog audio output 11
135	ADAC11_N	GA	Negative analog reference star connected at PNX3000.
136	ADAC12_N	GA	Negative analog reference star connected at PNX3000.
137	ADAC12	OA	analog audio output 12
138	ADAC12_P	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
139	V_{SS}	-	1.8 V ground
140	V_{DDM}	-	1.8 V supply voltage for KSFRAMs and KROMs
141	V_{DDE}	-	3.3 V supply voltage

Table 3: Pins in numerical sequence...*continued*

Pin	Symbol	Type	Description
142	V_{SSE}	-	3.3 V ground
143	V_{DDE}	-	3.3 V supply voltage
144	V_{SSE}	-	3.3 V ground

In the tables that follow, signals of the PNX2000 have been sorted by functional group. For quick reference Table 4 identifies each functional group and associated table.

Table 4: Signal groups

Functional group	Table number
I^2C-bus	Table 5
AUDIO	Table 6
I^2S-bus	Table 7
VIDDEC	Table 8
ITU-656	Table 9
JTAG	Table 10
I^2C-bus	Table 11
CLOCK	Table 12
GTU	Table 13
RESET	Table 14
DIGITAL SUPPLY	Table 15
ANALOG SUPPLY	Table 16

Table 5: I^2D pins

Symbol	Pin	Type	Description
DLINK1DP	2	IA	analog differential data link 1 positive termination
DLINK1DN	3	IA	analog differential data link 1 negative termination
DLINK1SP	4	IA	analog differential strobe link 1 positive termination
DLINK1SN	5	IA	analog differential strobe link 1 negative termination
DLINK2DP	7	IA	analog differential data link 2 positive termination
DLINK2DN	8	IA	analog differential data link 2 negative termination
DLINK2SP	9	IA	analog differential strobe link 2 positive termination
DLINK2SN	10	IA	analog differential strobe link 2 negative termination
DLINK3DP	12	IA	analog differential data link 3 positive termination
DLINK3DN	13	IA	analog differential data link 3 negative termination
DLINK3SP	14	IA	analog differential strobe link 3 positive termination
DLINK3SN	15	IA	analog differential strobe link 3 negative termination

Table 6: Audio pins

Symbol	Pin	Type	Description
ADAC1	104	OA	analog audio output 1
ADAC2	107	OA	analog audio output 2
ADAC3	110	OA	analog audio output 3
ADAC4	113	OA	analog audio output 4

Table 6: Audio pins...*continued*

Symbol	Pin	Type	Description
ADAC5	116	OA	analog audio output 5
ADAC6	119	OA	analog audio output 6
ADAC7	122	OA	analog audio output 7
ADAC8	125	OA	analog audio output 8
ADAC9	128	OA	analog audio output 9
ADAC10	131	OA	analog audio output 10
ADAC11	134	OA	analog audio output 11
ADAC12	137	OA	analog audio output 12
ADAC1_P	103	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
ADAC1_N	105	GA	Negative analog reference star connected at PNX3000.
ADAC2_P	108	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
ADAC2_N	106	GA	Negative analog reference star connected at PNX3000.
ADAC3_P	109	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
ADAC3_N	111	GA	Negative analog reference star connected at PNX3000.
ADAC4_P	114	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
ADAC4_N	112	GA	Negative analog reference star connected at PNX3000.
ADAC5_P	115	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
ADAC5_N	117	GA	Negative analog reference star connected at PNX3000.
ADAC6_P	120	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
ADAC6_N	118	GA	Negative analog reference star connected at PNX3000.
ADAC7_P	121	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
ADAC7_N	123	GA	Negative analog reference star connected at PNX3000.
ADAC8_P	126	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
ADAC8_N	124	GA	Negative analog reference star connected at PNX3000.
ADAC9_P	127	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
ADAC9_N	129	GA	Negative analog reference star connected at PNX3000.
ADAC10_P	132	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
ADAC10_N	130	GA	Negative analog reference star connected at PNX3000.
ADAC11_P	133	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
ADAC11_N	135	GA	Negative analog reference star connected at PNX3000.
ADAC12_P	138	SA	Positive analog reference derived via emitter follower from PNX3000 V_SND pin.
ADAC12_N	136	GA	Negative analog reference star connected at PNX3000.

Table 7: I^2S-bus pins

Symbol	Pin	Type	Description
I2S_IN_SD1	88	ID	I^2S-bus data in channel 1; TTL; 5VT
I2S_IN_SD2	87	ID	I^2S-bus data in channel 2; TTL; 5VT
I2S_IN_SD3	86	ID	I^2S-bus data in channel 3; TTL; 5VT
I2S_IN_SD4	85	ID	I^2S-bus data in channel 4; TTL; 5VT
I2S_IN_SD5	84	ID	I^2S-bus data in channel 5; TTL; 5VT
I2S_IN_SD6	83	ID	I^2S-bus data in channel 6; TTL; 5VT
I2S_OUT_SD1	77	OD	I^2S-bus data out channel 1; CMOS
I2S_OUT_SD2	76	OD	I^2S-bus data out channel 2; CMOS
I2S_OUT_SD4	75	OD	I^2S-bus data out channel 4; CMOS
I2S_OUT_SD5	74	OD	I^2S-bus data out channel 5; CMOS
I2S_OUT_SD6	73	OD	I^2S-bus data out channel 6; CMOS
I2S_OUT_SD3_SCK	71	OD	I^2S-bus bit clock channel 3; CMOS
I2S_OUT_SD3_WS	70	OD	I^2S-bus word select channel 3; CMOS
I2S_OUT_SD3	69	OD	I^2S-bus data-out channel 3; CMOS
I2S_SCK_SYS	79	IOD	I^2S-bus system bit clock; TTL-H; CMOS
I2S_WS_SYS	78	IOD	I^2S-bus system word select; TTL-H; CMOS
ADAC_CLK	89	OD	Used for 128 f_s or 256 f_s clock output to external audio DAC; CMOS.

Table 8: VIDDEC pins

Symbol	Pin	Type	Description
HVINFO	20	OD	horizontal and vertical sync information to PNX3000; CMOS
HSYNCFBL1	18	IA	horizontal sync (external); fastblanking signal from SCART
HSYNCFBL2	19	IA	horizontal sync (external); fastblanking signal from SCART
VSYNC1	21	ID	vertical sync (external); TTL; 5VT
VSYNC2	22	ID	vertical sync (external); TTL; 5VT

Table 9: ITU-656 pins

Symbol	Pin	Type	Description
DVO_DATA_0	55	OD	digital video output state 0; CMOS; Z
DVO_DATA_1	56	OD	digital video output state 1; CMOS; Z
DVO_DATA_2	57	OD	digital video output state 2; CMOS; Z
DVO_DATA_3	58	OD	digital video output state 3; CMOS; Z
DVO_DATA_4	60	OD	digital video output state 4; CMOS; Z
DVO_DATA_5	61	OD	digital video output state 5; CMOS; Z
DVO_DATA_6	62	OD	digital video output state 6; CMOS; Z
DVO_DATA_7	63	OD	digital video output state 7; CMOS; Z
DVO_DATA_8	64	OD	digital video output state 8; CMOS; Z
DVO_DATA_9	65	OD	digital video output state 9; CMOS; Z

Table 9: ITU-656 pins...*continued*

Symbol	Pin	Type	Description
DVO_VALID	52	OD	digital video data valid; CMOS; Z
DVO_CLK	51	OD	digital video output clock; CMOS; Z
LL_CLK	50	ID	reserved; TTL; 5VT [1]

[1] It is recommended to bias this pad with a 10 kΩ resistor

Table 10: JTAG pins

Symbol	Pin	Type	Description
TDO	93	OD	JTAG test data out; CMOS
TDI	92	ID	JTAG test data in; TTL-H; 5VT
TCK	94	ID	JTAG test clock; TTL-H; 5VT
TRST_N [1]	96	ID	JTAG reset (active low); TTL-H; 5VT
TMS	95	ID	JTAG test mode select; TTL-H; 5VT

[1] It is recommended to pull-down TRST_N with a 10 kΩ resistor. This ensures correct reset state of internal TAP circuitry and correct POR of the device within defined state machine.

Table 11: I^2C-bus pins

Symbol	Pin	Type	Description
I2C_SDA	27	IOD	I^2C-bus data; TTL; Z; 5VT
I2C_SCL	26	IOD	I^2C-bus clock; TTL; Z; 5VT
I2C_ADR	17	ID	I^2C-bus address select (internal pull-down); TTL; 5VT

Table 12: Clock pins

Symbol	Pin	Type	Description
MPIFCLK	31	OD	13.5 MHz or 27 MHz to PNX3000; CMOS
DCLK	47	OD	reserved; CMOS
XIN	38	OSCIN	crystal oscillator input
XOUT	39	OSCOUT	crystal oscillator output
XGND	40	OSCGND	crystal oscillator ground

Table 13: GTU pins

Symbol	Pin	Type	Description
INTOUT	48	OD	interrupt line output; Z; 5VT

Table 14: Reset pins

Symbol	Pin	Type	Description
RESET_N	45	IA	external reset input
RESET_SEL	46	ID	selects between using an external reset input or using internal POR; TTL; 5VT HIGH = internal reset LOW = external reset

Table 15: Digital supply pins

Symbol	Pin	Type	Description
V_{DDE}	32,49,66, 82,91, 141,143	-	3.3 V supply voltage
V_{SSE}	28,41,59, 72,99, 142,144	-	3.3 V ground
V_{DDI} [1]	30,35,53,67, 80,97	-	1.8 V supply voltage
V_{SS}	29,36,43, 54,68,81, 98,139	-	1.8 V ground
V_{DDM} [1]	44,140	-	1.8 V supply voltage for KSFRAMs and KROMs
$V_{SSD(I2D)}$	1	GD	I^2D digital ground
$V_{DDD(I2D)}$	16	SD	I^2D digital 1.8 V supply voltage
$V_{SS(ADAC)}$	100	GD	audio DAC 1.8 V digital ground
$V_{DDD(ADAC)}$	101	SD	audio DAC 1.8 V digital supply voltage
$V_{DD3(DTC)}$	23	SD	DTC 3.3 V supply voltage
$V_{DDD(DTC)}$	24	SD	DTC 1.8 V supply voltage

[1] V_{DDI} and V_{DDM} can be connected to same 1.8 V supply voltage.

Table 16: Analog supply pins

Symbol	Pin	Type	Description
$V_{SSA(I2D)}$	6	GA	I^2D analog ground
$V_{DDA(I2D)}$	11	SA	I^2D analog 1.8 V supply voltage
$V_{DDA(PLL)}$	33	-	phase locked loop 1.8 V supply voltage
$V_{DDA(ADAC)}$	102	SA	audio DAC 3.3 V supply voltage
$V_{SS(DTC)}$	25	GA	DTC analog ground
$V_{DDA(XTAL)}$	37	OSCVDD	1.8 V crystal oscillator supply voltage

7. Functional description

7.1 Overview

Table 17 describes the functions of the hardware blocks (see also PNX2000 Block Diagram Figure 1).

For more detailed functional description refer to the *PNX2000 User Manual*.

Table 17: Block function

Function	Block	Description
High speed data link	I^2D	Receives data in three streams from PNX3000.
Video decoder processor	VIDDEC	Decodes and processes CVBS, YUV or Y/C in YUV stream.
Serial interface	I^2C-bus	To access all the internal registers.
Global Task Unit	GTU	Generates all the internal clocks, reset and power management.

Table 17: Block function...*continued*

Function	Block	Description
TV sound decoder	DEMDEC DSP	Demodulation, decoding of terrestrial TV audio standards .
Audio processor	AUDIO DSP	Processing analog and digital audio sources.
Data Capture Unit	DCU	Acquires VBI data (Teletext; CC; VPS) and formats in a stream.
Formatter unit	ITU-656	Formats YUV, VBI data and CVBS data in ITU-656.
Bus Control Unit	BCU	Bus arbitration among all the internal blocks.

7.2 Interfaces

Table 18: Interfaces

Interface	Description
I^2C-bus	The PNX2000 IC is controlled using an I^2C-bus. It performs like an I^2C-bus to PI-bus bridge, i.e. translates I^2C-bus slave received commands to PI-bus master commands.
I^2D	Receives data in three streams from PNX3000.
I^2S-bus	Serial digital audio interface (6 stereo inputs, 6 stereo outputs) for connection to other devices that support the I^2S-bus standard. Can be used to receive decoded sound from a multi-channel digital audio decoder, provide additional ADCs and DACs, or loop audio signals through an external processor or delay line.
ITU-656	Mainly intended to transfer output data stream externally to the PNX8550, but the output data stream could also be readable by other ITU-656 input devices that implement data valid signalling.
DACS	Digital-analog converters used to generate analog outputs from Sound Core.

7.3 Features in detail

7.3.1 Video

- Automatic Gain Control (AGC) to correct amplitude errors at input source.
- Synchronization identification (used for channel search).
- Sync processing for $1f_H$ and $2f_H$ video input source.
- Standard detection of PAL, NTSC or SECAM and various $1f_H$ and $2f_H$ component video input sources.

$1f_H$ video

- Color decoding (ITU-601) for PAL, NTSC or SECAM input sources.
- 2D comb filtering.
- Support for component video sources with sync on CVBS or green.
- Fastblank insertion of RGB signals onto CVBS input.

$2f_H$ video

- Support for various progressive and interlaced component video sources.
- Synchronization of video sources with sync on Y or external H/V inputs.

VBI data capture

- Decoding of 525 line standards; WST, WSS, VPS, CC, VITC.
- Decoding of 625 line standards; WST, WSS, CC, VITC.

ITU-656 output interface

- Video and VBI formatting into ITU-style output data stream, compliant to ITU-656/1364 (exception being the use of a data valid signal).
- Interfacing to PNX8550 IC.
- Support for CVBS/C mode to interface to external picture improvement devices.

7.3.2 Audio

Demodulator and decoder

- Demodulator and Decoder Easy Programming (DDEP).
- Auto Standard Detection (ASD).
- Static Standard Selection (SSS).
- DQPSK demodulation for different standards, simultaneously with 1-channel FM demodulation.
- NICAM decoding (B/G, I, D/K and L standard).
- Two-carrier multi-standard FM demodulation (B/G, D/K and M standard).
- Decoding for three analog multi-channel systems (A2, A2+ and A2*) and satellite sound.
- Adaptive de-emphasis for satellite FM.
- Optional AM demodulation for system L, simultaneously with NICAM.
- Identification A2 systems (B/G, D/K and M standard) with different identification time constants.
- FM pilot carrier present detector.
- Monitor selection for FM/AM DC values and signals, with peak and quasi peak detection option.
- BTSC MPX decoding.
- SAP decoding.
- dbx® [3] TV noise reduction.
- Japan (EIAJ) decoding.
- FM radio decoding.
- Soft muting for DEMDEC outputs DEC, MONO and SAP.
- FM over modulation adaptation option to avoid clipping and distortion.
- Sample Rate Conversion (SRC) for up to three demodulated terrestrial audio signals. Allows processing of SCART and demodulated terrestrial signals.

Audio multi-channel decoder

- Dolby Pro Logic II™

3. dbx is a registered trademark of Carillon Electronics Corp.

- 6-channel processing for Main Left and Main Right, Subwoofer, Center, Surround Left and Surround Right.

Volume and tone control

- Automatic Volume Level (AVL) control.
- Smooth volume control.
- Master volume control and balance.
- Soft mute.
- Loudness.
- Bass, treble.
- Dynamic Bass Enhancement (DBE).
- Dynamic ULTRABASS (DUB).
- Non-processed subwoofer.
- 5-band equalizer.
- Acoustical compensation.
- Programmable beeper.
- Noise generation for loudspeaker level trimming.

Reflection and delay

- Dolby Pro Logic II™ delay.
- Pseudo hall/matrix function.

Psychoacoustic spatial algorithms, downmix and split

- Incredible Mono.
- Incredible Stereo.
- Virtual Dolby Surround™.
- Virtual Dolby Digital™.
- Bass Redirection according to Dolby™ specifications.
- BBE® Sound Processing [4]

Interfaces and switching

- Digital audio input interface (stereo I^2S-bus input interface).
- Digital audio output interface (stereo I^2S-bus output interface).
- Digital crossbar switch for all digital signal sources and destinations.
- Output crossbar for exchange of channel processing functionality.
- Voice recognition output interface (stereo I^2S-bus output interface).
- Audio monitoring for level detection.
- Eight audio DACs for 6-channel loudspeaker outputs and stereo headphones output.
- Four audio DACs for stereo SCART output and stereo LINE output.

4. BBE is a registered trademark of BBE Sound Inc. See Section 18.

- Serial data link interfacing for analog multi-purpose interface PNX3000.

8. Television application

Figure 3 shows an overview of the top level hardware architecture of a TV application, using the PNX3000 and PNX2000 as an analog front-end and the PNX8550 as the main processor. This system is aimed at the hybrid (analog or digital) TV market.

The main SOC in the system, PNX8550, performs key features for high quality television like video quality enhancement, motion compensation and picture-in-picture processing.

PNX2000 together with PNX3000 are used to perform the input decoding of a single stream of analog audio and a single stream of analog video ($1f_H$ or $2f_H$) broadcast signals.

PNX2000 performs the following main functions:

- Color decoding into ITU-601 compatible format ($1f_H$ or $2f_H$).
- A digital interface to external 3D comb filter.
- VBI data capture (Teletext, WSS, CC).
- ITU-656 formatting for communication to PNX8550.
- Audio demodulation and decoding.
- Audio processing and D-A conversion.

The audio data is transferred between PNX2000 and PNX8550 using I^2S-bus. PNX2000 and PNX3000 are controlled from PNX8550 via the I^2C-bus.

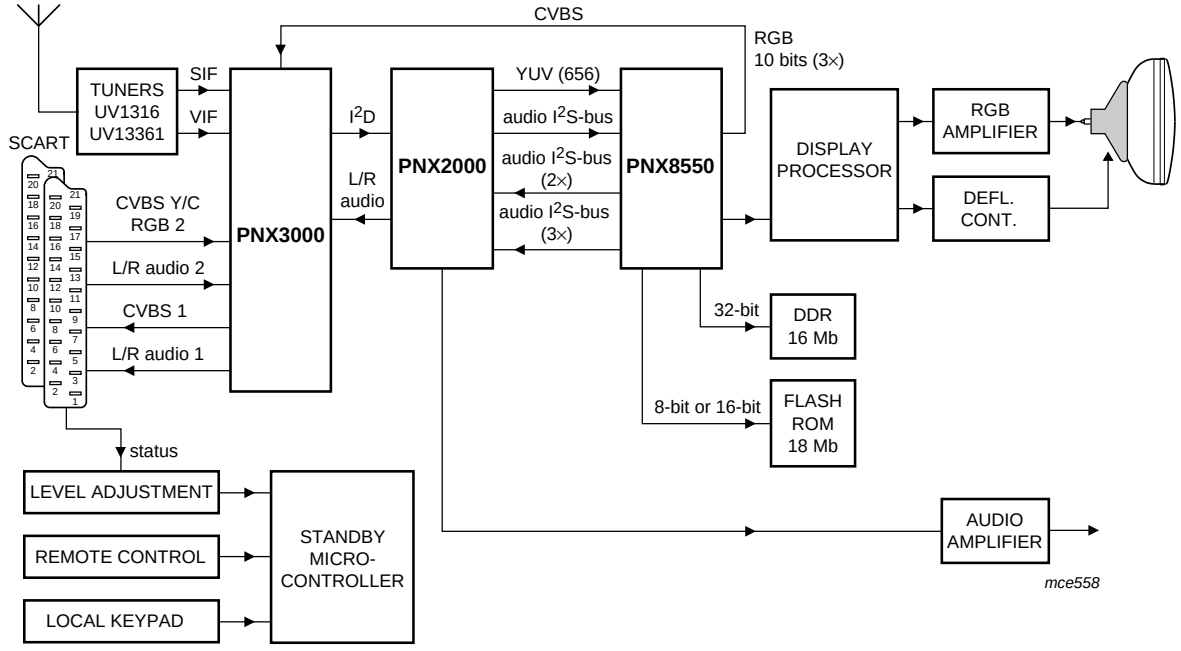


Fig 3. TV application

9. Limiting values

Permanent damage may occur if absolute maximum ratings are exceeded. Prolonged operation at maximum rating may significantly reduce the reliability of the product.

Table 19: Absolute maximum ratings

Ratings are valid only within operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise stated.

Symbol	Parameter	Min	Max	Unit
$V_{DD(core)}$	supply voltage	−0.5	+2.5	V
$V_{DD(I/O)}$	supply voltage	−0.5	+4.6	V
V_I	DC input voltage ([1] [2] and [3])	−0.5	$V_{DD(I/O)}$ + 0.5	V
V_I	DC input voltage 5V tolerant I/O pins ([2] and [3])	−0.5	+6	V
$I_{latchup}$	latch-up current ([4])	100	-	mA
V_{esd}	electrostatic discharge voltage HBM ([5] and [7])	-	±2	kV
V_{esd}	electrostatic discharge voltage MM ([6] and [7])	-	±200	V
T_{stg}	storage temperature	−40	+125	°C

[1] Not to exceed 4.6 V.

[2] Including voltage on outputs in 3-state mode.

[3] Only valid when the $V_{DD(I/O)}$ supply voltage is present.

[4] Valid for : $-(0.5 \times V_{DD}) < V < +(1.5 \times V_{DD})$; $T_j < 125$ °C.

[5] Human Body Model, $I_{leak} < 1$ mA.

[6] Machine Model 0.5 mH, $I_{leak} < 1$ mA.

[7] This product includes circuits specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. However, it is suggested that conventional precautions be taken to avoid applying voltages greater than the rated maximum.

10. Characteristics

10.1 Static characteristics

Table 20: Static characteristics: power supply pins

T_{amb} = 0 °C to +70 °C to commercial unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1.8V Power Supply Pins: V_{DDI}, V_{DDM}, $V_{DDD(I2D)}$, $V_{DDA(I2D)}$, $V_{DDA(PLL)}$, $V_{DDA(XTAL)}$, $V_{DDD(ADAC)}$, $V_{DDD(DTC)}$						
$V_{DD(core)}$	supply voltage, 1.8 V supplies	-	1.65	1.8	1.95	V
$I_{DD(core)}$	supply current, 1.8 V supplies	$V_{DD(core)}$ = 1.8 V	-	250	-	mA
3.3V Power Supply Pins: V_{DDE}, $V_{DD3(DTC)}$, $V_{DDA(ADAC)}$						
$V_{DD(3V3)}$	supply voltage, 3.3 V supplies	-	3.0	3.3	3.6	V
$I_{DD(3V3)}$	supply current, 3.3 V supplies	$V_{DD(core)}$ = 3.3 V	-	50	-	mA

Table 21: Static characteristics: digital pins

T_{amb} = 0 °C to +70 °C to commercial unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²S inputs: I2S_IN_SD1-6, I²C Address: I2C_ADR						
I_{IL}	LOW-level input current	V_i = 0	-	-	1	µA
V_I	input voltage	-	0	-	5.5	V
V_{IH}	HIGH-level input voltage	-	2.0	-	-	V
V_{IL}	LOW-level input voltage	-	-	-	0.8	V
I_{PD}	pull-down current	$V_i = V_{DD(I/O)}$	20	50	75	µA
External Sync: VSYNC1, VSYNC2, Reset: RESET_SEL, ITU-656: LL_CLK						
I_{IL}	LOW-level input current	V_i = 0	-	-	1	µA
I_{IH}	HIGH-level input current	$V_i = V_{DD(I/O)}$	-	-	1	µA
V_I	input voltage	-	0	-	5.5	V
V_{IH}	HIGH-level input voltage	-	2.0	-	-	V
V_{IL}	LOW-level input voltage	-	-	-	0.8	V
Jtag inputs: TDI, TCK, TRST_N, TMS						
I_{IH}	HIGH-level input current	$V_i = V_{DD(I/O)}$	-	-	1	µA
V_I	input voltage	-	0	-	5.5	V
V_{IH}	HIGH-level input voltage	-	2.0	-	-	V
V_{IL}	LOW-level input voltage	-	-	-	0.8	V
V_{hys}	hysteresis voltage	-	-	0.3	-	V
I_{PU}	pull-up current	V_i = 0	–25	–50	–65	µA
		$V_{DD(I/O)} < V_i < 5$ V	0	0	0	µA
I²C Pins: I2C_SDA, I2C_SCL						
C_I	input capacitance	-	-	5	-	pF
I_{LI}	input leakage current [1]	$V_{DD(3V3)}$ = 3.3 V; T_{amb} = 25 °C	1.37	1.85	2.45	µA
$I_{IN(MAX)}$	max. input current [2]	at 5 V	8.20	10.7	12.45	µA
V_I	input voltage	-	0	-	5	V
V_{IL}	LOW-level input voltage	-	-	-	0.8	V
V_{IH}	HIGH-level input voltage	-	2.0	-	-	V
V_{OL}	LOW-level output voltage	-	-	-	0.4	V
I_{OL}	LOW-level output current	V_{OL}=0.4V	-	8.45	-	mA
ITU-656 Outputs: DVO_DATA_0-9, DVO_VALID, DVO_CLK						
I_{oz}	3-state output leakage	V_O = 0 $V_O = V_{DD(I/O)}$	-	-	1	µA
V_I	input voltage	-	0	-	5.5	V
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA	2.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = 2.4	–4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	4	-	-	mA
I_{OH}	HIGH-level short circuit current	V_{OH} = 0	-	-	–45	mA
I_{OL}	LOW-level short circuit current	$V_{OL} = V_{DD(I/O)}$	-	-	50	mA
I²S I/O: I2S_SCK_SYS, I2S_WS_SYS						

Table 21: Static characteristics: digital pins...*continued*

T_{amb} = 0 °C to +70 °C to commercial unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IL}	LOW-level input current	V_i = 0	-	-	1	µA
I_{IH}	HIGH-level input current	$V_i = V_{DD(I/O)}$	-	-	1	µA
V_I	input voltage	-	0	-	$V_{DD(I/O)}$	V
V_{IH}	HIGH-level input voltage	-	2.0	-	-	V
V_{IL}	LOW-level input voltage	-	-	-	0.8	V
V_{hys}	hysteresis voltage	-	-	0.4	-	V
I_{oz}	3-state output leakage	V_O = 0 $V_O = V_{DD(I/O)}$	-	-	1	µA
V_{OH}	HIGH-level output voltage	I_{OH} = –8 mA	2.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 8 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = 2.4	–8	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	8	-	-	mA
I_{OH}	HIGH-level short circuit current	V_{OH} = 0	-	-	–95	mA
I_{OL}	LOW-level short circuit current	$V_{OL} = V_{DD(I/O)}$	-	-	95	mA
I^2S Outputs: I2S_OUT_SD1-6, JTAG Output: TDO, PNX3000 Clock: MPIFCLK, Sync Output: HVINFO						
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA	2.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = 2.4	–4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4V	4	-	-	mA
I_{OH}	HIGH-level short circuit current	V_{OH} = 0	-	-	–45	mA
I_{OL}	LOW-level short circuit current	$V_{OL} = V_{DD(I/O)}$	-	-	50	mA
I^2S Output: I2S_OUT_SD3_SCK, I2S_OUT_SD3_WS, ADAC_CLK, Clock Output: DCLK						
V_{OH}	HIGH-level output voltage	I_{OH} = –8 mA	2.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 8 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = 2.4	–8	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	8	-	-	mA
I_{OH}	HIGH-level short circuit current	V_{OH} = 0	-	-	–95	mA
I_{OL}	LOW-level short circuit current	$V_{OL} = V_{DD(I/O)}$	-	-	95	mA
Interrupt: INTOUT						
I_{oz}	3-state output leakage	V_O = 0 $V_O = V_{DD(I/O)}$	-	-	1	µA
V_I	input voltage	-	0	-	5.5	V
V_{OL}	LOW-level output voltage	I_{OL} = 8 mA	-	-	0.4	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	8	-	-	mA
I_{OL}	LOW-level short circuit current	$V_{OL} = V_{DD(I/O)}$	-	-	140	mA

Table 22: Static characteristics: analog pins

T_{amb} = 0 °C to +70 °C to commercial unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External Sync: HSYNCFBL1, HSYNCFBL2						
V_{IT}	input threshold	dtc_lowth = 0	-	1.65	-	V
V_{IT}	input threshold	dtc_lowth = 1	-	0.65	-	V
Reset: RESET_N						
V_{trip_high}	high trip level	RESET_SEL = 0	1.0	1.2	1.4	V
V_{trip_low}	low trip level	RESET_SEL = 0	0.95	1.1	1.3	V
I^2D Inputs: DLINK1-3DP, DLINK1-3DN,DLINK1-3SP, DLINK1-3SN						
V_{sens}	input sensitivity	-	-	6	-	mV
Z_{diff}	differential line load impedance	across input diff pair	-	100	-	Ω
$V_{DATA(pos)}$	data pos. range	-	0	-	300	mV
$V_{DATA(neg)}$	data neg. range	-	0	-	300	mV
$V_{STROBE(pos)}$	strobe pos. range	-	0	-	300	mV
$V_{STROBE(neg)}$	strobe neg. range	-	0	-	300	mV
Audio DACs: ADAC1-12P, ADAC1-12N						
V_{REFP}	positive reference voltage	-	3.0	3.3	3.6	V
V_{REFN}	negative reference voltage	-	-	0	-	V
I_{REFP}	positive reference current	-	-	820	-	μA
Audio DACs: ADAC1-12						
$V_{OUT(rms)}$	output voltage (rms); single-ended, digital i/p level = 0 dBFS	-	-	1.17	-	V
R_{OUT}	output resistance	-	0.7	1.0	1.3	kΩ
R_L	load resistance	-	10	-	-	kΩ

10.2 Dynamic characteristics

Table 23: Dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I^2C						
f_{clk}	clock frequency	-	-	400	-	kHz
t_r	rise time	1.5 kΩ ext. pull-up; 160 pF load	-	550	-	ns
t_f	fall time	1.5 kΩ ext. pull-up; 160 pF load	130	162	245	ns
Viddec: HVINFO (slew rate limited)						
t_{thl}	output transition time (H to L)	30 pF load	-	10	13.8	ns
t_{tlh}	output transition time (L to H)	30 pF load	-	10	13.8	ns
ITU-656						
$t_{su(DATA)}$	data setup at Rx	40 pF load	-	-	7.3	ns

Table 23: Dynamic characteristics...*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{h(DATA)}$	data hold at Rx	40 pF load	-	-	4.9	ns
I^2S						
f_s	audio sample frequency	-	32	48	48	kHz
f_{SCK}	SCK frequency	I^2S-bus master mode	-	$64f_s$	-	-
f_{SCK}	SCK frequency	I^2S-bus slave mode	$32f_s$	$64f_s$	$256f_s$	-
DF_{SCK}	SCK duty factor	I^2S-bus master mode	40	50	60	%
DF_{SCK}	SCK duty factor	I^2S-bus slave mode	35	-	65	%
t_{RSCK}	SCK rise / fall time	I^2S-bus master mode; C_{load} = 30 pF	-	-	5	ns
t_{RSCK}	SCK rise / fall time	I^2S-bus slave mode; f_{SCK} = 3.072 MHz	-	-	50	ns
t_d	delay time: SCK to WS and SD outputs [2]	$T_{SCK} = 1/f_{SCK}$	0.3	0.5	0.7	T_{SCK}
t_h	hold time: SCK to WS and SD inputs	-	0	-	-	ns
t_s	setup time: WS and SD inputs to SCK	$T_{SCK} = 1/f_{SCK}$	0.2	-	-	T_{SCK}
I^2D						
$f_{clock(WORD)}$	word clock frequency	-	-	13.5	-	MHz
WL	word length	-	-	44	-	bit
DR	data rate	-	-	594	-	Mbit/s
$f_{clock(BIT)}$	bit clock freq.	-	-	297	-	MHz
JTAG Clock Reset						
t_{low}	Time RESET_N should be below V_{trip_high} before internal reset = 1.	RESET_SEL = 0	-	-	11	µs
t_{high}	Time RESET_N should be above V_{trip_high} before internal reset = 0 (after t_{pulse}).	RESET_SEL = 0	-	-	2	µs
t_{pulse}	Time before PNX2000 internal reset = 0 [3].	RESET_SEL = 0	200	-	-	ns

[1] Allowed SCK/WS ratios are 32, 48, 64, 128 and 256 SCK periods per WS period.

[2] All timings relative to the rising edge of SCK.

[3] See Section 10.4 for waveforms.

10.3 Audio DAC characteristics

Table 24: Dynamic characteristics: Audio DAC

Tamb = 0 °C to +70 °C for commercial unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Audio DAC Outputs: ADAC1-12						
f_s	audio sample frequency	-	32	48 [1]	48	kHz
S/N	Signal to Noise Ratio, CCIR-2 k weighted	outputs muted; reference f = 2 kHz, 0 dBFS	-	94	-	dB
(THD+N)/S	Total Harmonic Distortion + Noise to Signal ratio	f =1 kHz; 0 dBFS; 22 kHz measurement bandwidth	-	–77	-	dB
f_{res}	frequency response	+/-1 dB	<10	-	22.5	kHz
α_{ct}	crosstalk between adjacent DACs	f = 1 kHz; 0 dBFS	-	–90	-	dB

[1] Allowed audio sample frequencies are 32 kHz, 44.1 kHz and 48 kHz. Default f_S in I^2S-bus master mode is 48 kHz.

The audio DACs are based on a switched-resistor architecture which acts as a controlled voltage divider between the positive and negative references ADACn_P and ADACn_N. Therefore all noise on the reference pins will spread directly to the associated output pin ADACn. Consequently it is important to provide adequate filtering of the reference voltage to allow optimum signal-to-noise performance. Also, the voltage difference between ADACn_P and SDAC_3V3 should be kept to a minimum as any difference will degrade distortion performance.

The DACs have an internal resolution of 4 bits, running at a clock frequency of 128 f_S, using a noise shaper circuit to shift the quantization noise to out-of-band frequencies. To prevent HF overloading of the circuit that is driven by the DAC outputs, a 3.3 nF capacitor should be used to filter off the HF signal content. Together with the DAC's nominal output impedance of 1 kΩ, a first order roll-off at approximately 50 kHz will result. One capacitor is required for each DAC output, connected between ADACn and the corresponding ADACn_N.

10.4 Timing

10.4.1 Clock

Crystal specification

The crystal oscillator can be used with an external crystal, or in bypass mode with external clock signal, see Figure 4.

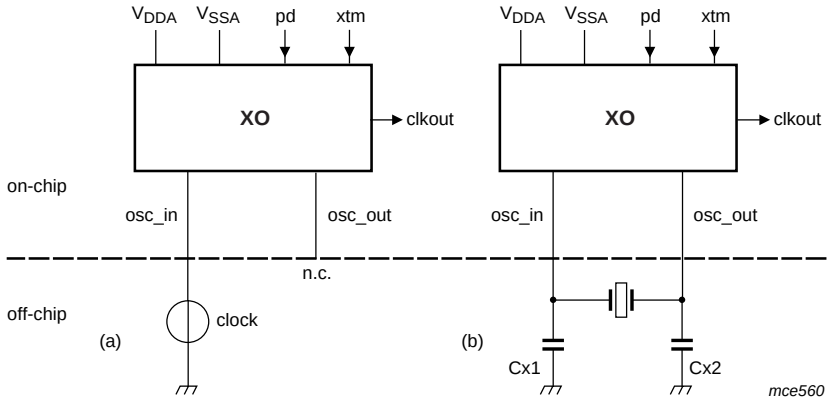


Fig 4. Application diagram: (a) slave/test mode, (b) oscillation mode

The supported crystal/external clock frequencies are 27 MHz and 13.5 MHz. The crystal oscillator is followed by a selectable divide-by-two frequency divider giving three available clock frequencies, as shown in Table 25.

Table 25: Primary clock settings

Clock/Crystal Input	Divider setting	Clock frequency
27 MHz	x/1	27 MHz
27 MHz	x/2	13.5 MHz
13.5 MHz	x/1	13.5 MHz
13.5 MHz	x/2	6.75 MHz

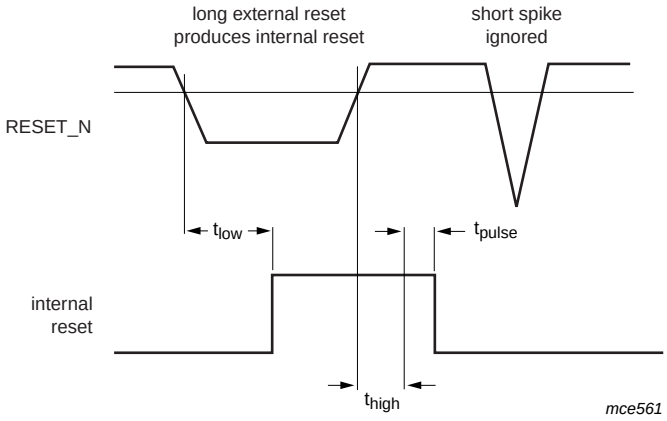
The crystal specification is:

- Package: surface mount.
- Accuracy: (±50 ppm).
- Temperature: (±50 ppm).
- Operating temperature range: −20 to +70 °C.
- Load capacitance: 30 pF.

Table 26: Crystal parameters

Oscillator frequency (f_c)	Crystal load capacitance (C_L)	Max.crystal series resistance (R_S)	External load capacitors (Cx1; Cx2)
13.5 MHz			
	10 pF	< 600 Ω	2 x 18 pF
	20 pF	< 255 Ω	2 x 38 pF
	30 pF	< 140 Ω	2 x 58 pF
27 MHz			
	10 pF	< 130 Ω	2 x 18 pF
	20 pF	< 50 Ω	38 pF; 18 pF
	30 pF	n.a.	n.a.

10.4.2 Reset



RESET_N pin and internal reset timing

Fig 5. PNX2000 reset

10.4.3 ITU-656

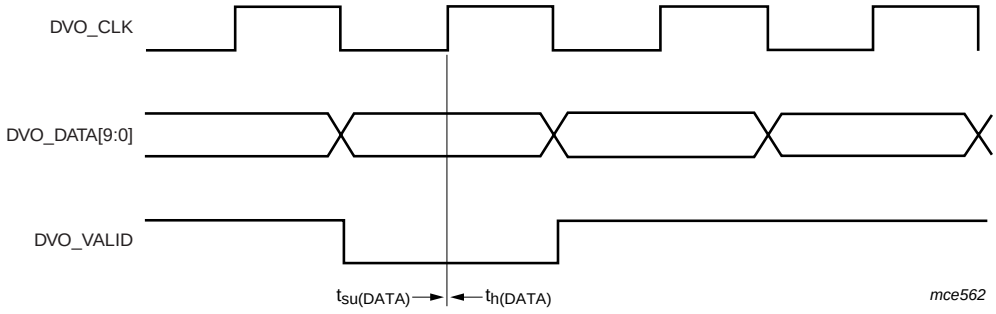


Fig 6. Timing ITU interface

11. Glossary

AGC..... Automatic Gain Control

ASD..... Auto Standard Detection

AVL..... Auto Volume Level

BCU..... Bus Control Unit

BTSC..... Broadcast TV System Committee

DBE..... Dynamic Base Enhancement

DCU..... Data Capture Unit

DDEP ..... Demodulator and Decoder Easy Programming

DEMDEC..... Demodulator Decoder

DQPSK..... Differential Quadrature Phase Shift Keying

DSP ..... Digital Signal Processor

DUB..... Dynamic UltraBass

DVD ..... Digital Video Disc

EIAJ ..... Electronic Industries Association of Japan

GTU..... Global Task Unit

HBM ..... Human Body Model

LQFP..... Low profile Quad Flat Package

MM ..... Machine Model

MPX..... Multiplexer

NICAM..... Near Instantaneous Compounded Audio Multiplex

NTSC..... National TV Systems Committee

PAL..... Phase Alternate Line

SAP ..... Secondary Audio Program

SCART ..... Syndicate for Constructors of Apparatus for Radio and Television

SECAM ..... Sequential Color and Memory

SMD ..... Surface Mount Device

SRC..... Sample Rate Conversion

SSS ..... Static Standard Selection

SSOP.....Shrink Small Outline Package

SOC.....System On Chip

VBI.....Vertical Blanking Interval

VIDDEC .....Video front-end Decoder

VITC.....Vertical Interval Time Code

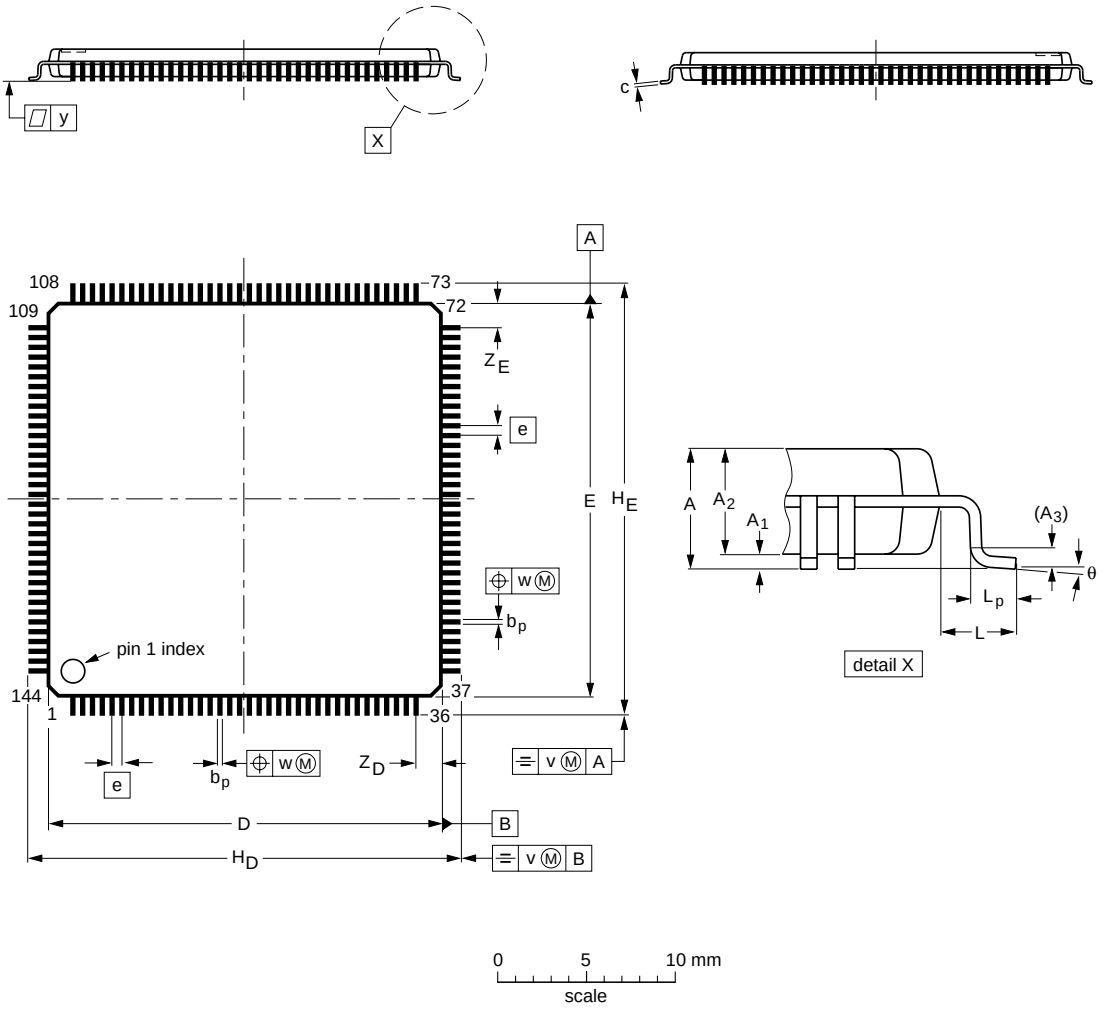
VPS.....Video Program System

WSS.....Wide Screen Signaling

WST.....World System Teletext

12. Package outline

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT486-1	136E23	MS-026				~~00-03-14~~ 03-02-20

Fig 7. LQFP package outline

13. Soldering

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):

— larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

— smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

13.5 Package related soldering information

Table 27: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, LBGA, LFBGA, SQFP, SSOP-T [3], TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
PMFP [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Hot bar or manual soldering is suitable for PMFP packages.

14. Revision history

Table 28: Revision history

Rev	Date	CPCN	Description
03	20040823		Minor revision (9397 750 13928)
02	20040712		Upgraded to Product data (9397 750 13591). Table 3 and Table 4 added.
01	20040504		Preliminary data (9397 750 12066)

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21. Contents

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