DIGITAL-LOGIC

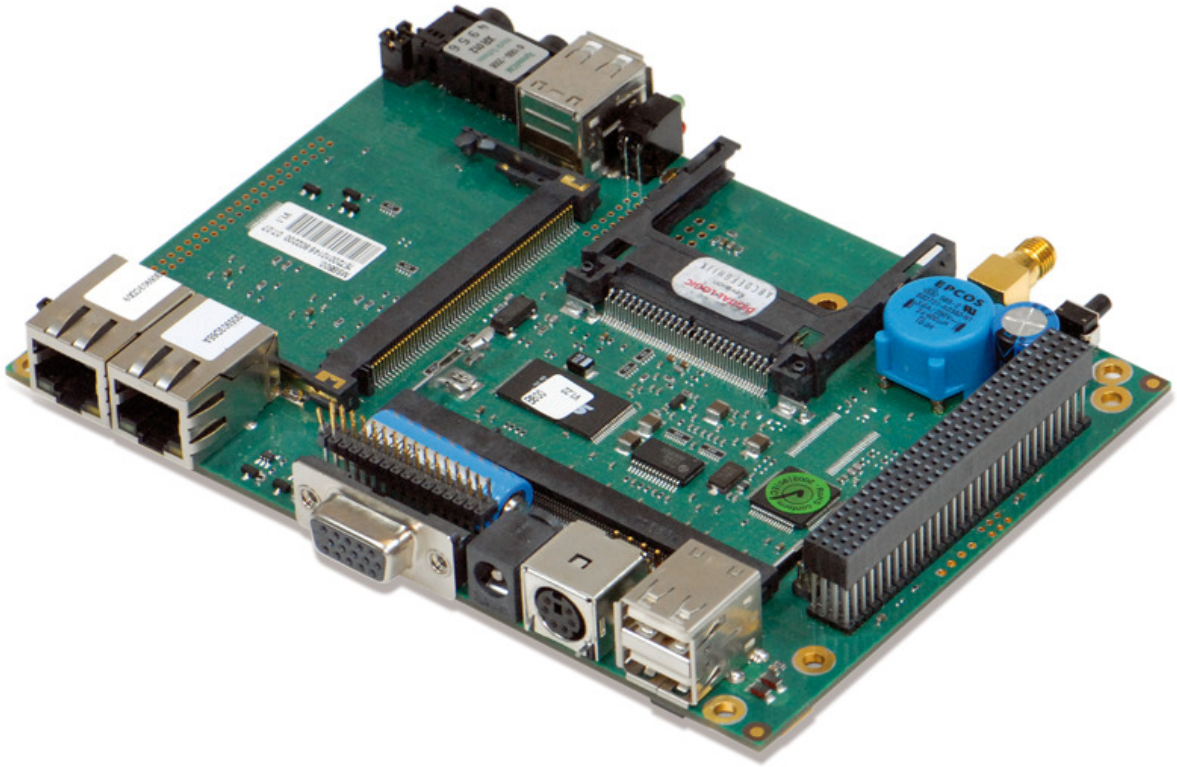
smart embedded computers

Detailed Technical USER MANUAL FOR:

MICROSPACE®

3.5”-SBC

MSB900/L



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For internal use only:
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Path: R:\HANDBUCH\MSB\MSB900\MSB900_Detailed_V1.0.doc

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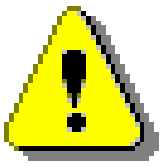
About this Manual and How to Use It

This manual is written for the original equipment manufacturer (OEM) who plans to build computer systems based on the single board MICROSPACE-PC. It is for integrators and programmers of systems based on the MICROSPACE-Computer family. This manual provides instructions for installing and configuring the board, and describes the system and setup requirements. This document contains information on hardware requirements, interconnections, and details of how to program the system. Please check the Product CD for further information and manuals.

REVISION HISTORY:

Document Version	Date/Initials:	Modification: Remarks, News, Attention:
V1.0	***02.2008 DAR***	***Initial document***



Attention!
1. All information in this manual, and the product, are subject to change without prior notice.
2. Read this manual prior to installation of the product.
3. Read the security information carefully prior to installation of the product.

Table of Contents

1. PREFACE

The information contained in this manual has been carefully checked and is believed to be accurate; it is subject to change without notice. Product advances mean that some specifications may have changed. DIGITAL-LOGIC AG assumes no responsibility for any inaccuracies, or the consequences thereof, that may appear in this manual. Furthermore, DIGITAL-LOGIC AG does not accept any liability arising from the use or application of any circuit or product described herein.

1.1. Trademarks

DIGITAL-LOGIC, DIGITAL-LOGIC-Logo, MICROSPACE, and smartModule are registered trademarks owned worldwide by DIGITAL-LOGIC AG, Luterbach (Switzerland). In addition, this document may include names, company logos, and registered trademarks which are, therefore, proprietary to their respective owners.

1.2. Disclaimer

DIGITAL-LOGIC AG makes no representations or warranties with respect to the contents of this manual, and specifically disclaims any implied warranty of merchantability or fitness, for any particular purpose. DIGITAL-LOGIC AG shall, under no circumstances, be liable for incidental or consequential damages or related expenses resulting from the use of this product, even if it has been notified of the possibility of such damage.

1.3. Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements wherever possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

1.4. Who should use this Product

- Electrical engineers with know-how in PC-technology.
- Because of the complexity and the variability of PC-technology, we cannot guarantee that the product will work in any particular situation or set-up. Our technical support will try to help you find a solution.
- Pay attention to electrostatic discharges; use a CMOS protected workplace.
- Power supply must be OFF when working on the board or connecting any cables or devices.

1.5. Recycling Information

All components within this product fulfill the requirements of the RoHS (Restriction of Hazardous Substances Directive). The product is soldered with a lead free process.

1.6. Technical Support

1. Contact your local DIGITAL-LOGIC Technical Support, in your country.
2. Use the Internet Support Request form at http://support.digitallogic.ch/ ➔ embedded products ➔ New Support Request

Support requests are only accepted with detailed information about the product (i.e., BIOS-, Board-version)!

1.7. Limited Two Year Warranty

DIGITAL-LOGIC AG guarantees the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for two years following the date of shipment from DIGITAL-LOGIC AG, Switzerland. This warranty is limited to the original purchaser of the product and is not transferable.

During the two year warranty period, DIGITAL-LOGIC AG will repair or replace, at its discretion, any defective product or part at no additional charge, provided that the product is returned, shipping prepaid, to DIGITAL-LOGIC AG. All replaced parts and products become property of DIGITAL-LOGIC AG.

Before returning any product for repair, direct customers of DIGITAL-LOGIC AG, Switzerland are required to register a RMA (Return Material Authorization) number in the Support Center at http://support.digitallogic.ch/

All other customers must contact their local distributors for returning defective materials.

This limited warranty does not extend to any product which has been damaged as a result of accident, misuse, abuse (such as use of incorrect input voltages, wrong cabling, wrong polarity, improper or insufficient ventilation, failure to follow the operating instructions that are provided by DIGITAL-LOGIC AG or other contingencies beyond the control of DIGITAL-LOGIC AG), wrong connection, wrong information or as a result of service or modification by anyone other than DIGITAL-LOGIC AG. Nor if the user has insufficient knowledge of these technologies or has not consulted the product manuals or the technical support of DIGITAL-LOGIC AG and therefore the product has been damaged.

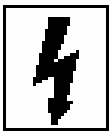
Empty batteries (external and onboard), as well as all other battery failures, are not covered by this manufacturer's limited warranty.

Except, as directly set forth above, no other warranties are expressed or implied, including, but not limited to, any implied warranty of merchantability and fitness for a particular purpose, and DIGITAL-LOGIC AG expressly disclaims all warranties not stated herein. Under no circumstances will DIGITAL-LOGIC AG be liable to the purchaser or any user for any damage, including any incidental or consequential damage, expenses, lost profits, lost savings, or other damages arising out of the use or inability to use the product.

1.8. Explanation of Symbols

CE Conformity
This symbol indicates that the product described in this manual is in compliance with all applied CE standards.

Caution, Electric Shock!
This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your equipment.



Caution, Electric Shock!
This symbol and title warn of hazards due to electrical shocks (> 32V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your equipment

Warning, ESD Sensitive Device!
This symbol and title inform that electronic boards and their components are sensitive to Electro Static Discharge (ESD). In order to ensure product integrity at all times, care must always be taken while handling and examining this product.

Attention!
This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your equipment.

Note...
This symbol and title emphasize aspects the user should read through carefully for his, or her, own advantage.

Warning, Heat Sensitive Device!
This symbol indicates a heat sensitive component.

Safety Instructions
This symbol shows safety instructions for the operator to follow.

This symbol warns of general hazards from mechanical, electrical, and/or chemical failure. This may endanger your life/health and/or result in damage to your equipment.

1.9. Applicable Documents and Standards

The following publications are used in conjunction with this manual. When any of the referenced specifications are superseded by an approved revision, that revision shall apply. All documents may be obtained from their respective organizations.

- Advanced Configuration and Power Interface Specification Revision 2.0c, August 25, 2003 Copyright © 1996-2003 Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, Phoenix Technologies Ltd., Toshiba Corporation. All rights reserved. http://www.acpi.info/
- ANSI/TIA/EIA-644-A-2001: Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, January 1, 2001. http://www.ansi.org/
- ANSI INCITS 361-2002: AT Attachment with Packet Interface - 6 (ATA/ATAPI-6), November 1, 2002. http://www.ansi.org/
- ANSI INCITS 376-2003: American National Standard for Information Technology – Serial Attached SCSI (SAS), October 30, 2003. http://www.ansi.org/
- Audio Codec '97 Revision 2.3 Revision 1.0, April 2002 Copyright © 2002 Intel Corporation. All rights reserved. http://www.intel.com/labs/media/audio/
- Display Data Channel Command Interface (DDC/CI) Standard (formerly DDC2Bi) Version 1, August 14, 1998 Copyright © 1998 Video Electronics Standards Association. All rights reserved. http://www.vesa.org/summary/sumddcci.htm
- ExpressCard Standard Release 1.0, December 2003 Copyright © 2003 PCMCIA. All rights reserved. http://www.expresscard.org/
- IEEE 802.3-2002, IEEE Standard for Information technology, Telecommunications and information exchange between systems–Local and metropolitan area networks–Specific requirements – Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications. http://www.ieee.org
- IEEE 802.3ae (Amendment to IEEE 802.3-2002), Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications, Amendment: Media Access Control (MAC) Parameters, Physical Layers, and Management Parameters for 10 GB/s Operation. http://www.ieee.org
- Intel Low Pin Count (LPC) Interface Specification Revision 1.1, August 2002 Copyright © 2002 Intel Corporation. All rights reserved. http://developer.intel.com/design/chipsets/industry/lpc.htm
- PCI Express Base Specification Revision 1.1, March 28, 2005, Copyright © 2002-2005 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI Express Card Electromechanical Specification Revision 1.1, March 28, 2005, Copyright © 2002-2005 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI Local Bus Specification Revision 2.3, March 29, 2002 Copyright © 1992, 1993, 1995, 1998, 2002 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI-104 Specification, Version V1.0, November 2003. All rights reserved. http://www.pc104.org
- PICMG® Policies and Procedures for Specification Development, Revision 2.0, September 14, 2004, PCI Industrial Computer Manufacturers Group (PICMG®), 401 Edgewater Place, Suite 500, Wakefield, MA 01880, USA, Tel: 781.224.1100, Fax: 781.224.1239. http://www.picmg.org/
- Serial ATA: High Speed Serialized AT Attachment Revision 1.0a January 7, 2003 Copyright © 2000-2003, APT Technologies, Inc, Dell Computer Corporation, Intel Corporation, Maxtor Corporation, Seagate Technology LLC. All rights reserved. http://www.sata-io.org/

- Smart Battery Data Specification Revision 1.1, December 11, 1998. www.sbs-forum.org
- System Management Bus (SMBus) Specification Version 2.0, August 3, 2000 Copyright © 1994, 1995, 1998, 2000 Duracell, Inc., Energizer Power Systems, Inc., Fujitsu, Ltd., Intel Corporation, Linear Technology Inc., Maxim Integrated Products, Mitsubishi Electric Semiconductor Company, Power-Smart, Inc., Toshiba Battery Co. Ltd., Unitrode Corporation, USAR Systems, Inc. All rights reserved. http://www.smbus.org/
- Universal Serial Bus Specification Revision 2.0, April 27, 2000 Copyright © 2000 Compaq Computer Corporation, Hewlett-Packard Company, Intel Corporation, Lucent Technologies Inc., Microsoft Corporation, NEC Corporation, Koninklijke Philips Electronics N.V. All rights reserved. http://www.usb.org/

1.10. For Your Safety

Your new DIGITAL-LOGIC product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long, fault-free life. However, this life expectancy can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and for the correct operation of your new DIGITAL-LOGIC product, please comply with the following guidelines.

Attention!
All work on this device must only be carried out by sufficiently skilled personnel.

Caution, Electric Shock!
Before installing your new DIGITAL-LOGIC product, always ensure that your mains power is switched off. This applies also to the installation of piggybacks or peripherals. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltage before performing work.

Warning, ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. In order to ensure product integrity at all times, be careful during all handling and examinations of this product.

1.11. RoHS Commitment

DIGITAL-LOGIC AG is committed to develop and produce environmentally friendly products according to the Restriction of Hazardous Substances (RoHS) Directive (2002/95/EC) and the Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) established by the European Union. The RoHS directive was adopted in February 2003 by the European Union and came into effect on July 1, 2006. It is not a law but a directive, which restricts the use of six hazardous materials in the manufacturing of various types of electronic and electrical equipment. It is closely linked with the Waste Electrical and Electronic Equipment Directive (WEEE) 2002/96/EC, which has set targets for collection, recycling and recovery of electrical goods and is part of a legislative initiative to solve the problem of huge amounts of toxic e-waste.

Each European Union member state is adopting its own enforcement and implementation policies using the directive as a guide. Therefore, there could be as many different versions of the law as there are states in the EU. Additionally, non-EU countries like China, Japan, or states in the U.S. such as California may have their own regulations for green products, which are similar, but not identical, to the RoHS directive.

RoHS is often referred to as the "lead-free" directive but it restricts the use of the following substances:

- Lead
- Mercury
- Cadmium
- Chromium VI
- PBB and PBDE

The maximum allowable concentration of any of the above mentioned substances is 0.1% (except for Cadmium, which is limited to 0.01%) by weight of homogeneous material. This means that the limits do not apply to the weight of the finished product, or even to a component but to any single substance that could (theoretically) be separated mechanically.

1.11.1. RoHS Compatible Product Design

All DIGITAL-LOGIC standard products comply with RoHS legislation.

Since July 1, 2006, there has been a strict adherence to the use of RoHS compliant electronic and mechanical components during the design-in phase of all DIGITAL-LOGIC standard products.

1.11.2. RoHS Compliant Production Process

DIGITAL-LOGIC selects external suppliers that are capable of producing RoHS compliant devices. These capabilities are verified by:

1. A confirmation from the supplier indicating that their production processes and resulting devices are RoHS compliant.
2. If there is any doubt of the RoHS compliancy, the concentration of the previously mentioned substances in a produced device will be measured. These measurements are carried out by an accredited laboratory.

1.11.3. WEEE Application

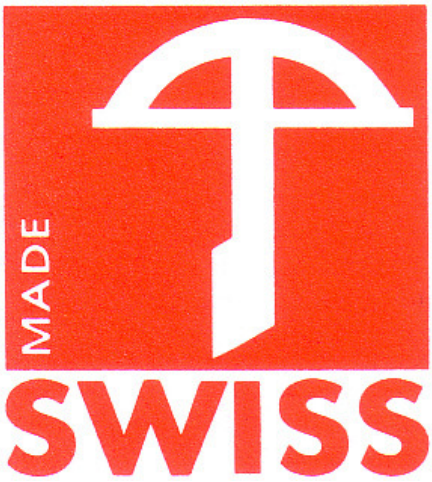
The WEEE directive is closely related to the RoHS directive and applies to the following devices:

- Large and small household appliances
- IT equipment
- Telecommunications equipment (although infrastructure equipment is exempt in some countries)
- Consumer equipment
- Lighting equipment – including light bulbs
- Electronic and electrical tools
- Toys, leisure and sports equipment
- Automatic dispensers

It does not apply to fixed industrial plants and tools. The compliance is the responsibility of the company that brings the product to market, as defined in the directive. Components and sub-assemblies are not subject to product compliance. In other words, since DIGITAL-LOGIC does not deliver ready-made products to end users the WEEE directive is not applicable for DIGITAL-LOGIC. Users are nevertheless encouraged to properly recycle all electronic products that have reached the end of their life cycle.

1.12. Swiss Quality

- 100% Made in Switzerland
- DIGITAL-LOGIC is a member of "Swiss-Label"
- This product was ***not*** manufactured by employees earning piecework wages
- This product was manufactured in humane work conditions
- All employees who worked on this product are paid customary Swiss market wages and are insured
- ISO 9000:2001 (quality management system)



1.13. The Swiss Association for Quality and Management Systems

The Swiss Association for Quality and Management Systems (SQS) provides certification and assessment services for all types of industries and services. SQS certificates are accepted worldwide thanks to accreditation by the Swiss Accreditation Service (SAS), active membership in the International Certification Network, IQNet, and co-operation contracts/agreements with accredited partners.

www.sqs.ch

The SQS Certificate ISO 9001:2000 has been issued to DIGITAL-LOGIC AG, the entire company, in the field of development, manufacturing and sales of embedded computer boards, embedded computer modules and computer systems. The certification is valid for three years at which time an audit is performed for recertification.

2. OVERVIEW

2.1. Standard Features of the MSB900/L

The MICROSPACE 3.5”-SBC is a miniaturized modular device incorporating the major elements of a PC/AT compatible computer. It includes standard PC/AT compatible elements, such as:

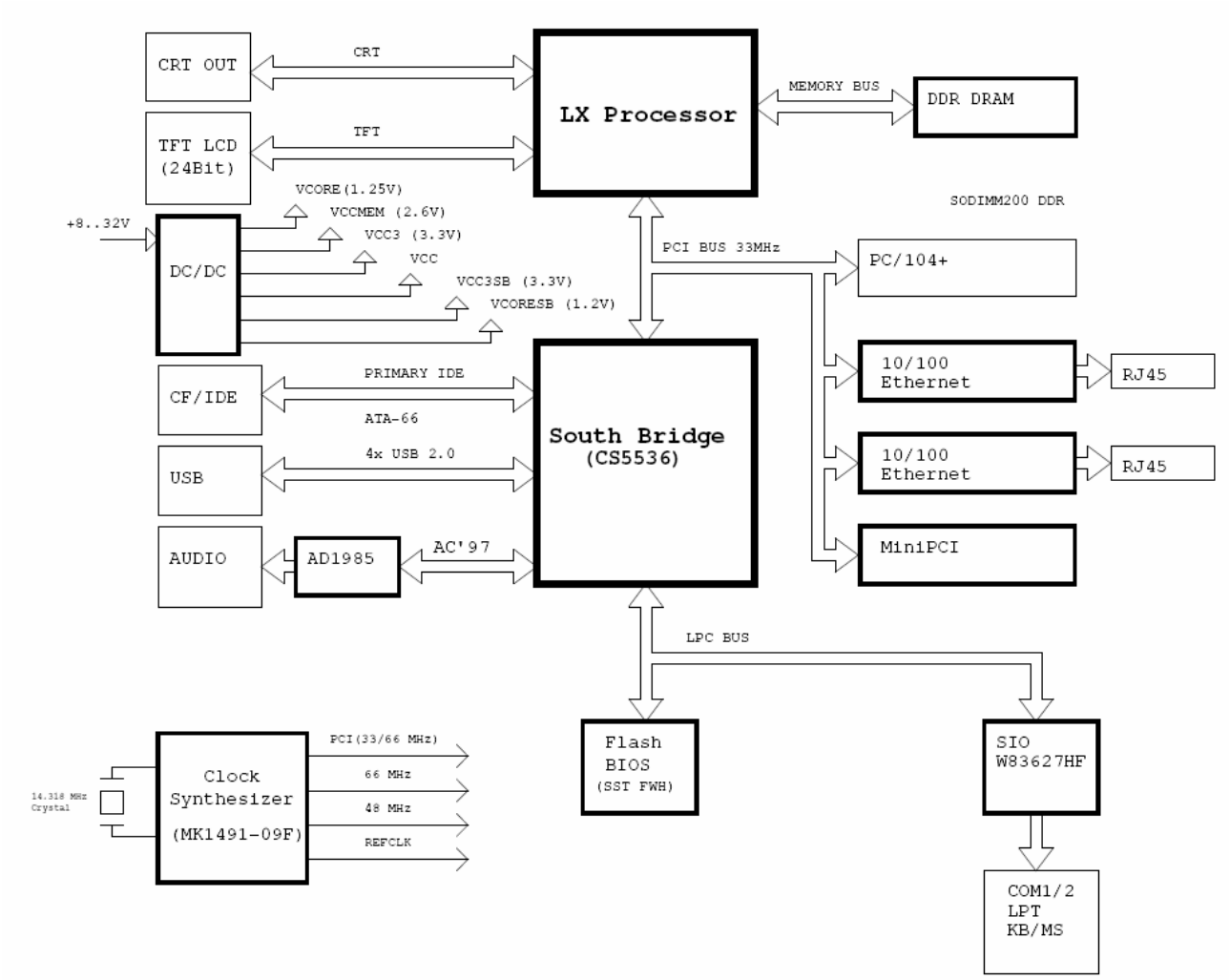
- Powerful GEODE™ LX-900 600MHz
- Legacy BIOS ROM
- DDR-SODIMM 200pin socket (for DDR-RAM 256-1024MB)
- 128k second level cache
- Timers
- DMA
- Real-time clock with CMOS-RAM and battery buffer (only on MSB900, not on MSB900L)
- LPT1 parallel port
- COM1-, COM2- RS2332 serial port
- Speaker interface
- PS/2-keyboard and mouse interface (shared on one mini DIN connector)
- PATA-IDE hard disk interface
- VGA video interface
- PCI/104 (one slot), limited I/O connector space
- 4 Channels USB 2.0
- Onboard CF socket Type II

2.2. Unique Features

The MICROSPACE 3.5”-SBC includes all standard PC/AT functions plus unique DIGITAL-LOGIC AG enhancements, such as:

- Two channel LAN Ethernet, INTEL 82551QM (LAN A) and INTEL 82551ER (LAN B)
- Boot from LAN (PXE and RPL)
- Single 8 - 32Volt supply
- Video input (only on MSB900, not available on MSB900L)
- Watchdog
- EEPROM for setup and configuration
- UL approved parts
- *Optional:* interface for operator display (LVDS, COM2, CRT, USB, SMBus)

2.3. MSB900 Block Diagram



2.4. MSB900/MSB900L specifications

CPU	Specification
CPU	GEODE LX900
CPU Core Supply	1.25V very low powered
Mode	Real / Protected
Compatibility	x86
Word Size	32Bits
Secondary Cache	128kB
Physical Addressing	32 lines
Virtual Addressing	16GB
Clock Rates	600MHz
Socket Standard	Soldered BGA

Chipset	Specification
Northbridge	AMD LX900
Southbridge	AMD CS5536
LAN	2x 10/100Mbit Intel 82551QM (LAN A), Intel 82551ER (LAN B)
Audio	Stereo In and Stereo Line-Out
Codec	AD1985 up to 96kHz sampling rate, 16Bit (Analog Devices)
Firewire IEEE1394	Not on board
Video	16MByte Video-DDRAM

Power Management:	Specification
	The LX900 supports ACPI and APM Version 1.2 The following ACPI Sleep States are supported: - S1 (Standby) - S3 (Suspend to RAM) **not available** - S4 (Hibernation)

DMA:	Specification
8237A comp.	4 channel 8bit 3 channel 16bit

Interrupts:	Specification
8259 comp.	8 + 7 levels PC compatible

Timers:	Specification
8254 comp.	3 programmable counters/timers

Memory:	Specification
SODIMM	SODIMM200pin DDR PC2700 333MHz 256-1024MByte

Video	Specification
Controller	GEODE LX900
BUS	32Bit high speed 33MHz PCI bus
Enhanced BIOS	VGA / LCD BIOS
Memory	2-16MByte shared RAM
CRT-Monitor	VGA, SVGA up to 1920x1440
Video Input	MSB900: yes, 1 channel *MSB900L: no*
Drivers	WIN2000, XP

Mass Storage	Specification
FD	Floppy disk interface not supported
HD	E-IDE interface, AT-type, for max. 2 hard disks, 44pin connector, for 1.3, 1.8 and 2.5" hard disk with 44 pins IDE

Standard AT Interfaces:	Specification					
Serial	**Name**	**FIFO**	**IRQs**	**Addr.**	**Standard**	**Option**
	COM1	yes	IRQ4	3F8	RS232C	
	COM2	yes	IRQ3	2F8	RS232C	
	COM1/2 available on headers onboard. For DSub-connectors, option MSB800-CON is needed.					
SuperIO Chip	W83627HF from WINBOND					
Parallel	LPT1 printer interface mode: SPP (output), EPP (bidir.)					
Keyboard	AT or PS/2-keyboard					
Mouse	PS/2					
Speaker	No speaker					
RTC	Integrated into the chipset, RTC with CMOS-RAM 256Byte					
Backup current	<5 µA					
RTC-backup MSB900	Onboard 3.6Volt Lithium 400mAh available					
RTC-backup MSB900L	*External connection, no onboard battery available*					

BUS	Specification
PCI/104	PCI 32Bit Bus, 1 slot
Clock	33MHz defined by the GEODE

USB	Specification
USB	2.0
Transfer rate	480MBps, 12.5MBps / 1.5MBps
Channels	4

Peripheral Extension	Specification
ISA	Not supported
PCI MSB900	With PCI/104 BUS (1 slot), limited I/O space
PCI MSB900L	*Not available*

Power Supply	Specification
Working	8-32Volt ± 5% (peak 36Volt)
Power Rise Time	Unspecified
Power consumption	MSB900/L with HD, MS/KB (PS/2), CRT Monitor Windows XP Desktop: type 8.5-10W
Standby power consumption	MSB900/L: Windows Standby: 2.5W (without MS/KB wakeup function) Windows Standby: 4.5W (with PS/2 wakeup function)

Physical Characteristics	Specification
Dimensions	Length: 146 mm Depth: 102 mm Height: 20 mm
Weight	160g
PCB Thickness	1.6mm / 0.0625 inches nominal
PCB Layer	Multilayer

Operating Environment	Specification
Relative humidity	5-90%, non-condensing
Vibration	5-2000Hz, 0.1G
Shock	1G
Temperature	MSB900*: Operating: Standard version: -25°C to +70°C Extended version: -40°C to +85°C Storage: -55°C to +85°C * = with passive cooler *MSB900L**:* *Operating: Standard version: 0°C to +60°C* *Storage: -55°C to +85°C* *** = without passive cooler*

EMI/EMC (IEC1131-2 refer MIL 461/462)	Specification
ESD Electro Static Discharge	IEC 801-2, EN55101-2, VDE 0843/0847 Part 2 Metallic protection needed Separate ground layer included 15kV single peak
REF Radiated Electromagnetic Field	IEC 801-3, VDE 0843 Part 3, IEC770 6.2.9. (not tested)
EFT Electric Fast Transient (Burst)	IEC 801-4, EN50082-1, VDE 0843 Part 4 250V - 4kV, 50 ohms, Ts=5ns Grade 2: 1kV Supply, 500 I/O, 5kHz
SIR Surge Immunity Requirements	IEC 801-5, IEEE587, VDE 0843 Part 5 Supply: 2kV, 6 pulse/minute I/O: 500V, 2 pulse/minute FD, CRT: none
High-frequency Radiation	EN55022

Compatibility	Specification
MSB900/L	Mechanically compatible to 3.5inch industrial embedded computer boards

All information is subject to change without notice.

2.5. Examples of Ordering Codes

802220 MSB900 with LX900 CPU, 0MB-RAM, Battery, PCI/104 and Video input
802221 MSB900L with LX900 CPU, 0MB RAM, …
802205 MSB800CON COM1, LPT1 Expansion board.

These are only examples; for current ordering codes, please see the current price list.

2.6. Related Application Notes

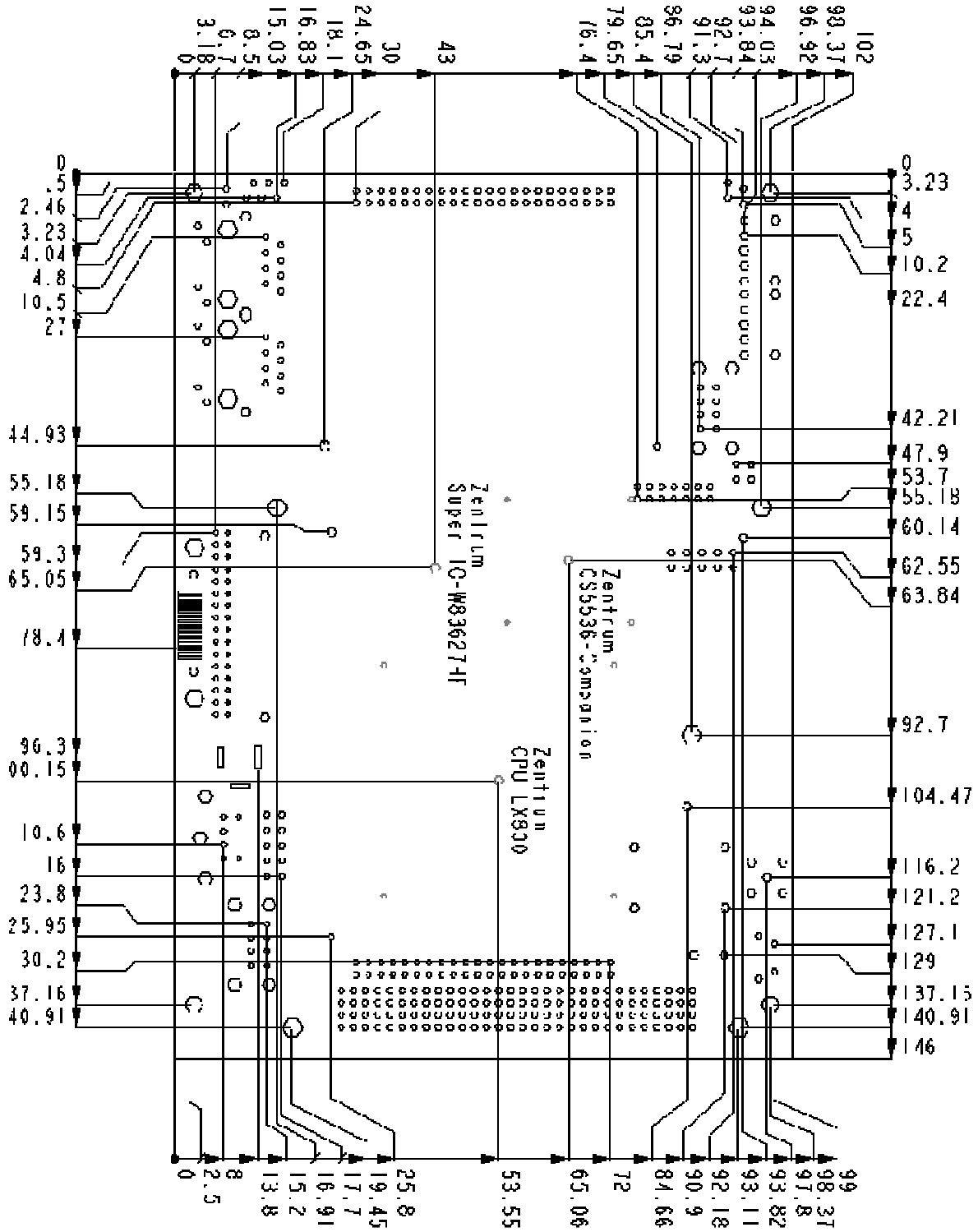
Application Notes are available at *http://www.digitallogic.com* ➔ support, or on any DIGITAL-LOGIC Application CD.

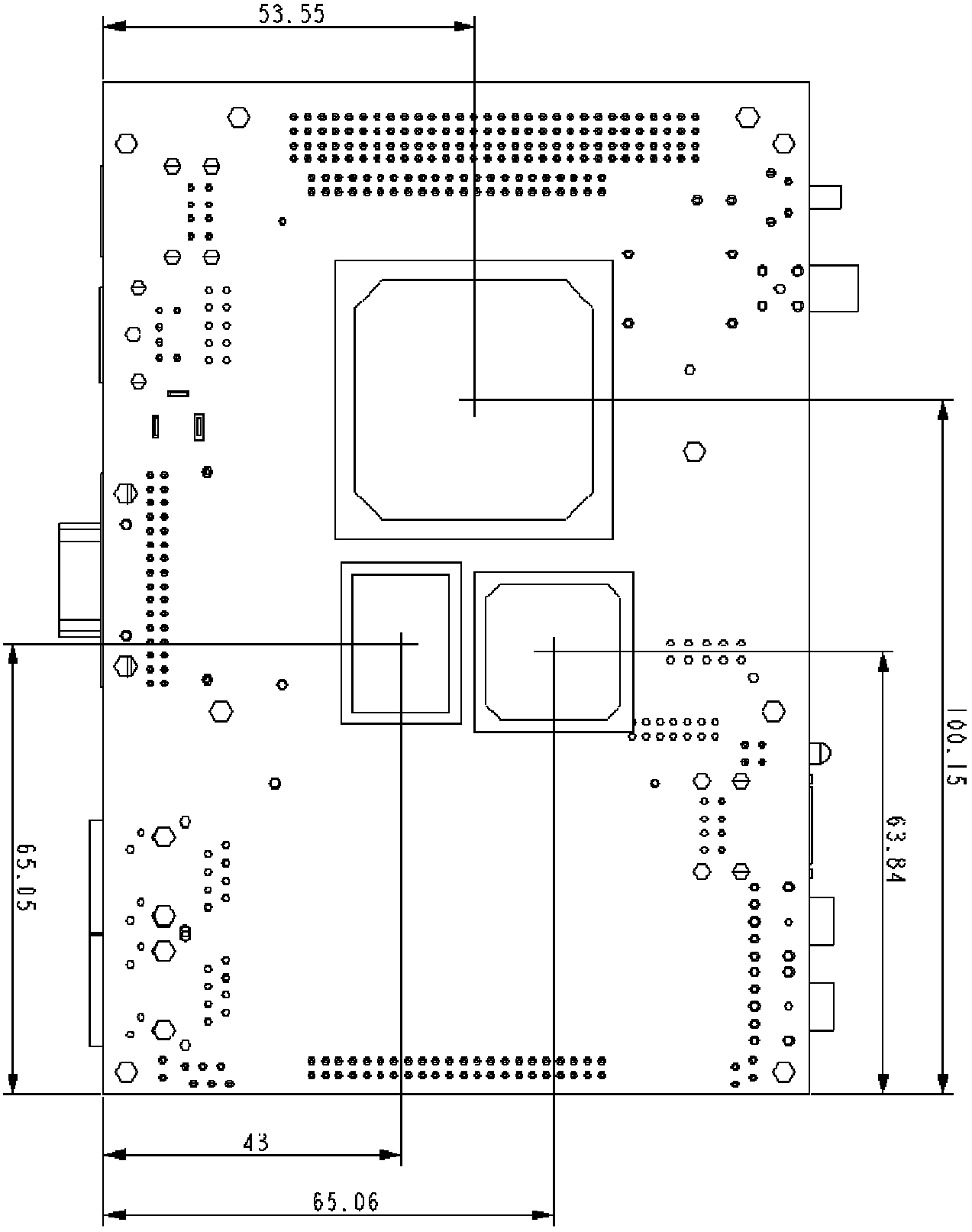
#	Description

2.7. Dimensions & Diagrams

2.7.1. MSB900/L

Board / Version	Unit:	Tolerance:	Date / Author
MSB900/L	mm (millimeter)	+ / - 0.1mm	25.10.2006 / BRR

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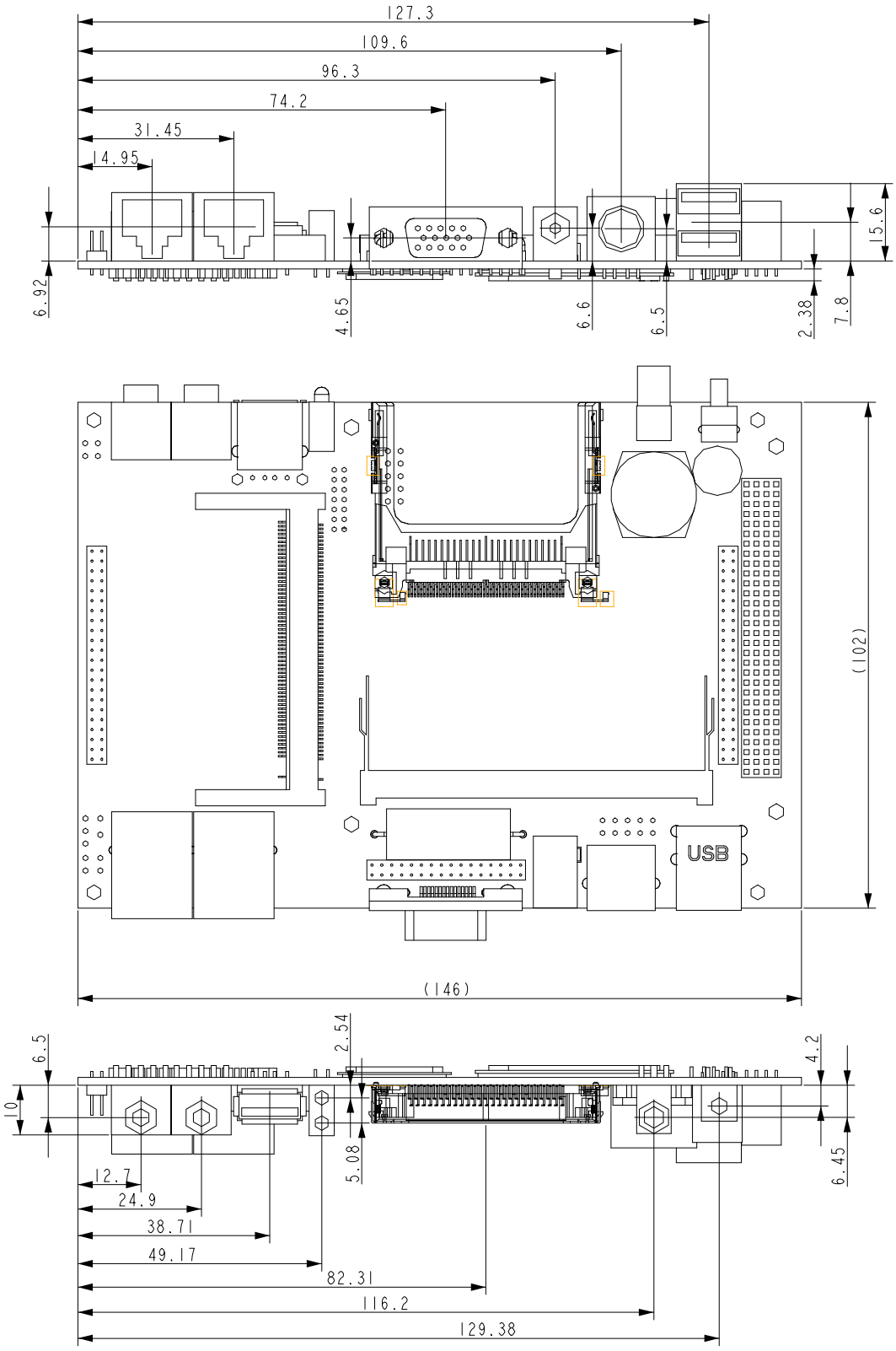
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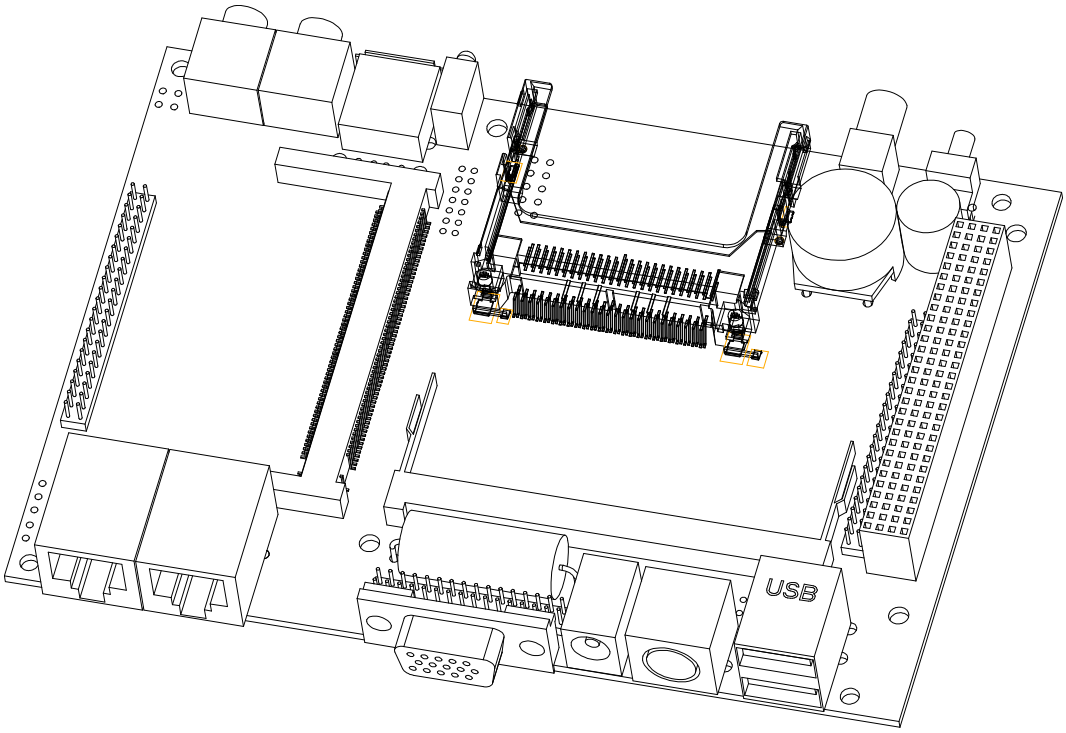
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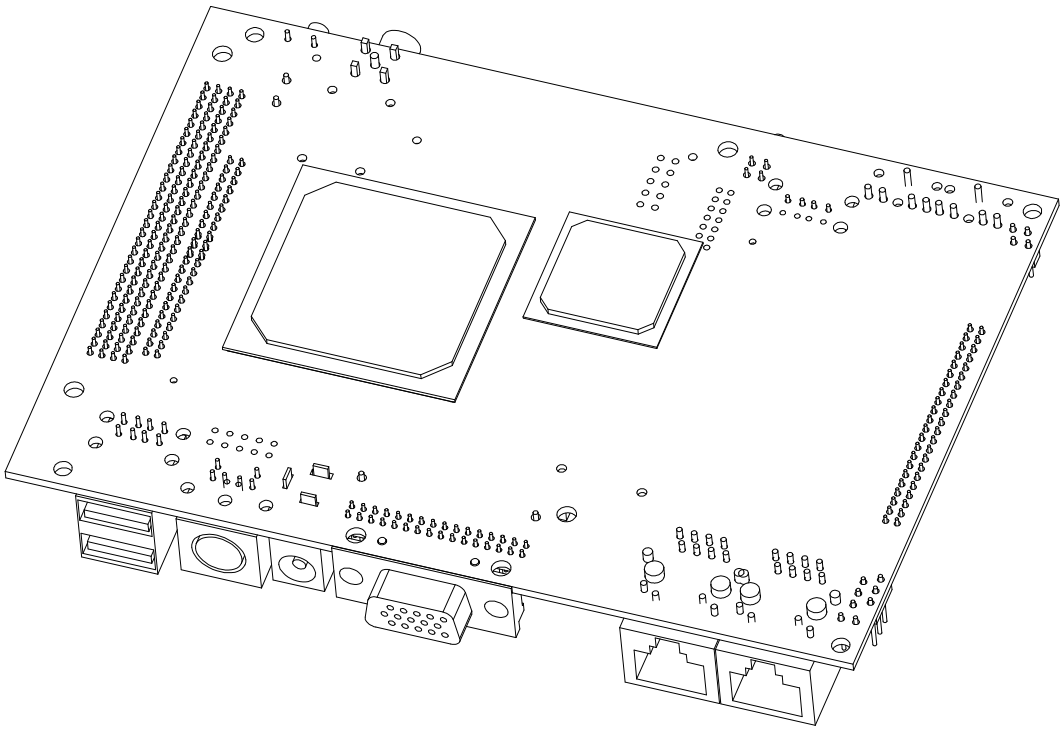
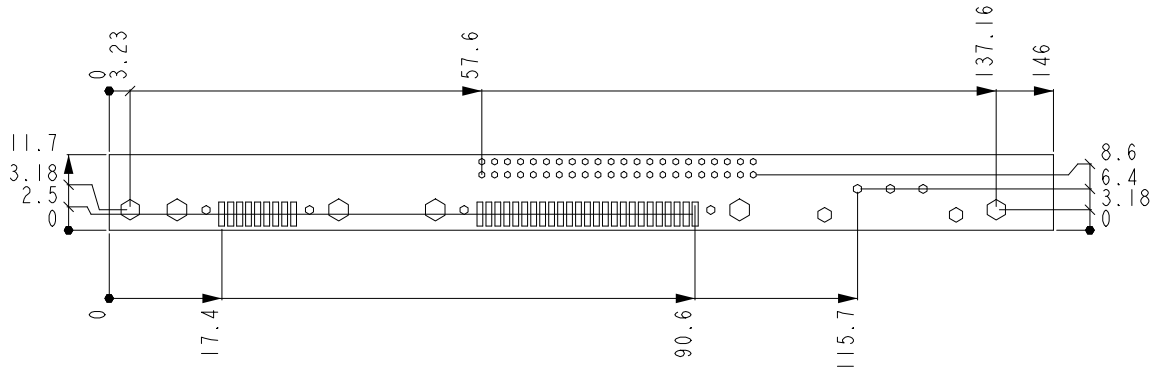
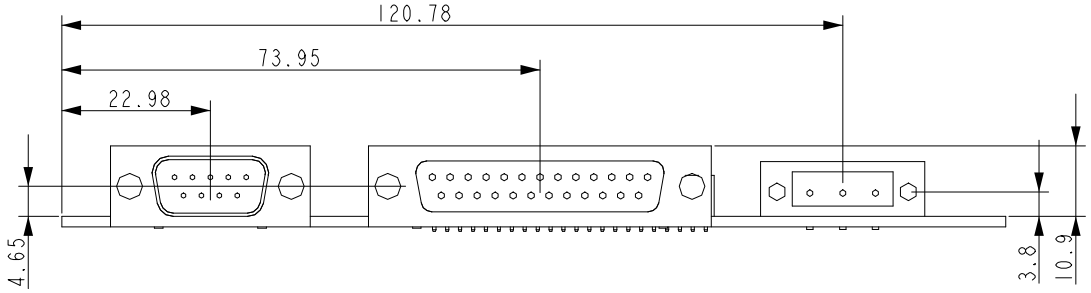
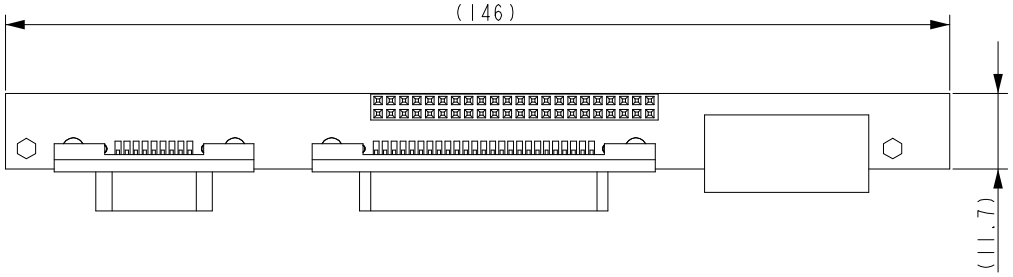


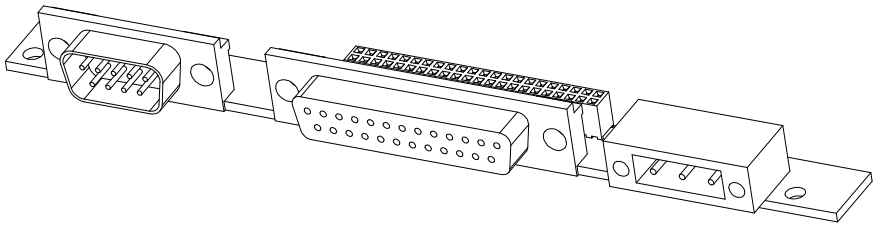
2.7.2. MSB800CON Part Nr 802205

Board / Version	Unit:	Tolerance:	Date / Author
MSB800CON	mm (millimeter)	+ / - 0.1mm	25.10.2006 / BRR









2.8. MSB900/L Incompatibilities to a standard PC/AT

None.

2.9. Related Application Notes

Application Notes are available at *http://www.digitallogic.com* ➔ support, or on any DIGITAL-LOGIC Application CD.

#	Description

2.10. High Frequency Radiation (to meet EN55022)

All connectors are filtered onboard to comply with the EMI standards.

The following filters are used:

Interface	3db-Frequency	Inductivity L and R	Capacitor to GND	Filter-Type	Protection
VGA-RGB		Ferrite	2x 10pF		0V/3V Diode
VGA-HS/VS		33ohms	33pF		0V/3V Diode
VGA-VCC		Ferrite	1nF		None
Video Input	-	-	-	-	None
USB		Inductors	none	DLP31D	Diode SRV05-4 GND/5V
IDE		33ohms series	-	-	None
Sound I/O		Ferrite	1nF		None
PS2-KB		Ferrite	47pF		None
PS2-MS		Ferrite	47pF		None
PS2-VCC		Ferrite	1nF		None
PS2-GND		Ferrite	1nF		None
COM1			47pF		MAX211E
COM2			47pF		MAX211E
LPT1			47pF		none
LAN		Integrated	PULSE	J00-0065NL	Isolated 500V
All 33MHz-Clocks		33Ohms series	10pF		None

2.11. Battery-Lifetime

Battery specs:		Lowest temp. -40°C	Nominal temp. +20°C	Highest temp. +85°C
Manufacturer:	pba			
Type:	ER10280			
Capacity versus Temp:	10uA	420mAh	400mAh	350mAh
Voltage versus Temp.	10uA	3.6V	3.6V	Ca. 3.6V
Nominal values:	3.6V / 400mAh @ 0.5mA / -55°C...~+85°C			

Information taken from the datasheet of ER10280

PRODUCT:	Temperature °C	Battery voltage V	VCC (+5) switched ON µA	VCC (+5V) switched off µA
Battery current:	+25°C	3.6	< 1	< 3
Battery-Lifetime:	+25°C		>3.5 years	>3.5 year

2.11.1. External battery assembling (for the MSB900L):

On the MSB900L board, an external battery can be connected to J3. Attach the battery ground to pin 2.

If the customer wants to connect an external battery, then some precautions have to be taken:

The battery is prohibited from charging. Do not use a rechargeable battery!

The RTC device defines a voltage level of 3.0-3.6V, so use an external battery within this range (inclusive of the diode which is pre-assembled onboard).

3. BUS SIGNALS

3.1. Addressing PCI Devices

3.1.1. MSB900 and MSB900L

DEVICE	IDSEL	PIRQ	#REG	#GNT	Remarks
SLOT 1	AD20	A / B / C / D	3	3	For additional cards (peripheral boards)
Onboard used:					
LAN A	AD28	C	1	1	Onboard device
LAN B	AD29	A	4	4	Onboard device
Mini-PCI	AD27	A / B	5	5	Optional device
CPU	AD11	A	2	2	Onboard device

4. BIOS HISTORY

This BIOS history is for the MSB900/L.

This BIOS history is not for the following products:
MSEP900, MSM900, SM900

Version:	Date:	Status:	Modifications:
1.23	***02.2007***	***Initial Release***	-
			-
			-
			-
			-
			-
			-

Note…
This product has a unique BIOS version. For a description of the other features of the BIOS, please refer to the driver/software/BIOS manual “GEODE_LX800-LX900” on the Product CD.

5. DETAILED SYSTEM DESCRIPTION

This system configuration is based on the ISA architecture. Check the I/O and memory map in this chapter.

5.1. Power Requirements

The power is connected through the wide-range power connector. The supply uses only the +8V to +32V and the ground connection.

Attention:
Make sure the power plug is wired correctly before supplying power to the board! A built-in diode protects the board against reverse polarity.

Tolerance of supply: Must be within 8-32Volt norm.

Test environment for power consumption measurement:

Peripheries:
Hard disk Hitachi Model HTA422020F9ATJ0 20GB
Monitor Eizo Flexscan F340I-W
PS/2-KB Logitech Model iTouch Keyboard
PS/2-MS Logitech Model M-CAA43

Software:
MS-DOS V6.22
WinXP

Current consumption @ 12Volt supply at -40°C/+25°C/+85°C

Mode	Memory	DLAG-Nr.	-30 °C	+25°C	+85 °C
MSB900-600MHz			[mA]	[mA]	[mA]
DOS: C:	1GB			700	
WinXP: Desktop	1GB			700	

5.2. Boot Time

System Boot-Times

Definitions/Boot-Medium	Quick Boot	Normal Boot
MSB900-600MHz	time [s]	time [s]
From hard disk Hitachi Model J4K20-20:		
Boot from hard disk to “Starting MS-DOS”.-Prompt	-	15
Boot from hard disk to XP desktop	-	45
Booting without a storage device (only BIOS)		10

5.3. CPU, Boards and RAMs

5.3.1. CPUs of this MICROSPACE Product

Processor:	Type:	Clock:
GEODE LX900	National	600 MHz

5.3.2. Numeric Coprocessor

It is integrated in the LX900 CPU.

5.3.3. DDRAM Memory

Speed:	333
Size:	DDR-SODIMM
	DDRDIMM 200pin
Bits:	64bit
Capacity:	256-1024MBytes
	DDR-SODIMM
Bank:	1

5.4. Interfaces

5.4.1. Keyboard AT compatible and PS/2 Mouse

The PS/2 Keyboard and Mouse are combined on the PS2-connector. It is needed to use a Y-Cable to connect both, the mouse and the keyboard.

5.4.2. Line Printer Port LPT1

A standard bi-directional LPT port is integrated into the MICROSPACE PC.

Further information about these signals is available in numerous publications, including the IBM technical reference manuals for the PC and AT computers and from other reference documents.

5.4.3. Serial Ports COM1-COM2

The serial channels are fully compatible with 16C550 UARTS. COM1 is the primary serial port, and is supported by the board's ROM-BIOS as the PC-DOS 'COM1' device. The secondary serial port is COM2; it is supported as the 'COM2' device.

Standard: COM 1/2: National PC87317VUL: 2 x 16C550 compatible serial interfaces

Serial Port Connectors COM1, COM2

Pin	Signal Name	Function	in/out	DB25 Pin	DB9 Pin
1	CD	Data Carrier Detect	in	8	1
2	DSR	Data Set Ready	in	6	6
3	RXD	Receive Data	in	3	2
4	RTS	Request To Send	out	4	7
5	TXD	Transmit Data	out	2	3
6	CTS	Clear to Send	in	5	8
7	DTR	Data Terminal Ready	out	20	4
8	RI	Ring Indicator	in	22	9
9	GND	Signal Ground		7	5

The serial port signals are compatible with the RS232C specifications.

5.4.4. Floppy Disk Interface

This is not available with this product; use a USB Floppy.

5.5. Controllers

5.5.1. Interrupt Controllers

An 8259A compatible interrupt controller, within the chipset, provides seven prioritized interrupt levels. Of these, several are normally associated with the board's onboard device interfaces and controllers, and several are available on the AT expansion bus.

Interrupt:	Sources:	Onboard used:
IRQ0	ROM-BIOS clock tick function, from timer 0	yes
IRQ1	Keyboard controller output buffer full	yes
IRQ2	Used for cascade 2. 8259	yes
IRQ3	COM2 serial port	yes
IRQ4	COM1 serial port	yes
IRQ5	LPT2 parallel printer (if present)	no *
IRQ6	Floppy controller	yes
IRQ7	LPT1 parallel printer	yes
IRQ8	Battery backed clock	yes
IRQ9	Free for user	no *
IRQ10	Free for user	no *
IRQ11	Free for user	no *
IRQ12	PS/2 mouse	yes
IRQ13	Math. coprocessor	yes
IRQ14	Hard disk IDE	yes
IRQ15	Free for user	no *

* It may depend on the LAN configuration.

5.6. Timers and Counters

5.6.1. Programmable Timers

An 8253 compatible timer/counter device is also included in the board's ASIC device. This device is utilized in precisely the same manner as in a standard AT implementation. Each channel of the 8253 is driven by a 1.190 MHz clock, derived from a 14.318 MHz oscillator, which can be internally divided in order to provide a variety of frequencies.

Timer 2 can also be used as a general purpose timer if the speaker function is not required.

Timer Assignment

Timer	Function
0	ROM-BIOS clock tick (18.2Hz)
1	DRAM refresh request timing (15 µs)
2	Speaker tone generation time base

5.6.2. RTC (Real Time Clock)

An AT compatible date/time clock is located within the chipset. The device also contains a CMOS static RAM, compatible with that in standard ATs. System configuration data is normally stored in the clock chip's CMOS RAM in a manner consistent with the convention used in other AT compatible computers. To attach an external battery on a MSB900L board refer to section 2.11.1.

5.6.3. Watchdog

The watchdog timer detects a system crash and performs a hardware reset. After power up, the watchdog is always disabled as the BIOS does not send strobes to the watchdog. In case the user wants to take advantage of the watchdog, the application must produce a strobe at least every 800 ms. If no strobe occurs within the 800 ms, the watchdog resets the system.

For more information, please refer to the driver/software/BIOS manual “GEODE_LX800-LX900” on the Product CD. The watchdog feature is integrated in the INT15 function.

There are some programming examples available:
Product CD-Rom or customer download area: \tools\SM855\int15dl\…

5.6.4. ROM-BIOS Sockets

An EPROM socket with 8bit wide data access normally contains the board’s AT compatible ROM-BIOS. The socket takes a 29F020 EPROM (or equivalent) device. The board's wait-state control logic automatically inserts four memory wait states in all CPU accesses to this socket. The ROM-BIOS sockets occupy the memory area from C0000H through FFFFFh; however, the board's ASIC logic reserves the entire area from C0000h through FFFFFh for onboard devices, so that this area is already usable for ROM-DOS and BIOS expansion modules. Consult the appropriate address map for the MICROSPACE PC-Product ROM-BIOS sockets.

5.6.4.1. Standard BIOS ROM

Device:	FWH	
Map:	E0000 - FFFFFh	Core BIOS 128k
	C0000 - C7FFFh	VGA BIOS 32k
	CC000 - CFFFFh	FREE

5.6.5. BIOS CMOS Setup

If wrong setups are memorized in the CMOS-RAM, the default values will be loaded after resetting the RTC/CMOS-RAM by de-soldering the battery.

If the battery is down, it is always possible to start the system with the default values from the BIOS.

5.7. CMOS RAM Map

Systems based on the industry-standard specification include a battery backed Real Time Clock chip. This clock contains at least 64Bytes of non-volatile RAM. The system BIOS uses this area to store information including system configuration and initialization parameters, system diagnostics, and the time and date. This information remains intact even when the system is powered down.

The BIOS supports 128Bytes of CMOS RAM. This information is accessible through I/O ports 70h and 71h. CMOS RAM can be divided into several segments:

- Locations 00h - 0Fh contain the real time clock (RTC) and status information
- Locations 10h - 2Fh contain system configuration data
- Locations 30h - 3Fh contain system BIOS-specific configuration data as well as chipset-specific information
- Locations 40h - 7Fh contain chipset-specific information as well as power management configuration parameters

The following table provides a summary of how these areas may be further divided.

Beginning	Ending	Checksum	Description
00h	0Fh	No	RTC and Checksum
10h	2Dh	Yes	System Configuration
2Eh	2Fh	No	Checksum Value of 10h - 2Dh
30h	33h	No	Standard CMOS
34h	3Fh	No	Standard CMOS - SystemSoft Reserved
40h	5Bh	Yes	Extended CMOS - Chipset Specific
5Ch	5Dh	No	Checksum Value of 40h - 5Bh
5Eh	6Eh	No	Extended CMOS - Chipset Specific
6Fh	7Dh	Yes	Extended CMOS - Power Management
7Eh	7Fh	No	Checksum Value of 6Fh - 7Dh

CMOS Map

Location	Description
00h	Time of day (seconds) specified in BCD
01h	Alarm (seconds) specified in BCD
02h	Time of day (minutes) specified in BCD
03h	Alarm (minutes) specified in BCD
04h	Time of day (hours) specified in BCD
05h	Alarm (hours) specified in BCD
06h	Day of week specified in BCD
07h	Day of month specified in BCD
08h	Month specified in BCD
09h	Year specified in BCD
0Ah	Status Register A Bit 7 = Update in progress Bits 6-4 = Time based frequency divider Bits 3-0 = Rate selection bits that define the periodic interrupt rate and output frequency.
0Bh	Status Register B Bit 7 = Run/Halt 0 Run 1 Halt Bit 6 = Periodic Timer 0 Disable 1 Enable Bit 5 = Alarm Interrupt 0 Disable 1 Enable Bit 4 = Update Ended Interrupt 0 Disable 1 Enable Bit 3 = Square Wave Interrupt 0 Disable 1 Enable Bit 2 = Calendar Format 0 BCD 1 Binary Bit 1 = Time Format 0 12-Hour 1 24-Hour Bit 0 = Daylight Savings Time 0 Disable 1 Enable
0Ch	Status Register C Bit 7 = Interrupt Flag Bit 6 = Periodic Interrupt Flag Bit 5 = Alarm Interrupt Flag Bit 4 = Update Interrupt Flag Bits 3-0 = Reserved
0Dh	Status Register D Bit 7 = Real Time Clock 0 Lost Power 1 Power

Continued...

CMOS Map *continued...*

Location	Description
0Eh	CMOS Location for Bad CMOS and Checksum Flags Bit 7 = Flag for CMOS Lost Power 0 = Power OK 1 = Lost Power Bit 6 = Flag for CMOS checksum bad 0 = Checksum is valid 1 = Checksum is bad
0Fh	Shutdown Code
10h	Diskette Drives Bits 7-4 = Diskette Drive A 0000 = Not installed 0001 = Drive A = 360 kB 0010 = Drive A = 1.2MB 0011 = Drive A = 720 kB 0100 = Drive A = 1.44MB 0101 = Drive A = 2.88MB Bits 3-0 = Diskette Drive B 0000 = Not installed 0001 = Drive B = 360 kB 0010 = Drive B = 1.2MB 0011 = Drive B = 720 kB 0100 = Drive B = 1.44MB 0101 = Drive B = 2.88MB
11h	Reserved
12h	Fixed (Hard) Drives Bits 7-4 = Hard Drive 0, AT Type 0000 = Not installed 0001-1110 = Types 1-14 1111 = Extended drive types 16-44. See location 19h. Bits 3-0 = Hard Drive 1, AT Type 0000 = Not installed 0001-1110 = Types 1-14 1111 = Extended drive types 16-44. See location 2Ah.
13h	Reserved
14h	Equipment Bits 7-6 = Number of Diskette Drives 00 = One diskette drive 01 = Two diskette drives 10, 11 = Reserved Bits 5-4 = Primary Display Type 00 = Adapter with option ROM 01 = CGA in 40 column mode 10 = CGA in 80 column mode 11 = Monochrome Bits 3-2 = Reserved Bit 1 = Math Coprocessor Presence 0 = Not installed 1 = Installed Bit 0 = Bootable Diskette Drive 0 = Not installed 1 = Installed

Continued...

CMOS Map *continued...*

Location	Description
15h	Base Memory Size (in kB) - Low Byte
16h	Base Memory Size (in kB) - High Byte
17h	Extended Memory Size (in kB) - Low Byte
18h	Extended Memory Size (in kB) - High Byte
19h	Extended Drive Type - Hard Drive 0
1Ah	Extended Drive Type - Hard Drive 1
1Bh	Custom and Fixed (Hard) Drive Flags Bits 7-6 = Reserved Bit 5 = Internal Floppy Disk Controller 0 = Disabled 1 = Enabled Bit 4 = Internal IDE Controller 0 = Disabled 1 = Enabled Bit 3 = Hard Drive 0 Custom Flag 0 = Disabled 1 = Enabled Bit 2 = Hard Drive 0 IDE Flag 0 = Disabled 1 = Enabled Bit 1 = Hard Drive 1 Custom Flag 0 = Disabled 1 = Enabled Bit 0 = Hard Drive 1 IDE Flag 0 = Disabled 1 = Enabled
1Ch	Reserved
1Dh	EMS Memory Size Low Byte
1Eh	EMS Memory Size High Byte
1Fh - 24h	Custom Drive Table 0 These 6 Bytes (48 bits) contain the following data: Cylinders 10bits range 0-1023 Landing Zone 10bits range 0-1023 Write Precompensation 10bits range 0-1023 Heads 8bits range 0-15 Sectors/Track 8bits range 0-254
1Fh	Byte 0 Bits 7-0 = Lower 8 bits of Cylinders
20h	Byte 1 Bits 7-2 = Lower 6 bits of Landing Zone Bits 1-0 = Upper 2 bits of Cylinders
21h	Byte 2 Bits 7-4 = Lower 4 bits of Write Precompensation Bits 3-0 = Upper 4 bits of Landing Zone

Continued...

CMOS Map *continued...*

Location	Description
22h	Byte 3 Bits 7-6 = Reserved Bits 5-0 = Upper 6 bits of Write Precompensation
23h	Byte 4 Bits 7-0 = Number of Heads
24h	Byte 5 Bits 7-0 = Sectors Per Track
25h - 2Ah	Custom Drive Table 1 These 6 Bytes (48 bits) contain the following data: Cylinders 10bits range 0-1023 Landing Zone 10bits range 0-1023 Write Precompensation 10bits range 0-1023 Heads 8bits range 0-15 Sectors/Track 8bits range 0-254
25h	Byte 0 Bits 7-0 = Lower 8 bits of Cylinders
26h	Byte 1 Bits 7-2 = Lower 6 bits of Landing Zone Bits 1-0 = Upper 2 bits of Cylinders
27h	Byte 2 Bits 7-4 = Lower 4 bits of Write Precompensation Bits 3-0 = Upper 4 bits of Landing Zone
28h	Byte 3 Bits 7-6 = Reserved Bits 5-0 = Upper 6 bits of Write Precompensation
29h	Byte 4 Bits 7-0 = Number of Heads
2Ah	Byte 5 Bits 7-0 = Sectors Per Track
2Bh	Boot Password Bit 7 = Enable/Disable Password 0 = Disable Password 1 = Enable Password Bits 6-0 = Calculated Password
2Ch	SCU Password Bit 7 = Enable/Disable Password 0 = Disable Password 1 = Enable Password Bits 6-0 = Calculated Password
2Dh	Reserved
2Eh	High Byte of Checksum - Locations 10h to 2Dh
2Fh	Low Byte of Checksum - Locations 10h to 2Dh
30h	Extended RAM (kB) detected by POST - Low Byte
31h	Extended RAM (kB) detected by POST - High Byte
32h	BCD Value for Century

Continued...

CMOS Map *continued...*

Location	Description
33h	Base Memory Installed Bit 7 = Flag for Memory Size 0 = 640kB 1 = 512kB Bits 6-0 = Reserved
34h	Minor CPU Revision Differentiates CPUs within a CPU type (i.e., 486SX vs 486 DX, vs 486 DX/2). This is crucial for correctly determining CPU input clock frequency. During a power-on reset, Reg DL holds minor CPU revision.
35h	Major CPU Revision Differentiates between different CPUs (i.e., 386, 486, Pentium). This is crucial for correctly determining CPU input clock frequency. During a power-on reset, Reg DH holds major CPU revision.
36h	Hotkey Usage Bits 7-6 = Reserved Bit 5 = Semaphore for Completed POST Bit 4 = Semaphore for 0 Volt POST (not currently used) Bit 3 = Semaphore for already in SCU menu Bit 2 = Semaphore for already in PM menu Bit 1 = Semaphore for SCU menu call pending Bit 0 = Semaphore for PM menu call pending
40h-7Fh	Definitions for these locations vary depending on the chipset.

5.8. EEPROM saved CMOS Setup

The EEPROM has different functions, as listed below:

- Backup of the CMOS-Setup values.
- Storing system information (i.e., version, production date, customization of the board, CPU type).
- Storing user/application values.

The EEPROM will be updated automatically after exiting the BIOS setup menu. The system will operate also without any CMOS battery. While booting, the CMOS is automatically updated with the EEPROM values.

Press the Esc-key while powering on the system before the video shows the BIOS message and the CMOS will **not** be updated.

This would be helpful, if wrong parameters are stored in the EEPROM and the setup of the BIOS does not start.

If the system hangs or a problem appears, the following steps must be performed:

1. Reset the CMOS-Setup (disconnect the battery for at least 10 minutes).
2. Press **Esc** until the system starts up.
3. Enter the BIOS Setup:
    a) load DEFAULT values
    b) enter the settings for the environment
    c) exit the setup
4. Restart the system.

The user may access the EEPROM through the INT15 special functions. Refer to that chapter in the GEODE LX800-LX900 manual on the Product CD.

The system information is read-only and uses the SFI functions. Refer to the GEODE LX800-LX900 manual.

5.8.1. EEPROM Memory for Setup

The EEPROM is used for setup and configuration data, stored as an alternative to the CMOS-RTC. Optionally, the EEPROM setup driver may update the CMOS RTC, if the battery is running down and the checksum error would appear and stop the system. The capacity of the EEPROM is 2 kByte.

Organization of the 2048Byte EEPROMs:

Address MAP:	Function:
0000h	**CMOS-Setup valid (01=valid)**
0001h	**Reserved**
0003h	**Flag for DLAG-Message (FF=no message)**
0010h-007Fh	**Copy of CMOS-Setup data**
0080h-00FFh	**Reserved for AUX-CMOS-Setup**
0100h-010Fh	**Serial-Number**
0110h-0113h	Production date (year/day/month)
0114h-0117h	1. Service date (year/day/month)
0118h-011Bh	2. Service date (year/day/month)
011Ch-011Fh	3. Service date (year/day/month)
0120h-0122h	Boot errors (Auto incremented if any boot error occurs)
0123h-0125h	Setup Entries (Auto incremented on every Setup entry)
0126h-0128h	Low Battery (Auto incremented every time the battery is low, EEPROM -> CMOS)
0129h-012Bh	Startup (Auto incremented on every power-on start)
0130h	Reserved
0131h	Reserved
0132h/0133h	BIOS Version (V1.4 => [0132h]:= 4, [0133h]:=1)
0134h/0135h	BOARD Version (V1.5 => [0124h]:=5, [0125h]:=1)
0136h	BOARD TYPE (‘M’=PC/104, ‘E’=Euro, ‘W’=MSWS, ‘S’=Slot, ‘C’=Custom, ‘X’= smartCore or smartModule)
0137h	CPU TYPE: (01h=ELAN300/310, 02h=ELAN400, 05h=P5, 08h=P3, 09h=ELAN520, 10h=P-M).
0200h-03FFh	**Reserved**
0200h-027Fh	Reserved
0400h-07FFh	**Free for Customer use**

5.9. Memory & I/O Map

5.9.1. System Memory Map

The X86 CPU, used as a central processing unit on the MICROSPACE, has a memory address space which is defined by 32 address bits. Therefore, it can address 1 GByte of memory. The memory address MAP is as follows:

CPU GEODE

Address:	Size:	Function / Comments:
000000 - 09FFFFh	640 kBytes	Onboard DRAM for DOS applications
0A0000 - 0BFFFFh	128 kBytes	CGA, EGA, LCD Video RAM 128kB
0C0000 - 0C7FFFh 0C8000 - 0CFFFFh	32 kBytes 32 kBytes	VGA BIOS Free for user
0D0000 - 0DFFFFh	64 kBytes	Free for user
0E0000 - 0EBFFFh 0EC000 - 0EFFFFh	32 kBytes 16 kBytes	Bios BIOS extensions
0F0000 - 0FFFFFh	64 kBytes	Core BIOS
100000 - 1FFFFFFh	31 MBytes	DRAM for extended onboard memory

5.9.2. System I/O map

The following table details the legacy I/O range for 000h through 4FFh. Each I/O location has a read/write (R/W) capability.

Note the following abbreviations:

---	Unknown or can not be determined.
Yes	Read and write the register at the indicated location. No shadow required.
WO	Write only. Value written can not be read back. Reads do not contain any useful information.
RO	Read only. Writes have no effect.
Shw	The value written to the register can not be read back via the same I/O location. Read back is accomplished via a “Shadow” register located in MSR space.
Shw@	Reads of the location return a constant or meaningless value.
Shw$	Reads of the location return a status or some other meaningful information
Rec	Writes to the location are “recorded” and written to the LPC. Reads to the location return the recorded value. The LPC is not read.

I/O Map

I/O Addr.	Function	Size	R/W	Comment
000h	Slave DMA Address - Channel 0	8bit	Yes	16bit values in two transfers.
001h	Slave DMA Counter - Channel 0	8bit	Yes	16bit values in two transfers.
002h	Slave DMA Address - Channel 1	8bit	Yes	16bit values in two transfers.
003h	Slave DMA Counter - Channel 1	8bit	Yes	16bit values in two transfers.
004h	Slave DMA Address - Channel 2	8bit	Yes	16bit values in two transfers.
005h	Slave DMA Counter - Channel 2	8bit	Yes	16bit values in two transfers.
006h	Slave DMA Address - Channel 3	8bit	Yes	16bit values in two transfers.
007h	Slave DMA Counter - Channel 3	8bit	Yes	16bit values in two transfers.
008h	Slave DMA Command/Status - Channels [3:0]	8bit	Shw$	
009h	Slave DMA Request - Channels [3:0]	8bit	WO	Reads return value B2h.
00Ah	Slave DMA Mask - Channels [3:0]	8bit	Shw@	Reads return value B2h.
00Bh	Slave DMA Mode - Channels [3:0]	8bit	Shw@	Reads return value B2h.
00Ch	Slave DMA Clear Pointer - Channels [3:0]	8bit	WO	Reads return value B2h.
00Dh	Slave DMA Reset - Channels [3:0]	8bit	WO	Reads return value B2h.
00Eh	Slave DMA Reset Mask - Channels [3:0]	8bit	Shw@	Reads return value B2h.
00Fh	Slave DMA General Mask - Channels [3:0]	8bit	Shw@	Reads return value B2h.
010h-01Fh	No Specific Usage	---	---	
020h	PIC Master - Command/Status	8bit	Shw$	
021h	PIC Master - Command/Status	8bit	Shw$	
022h-03Fh	No Specific Usage	---	---	
040h	PIT – System Timer	8bit	Shw$	
041h	PIT – Refresh Timer	8bit	Shw$	
042h	PIT – Speaker Timer	8bit	Shw$	
043h	PIT – Control	8bit	Shw$	
044h-05Fh	No Specific Usage	---	---	

Continued…

I/O Map *Continued…*

I/O Addr.	Function	Size	R/W	Comment
060h	Keyboard/Mouse - Data Port	8bit	Yes	If KEL Memory Offset 100h[0] = 1(Emulation-Enabled bit). If MSR 5140001Fh[0] = 1 (SNOOP bit) and KEL Memory Offset 100h[0] = 0 (Emulation-Enabled bit).
061h	Port B Control	8bit	Yes	
062h-063h	No Specific Usage	---	---	
064h	Keyboard/Mouse - Command/ Status	8bit	Yes	If KEL Memory Offset 100h[0] = 1 (Emulation-Enabled bit). If MSR 5140001Fh[0] = 1 (SNOOP bit) and KEL Memory Offset 100h[0] = 0 (Emulation-Enabled bit)
065h-06Fh	No Specific Usage	---	---	
070h-071h	RTC RAM Address/Data Port	8bit	Yes	Options per MSR 51400014h[0]. (***Note 1***)
072h-073h	High RTC RAM Address/Data Port	8bit	Yes	Options per MSR 51400014h[1].
074-077h	No Specific Usage	---	---	
078h-07Fh	No Specific Usage	---	---	
080h	Post Code Display	8bit	Rec	Write LPC and DMA. Read only DMA.
081h	DMA Channel 2 Low Page	8bit	Rec	Upper addr bits [23:16]. Write LPC and DMA. Read only DMA.
082h	DMA Channel 3 Low Page			
083h	DMA Channel 1 Low Page			
084h-086h	No Specific Usage	8bit	Rec	Write LPC and DMA. Read only DMA.
087h	DMA Channel 0 Low Page	8bit	Rec	Upper addr bits [23:16]. Write LPC and DMA. Read only DMA.
088h	No Specific Usage	8bit	Rec	Write LPC and DMA. Read only DMA.
089h	DMA Channel 6 Low Page	8bit	Rec	Upper addr bits [23:16]. Write LPC and DMA. Read only DMA.
08Ah	DMA Channel 7 Low Page			
08B	DMA Channel 5 Low Page			
08Ch-08Dh	No Specific Usage	8bit	Rec	Write LPC and DMA. Read only
08Eh	DMA			
08Fh	DMA C4 Low Page	8bit	Rec	Upper addr bits [23:16]. See comment at 080h.
090h-091h	No Specific Usage	---	---	
092h	Port A	8bit	Yes	If kel_porta_en is enabled, then access Port A; else access LPC.
093h-09Fh	No Specific Usage	---	---	
0A0h	PIC Slave - Command/Status	8bit	Shw$	
0A1h	PIC Slave - Command/Status	8bit	Shw$	
0A2h-0BFh	No Specific Usage	8bit	---	
0C0h	Master DMA Address - Channel 4	8bit	Yes	16bit values in two transfers.
0C1h	No Specific Usage	8bit	---	
0C2h	Master DMA Counter - Channel 4	8bit	Yes	16bit values in two transfers.
0C3h	No Specific Usage	8bit	---	
0C4h	Master DMA Address - Channel 5	8bit	Yes	16bit values in two transfers.
0C6h	Master DMA Counter - Channel 5	8bit	Yes	16bit values in two transfers.
0C7h	No Specific Usage	8bit	---	
0C8h	Master DMA Address - Channel 6	8bit	Yes	16bit values in two transfers.
0CAh	Master DMA Counter - Channel 6	8bit	Yes	16bit values in two transfers.
0CBh	No Specific Usage	8bit	---	

Continued…

I/O Map *Continued…*

I/O Addr.	Function	Size	R/W	Comment
0CCh	Master DMA Address - Channel 7	8bit	Yes	16bit values in two transfers.
0CDh	No Specific Usage	8bit	---	
0CEh	Master DMA Counter - Channel 7	8bit	Yes	16bit values in two transfers.
0CFh	No Specific Usage	8bit	---	
0D0h	Master DMA Command/Status – Channels [7:4]	8bit	Shw$	
0D1h	No Specific Usage	8bit	---	
0D2h	Master DMA Request - Channels [7:4]	8bit	WO	
0D3h	No Specific Usage	8bit	---	
0D4h	Master DMA Mask - Channels [7:4]	8bit	Yes	
0D5h	No Specific Usage	8bit	---	
0D6h	Master DMA Mode - Channels [7:4]	8bit	Shw@	
0D7h	No Specific Usage	8bit	---	
0D8h	Master DMA Clear Pointer - Channels [7:4]	8bit	WO	
0D9h	No Specific Usage	8bit	---	
0DAh	Master DMA Reset - Channels [7:4]	8bit	WO	
0DBh	No Specific Usage	8bit	---	
0DCh	Master DMA Reset Mask - Channels [7:4]	8bit	WO	
0DDh	No Specific Usage	8bit	---	
0DEh	Master DMA General Mask - Channels [7:4]	8bit	Shw@	
0DFh	No Specific Usage	8bit	---	
0E0h-2E7h	No Specific Usage	---	---	
2E8h-2EFh	UART/IR - COM4	8bit	---	MSR bit enables/disables into I/O 2EFh space. (UART1 MSR 51400014h[18:16], UART2 MSR 51400014h[22:20]). Defaults to LPC.
2F0h-2F7h	No Specific Usage	---	---	
2F8h-2FFh	UART/IR - COM2	8bit	---	MSR bit enables/disables into I/O 2FFh space. (UART1 MSR 51400014h[18:16], UART2 MSR 51400014h[22:20]). Defaults to LPC.
300h- 36Fh	No Specific Usage	---	---	
370h	Floppy Status R A	8bit	RO	Second Floppy.
371h	Floppy Status R B	8bit	RO	Second Floppy.
372h	Floppy Digital Out	8bit	Shw@	Second Floppy.
373h	No Specific Usage	8bit	---	
374h	Floppy Cntrl Status	8bit	RO	Second Floppy.
375h	Floppy Data	8bit	Yes	Second Floppy.
376h	No Specific Usage	8bit	---	
377h	Floppy Conf Reg	8bit	Shw$	Second Floppy.
378h-3E7h	No Specific Usage	---	---	
3E8h-3EFh	UART/IR - COM3	8bit	---	MSR bit enables/disables into I/O 3EFh space. (UART1 MSR 51400014h[18:16], UART2 MSR 51400014h[22:20]). Defaults to LPC.
3F0h	Floppy Status R A	8bit	RO	First Floppy.

Continued…

I/O Map *Continued…*

I/O Addr.	Function	Size	R/W	Comment
3F1h	Floppy Status R B	8bit	RO	First Floppy.
3F2h	Floppy Digital Out	8bit	Shw@	First Floppy.
3F3h	No Specific Usage	8bit	---	
3F4h	Floppy Cntrl Status	8bit	RO	First Floppy.
3F5h	Floppy Data	8bit	Yes	First Floppy.
3F6h	No Specific Usage	8bit	---	
3F7h	Floppy Conf Reg	8bit	Shw$	First Floppy.
3F8h-3FFh	UART/IR - COM1	8bit	---	MSR bit enables/disables into I/O 3FFh space. (UART1 MSR 51400014h[18:16], UART2 MSR 51400014h[22:20]). Defaults to LPC.
480h	No Specific Usage	8bit	WO	Write LPC and DMA. Read only DMA.
481h	DMA Channel 2 High Page	8bit	Rec	Upper addr bits [31:24]. Write LPC and DMA. Read only DMA.
482h	DMA Channel 3 High Page			
483h	DMA Channel 1 High Page			
484h-486h	No Specific Usage	8bit	WO	Write LPC and DMA. Read only DMA.
487h	DMA Channel 0 High Page	8bit	Rec	Upper addr bits [31:24]. Write LPC and DMA. Read only DMA.
489h	DMA Channel 6 High Page	8bit	Rec	Upper addr bits [31:24]. Write LPC and DMA. Read only DMA.
48Ah	DMA Channel 7 High Page			
48Bh	DMA Channel 5 High Page			
48Ch-48Eh	No Specific Usage	8bit	WO	Write LPC and DMA. Read only DMA.
48Fh	DMA Channel 4 High Page	8bit	Rec	Upper addr bits [31:24]. Write LPC and DMA. Read only DMA.
490h-4CFh	No Specific Usage	---	---	
4D0h	PIC Level/Edge	8bit	Yes	IRQ0-IRQ 7.
4D1h	PIC Level/Edge	8bit	Yes	IRQ8-IRQ15.
4D2h-4FFh	No Specific Usage	---	---	

Note 1: The Diverse Device Snoops writes to this port and maintains the MSB as NMI enabled. When low, NMI is enabled. When high, NMI is disabled. This bit defaults high. Reads of this port return bits [6:0] from the on-chip or off-chip target, while Bit 7 is returned from the “maintained” value.

6. VGA

6.1. VGA/LCD Controller of the Geode LX900

- Highly integrated flat panel and CRT GUI Accelerator & Multimedia Engine, Palette/DAC, Clock Synthesizer, and integrated frame buffer
- HiQColor™ Technology implemented with TMED (Temporal Modulated Energy Distribution)
- Hardware Windows Acceleration
- Hardware Multimedia Support
- High-Performance flat panel display resolution and color depth at 3.3V
- 18/24bit direct interface to color TFT panels (X1)
- Advanced Power Management minimizes power usage in:
  - Normal operation
  - Standby (Sleep) modes
  - Panel-Off Power-Saving Mode
- VESA standards supported
- Fully compatible with IBM® VGA
- Driver support for Windows XP, Windows 2000, Windows 98, Windows NT4.0

Attention!
When connecting or disconnecting the monitor, be very careful. Also hold the socket on the board at the same time to add stability.

6.2. Graphic Modes

Bios settings: 254MB video memory (shared)

Resolution	Col. Dept.	Frequency
800x600	16bit / 32bit	60Hz – 100Hz
1024x768	16bit / 32bit	60Hz – 100Hz
1152x864	16bit / 32bit	60Hz – 100Hz
1280x1024	16bit / 32bit	60Hz – 100Hz
1600x1200	16bit / 32bit	60Hz – 100Hz
1920x1440	16bit / 32bit	60Hz – 85Hz

7. VIDEO INPUT

The MSB900 contains a low-cost video input port. It consist of LX900's video input port (VIP) and the external frame grabber chip SAA7111A. This port is capable of digitizing a CVBS video signal with 15 frames per second at a resolution of 352x288bits. Note that this frame rate is only achievable when the raw data stream is compressed before being stored on the hard drive. Driver support is currently available for the Windows XP platform.

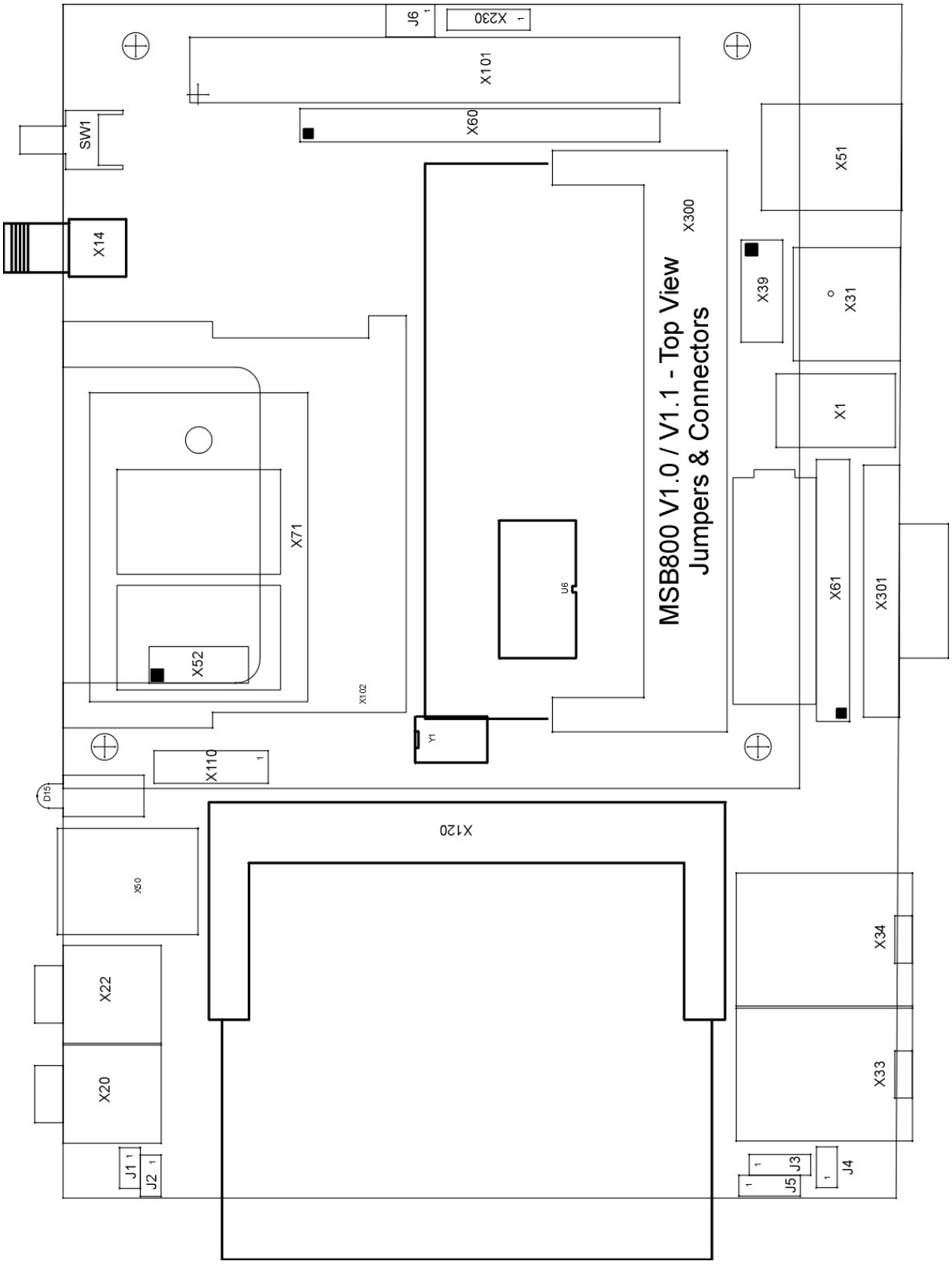
8. DESCRIPTION OF THE CONNECTORS

Flat cable

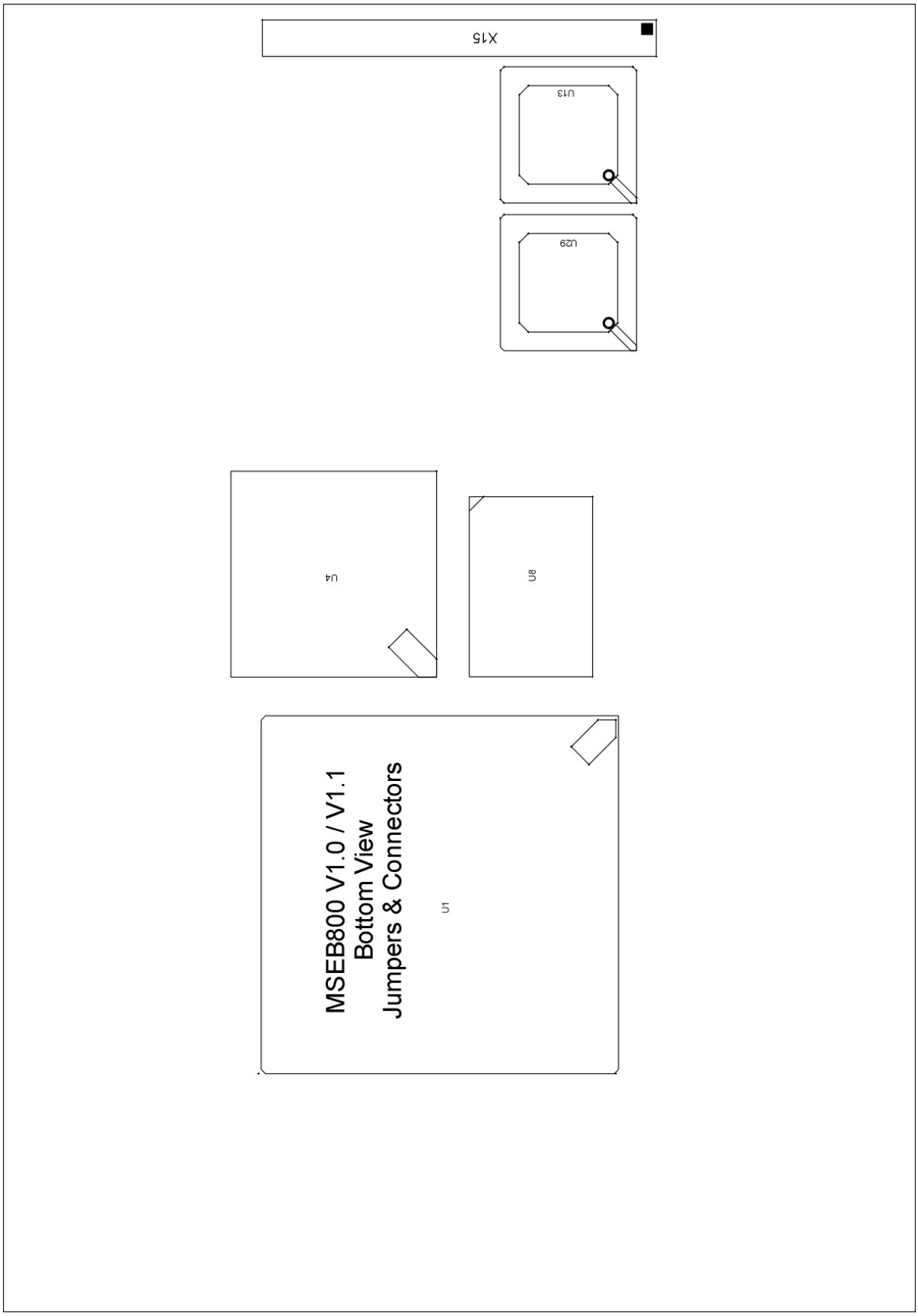
- 44pin IDE is: IDT Terminal for Dual Row (2.00mm grid) and 1.00mm flat cable
- All others are: IDT Terminal for Dual Row 0.1" (2.54mm grid) and 1.27mm flat cable
- **NC**: not connected

Connector	Structure	Pin	Remarks
X1	Power	2pin jack plug	
X14	Video Input	SMA	
X15	Operator panel connector / Flat panel	44pin RM 2.0	Not assembled
X20	Sound MIC stereo input	3.5mm jack plug	
X22	Sound speaker stereo output	3.5mm jack plug	
X31	Keyboard PS/2 and Mouse Utility connector	PS/2	
X33	LAN Port A	RJ45	
X34	LAN Port B	RJ45	
X39	COM2 serial interface connector	10pin RM 2.54mm	
X50	USB 0/1 connector	Dual-USB	
X51	USB 2/3 connector	Dual-USB	
X52	Socket for USB UDOC	10pin RM2.54mm	Not assembled
X60	IDE PATA connector	44pin RM 2.0	
X61	COM1 and LPT connector	32pin RM 2.54mm	
X71	CompactFlash Socket	50pin	
X101	PCI/104 expansion connector	120pin	
X110	POD-Port interface connector	14pin	
X120	MiniPCI socket	124pin	
X230	JTAG-Port	4 pin	
X301	DSUB VGA connector	15pin DSUB	High-density

Top view of the MSB900/L



Bottom view of the MSB900/L



X1 Power Supply

Pin	Signal
1 (Shield)	Power supply 8-30V
2	**NC**
3	Power supply GND

X14 Video IN

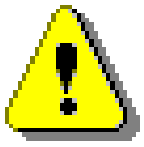
Pin	Signal	Pin	Signal
1	CVBS	2	GND

X15 Operator Panel / Flat Panel (bottom side)

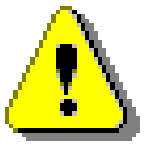
X15 is intended to be used internally to attach an operator panel. Some signals may not be present or are shared with other connectors. This connector is not assembled and is only for OEM-specific applications. A 2mm x 44pin header is needed.

Pin	Signal
1	GND
2	VCC (+5V output)
3	LVDS YAM0
4	LVDS YAP0
5	GND
6	VCC (+5V output)
7	LVDS YAM1
8	LVDS YAP1
9	GND
10	VCC (+5V output)
11	LVDS YAM2
12	LVDS YAP2
13	GND
14	Enable VDD
15	LVDS CLKAP
16	LVDS CLKAM
17	CRT red
18	CRT green
19	CRT blue
20	CRT hsync
21	CRT vsync
22	CRT SCL
23	CRT SDA
24	GND
25	COM2 DCD
26	COM2 DSR
27	COM2 RXD
28	COM2 RTS
29	COM2 TXD
30	COM2 CTS
31	COM2 DTR
32	COM2 RI
33	SYS_RST#
34	VCC3 (+3.3V output)
35	USB D-
36	USB D+
37	VCC3 (+3.3V output)
38	SMB SCL
39	SMB SDA
40	AVR PA0
41	AVR PA3
42	DCMAIN (filtered power input)
43	GND
44	VCC (+5V output)

Note...
VCC: max. 0.5 Amp
VCC3: max. 0.5 Amp
DCMAIN: DC supply input must be within the 8-30V range.

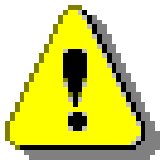


Attention!
If the VGA or COM2 signals on X15 are used, the X10 (VGA connector) or the X39 (COM2 connector) **must not** be connected.



Attention!
USB-signals on X15 are multiplexed with the USB-Port1. They must be enabled by soldering the two resistors.

X15 Reverse Pin Configuration MSB900 LVDS X15 (on component side)



Attention!
When X15 is soldered on the component side, a different pin numbering schema must be applied. Odd and even pin numbers are swapped. ***Ignoring this warning may result in the destruction of any attached devices such as displays!***

Pin	Signal
1	VCC (+5V Output)
2	GND
3	LVDS_YAP0
4	LVDS_YAM0
5	VCC (+5V Output)
6	GND
7	LVDS_YAP1
8	LVDS_YAM1
9	VCC (+5V Output)
10	GND
11	LVDS_YAP2
12	LVDS_YAM2
13	Enable VDD
14	GND
15	LVDS_CLKAM
16	LVDS_CLKAP
17	CRT green
18	CRT red
19	CRT hsync
20	CRT blue
21	CRT SCL
22	CRT vsync
23	GND
24	CRT SDA
25	COM2 DSR
26	COM2 DCD
27	COM2 RTS
28	COM2 RXD
29	COM2 CTS
30	COM2 TXD
31	COM2 RI
32	COM2 DTR
33	VCC3 (+3.3V Output)
34	SYS_RST#
35	USB D+
36	USB D-
37	SMB SCL
38	VCC3 (+3.3V Output)
39	AVR PA0
40	SMB SDA
41	DCMAIN (filtered power input)
42	AVR PA3
43	VCC (+5V Output)
44	GND

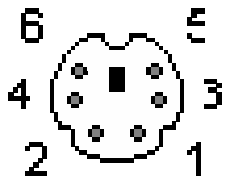
X31 Keyboard PS/2 and Mouse Utility Connector

Connector and Adapter

	Mini- DIN PS/2 (6 PC)	Remarks
Shield	Shield	KEYBOARD
DATA	1	
GND	3	
VCC (+5V)	4	
CLK	5	

	Mini- DIN PS/2 (6 PC)	Remarks
VCC (+5V)	4	MOUSE
DATA	2	
GND	3	
CLK	6	

PS/2 Front side (female)



X33 10/100 BASE-T Interface Connector 0

Pin	Signal (CAT 5)
1	TX+
2	TX-
3	RX+
4	
5	
6	RX-
7	
8	

X34 10/100 BASE-T Interface Connector 1

Pin	Signal
1	TX+
2	TX-
3	RX+
4	
5	
6	RX-
7	
8	

X39 Serial Port COM2

Header onboard	D-SUB connector	Signal
Pin 1	Pin 1	DCD
Pin 2	Pin 6	DSR
Pin 3	Pin 2	RxD
Pin 4	Pin 7	RTS
Pin 5	Pin 3	TxD
Pin 6	Pin 8	CTS
Pin 7	Pin 4	DTR
Pin 8	Pin 9	RI
Pin 9	Pin 5	GND
Pin 10		open

Attention!
If the X39 connector is used, **DO NOT** connect the COM2 signals on the X15 connector!

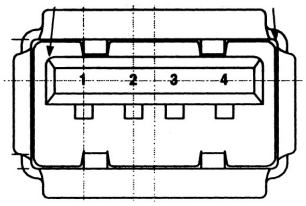
X50 USB 1 Connector (Dual-USB)

Pin	Signal	Remarks
1	VCC	
2	USB-P1-	
3	USB-P1+	
4	GND	
5	VCC	On MPC20/21, not assembled.
6	USB-P2-	
7	USB-P2+	
8	GND	

X51 USB 2 Connector (Dual USB)

Pin	Signal	Remarks
1	VCC	
2	USB-P2-	
3	USB-P2+	
4	GND	
5	VCC	
6	USB-P4-	
7	USB-P4+	
8	GND	

Pin 1	VCC
Pin 2	USB-P-
Pin 3	USB-P+
Pin 4	GND



X52 USB UDOC (not assembled)

Pin	Signal	Pin	Signal
1	VCC	6	**NC**
2	**NC**	7	GND
3	USB-P2-	8	**NC**
4	**NC**	9	**NC**
5	USB-P2+	10	**NC**

Attention!
X52 for USB-DOC-Flash drives are only for OEM use. The connector is not assembled. The UDOC may be assembled if the CompactFlash is not assembled.

X60 IDE Interface

Pin	Signal	Pin	Signal
1	Reset (active low)	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	(keypin) **NC**
21	DREQ	22	GND
23	IOW (active low)	24	GND
25	IOR (active low)	26	GND
27	IORDY	28	ALE / Master-Slave
29	DACK	30	GND
31	IRQ14	32	**NC**
33	ADR1	34	**NC**
35	ADR0	36	ADR2
37	CS0 (active low)	38	CS1 (active low)
39	LED (active low)	40	GND
41	VCC Logic	42	VCC Motor
43	GND	44	**NC**

X61 Serial Port COM1, Parallel Port LPT1

Header onboard	D-SUB connector	Signal
Pin 1	Pin 1	DCD
Pin 2	Pin 6	DSR
Pin 3	Pin 2	RxD
Pin 4	Pin 7	RTS
Pin 5	Pin 3	TxD
Pin 6	Pin 8	CTS
Pin 7	Pin 4	DTR
Pin 8	Pin 9	RI
Pin 9	Pin 5	GND
Pin 10		GND
Pin 11		select
Pin 12	Pin 12	paper end
Pin 13	Pin 11	busy
Pin 14	Pin 10	acknowledge
Pin 15	Pin 9	data 7
Pin 16	Pin 8	data 6
Pin 17	Pin 7	data 5
Pin 18	Pin 6	data 4
Pin 19	Pin 5	data 3
Pin 20	Pin 17	shift in
Pin 21	Pin 4	data 2
Pin 22	Pin 16	init printer
Pin 23	Pin 3	data 1
Pin 24	Pin 15	error
Pin 25	Pin 2	data 0
Pin 26	Pin 14	auto feed
Pin 27	Pin 1	strobe
Pin 28	Pin 23-25	GND
Pin 29		power supply GND
Pin 30		power supply 8-30V
Pin 29		power supply GND
Pin 30		power supply 8-30V

X101 PCI-104 BUS Interface

Pin	A	B	C	D
1	GND/5.0V KEY2	Reserved	+5	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0*	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1*	AD15	+3.3V
9	SERR*	GND	SB0*	PAR
10	GND	PERR*	+3.3V	SDONE
11	STOP*	+3.3V	LOCK*	GND
12	+3.3V	TRDY*	GND	DEVSEL*
13	FRAME*	GND	IRDY*	+3.3V
14	GND	AD16	+3.3V	C/BE2*
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3*	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0*	GND	REQ1*	VI/O
24	GND	REQ2*	+5V	GNT0*
25	GNT1*	VI/O	GNT2*	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD*	+5V	RST*
29	+12V	INTA*	INTB*	INTC*
30	-12V	Reserved	Reserved	GND/3.3V KEY2

Notes:

1. The shaded area denotes power or ground signals.
2. The KEY pins are to guarantee proper module installation. Pin-A1 will be removed and the female side plugged for 5.0V I/O signals and Pin-D30 will be modified in the same manner for 3.3V I/O. It is highly recommended that both KEY pins (A1 and D30) be electrically connected to GND for shielding. **DLAG boards have them as NC (not connected).**

X110 LPC-Port

Only for factory and POD-Diagnostic use.

Pin	Signal	Pin	Signal
1	VCC 3.3V	2	LAD0
3	LFrame#	4	LAD1
5	PCI_RST#	6	LAD2
7	FWH_TBL#	8	LAD3
9	VCC 5V	10	PCI_RST#
11	LPC_Clock	12	nc
13	Ground	14	FWH_Control

X230 JTAG-Port

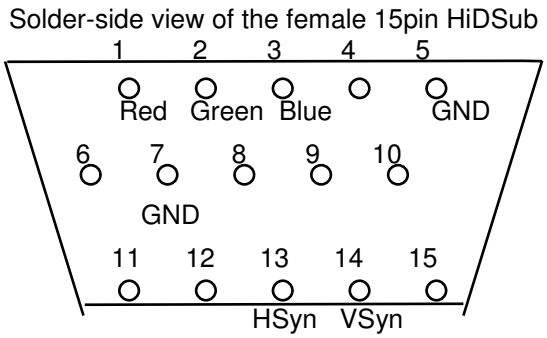
Pin	Signal	Pin	Signal
1	TCK	2	TMS
3	TDI	4	TDO

X301 VGA Monitor (CRT-Signals)

15pins High-Density DSub	
Pin	**Signal**
1	Red
2	Green
3	Blue
13	H-Synch
14	V-Synch
5 + 11	Bridged
5, 6, 7, 8	Grounded

The VGA-CRT signals from J2 must be wired to a standard VGA High Density DSub-connector (female):

The LCD signals must be wired panel-specific.



Attention!
If the X10 connector is used, **DO NOT** connect the VGA signals on the X15 connector!

9. JUMPER LOCATIONS ON THE BOARD

The following figure shows the location of all jumper blocks on the MSB900/L board. The numbers shown in this figure are silk screened on the board so that the pins can easily be located. This chapter refers to the individual pins for these jumpers. The default jumper settings are indicated with asterisks.

Be careful: some jumpers are soldering bridges; you will need a miniature soldering station with a vacuum pump.

9.1. The Jumpers on MSB900/L

Settings written in bold are defaults.

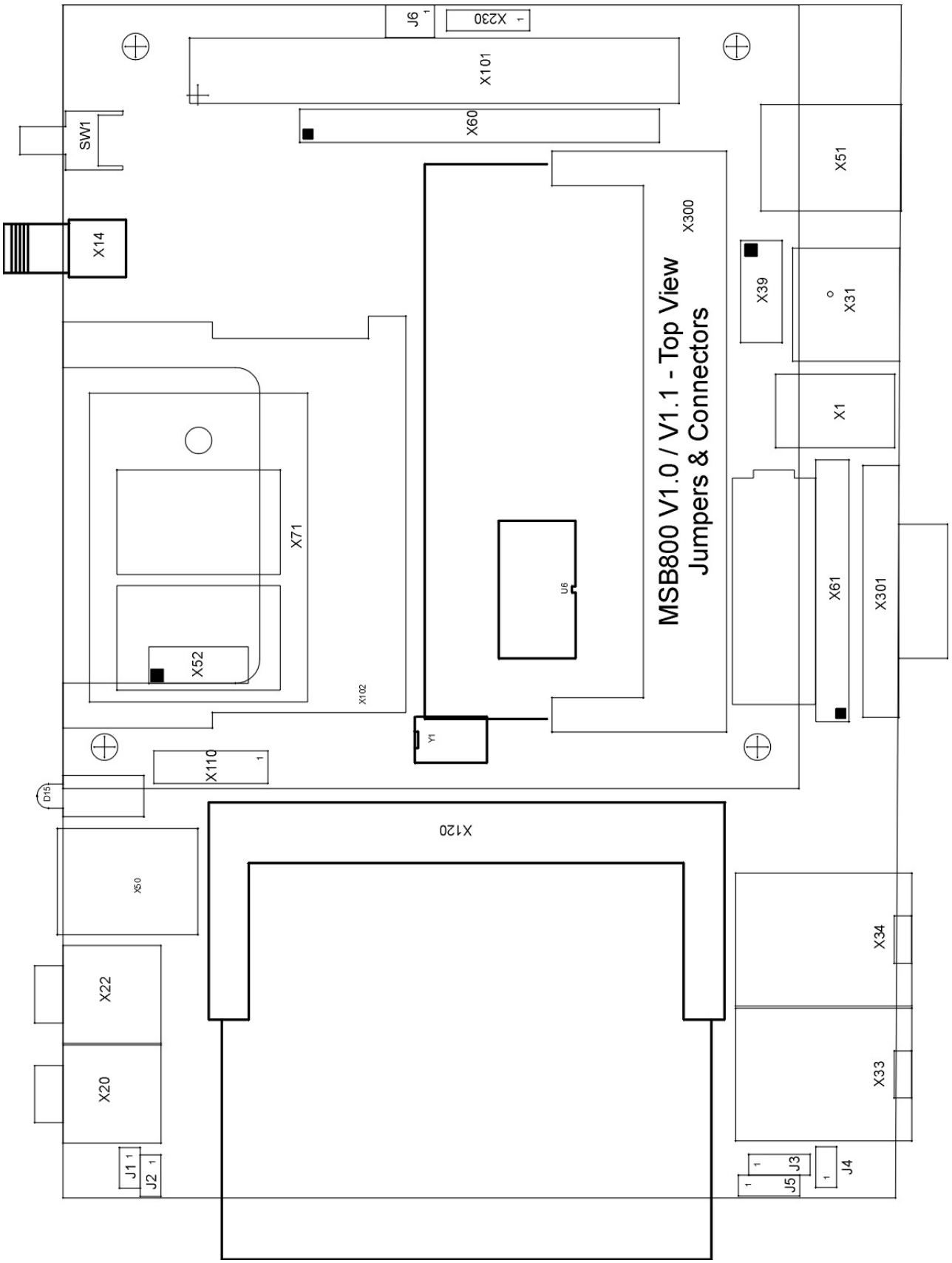
Jumper	Structure	1-2 / open	2-3 / closed	Remarks
J1	CompactFlash master	Slave	**Master**	
J2	Autostart function	Enabled	N/A	1)
J3	Disconnect Battery	**Disabled**	N/A	
J4	Disconnect CMOS EEPROM	**Disabled**	N/A	

1) With the autostart function enabled, the system will start booting up within 2 seconds after the power supply is turned on.

9.2. Reload Default BIOS Settings

To reload default BIOS settings when the system refuses to boot after defective BIOS settings have been made please proceed as follows.

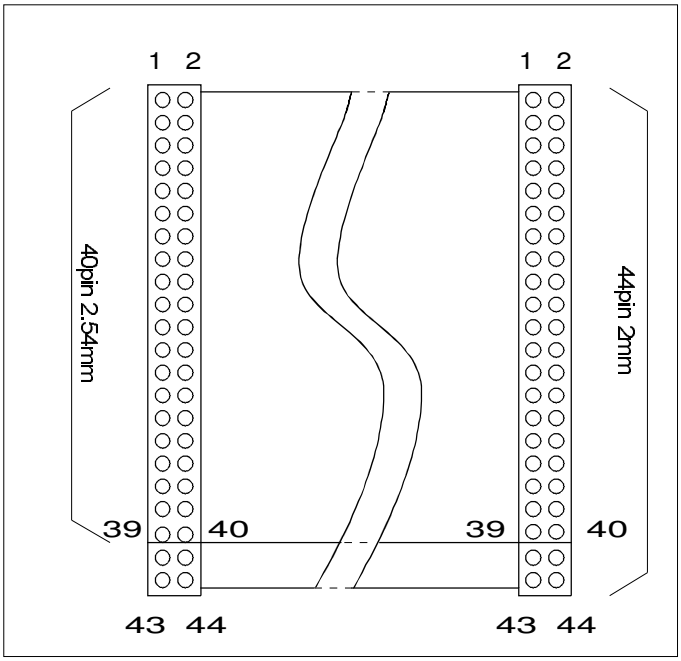
- Turn off the system.
- Remove J3 on MSB900 or disconnect the optional external battery on the MSB900L.
- Remove J4.
- Turn on the system and enter the BIOS setup menu.
- Close J4 and J5 or attach the optional external battery.
- Choose save and exit in the BIOS setup menu.


MSB800 V1.0 / V1.1 - Top View
Jumpers & Connectors
J6
X230
X101
X60
SW1
X51
X14
X300
X39
X31
X1
X71
U6
X61
X301
X52
X102
Y1
X110
D15
X120
X50
X34
X22
X33
X20
J1
J2
J3
J4
J5

10.CABLE INTERFACES

10.1. The Hard Disk Cable 44pin

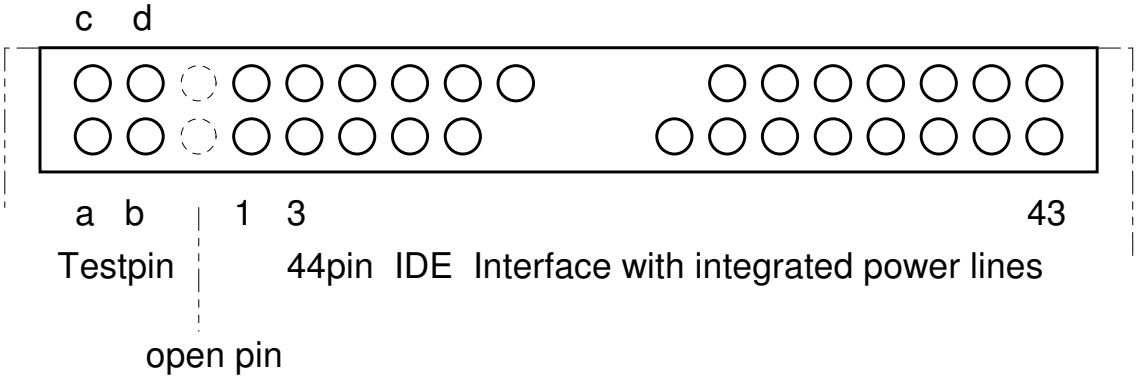
IDT Terminal for Dual Row (2.00mm grid) and 1.00mm flat cable; 44pins = 40pins signal and 4pins power.



Max. length for the IDE cable is 30cm.

Attention!
Check the pin 1 marker of the cable and the connector before you power-on. Refer to the technical manual of the installed drives because a wrong cable will immediately destroy the drive and/or the MICROSPACE MSB900/L board. In this case the warranty is void! Without the technical manual you may not connect this type of drive.

The 44pin IDE connector on the drives is normally composed of the 44 pins, 2 open pins and 4 test pins, 50 pins in total. Leave the 4 test pins unconnected.



10.2. The COM1/LPT Serial Interface Cable

Terminal for dual row 2mm grid and 1mm flat cable.

Connector X61

Pin	Signal	COM1 9pin D-Sub male
Pin 1	= DCD	1
Pin 2	= DSR	6
Pin 3	= RXD	2
Pin 4	= RTS	7
Pin 5	= TXD	3
Pin 6	= CTS	8
Pin 7	= DTR	4
Pin 8	= RI	9
Pin 9	= GND	5
Pin 10		

Pin	Signal	LPT1 25pin D-Sub female
Pin 11	= SELECT	13
Pin 12	= Paper end	12
Pin 13	= Busy	11
Pin 14	= Acknowledge	10
Pin 15	= Data 7	9
Pin 16	= Data 6	8
Pin 17	= Data 5	7
Pin 18	= Data 4	6
Pin 19	= Data 3	5
Pin 20	= Shift in	17
Pin 21	= Data 2	4
Pin 22	= Init	16
Pin 23	= Data 1	3
Pin 24	= Error	15
Pin 25	= Data 0	2
Pin 26	= Autofeed	14
Pin 27	= Strobe	1
Pin 28	= GND	18-25

Attention!

- Do not short circuit these signal lines.
- Never connect any pins on the same plug or to any other plug on the MICROSPACE MSB900/L. The +/-10 Volts will immediately destroy the MICROSPACE core logic. In this case the warranty is void!
- Do not overload the output; the maximum output of the current converters is 10mA.

10.3. The COM2 Serial Interface Cable

DT terminal for dual row 0.1" (2.54mm grid) and 1.27mm flat cable.

Connector X39

Pin	Signal	COM2 9pin D-Sub male
Pin 1	= DCD	1
Pin 2	= DSR	6
Pin 3	= RXD	2
Pin 4	= RTS	7
Pin 5	= TXD	3
Pin 6	= CTS	8
Pin 7	= DTR	4
Pin 8	= RI	9
Pin 9	= GND	5
Pin 10		

Attention!

- Do not short circuit these signal lines.
- Never connect any pins on the same plug or to any other plug on the MICROSPACE MSB900/L. The +/-10 Volts will immediately destroy the MICROSPACE core logic. In this case the warranty is void!
- Do not overload the output; the maximum output of the current converters is 10mA.

11. THERMAL SPECIFICATIONS

11.1. Thermal Analysis for Case Integration

The MSB900/L has a unique thermal design. Heat sources are located on the bottom side of the PCB.

Usually this means the board will be mounted upside down with the CPU thermally in contact with a heat sink. Alternatively, the CPU will be in contact with the system enclosure which then works as a heat sink.

The LX900 CPU is rated with a Total Dissipated Power (TDP) of 3.8W maximum and 1.6W typical @ 600 MHz.

The following picture is a thermal analysis of the bottom side. It was taken after one hour of operating (BIOS screen) at room temperature. There was no heat sink mounted on the CPU.

f_{CPU} [MHz]	U_{in} [V]	T_{CPUmax} [°C]	$T_{CS5536max}$[°C]
600	12		

Pay particular attention when mounting the PC-product in a fully enclosed case/box. The thermal energy will be stored in the interior of this environment.

If the case has a fan:

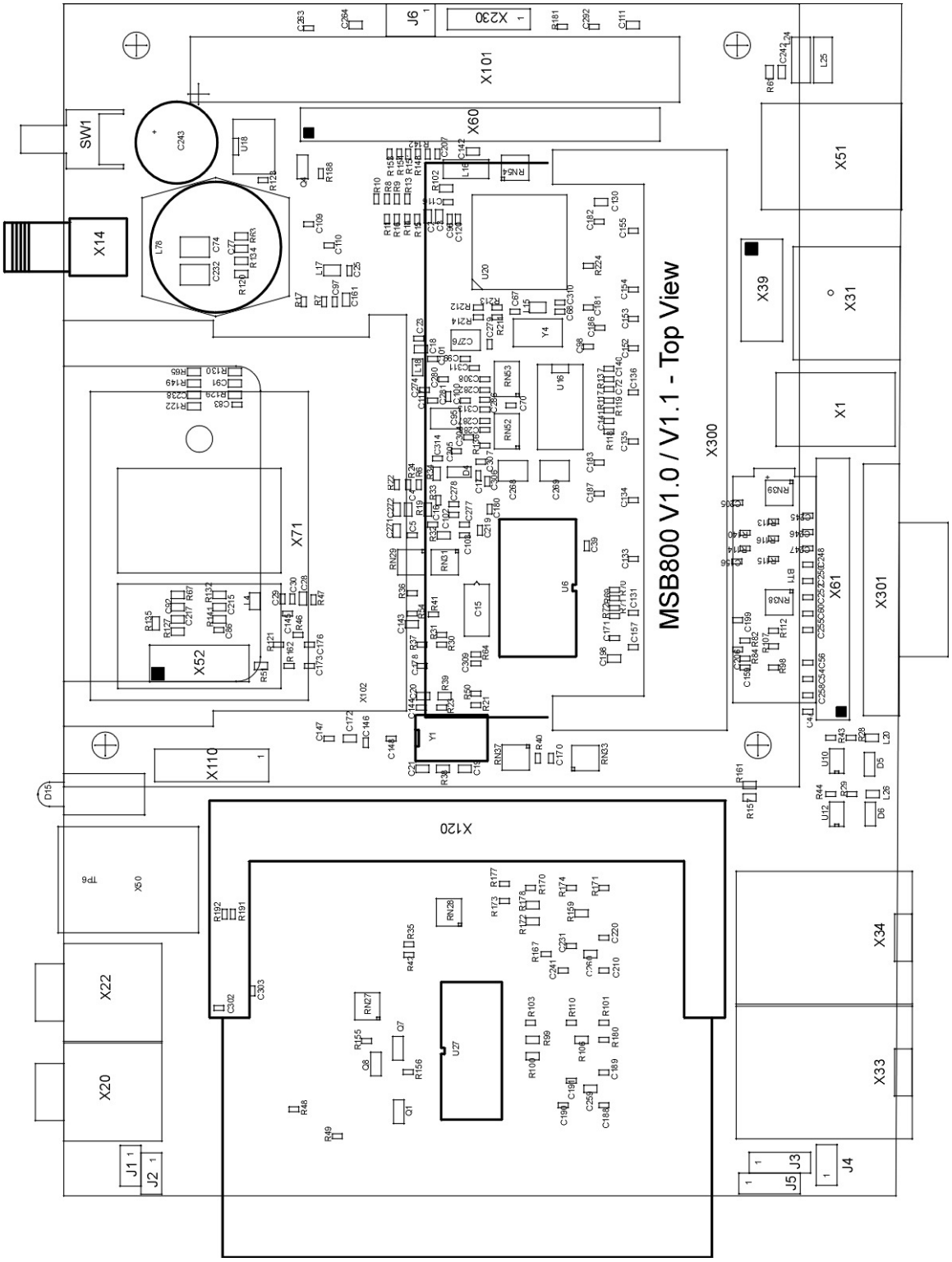
- The hot air must be exchanged with cool air from outside using a filtered fan.
- The hot air must be cooled with a heat exchanger.

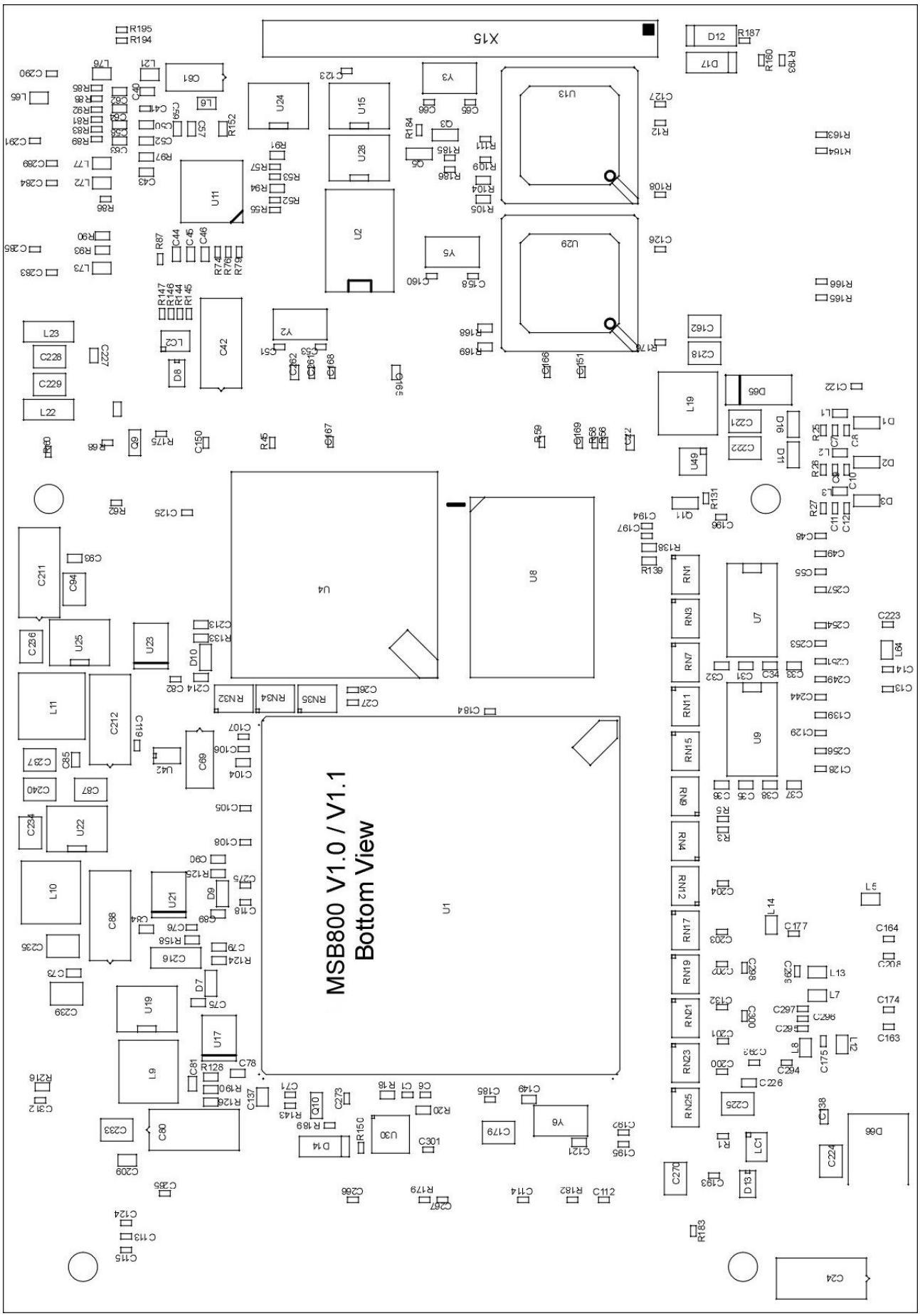
If the case has no fan or opening to exchange hot air:

- The heat sink of the CPU must be mounted directly to a heat sink integrated in the case. The heat will be conducted directly through the alloy of the heat sink to the outside.

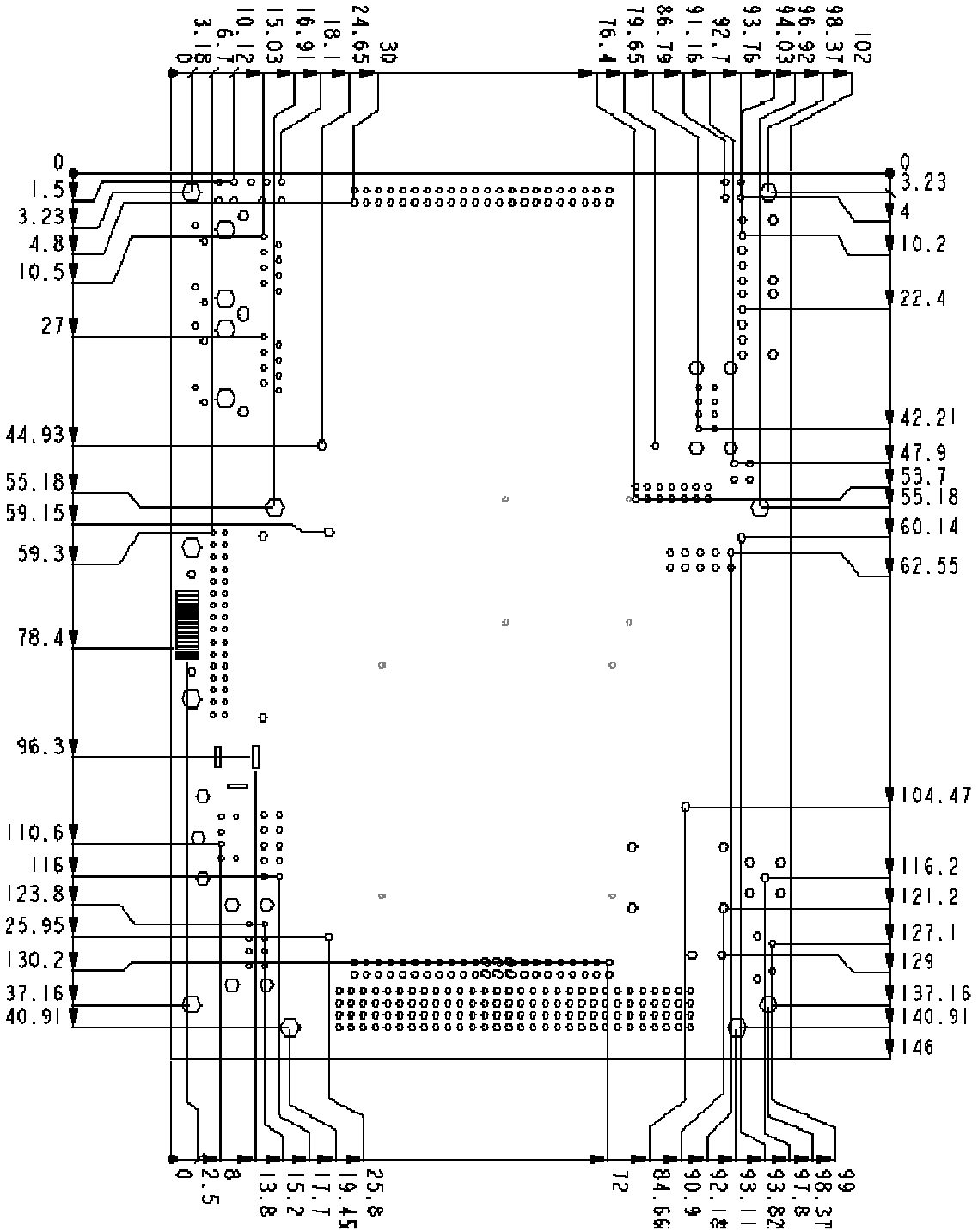
12. ASSEMBLY VIEWS

12.1. MSB900/L




MSB800 V1.0 / V1.1
Bottom View

12.2. Mechanical Dimensions



MSB900 Version

Unit: mm (millimeter)
Tolerance: +/- 0.1mm

Date: 28.03.2006
Author: BRR

13.PXE-BOOT AND PXE-SETUP IN THE BIOS

PXE Protocol
PXE is defined on a foundation of industry-standard Internet protocols and services that are widely deployed in the industry, namely TCP/IP, DHCP, and TFTP. These standardize the *form* of the interactions between clients and servers. To ensure that the *meaning* of the client-server interaction is standardized as well, certain vendor option fields in DHCP protocol are used, which are allowed by the DHCP standard. The operations of standard DHCP and/or BOOTP servers (that serve up IP addresses and/or NBPs) will not be disrupted by the use of the extended protocol. Clients and servers that are aware of these extensions will recognize and use this information, and those that do not recognize the extensions will ignore them.

In brief, the PXE protocol operates as follows. The client initiates the protocol by broadcasting a DHCPDISCOVER containing an extension that identifies the request as coming from a client that implements the PXE protocol. Assuming that a DHCP server or a Proxy DHCP server implementing this extended protocol is available, after several intermediate steps, the server sends the client a list of appropriate Boot Servers. The client then discovers a Boot Server of the type selected and receives the name of an executable file on the chosen Boot Server. The client uses TFTP to download the executable from the Boot Server. Finally, the client initiates execution of the downloaded image. At this point, the client's state must meet certain requirements that provide a predictable execution environment for the image. Important aspects of this environment include the availability of certain areas of the client's main memory, and the availability of basic network I/O services.

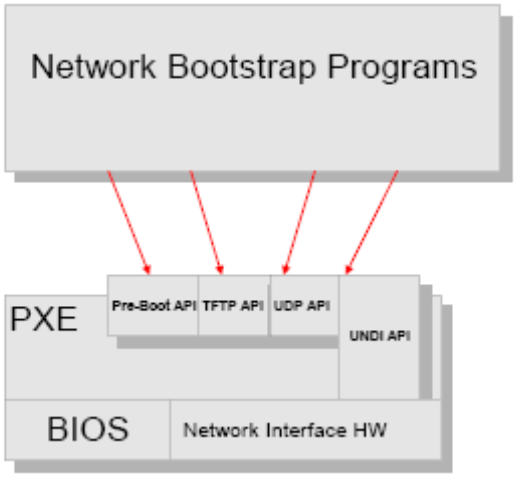
Deployment of servers
On the server end of the client-server interaction there must be available services that are responsible for providing redirection of the client to an appropriate Boot Server. These redirection services may be deployed in two ways:

1. **Combined standard DHCP and redirection services.**
   The DHCP servers that are supplying IP addresses to clients are modified to become, or are replaced by servers that serve up IP addresses for all clients and redirect PXE-enabled clients to Boot Servers as requested.

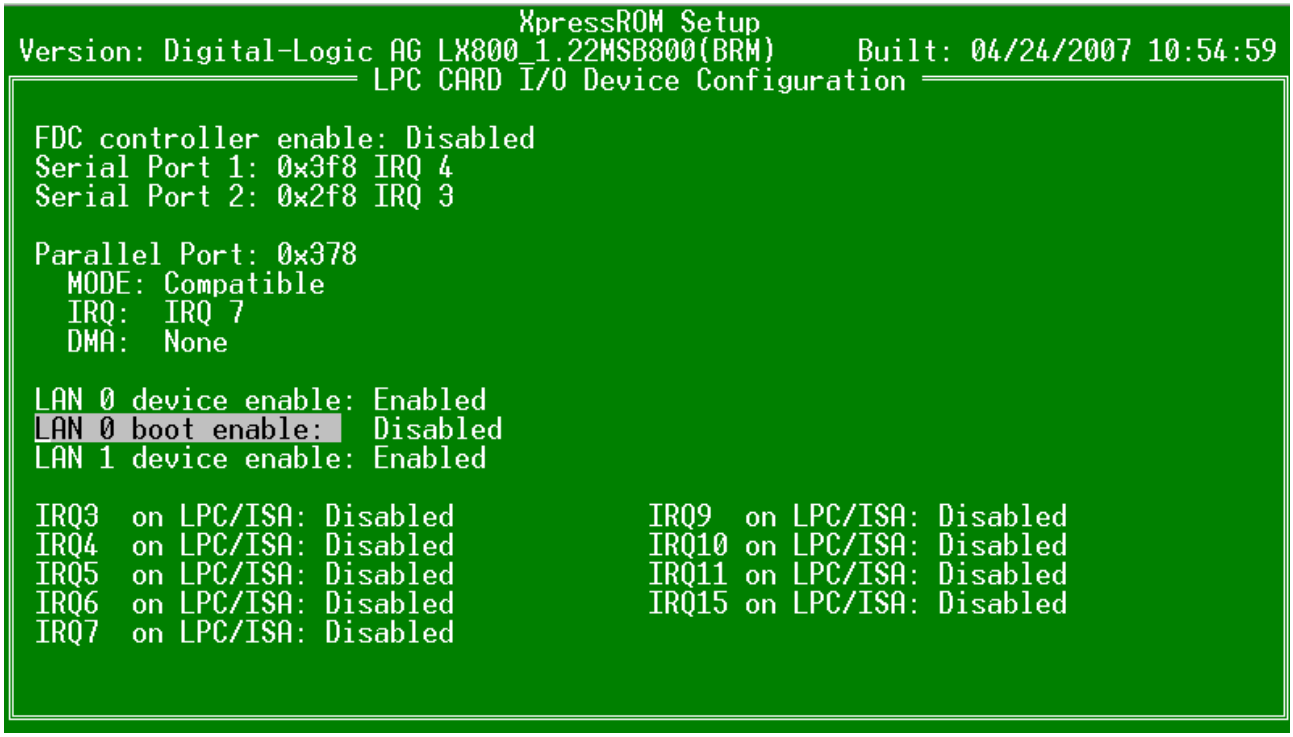
2. **Separate standard DHCP and redirection services.**
   PXE redirection servers (Proxy DHCP servers) are added to the existing network environment. They respond only to PXE-enabled clients, and provide only redirection to Boot Servers. Each PXE Boot Server must have one or more executables appropriate to the clients that it serves.

Preboot Execution Environment (PXE) Specification 11
Version 2.1 September 20, 1999

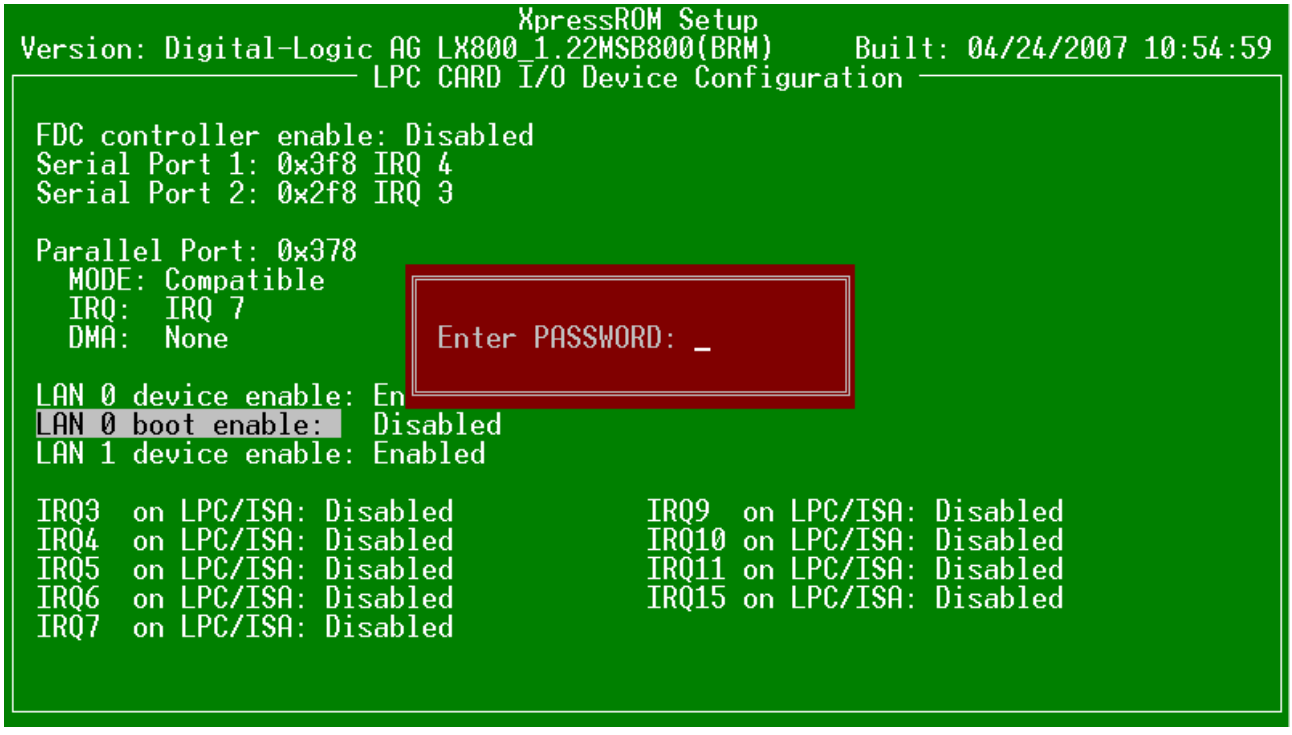
This diagram illustrates the relationship between the NBP (the remote boot program) and the PXE APIs.



BIOS-Setup Screen with the LAN-BOOT (PXE) DISABLE / ENABLE menu:



After ENABLING the LAN-Boot, the Password must be entered.



The Password must be requested with the PXE-licence order form on the following page.

14.PXE-LICENSE ORDER

The PXE-Function ***must be*** licensed before it can be enabled. To order, fill out and sign this form; return to the fax number below. This form may be printed out separately from the digital copy of this manual on the Product CD.

Note... One license per form
Each computer system requires an individual, one-time royalty payment for the PXE-license. After receipt of payment, you will be emailed the password necessary to enable the PXE-Function (see Section 13).

Customer Information:

Company Name: _____

Your Name: _____

Street Address: _____

ZIP / City: _____

Email: _____

Information for the PXE-License:

Product		**Currency (circle one)**
MPC20	☐	USD
		Euro
MPC21/A	☐	CHF

Price per license	23 USD	17 Euro	28 CHF

For each additional license, please fill out another form.

Date: _____ Signature: _____

dd / mm / yyyy

Fax this form to your DIGITAL-LOGIC Sales Manager:

_____
(please write in his/her name)

Fax: +0041 32 681 58 01

15.INDEX