EM78P312N

8-BIT Microcontroller

Green Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial Version	2006/10/03

1 General Description

The EM78P312N is an 8-bit microprocessor with low-power, high-speed CMOS technology and **high noise immunity**. It has an on-chip 4K×13-bits Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides **multi-protection bits** to prevent intrusion of user's OTP memory codes. Seven Option bits are also available to meet user's requirements. With its OTP-ROM feature, the EM78P312N provides a convenient way of developing and verifying user's programs. Moreover, this OTP device offers the advantages of easy and effective program updates, using development and programming tools. User can avail of the ELAN Writer to easily program his development code.

2 Features

- CPU configuration
  - 4K×13 bits on-chip ROM
  - 144×8 bits on-chip registers (SRAM)
  - 8-level stacks for subroutine nesting
  - Less than 3.5mA at 5V/8MHz
  - Typically 0.8 μA, during sleep mode
  - Typically 1.1 μA, during idle mode
- I/O port configuration
  - 4 bidirectional I/O ports : P6, P7, P8, P9
  - 22 I/O pins
  - 10 Programmable pull-down I/O pins
  - 10 programmable pull-high I/O pins
  - External interrupt : P60, P61, P73, P80
- Operating voltage range**:**
  - OTP version

    Operating voltage range:2.5v~5.5v
- Operating temperature range**:**
  - -40~85°C
- Operating frequency range:

  Main clock
  - Crystal mode:

    DC ~ 20MHz/2clks @ 5V; DC ~100ns inst. cycle @ 5V

    DC ~ 8MHz/2clks @ 3V;DC ~ 250ns inst. cycle @ 3V
  - ERC mode:

    DC ~ 16MHz/2clks @ 5V;DC ~ 125ns inst. cycle @ 5V

    DC ~ 8MHz/2clks @ 3V;DC ~ 250ns inst. cycle @ 3V
- Peripheral configuration
  - Serial peripheral interface (SPI) available
  - Universal asynchronous receiver transmitter interface (UART)available
  - 16 bits Counter/Timer

    TC2: Timer/Counter/Window
  - 8 bits Timer/Counter

    TCC: 8-bit real time clock/counter with overflow interrupt

    TC3: Timer/Counter/Capture

    TC4: Timer/Counter/ PWM (pulse width modulation) / PDO (Programmable divider output)
  - 8-bit channels Analog-to-Digital Converter with 10-bit resolution
  - Time Base Timer:(1Hz~16kHz at 8MHz)
  - Key tone output:(1kHz~8kHz at 8MHz)
  - 8-bit channels Analog-to-Digital Converter with 10-bit resolution
- Fifteen available interrupts:
  - WDT time-out interrupt
  - TCC overflow interrupt
  - Time base timer interrupt (the first falling edge of the source clock)
  - Serial UART transmit interrupt
  - Serial UART receive interrupt
  - Serial UART receive error interrupt
  - Four External interrupt
  - ADC completion interrupt
  - TC2 overflow interrupt
  - TC3 overflow interrupt
  - TC4 overflow interrupt
  - Serial SPI interrupt
- Special features
  - Programmable free running watchdog timer
  - Two clocks per instruction cycle
  - Power-on Reset
  - High noise immunity
  - Power saving Sleep mode
  - Selectable Oscillation mode
- Package type:
  - 28-pin DIP 600 mil: EM78P312NP
  - 28-pin Skinny DIP 300 mil: EM78P312NAK
  - 28-pin Skinny DIP 400 mil: EM78P312N
  - 28-pin SOP 300 mil: EM78P312NM
  - 28-pin SSOP 209 mil: EM78P312NS

3 Pin Assignment

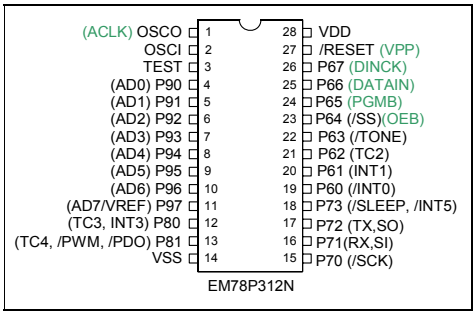


Fig. 3- Pin Assignment

4 Pin Description

Table 1

Symbol	Pin No.	Type	Function
VDD	28	–	Power supply
OSCI	2	I	Crystal type: Crystal input terminal RC type: RC oscillator input pin
OSCO	1	I/O	Crystal type: Output terminal for crystal oscillator RC type: Instruction clock output External clock signal input
/RESET	27	I	Input pin with Schmitt Trigger. If this pin remains at logic low, the controller will also remain in reset condition.
P60~P67	19~26	I/O	8-bit bidiectional input/output pins. P60 can be used as external Interrupt 0 (/INT0). P61 can be used as external Interrupt 1 (INT1). P62 can be used as 16-bit Timer/Counter 2 (TC2). P63 can be used as divider output (/TONE). P64 slave mode enable (/SS). P60 ~ P63 can be used as pull-high or pull-low pins.
P70~P73	15~18	I/O	8-bit bidiectional input/output pins. P70 can be used as SPI serial clock input/output (/SCK) P71 can be used as SPI serial data input (SI) or UART data receive input (RX) P72 can be used as SPI serial data output (SO) or UART data transmit output (TX) P73 can be used as Sleep mode release input (/SLEEP) or external interrupt Input 5 (/INT5) P70 ~ P73 can be used as pull-high or pull-low pins
P80~P81	12~13	I/O	2-bit bidiectional input/output pins. P80 can be used as 8-bit Timer/Counter 3 (TC3) or external Interrupt Input 3 (INT3). P81 can be used as 8-bit Timer/Counter 4 (TC4) or programmable divider output (PDO). P80 ~ P81 can be used as pull-high or pull-low pins.
P90~P97	4~11	I/O	8-bit bidiectional input/output pins. P90~P97 can be used as 8 channel 10-bit resolution A/D converter. P97 can be used as AD reference power supply input (VREF).
VSS	14	–	Ground
NC	3	–	No connection
OTP Programming Pins			
VPP	27	I	Programming voltage input
ACLK	1	I	CLK for OTP memory address increment
DATAIN	25	I/O	ROM code series input and series output pin
DINCK	26	I	ROM code input clock
PGMB	24	I	Program write enable pin. Active low.
OEB	23	I	Output enable pin. Active low.

5 Function Description

5.1 Functional Block Diagram

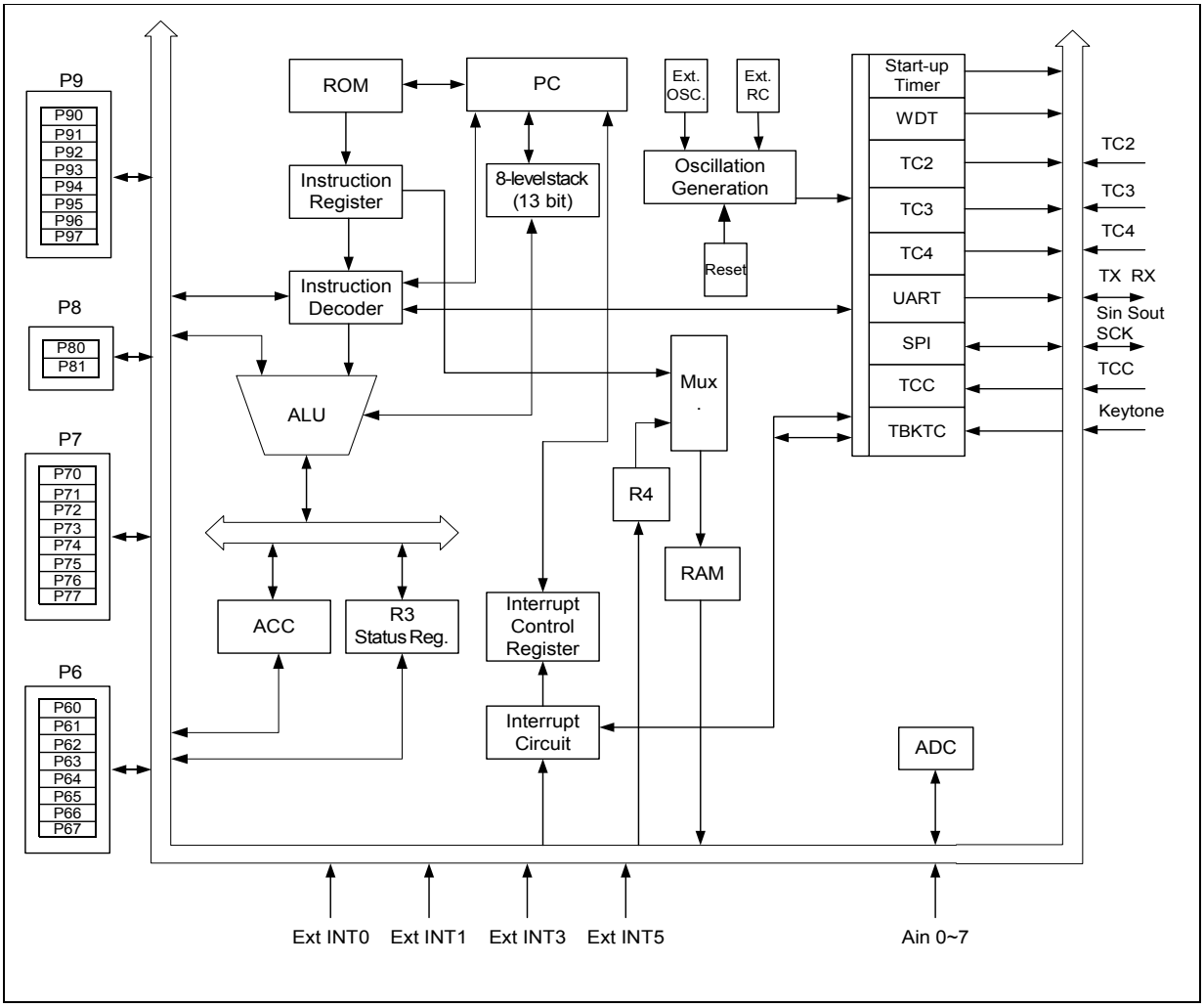


Fig. 5-1 Functional Block Diagram

5.2 Operating Registers

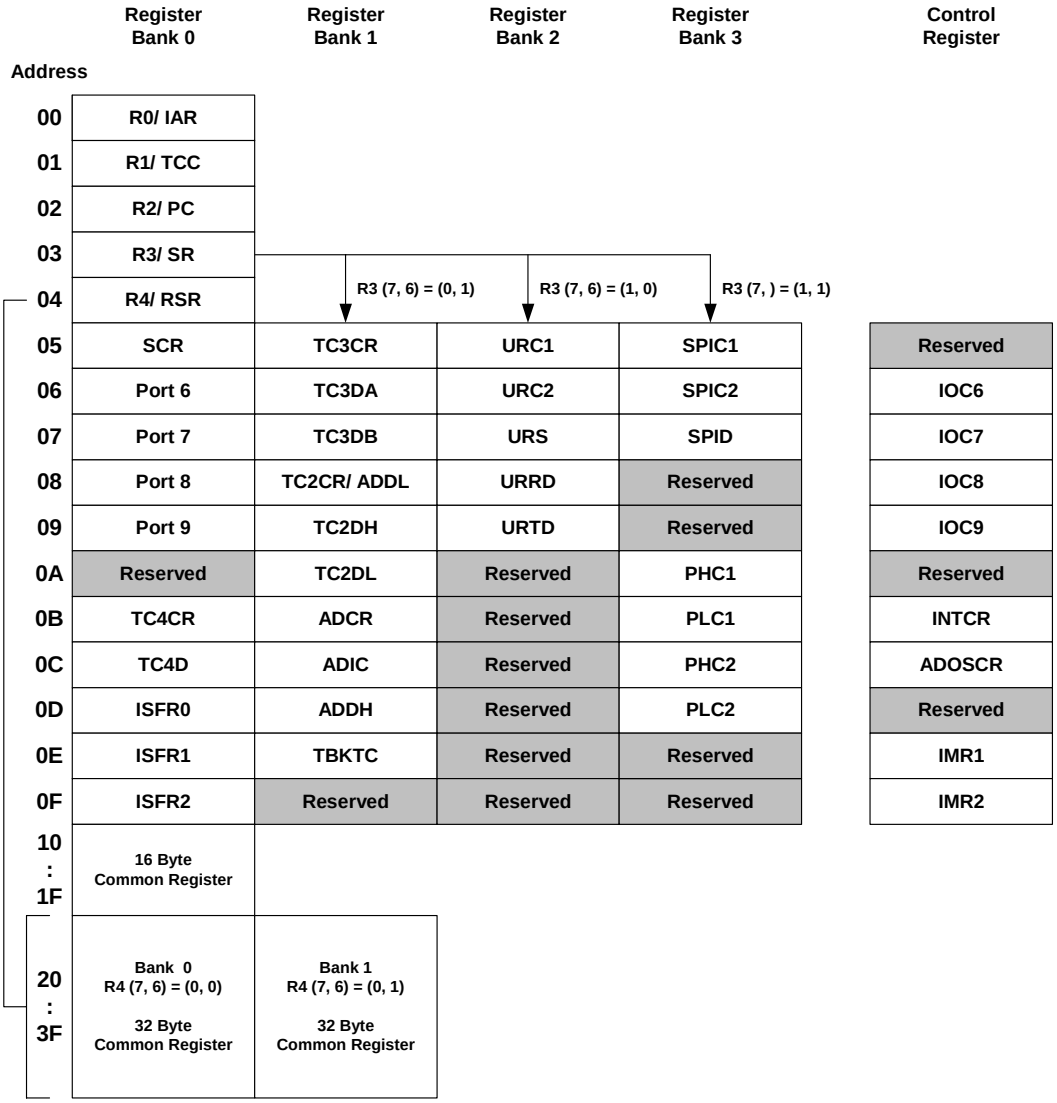


Fig. 5-2 Operating Registers

R0 (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to act as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

R1 (Time Clock /Counter)

This register is writable and readable just like the other registers. The contents of the prescaler counter are cleared only when a value is written into the TCC register.

R2 (Program Counter) & Stack

- Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in Fig.5-3.
- Generates 8192 ×13 bits on-chip OTP ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- R2 is set as all "0"s when under RESET condition
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to go to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- All instructions are single instruction cycle (fclk/2 or fclk/4) except for the instruction that would change the contents of R2. Such instruction will need one more instruction cycle.
- For an interrupt trigger, the program ROM will jump to individual interrupt vector at Page 0. The CPU will store ACC, R3 status and R5 PAGE automatically, it will restore after instruction RETI.

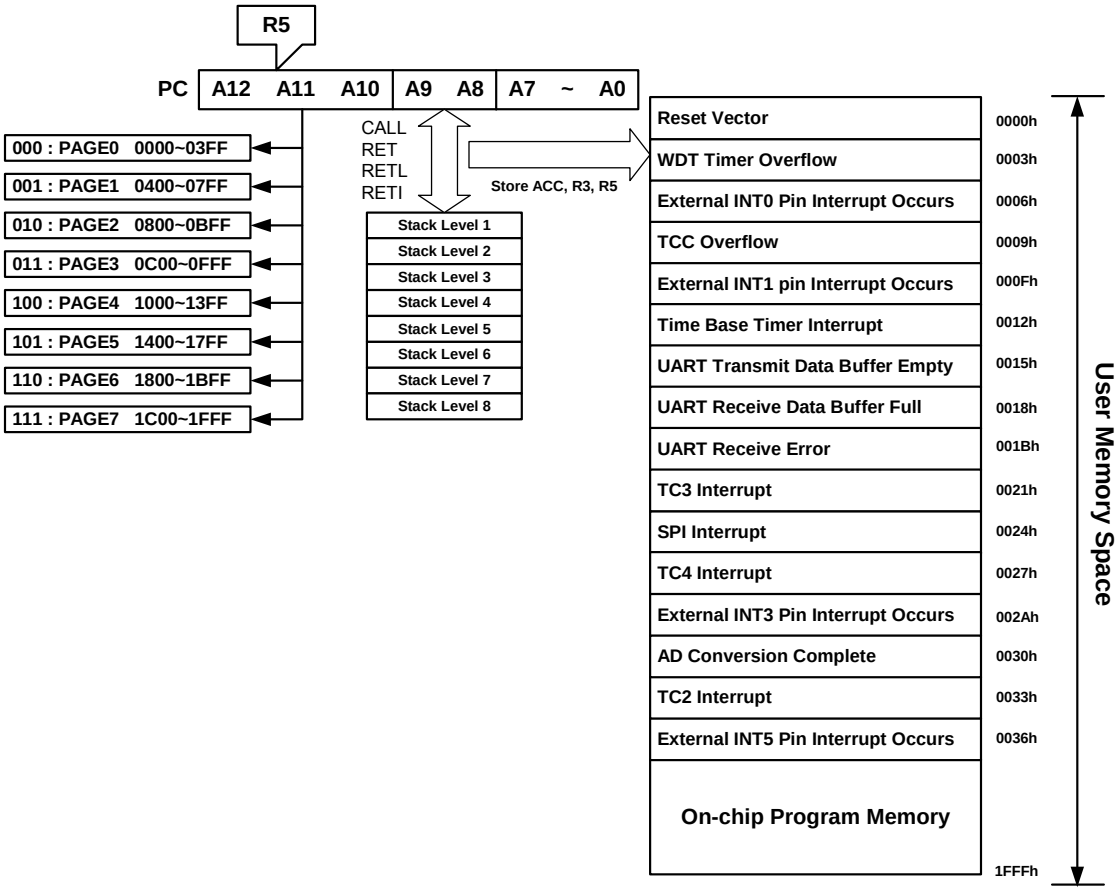


Fig. 5-3 Program Counter Organization

■ R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBS1	RBS0	0	T	P	Z	DC	C

Bit 7 ~ Bit 6 (RBS1 ~ RBS0): R-Register page select

RBS1	RBS0	Register Bank (Address 05H ~ 0FH)
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 3

Bit 5: Not used

Bit 4 (T): Time-out bit. Set to “1” with the "SLEP" and "WDTC" commands, or during power up, and reset to “0” with the WDT time-out.

Bit 3 (P): Power down bit. Set to “1” during power on or by a "WDTC" command and reset to “0” by a "SLEP" command.

Bit 2 (Z): Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC) : Auxiliary carry flag

Bit 0 (C) : Carry flag

■ **R4 (RAM Select Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GRBS1	RBS0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0

Bit 7: 6 (GRBS1: GRBS0): determine which general purpose banks are activated among the two banks. Use BANK instruction (e.g. BABK 1) to change bank.

GRBS1	GRBS0	General Purpose Register Bank (Address 20H ~ 3FH)
0	0	Bank 0
0	1	Bank 1

Bit 5: 0 (RSR5 : RSR0): used to select the registers (Address: 00h~3Fh) in indirect addressing mode. If no indirect addressing is used, the RSR can be used as an 8-bit general-purpose read/write register. See the data memory configuration in Fig. 5-2.

■ **R5 (System Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	PS1	PS0	0	1	SIS	REM

Bits 5~4 (PS1~PS0): ROM Page select bits. User can use PAGE instruction (e.g. PAGE 1) or set PS1~PS0 bits to change the ROM page. When executing a "JMP", "CALL", or other instructions which cause the program counter to change (e.g. MOV R2, A), PS1~PS0 are loaded into the 12th to11th bits of the program counter and select one of the available program memory pages. Note that RET (RETL, RETI) instruction does not change the PS1~PS0 bits. That is, return will always be to the page from where the subroutine was called, regardless of the PS1~PS0 bits current setting.

PS1	PS0	Program Memory Page [Address]
0	0	Page 0 [0000~03FF]
0	1	Page 1 [0400~07FF]
1	0	Page 2 [0800~0BFF]
1	1	Page 3 [0C00~0FFF]

Bit 1 (SIS) : Sleep and Idle mode select

SIS = “0” : Idle mode

SIS = “1” : Sleep mode

Bit 0 (REM) : Release method for sleep mode

REM = “0” : /SLEEP pin input rising edge released

REM = “1” : /SLEEP pin input “H” level released

■ **R6 (Port 6 I/O Data Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	P63	P62	P61	P60

Bit 7 ~ Bit 0 (P67 ~ P60) : 8-bit Port 6 I/O data register

User can use IOC6 register to define each bit whether input or output.

■ **R7 (Port 7 I/O Data Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	P73	P72	P71	P70

Bit 3 ~ Bit 0 (P73 ~ P70) : Port 73 ~ Port 70 I/O data register

User can use IOC7 register to define each bit whether input or output.

■ **R8 (Port8 I/O Data Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	P81	P80

Bit 1 ~ Bit 0 (P81 ~ P80) : Port 81 ~ Port 80 I/O data register

User can use IOC8 register to define each bit whether input or output.

■ **R9 (Port9 I/O Data Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P97	P96	P95	P94	P93	P92	P91	P90

Bit 7 ~ Bit 0 (P97 ~ P90) : 8-bit Port 97 ~ Port 90 I/O data register

User can use IOC9 register to define each bit whether input or output.

■ **RB (Timer/Counter 4 Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC4FF1	TC4FF0	TC4S	TC4CK2	TC4CK1	TC4CK0	TC4M1	TC4M0

Bit 7 ~ Bit 6 (TC4FF1 ~ TC4FF0) : Timer/Counter 4 flip-flop control

TC4FF1	TC4FF0	Operating Mode
0	0	Clear
0	1	Toggle
1	0	Set
1	1	Reserved

Bit 5 (TC4S) : Timer/Counter 4 start control

TC4S = "0" : Stop and clear counter

TC4S = "1" : Start

Bit 4 ~ Bit 2 (TC4CK2 ~ TC4CK 0) : Timer/Counter 4 Clock Source Select

TC4CK2	TC4CK1	TC4CK0	Clock Source (Normal, Idle)	Resolution (Fosc=8M)	Max. Time (Fosc=8M)
0	0	0	$Fc/2^{11}$	256μS	65mS
0	0	1	$Fc/2^{7}$	16μS	4mS
0	1	0	$Fc/2^{5}$	4μS	1mS
0	1	1	$Fc/2^{3}$	1μS	255μS
1	0	0	$Fc/2^{2}$	500nS	127.5μS
1	0	1	$Fc/2^{1}$	250nS	63.8μS
1	1	0	Fc	125nS	31.9μS
1	1	1	External clock (TC4 pin)	–	–

Bit 1 ~ Bit 0 (TC4M1 ~ TC4M0) : Timer/Counter 4 Operating Mode Select

TC4M1	TC4M0	Operating Mode
0	0	Timer/Counter
0	1	Reserved
1	0	Programmable Divider output
1	1	Pulse Width Modulation output

- **RC (Timer 4 Data Buffer)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC4D7	TC4D6	TC4D5	TC4D4	TC4D3	TC4D2	TC4D1	TC4D0

Bit 7 ~ Bit 0 (TC4D7 ~ TC4D0) : Data buffer of 8-bit Timer/Counter 4.

- **RD (Interrupt Status Flag Register 0 and INT3 Edge Detect Flag)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	INT3F	INT3R	0	0	WDTIF	EXIF0

Bit 5 (INT3F) : External Interrupt 3 falling edge detect flag.

INT3F = "0" : Falling edge is not detected

INT3F = "1" : Falling edge is detected

Bit 4 (INT3R) : External Interrupt 3 rising edge detect flag.

INT3R = "0" : Rising edge is not detected

INT3R = "1" : Rising edge is detected

Bit 1 (WDTIF) : WDT time-out flag, flag cleared by software.

Bit 0 (EXIF0) : External interrupt flag (INT0). Flag cleared by software. If the INT0EN is reset to "0", the flag is cleared.

■ **RE (Interrupt Status Flag Register 1)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXIF5	TCIF2	ADIF	0	EXIF3	TCIF4	SPIF	TCIF3

Bit 7 (EXIF5) : External Interrupt Flag (/INT5), flag cleared by software.

Bit 6 (TCIF2) : 16-bit Timer/Counter 2 Interrupt Flag, flag cleared by software.

Bit 5 (ADIF) : AD conversion complete flag, flag cleared by software.

Bit 3 (EXIF3) : External Interrupt Flag (/INT3), flag cleared by software.

Bit 2 (TCIF4) : 8-bit Timer/Counter 4 Interrupt Flag, flag cleared by software.

Bit 1 (SPIF) : SPI Mode Interrupt Flag, flag cleared by software.

Bit 0 (TCIF3) : 8-bit Timer/Counter 3 interrupt flag, flag cleared by software.

0 : means no interrupt request

1 : means with interrupt request

- ISFR1 can be cleared by instruction, but cannot be set by instruction
- IMR1 is the interrupt mask register
- Note that reading ISFR1 will obtain the result of the ISFR1 "logic AND" and IMR1.

■ **RF(Interrupt Status Flag Register 2)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	UERRIF	RBFF	TBEF	TBIF	EXIF1	0	TCIF0

Bit 6 (UERRIF) : UART Receiving Error Interrupt, cleared by software or UART disabled.

Bit 5 (RBFF) : UART Receive Mode Data Buffer Full Interrupt Flag. Flag cleared by software.

Bit 4 (TBEF) : UART Transmit Mode Data Buffer Empty Interrupt Flag. Flag cleared by software.

Bit 3 (TBIF) : Time Base Timer Interrupt Flag. Flag cleared by software.

Bit 2 (EXIF1) : External Interrupt Flag (INT1). Flag cleared by software.

Bit 0 (TCIF0) : TCC Overflow Interrupt Flag. Set as TCC overflows; flag cleared by software.

0 : means no interrupt request

1 : means with interrupt request

- ISFR2 can be cleared by instruction, but cannot be set by instruction
- IMR2 is the interrupt mask register
- Note that reading ISFR2 will obtain the result of the ISFR2 "logic AND" and IMR2

■ **Bank 1 R5 TC3CR (Timer/Counter 3 Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3CAP	TC3S	TC3CK1	TC3CK0	TC3M	0	0	0

Bit 7 (TC3CAP) : Software capture control

TC3CAP = "0" : -

TC3CAP = "1" : Software capture

Bit 6 (TC3S) : Timer/Counter 3 start control

TC3S = "0" : Stop and counter clear

TC3S = "1" : Start

Bit 5 ~ Bit 4 (TC3CK1 ~ TC3CK0) : Timer/Counter 3 Clock Source Select

TC3CK1	TC3CK0	Clock source (Normal, Idle)	Resolution (Fc=8M)	Max. time (Fc=8M)
0	0	$Fc/2^{12}$	512μS	131.1mS
0	1	$Fc/2^{10}$	128μS	32.6mS
1	0	$Fc/2^{7}$	16μS	4.1mS
1	1	External clock (TC3 pin)	-	-

Bit 3 (TC3M) : Timer/Counter 3 mode select

TC3M = "0" : Timer/Counter3 mode

TC3M = "1" : Capture mode

■ **Bank 1 R6 TC3DA (Timer 3 Data Buffer A)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3DA7	TC3DA6	TC3DA5	TC3DA4	TC3DA3	TC3DA2	TC3DA1	TC3DA0

Bit 7 ~ Bit 0 (TC3DA7 ~ TC3DA0) : Data buffer of 8-bit Timer/Counter 3.

Reset does not affect this register.

■ **Bank 1 R7 TC3DB (Timer 3 Data Buffer B)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3DB7	TC3DB6	TC3DB5	TC3DB4	TC3DB3	TC3DB2	TC3DB1	TC3DB0

Bit 7 ~ Bit 0 (TC3DB7 ~ TC3DB0) : Data buffer of 8-bit Timer/Counter 3

Reset does not affect this register.

■ **Bank 1 R8 TC2CR/ ADDL (Timer/Counter 2 Control Register, AD Low 2 bits Data Buffer)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADD1	ADD0	0	TC2M	TC2S	TC2CK2	TC2CK1	TC2CK0

Bit 7 ~ Bit 6 (ADD1 ~ ADD0) : AD low 2-bit data buffer

Bit 4 (TC2M) : Timer/Counter 2 mode select

TC2M = "0" : Timer/counter mode

TC2M = "1" : Window mode

Bit 3 (TC2S) : Timer/Counter 2 start control

TC2S = "0" : Stop and counter clear

TC2S = "1" : Start

Bit 2 ~ Bit 0 (TC2CK2 ~ TC2CK0) : Timer/Counter 2 Clock Source Select

TC2CK2	TC2CK1	TC2CK0	Clock Source (Normal, Idle)	Resolution (Fc=8M)	Max. Time (Fc=8M)
0	0	0	$Fc/2^{23}$	1.05s	19.1h
0	0	1	$Fc/2^{13}$	1.02ms	1.1min
0	1	0	$Fc/2^{8}$	32μs	2.1s
0	1	1	$Fc/2^{3}$	1μs	65.5ms
1	0	0	Fc	125ns	7.9ms
1	0	1	-	-	-
1	1	0	-	-	-
1	1	1	External clock (TC2 pin)		

■ **Bank 1 R9 TC2DH (Timer 2 Data Buffer High Byte)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC2D15	TC2D14	TC2D13	TC2D12	TC2D11	TC2D10	TC2D9	TC2D8

Bit 7 ~ Bit 0 (TC2D15 ~ TC2D8) : 16-bit Timer/Counter 2 data buffer high byte.

■ **Bank 1 RA TC2DL (Timer 2 Data Buffer Low Byte)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC2D7	TC2D6	TC2D5	TC2D4	TC2D3	TC2D2	TC2D1	TC2D0

Bit 7 ~ Bit 0 (TC2D7 ~ TC2D0) : 16-bit Timer/Counter 2 data buffer low byte.

■ **Bank 1 RB ADCR (AD Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADREF	ADRUN	ADCK1	ADCK0	ADP	ADIS2	ADIS1	ADIS0

Bit 7 (ADREF) : AD reference voltage input select.

ADREF = "0" : Internal VDD, P97 is used as IO.

ADREF = "1" : External reference pin, P97 is used as reference input pin.

Bit 6 (ADRUN) : AD Conversion start

ADRUN = "0" : Reset on completion of the conversion by hardware, this bit cannot be reset by software.

ADRUN = "1" : Conversion starts

Bit 5~ Bit 4 (ADCK1 ~ ADCK0) : AD Conversion Time Select

ADCK1	ADCK0	Clock Source (Normal, Idle)	Max. Operating Frequency (Fc)
0	0	Fc/4	1MHz
0	1	Fc/16	4MHz
1	0	Fc/32	8MHz
1	1	Reserved	-

Bit 3 (ADP) : AD power control

ADP = "0" : Power on

ADP = "1" : Power down

Bit 2 ~ Bit 0 (ADIS2 ~ ADIS0) : Analog Input Pin Select

ADIS2	ADIS1	ADIS0	Analog Input Pin
0	0	0	AD0
0	0	1	AD1
0	1	0	AD2
0	1	1	AD3
1	0	0	AD4
1	0	1	AD5
1	1	0	AD6
1	1	1	AD7

■ **Bank 1 RC ADIC (AD Input Pin Control)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0

Bit 7 ~ Bit 0 (ADE7 ~ ADE0) : AD input pin enable control.

ADEx = "0" : Port 9.x functions as I/O pin

ADEx = "1" : Port 9.x functions as analog input pin

■ **Bank 1 RD ADDH (AD High 8-bit Data Buffer)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADD9	ADD8	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2

Bit 7 ~ Bit 0 (ADD9 ~ ADD2) : AD high 8-bit data buffer

■ **Bank 1 RE TBKTC (TBT/Keytone Control)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TEN	TCK1	TCK0	0	TBTEN	TBTCK2	TBTCK1	TBTCK0

Bit 7 (TEN) : Keytone enable control

TEN = "0" : Disable

TEN = "1" : Enable

Bit 6 ~ Bit 5 (TCK1 ~ TCK0) : Keytone Output Clock Source Select

TCK1	TCK0	Clock Source (Normal, Idle)	Keytone Output Frequency (Fc = 8MHz)
0	0	$Fc/2^{13}$	0.976kHz
0	1	$Fc/2^{12}$	1.953kHz
1	0	$Fc/2^{11}$	3.906kHz
1	1	$Fc/2^{10}$	7.812kHz

Bit 3 (TBTEN) : Time Base Timer Enable Control

TBTEN = "0" : Disable

TBTEN = "1" : Enable

Bit 2 ~ Bit 0 (TBTCK2 ~ TBTCK0) : Time Base Timer Clock Source Select

TBTCK2	TBTCK1	TBTCK0	Clock Source (Normal, Idle)	Interrupt Frequency (Fc = 8MHz)
0	0	0	$Fc/2^{23}$	0.95Hz
0	0	1	$Fc/2^{21}$	3.81Hz
0	1	0	$Fc/2^{16}$	122.07Hz
0	1	1	$Fc/2^{14}$	488.28Hz
1	0	0	$Fc/2^{13}$	976.56Hz
1	0	1	$Fc/2^{12}$	1953.12Hz
1	1	0	$Fc/2^{11}$	3906.25Hz
1	1	1	$Fc/2^{9}$	15625Hz

■ **Bank 2 R5 URC1 (UART Control Register 1)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD8	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE

Bit 7 (URTD8) : Transmission data Bit 8

Bit 6 ~ Bit 5 (UMODE1 ~ UMODE0) : UART Transmission Mode Select Bit

UMODE1	UMODE0	UART Mode
0	0	Mode 1: 7-bits
0	1	Mode 2: 8-bits
1	0	Mode 3: 9-bits
1	1	Reserved

Bit 4 ~ Bit 2 (BRATE2 ~ BRATE1) : Transmit Baud Rate Select

BRATE2	BRATE1	BRATE0	Baud Rate	e.g. Fc=8MHz
0	0	0	Fc/13	38400
0	0	1	Fc/26	19200
0	1	0	Fc/52	9600
0	1	1	Fc/104	4800
1	0	0	Fc/208	2400
1	0	1	Fc/416	1200
1	1	0	TC4	-
1	1	1	reserved	-

Bit 1 (UTBE): UART transfer buffer empty flag. Set to 1 when transfer buffer is empty. Reset to 0 automatically when writing into the URTD register. UTBE bit will be cleared by hardware when enabling the transmission. UTBE bit is read-only. Therefore, writing to the URTD register is necessary when starting transmission shifting.

Bit 0 (TXE): Enable transmission

TXE = "0" : Disable

TXE = "1" : Enable

■ **Bank 2 R6 URC2 (UART Control Register 2)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	SBIM1	SBIM0	UINVEN	0	0	0

Bit 5 ~ Bit 4 (SBIM1 ~ SBIM0) : Serial bus interface operation mode select.

TC2CK1	TC2CK0	Operation Mode
0	0	I/O mode
0	1	SPI mode
1	0	UART mode
1	1	Reserved

Bit 3 (UINVEN) : Enable UART TXD and RXD port inverse output.

UINVEN = "0" : Disable TXD and RXD port inverse output.

UINVEN = "1" : Enable TXD and RXD port inverse output.

■ **Bank 2 R7 URS (UART Status Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE

Bit 7 (URRD8) : Receiving data Bit 8

Bit 6 (EVEN) : Select parity check

EVEN = "0" : Odd parity

EVEN = "1" : Even parity

Bit 5 (PRE) : Enable parity addition

PRE = "0" : Disable

PRE = "1" : Enable

Bit 4 (PRERR) : Parity error flag.

Set to 1 when parity error occurred, and cleared to 0 by software.

Bit 3 (OVERR) : Overrun error flag.

Set to 1 when overrun error occurred, and cleared to 0 by software.

Bit 2 (FMERR) : Framing error flag.

Set to 1 when framing error occurred, and cleared to 0 by software.

Bit 1 (URBF) : UART read buffer full flag.

Set to 1 when one character is received. Reset to 0 automatically when read from the URS register. URBF will be cleared by hardware when receiving is enabled. URBF bit is read-only. Therefore, reading the URS register is necessary to avoid an overrun error.

Bit 0 (RXE) : Enable receiving

RXE = "0" : Disable

RXE = "1" : Enable

■ **Bank 2 R8 URRD (UART Receive Data Buffer)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0

Bit 7 ~ Bit 0 (URRD7 ~ URRD0) : UART receive data buffer. Read only.

■ **Bank 2 R9 URTD (UART Transmit Data Buffer)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URTD 7	URTD 6	URTD 5	URTD 4	URTD 3	URTD 2	URTD 1	URTD0

Bit 7 ~ Bit 0 (URTD 7 ~ URTD 0) : UART transmit data buffer. Write only.

■ **Bank 3 R5 SPIC1 (SPI Control Register 1)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SMP	DCOL	BRS2	BRS1	BRS0	EDS	DORD	WBE

Bit 7 (SMP) : SPI data input sample phase.

SMP = "0" : Input data sampled at middle of data output time

SMP = "1" : Input data sampled at the end of data output time

In using the external clock, data input sample is fixed at the middle of data output time.

Bit 6 (DCOL) : SPI Data collision.

DCOL = "0" : No occurrence of Data collision

DCOL = "1" : Data collision occurred. It should be cleared by software.

Bit 5 ~ Bit 3 (BRS0 ~ BRS2) : SPI Clock Source Select

BRS2	BRS1	BRS0	Clock Source (Normal, Idle)	Max. Transfer Rate (Fc = 8MHz)
0	0	0	$Fc/2^{13}$	0.95Kbit/s
0	0	1	$Fc/2^{11}$	3.8Kbit/s
0	1	0	$Fc/2^{10}$	7.6Kbit/s
0	1	1	$Fc/2^{8}$	30.5Kbit/s
1	0	0	$Fc/2^{6}$	122Kbit/s
1	0	1	$Fc/2^{5}$	244Kbit/s
1	1	0	External clock (/SCK pin)	Enable /ss pin
1	1	1	External clock (/SCK pin)	Disable /ss pin

Bit 2 (EDS) : Data shift out edge select.

EDS = "0" : Rising edge

EDS = "1" : Falling edge

Bit 1 (DORD) : Data transmission order.

DORD = "0" : Shift left (MSB first)

DORD = "1" : Shift right (LSB first)

Bit 0 (WBE) : Write buffer empty flag. Read only.

WBE = "0" : Write buffer empty

WBE = "1" : Not empty, set to "1" automatically when writing data to the data buffer.

■ **Bank 3 R6 SPIC2 (SPI Control Register 2)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPIS	0	0	0	0	SPIM1	SPIM0	RBF

Bit 7 (SPIS) : SPI start shift, set the bit to "1" and shift register starts to shift. It is cleared by hardware when shifting is finished. In transferring the next data, it must be set to "1" again.

SPIS = "0" : Finish shifting

SPIS = "1" : Start shifting

Bit 2 ~ Bit 1 (SPIM1 ~ SPIM0) : SPI Transfer Mode Select

TC2CK1	TC2CK0	Transfer Mode
0	0	8-bit Transmit/Receive mode
0	1	8-bit Transmit mode
1	0	8-bit Receive mode
1	1	Reserved

Bit 0 (RBF) : Set to 1 by Buffer Full Detector, and cleared to 0 automatically when reading data from the SPID register. RBF bit will be cleared by hardware when enabling SPI. And RBF bit is read-only. Therefore, reading the SPRL register is necessary to avoid data collision to occur (DCOL).

■ **Bank 3 R7 SPID (SPI Data Buffer)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPID7	SPID6	SPID5	SPID4	SPID3	SPID2	SPID1	SPID0

Bit 7 ~ Bit 0 (SPID7 ~ SPID0) : SPI data buffer.

■ **Bank 3 RA PHC1 (Pull High Control Register 1)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	/PHE81	/PHE80	/PHE63	/PHE62	/PHE61	/PHE60

Bit 5 ~ 4 (/PHE81 ~ /PHE80) : bits 1, 0 of Port 8 Pull high enable bit

/PHE8x = "0" : Enable P8x pull high

/PHE8x = "1" : Disable P8x pull high

Bit 3 ~ 0 (/PHE63 ~ /PHE60) : Bits 3 ~ 0 of Port 6 Pull high enable bit

/PHE6x = "0" : Enable P6x pull high

/PHE6x = "1" : Disable P6x pull high

■ **Bank 3 RB PLC1 (Pull Low Control Register 1)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	/PLE81	/PLE80	/PLE63	/PLE62	/PLE61	/PLE60

Bit 5 ~ 4 (/PLE81 ~ /PLE80) : Bits 1, 0 of Port 8 Pull low enable bit

/PLE8x = "0" : Enable P8x pull low

/PLE8x = "1" : Disable P8x pull low

Bit 3 ~ 0 (/PLE63 ~ /PLE60) : Bits 3 ~ 0 of Port 6 Pull low enable bit

/PLE6x = "0" : Enable P6x pull low

/PLE6x = "1" : Disable P6x pull low

■ **Bank 3 RC PHC2 (Pull High Control Register 2)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	/PHE73	/PHE72	/PHE71	/PHE70

Bit 3 ~ 0 (/PHE73 ~ /PHE70) : Bits 3 ~ 0 of Port 7 Pull high enable bit

/PHE7x = "0" : Enable P7x pull high

/PHE7x = "1" : Disable P7x pull high

■ **Bank 3 RD PLC2 (Pull Low Control Register 2)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	/PLE73	/PLE72	/PLE71	/PLE70

Bit 3 ~ 0 (/PLE73 ~ /PLE70) : Bits 3 ~ 0 of Port 7 Pull low enable bit

/PLE7x = "0" : Enable P7x pull low

/PLE7x = "1" : Disable P7x pull low

■ **R10~R1F and R20~R3F (including Banks 0~3) are General Purpose Register**

5.3 Special Purpose Registers

A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator. It is not an addressable register.

■ **CONT (Control Register)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTO	/INT	WDTP1	WDTP0	WDTE	PSR2	PSR1	PSR0

The CONT register is both readable and writable.

Bit 7 (WDTO) : WDT output select

WDTO = "0" : Interrupt request

WDTO = "1" : Internal reset

Bit 6 (/INT) : Interrupt enable flag

/INT = "0" : masked by DISI or hardware interrupt

/INT = "1" : enabled by ENI/RETI instructions

Bit 5 ~ Bit 4 (WDTP1 ~ WDTP0): WDT prescaler bits

WDTP1	WDTP0	Operating Mode
0	0	1:4
0	1	1:16
1	0	1:64
1	1	1:256

Bit 3 (WDTE) : WDT enable control.

WDTE = "0" : Disable

WDTE = "1" : Enable

Bit 2 (PSR2) ~ Bit 0 (PSR0) : TCC prescaler bits

PSR2	PSR1	PSR0	Operating Mode
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

- **IOC6 ~ IOC9 – I/O Port Control Register**
  - "1" puts the relative I/O pin into high impedance, while "0" defines the relative I/O pin as output.
  - IOC6 and IOC9 registers are both readable and writable.

- **INTCR – INT Control Register (Address : 0Bh)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT1NR	INT0EN	0	INT3ES1	INT3ES0	0	INT1ES	TC2ES

Bit 7 (INT1NR) : INT1 noise reject time select

INT1NR = "0" : Pulses less than 63/fc are eliminated as noise

INT1NR = "1" : Pulses less than 15/fc are eliminated as noise

Bit 6 (INT0EN) : INT0 enable control

INT0EN = "0" : General I/O

INT0EN = "1" : /INT0 pin

Bit 5 : Reserved

Bit 4 ~ Bit 3 (INT3ES1 ~ INT3ES0) : INT3 edge select

INT3ES1	INT3ES0	Edge Select
0	0	Rising
0	1	Falling
1	0	Both edge
1	1	Reserved

Bit 2: Reserved

Bit 1 (INT1ES) : INT1 edge select

INT1ES = "0" : Rising edge

INT1ES = "1" : Falling edge

Bit 0 (TC2ES) : Timer/Counter 2 edge select.

TC2ES = "0" : Rising edge

TC2ES = "1" : Falling edge

External Interrupt

INT Pin	Secondary Function Pin	Enable Condition	Edge	Digital Noise Reject
/INT0	P60	ENI + INT0EN (IOCB)	Falling	-
INT1	P61	ENI + EXIE1 (IMR2)	Rising or Falling	15/Fc, 63/Fc
INT3	P80, TC3	ENI + EXIE3 (IMR2)	Rising or Falling or Rising/Falling	7/Fc
/INT5	P73, /SLEEP	ENI + EXIE5 (IMR2)	-	-

■ **ADOSCR – AD Offset Control Register (Address : 0Ch)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	0	0	0

Bit 7 (CALI) : Calibration enable bit for A/D offset

CALI = "0" : disable Calibration

CALI = "1" : enable Calibration

Bit 6 (SIGN) : Offset voltage Polarity bit

SIGN = "0" : Negative voltage

SIGN = "1" : Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]) : Offset voltage bits

■ **IMR1 – Interrupt Mask Register 1 (Address : 0Eh)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXIE5	TCIE2	ADIE	0	EXIE3	TCIE4	SPIE	TCIE3

Bit 7 (EXIE5) : External/INT5 pin Interrupt enable bit.

EXIE5 = "0" : disable EXIF5 interrupt

EXIE5 = "1" : enable EXIF5 interrupt

Bit 6 (TCIE2) : Timer/Counter 2 Interrupt enable bit.

TCIE2 = "0" : disable TCIF2 interrupt

TCIE2 = "1" : enable TCIF2 interrupt

Bit 5 (ADIE) : ADC complete interrupt enable bit.

ADIE = "0" : disable ADIF interrupt

ADIE = "1" : enable ADIF interrupt

Bit 3 (EXIE3) : External INT3 pin Interrupt enable bit.

EXIE3 = "0" : disable EXIF3 interrupt

EXIE3 = "1" : enable EXIF3 interrupt

Bit 2 (TCIE4) : Timer/Counter 4 Interrupt enable bit.

TCIE4 = "0" : disable TCIF4 interrupt

TCIE4 = "1" : enable TCIF4 interrupt

Bit 1 (SPIE) : SPI Interrupt enable bit.

SPIE = "0" : disable SPIF interrupt

SPIE = "1" : enable SPIF interrupt

Bit 0 (TCIE3) : Timer/Counter 3 Interrupt enable bit.

TCIE3 = "0" : disable TCIF3 interrupt

TCIE3 = "1" : enable TCIF3 interrupt

Individual interrupt is enabled by setting its associated control bit in the IMR1 to "1".

Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction.

The IMR1 register is both readable and writable.

■ **IMR2 – Interrupt Mask Register 2(Address: 0Fh)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	UERRIE	URIE	UTIE	TBIE	EXIE1	0	TCIE0

Bit 6 (UERRIE) : UART receive error interrupt enable bit.

UERRIE = "0" : disable UERRIF interrupt

UERRIE = "1" : enable UERRIF interrupt

Bit 5 (URIE) : UART receive mode interrupt enable bit.

URIE = "0" : disable RBFF interrupt

URIE = "1" : enable RBFF interrupt

Bit 4 (UTIE) : UART transmit mode interrupt enable bit.

UTIE = "0" : disable TBEF interrupt

UTIE = "1" : enable TBEF interrupt

Bit 3 (TBIE) : Time base timer interrupt enable bit.

TBIE = "0" : disable TBIF interrupt

TBIE = "1" : enable TBIF interrupt

Bit 2 (EXIE1) : External INT 1 Interrupt enable bit.

EXIE1 = "0" : disable EXIF1 interrupt

EXIE1 = "1" : enable EXIF1 interrupt

Bit 0 (TCIE0) : TCC Interrupt enable bit.

TCIE0 = "0" : disable TCIF0 interrupt

TCIE0 = "1" : enable TCIF0 interrupt

Individual interrupt is enabled by setting its associated control bit in the IMR2 to "1".

Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction.

The IMR2 register is both readable and writable.

5.4 CPU Operation Mode

Registers for CPU Operation Mode

R_BANK	Address	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0X05	**SCR**	0	PS2	PS1	PS0	0	1	**SIS**	**REM**
–	–	–	–	R/W	R/W	R/W	–	–	R/W	R/W

* R_BANK: Register Bank (Bits 7, 6 of R3), R/W: Read/Write

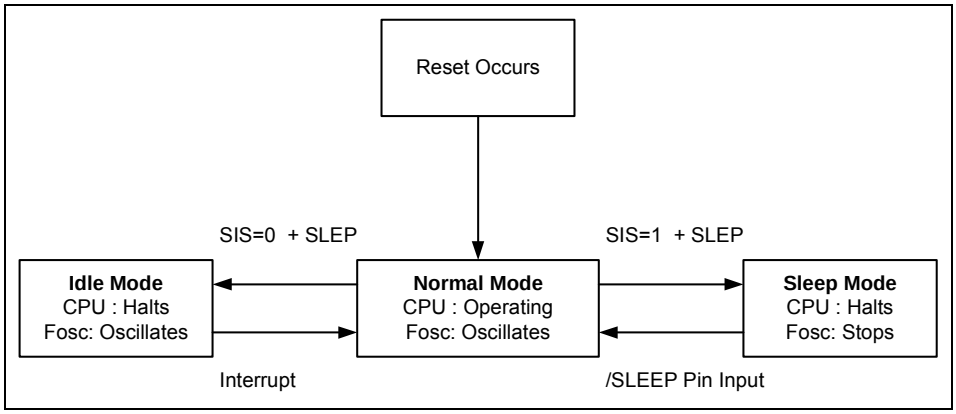


Fig. 5-4 Operation Mode and Switching

Table 2. Mode Switching Control

Mode Switch	Switch Method	Note
Normal → Sleep	Set SIS = 1, execute SLEP instruction	–
Sleep → Normal	/SLEEP pin wake up	–
Normal → Idle	Set SIS = 0, execute SLEP instruction	–
Idle → Normal	Interrupt	–

Table 3. Operation Mode

Operation Mode		Frequency	CPU Code	On-chip Peripherals
Signal Clock	Reset	Turn on	Reset	Reset
	Normal		Fosc	Fosc
	Idle		Halt	
	Sleep	Turn off		Halt

In Normal mode, the CPU core and on-chip peripherals operate in oscillator frequency.

In Idle mode, the CPU core halts, but the on-chip peripheral and oscillator circuit remain active. Idle mode is released to Normal mode by any interrupt source. If the ENI instruction is set, an interrupt will be serviced first followed by executing the next instruction which is after the Idle mode is released and the interrupt service is finished. If the ENI instruction is not set, the next instruction will be executed which is after the Idle mode start instruction. Idle mode can also be released by setting the /RESET pin to low and executing a reset operation.

In Sleep mode, the internal oscillator is turned off and all system operation is halted. Sleep mode is released by /SLEEP pin (level sensitive or edge sensitive can be set by System Control Register (SCR) Bit 0 (REM)). After a warm-up period, the next instruction will be executed which is after the Sleep mode start instruction. Sleep mode can also be released by setting the /RESET pin to low and executing a reset operation. In level sensitive mode, the /SLEEP pin must be confirmed in low level before entering Sleep mode. In edge sensitive mode, Sleep mode is started even when the /SLEEP pin is in high level.

Table 4. Wake-up Methods

Wake-up Signal	Sleep Mode R5 (SIS) = 1+SLEP Instruction	Idle Mode R5 (SIS)= 0 + SLEP Instruction	Normal Mode R5 (SIS)=(*)
1. Individual interrupt source in IMR1, IMR2 2. WDT interrupt request 3. /INT0 4. ENI instruction is not executed	No effect **	1. Wake-up 2. Jump to the next instruction or enter Idle mode	No effect**
1. Individual interrupt source in IMR1, IMR2 2. WDT interrupt request 3. /INT0 4. Execute ENI instruction	No effect **	1. Wake-up 2. Jump to an Interrupt vector after RETI instruction, then jump to the next instruction or enter Idle mode	Interrupt
/SLEEP pin	1. Wake-up 2. Jump to the next instruction or enter Sleep mode	No effect	No effect
/RESET pin	Reset	Reset	Reset
WDT time out	Reset	Reset	Reset

Note: * Don't care

** Interrupt request flag will be recorded

5.5 AD Converter

Registers for AD Converter Circuit

R_BANK	Address	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 1	0X0B	**ADCR**	**ADREF**	**ADRUN**	**ADCK1**	**ADCK0**	**ADP**	**ADIS2**	**ADIS1**	**ADIS0**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0X0C	**ADIC**	**ADE7**	**ADE6**	**ADE5**	**ADE4**	**ADE3**	**ADE2**	**ADE1**	**ADE0**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0X0D	**ADDH**	**ADD9**	**ADD8**	**ADD7**	**ADD6**	**ADD5**	**ADD4**	**ADD3**	**ADD2**
			R	R	R	R	R	R	R	R
Bank 1	0X08	**ADDL**	**ADD1**	**ADD0**	0	TC2M	TC2S	TC2CK2	TC2CK1	TC2CK0
			R	R	--	R/W	R/W	R/W	R/W	R/W
Bank 0	0x0E	**ISFR1**	EXIF5	TCIF2	**ADIF**	0	EXIF3	TCIF4	SPIF	TCIF3
			R/W	R/W	R/W	0	R/W	R/W	R/W	R/W
SPR	0x0C	**ADOSCR**	**CALI**	**SIGN**	**VOF[2]**	**VOF[1]**	**VOF[0]**	0	0	0
			R/W	R/W	R/W	R/W	R/W	--	--	--
SPR	0x0E	**IMR1**	EXIE5	TCIE2	**ADIE**	0	EXIE3	TCIE4	SPIE	TCIE3
			R/W	R/W	R/W	0	R/W	R/W	R/W	R/W

* R_BANK : Register Bank (Bits 7, 6 of R3), R/W: Read / Write

* SPR : Special Purpose Registers

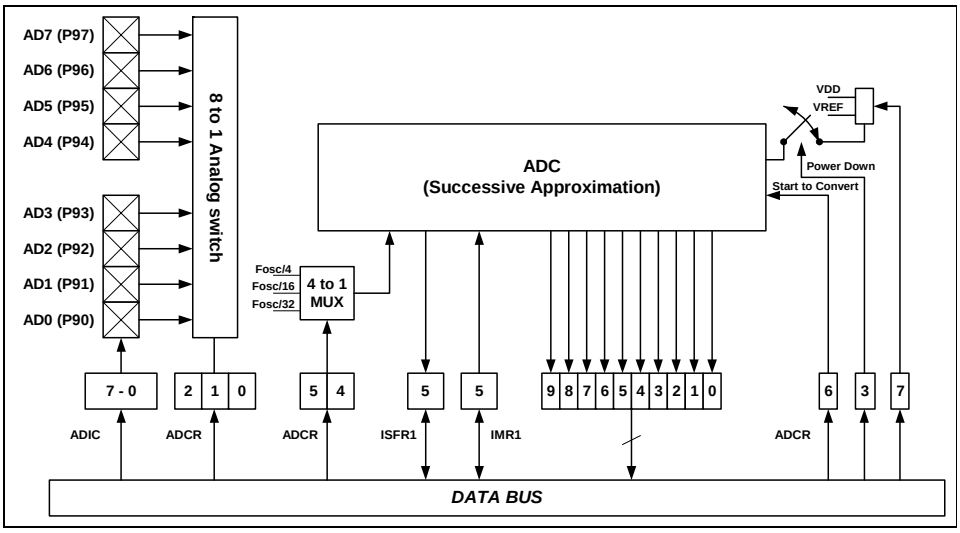


Fig. 5-5 AD Converter

It is a 10-bit successive approximation type AD converter. The upper side of analog reference voltage can select either internal VDD or external input pin P97 (VREF) by setting the ADREF bit in ADCR.

ADC Data Register

When the A/D conversion is completed, the result is loaded to the ADDH (8 bit) and ADDL (2 bit). The START/END bit is cleared, and the ADIF is set.

A/D Sampling Time

The accuracy, linearity, and speed of the successive approximation A/D converter are dependent on the properties of the ADC. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 2 μs for each KΩ of the analog source impedance and at least 2 μs for the low-impedance source. The maximum recommended impedance for the analog source is 10KΩ at V_{DD} =5V. After the analog input channel is selected, this acquisition time must be done before A/D conversion can be started.

A/D Conversion Time

ADCK0 and ADCK1 select the conversion time (Tct), in terms of instruction cycles. This allows the MCU to run at maximum frequency without sacrificing accuracy of A/D conversion. For the EM78P312N, the conversion time per bit is about 4μs. Table 5 shows the relationship between Tct and the maximum operating frequencies.

Table 5

ADCK1:0	Operation Mode	Max. Frequency (Fc)	Max. Conversion Rate per Bit	Max. Conversion Rate
0 0	Fc/4	1MHz	250kHz (4μs)	48μs (20.8kHz)
0 1	Fc/16	4MHz	250kHz (4μs)	48μs (20.8kHz)
1 0	Fc/32	8MHz	250kHz (4μs)	48μs (20.8kHz)
1 1	Reserved	-	-	-

5.6 Time Base Timer and Keytone Generator

Registers for AD Converter Circuit

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 1	0X0E	TBKTC	TEN	TCK1	TCK0	0	TBTEN	TBTCK2	TBTCK1	TBTCK0
			R/W	R/W	R/W	--	R/W	R/W	R/W	R/W
Bank 0	0x0F	ISFR2	0	UERRIF	RBFF	TBEF	TBIF	EXIF1	0	TCIF0
			0	R/W	R/W	R/W	R/W	R/W	0	R/W
SPR	0x0F	IMR2	0	UERRIE	URIE	UTIE	TBIE	EXIE1	0	TCIE0
			0	R/W	R/W	R/W	R/W	R/W	0	R/W

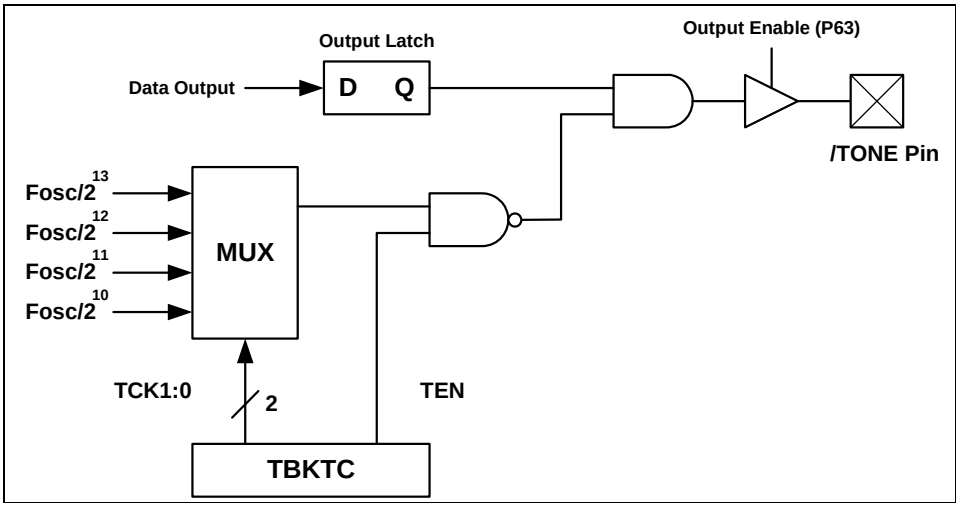


Fig. 5-6 Tone Output Pin Configuration

The Keytone output can generate 50% duty pulse for driving a piezo-electric buzzer. The P63 must be set to “1” before the keytone is enabled and it can be halted by setting P63 to “0”.

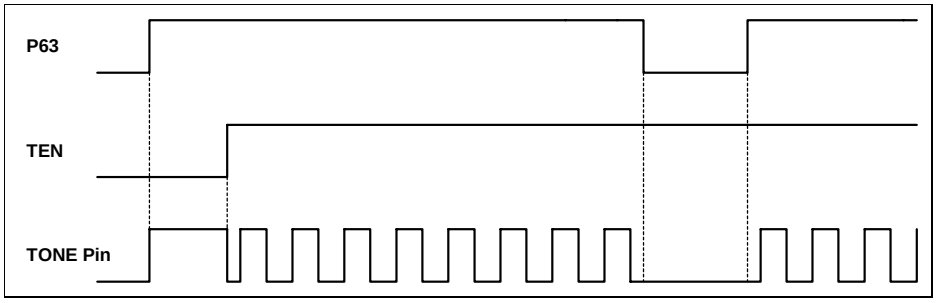


Fig. 5-7 Tone Output Pin Timing Chart

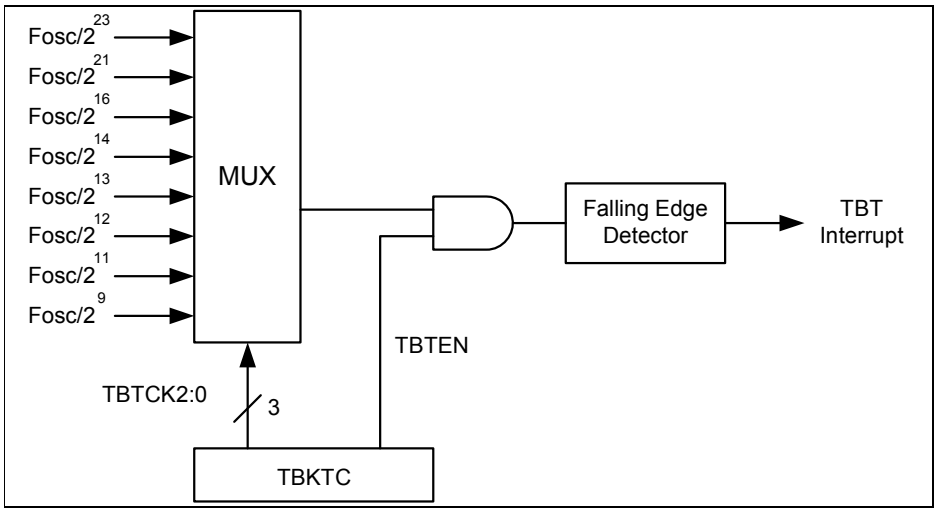


Fig. 5-8 TBT Configuration

The Time Base Timer is used to generate the base time for key scan or dynamic display processing. The interrupt is generated in the first falling edge of the source clock after TBTEN is set to "1".

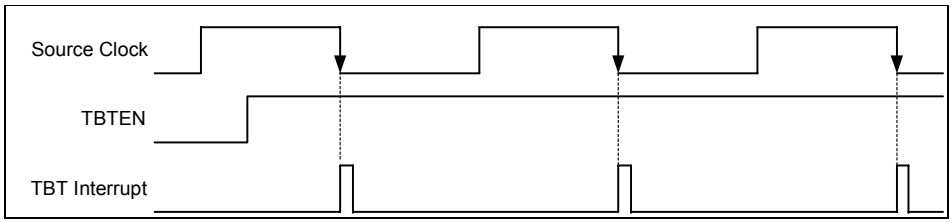


Fig. 5-9 Time Base Timer Timing Chart

5.7 UART (Universal Asynchronous Receiver/Transmitter)

Registers for UART Circuit

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 2	0X05	URC1	URTD8	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE
			R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Bank 2	0X06	URC2	0	0	SBIM1	SBIM0	UINVEN	0	0	0
			--	--	R/W	R/W	R/W	--	--	--
Bank 2	0X07	URS	URRD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE
			R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Bank 2	0X08	URRD	URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0
			R	R	R	R	R	R	R	R
Bank 2	0X09	URTD	URTD 7	URTD 6	URTD 5	URTD 4	URTD 3	URTD 2	URTD 1	URTD0
			W	W	W	W	W	W	W	W
Bank 0	0x0F	ISFR2	0	UERRIF	RBFF	TBEF	TBIF	EXIF1	0	TCIF0
			--	R/W	R/W	R/W	R/W	R/W	--	R/W
SFR	0x0F	IMR2	0	UERRIE	URIE	UTIE	TBIE	EXIE1	0	TCIE0
			--	R/W	R/W	R/W	R/W	R/W	--	R/W

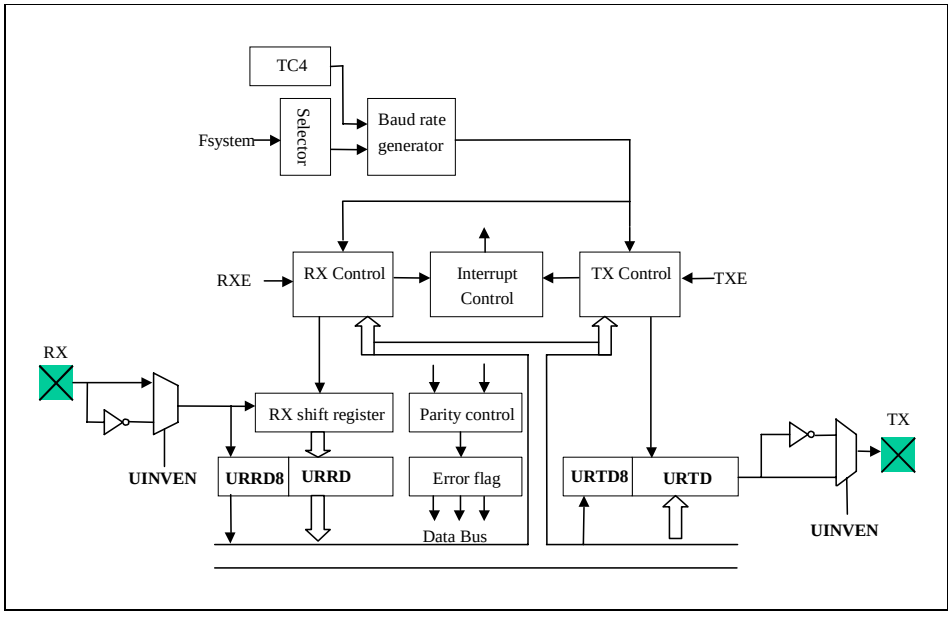


Fig. 5-10 Function Block Diagram

In Universal Asynchronous Receiver Transmitter (UART), each transmitted or received character is individually synchronized by framing it with a start bit and stop bit.

Full duplex data transfer is possible since the UART has independent transmit and receive sections. Double buffering for both sections allows the UART to be programmed for continuous data transfer.

The figure below shows the general format of one character sent or received. The communication channel is normally held in the marked state (high). Character transmission or reception starts with a transition to the space state (low).

The first bit transmitted or received is the start bit (low). It is followed by the data bits, in which the least significant bit (LSB) comes first. The data bits are followed by the parity bit. If present, then the stop bit or bits (high) confirm the end of the frame.

In receiving, the UART synchronizes on the falling edge of the start bit. When two or three "0" are detected during three samples, it is recognized as normal start bit and the receiving operation is started.

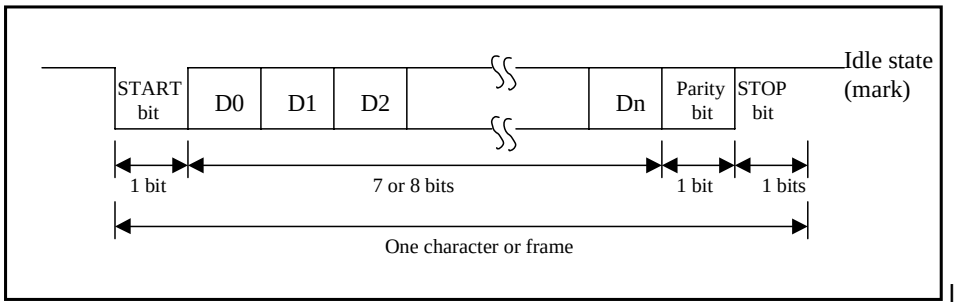


Fig. 5-11 Data Format in UART

5.7.1 UART Mode

There are three UART modes. Mode 1 (7 bits data) and Mode 2 (8 bits data) allow the addition of a parity bit. The parity bit addition is not available in Mode 3. The Figure below shows the data format in each mode.

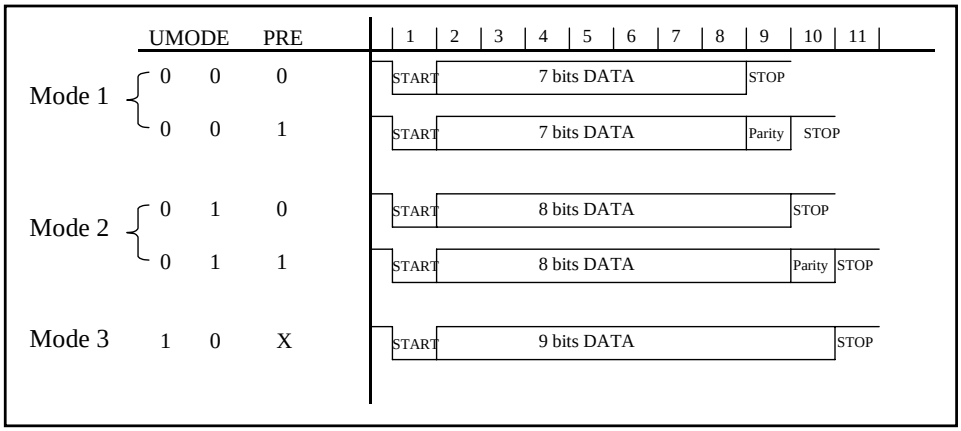


Fig. 5-12 UART Mode

5.7.2 Transmitting

In transmitting serial data, the UART operates as follows:

1. Set the TXE bit of the URC1 register to enable the UART transmission function.
2. Write data into the URTD register and the UTBE bit of the URC1 register will be set by hardware.

3. Start transmitting.
4. Serially transmitted data are transmitted in the following order from the TX pin.
5. Start bit: one “0” bit is output.
6. Transmit data: 7, 8 or 9 bits data are output from the LSB to the MSB.
7. Parity bit: one parity bit (odd or even selectable) is output.
8. Stop bit: one “1” bit (stop bit) is output.

Mark state: output “1” continues until the start bit of the next transmitted data.

After transmitting the stop bit, the UART generates a TBEF interrupt (if enabled).

5.7.3 Receiving

In receiving, the UART operates as follows:

1. Set RXE bit of the URS register to enable the UART receiving function.

   The UART monitors the RX pin and synchronizes internally when it detects a start bit.

2. Receive data is shifted into the URRD register in the order from LSB to MSB.
3. The parity bit and the stop bit are received.

   After one character received, the UART generates a RBFF interrupt (if enable). And URBF bit of URS register will be set to 1.

4. The UART makes the following checks:

   (a) Parity check: The number of 1 of the received data must match the even or odd parity setting of the EVEN bit in the URS register.

   (b) Frame check: The start bit must be 0 and the stop bit must be 1.

   (c) Overrun check: The URBF bit of the URS register must be cleared (that means the URRD register should be read out) before next received data is loaded into the URRD register.

   If any checks failed, the UERRIF interrupt will be generated (if enabled), and an error flag is indicated in PRERR, OVERR or FMERR bit. The error flag should be cleared by software else the UERRIF interrupt will occur when the next byte is received.

5. Read received data from URRD register. And URBF bit will be clear by hardware.

5.7.4 Baud Rate Generator

The baud rate generator is comprised of a circuit that generates a clock pulse to determine the transfer speed for transmission/reception in the UART.

The BRATE2~BRATE0 bits of the URC1 register can determine the desired baud rate.

5.8 SPI (Serial Peripheral Interface)

Registers for the SPI Circuit

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 3	0X05	**SPIC1**	**SMP**	**DCOL**	**BRS2**	**BRS1**	**BRS0**	**EDS**	**DORD**	**WBE**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Bank 3	0X06	**SPIC2**	**SPIS**	0	0	0	0	**SPIM1**	**SPIM0**	**RBF**
			R/W	--	--	--	--	R/W	R/W	R
Bank 3	0X07	**SPID**	**SPID7**	**SPID6**	**SPID5**	**SPID4**	**SPID3**	**SPID2**	**SPID1**	**SPID0**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x0E	**ISFR1**	EXIF5	TCIF2	ADIF	0	EXIF3	TCIF4	**SPIF**	TCIF3
			R/W	R/W	R/W	--	R/W	R/W	R/W	R/W
SFR	0x0E	**IMR1**	EXIE5	TCIE2	ADIE	0	EXIE3	TCIE4	**SPIE**	TCIE3
			R/W	R/W	R/W	--	R/W	R/W	R/W	R/W

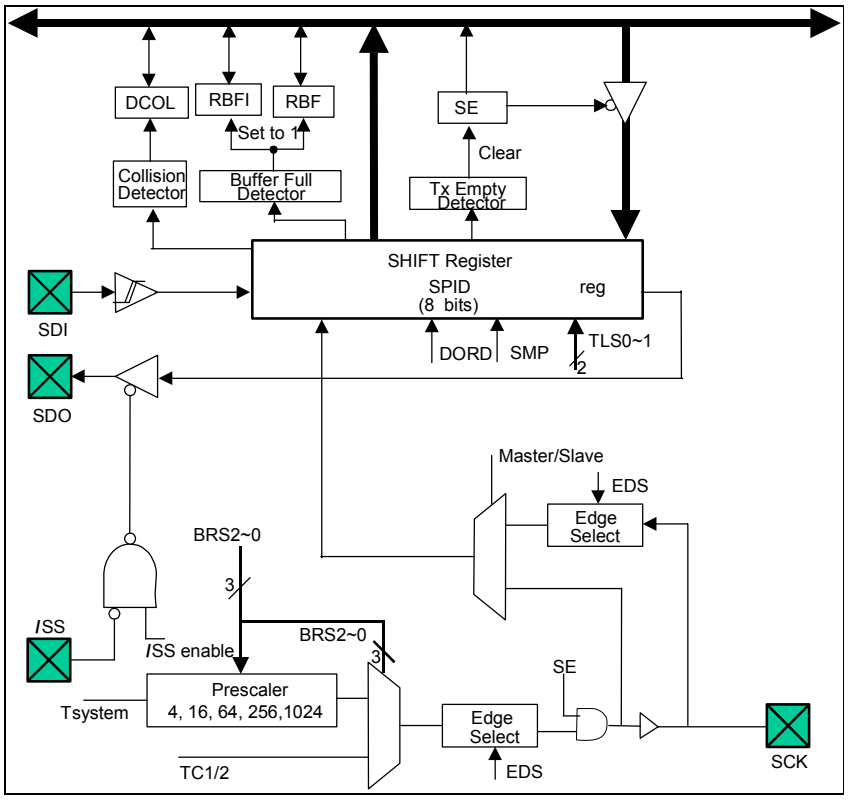


Fig. 5-13 SPI Block Diagram

The serial interface are connected to external devices via P70 (/SCK), P71 (SI), P72 (SO). The serial interface can also be used as I/O port. In the transmit mode, P71 can be used as normal I/O port and in receive mode, P72 and P71 can be used as normal I/O ports.

5.8.1 Serial Clock

Six internal clocks can be selected by setting BRS0 ~ BRS2 and the clock output to the outside from /SCK (P70) pin. The External clock can also be used and connected to /SCK (P70) pin.

5.8.2 Shift Direction and Sample Phase

Setting up the DORD bit of the SPIC1 register can determine the shift direction. Setting up the EDS bit of the SPIC1 register can select the rising edge or falling edge and latch the data. Setting up the SMP bit of the SPIC2 register can select the sample phase at the middle or at the end of the data output time.

5.8.3 Transfer Mode

The transmit, receive, transmit/receive mode can be selected by setting SPIM0 ~ SPIM1.

(a) 8-bit Transmit Mode

Set SPIM0 ~ SPIM12 to transmit mode and write data to the data buffer SPID. Set SPIS to "1" to start transmission. The data are output sequentially to the SO pin in synchronous with the serial clock. When the final bit of transfer data has been transferred, the SPI interrupt is generated and SPIS is cleared to "0" by hardware. In order to transmit the next data, the SPIS must be set to "1" again by software. If the next data is not written to the data buffer, the transfer is not started when using the internal clock.

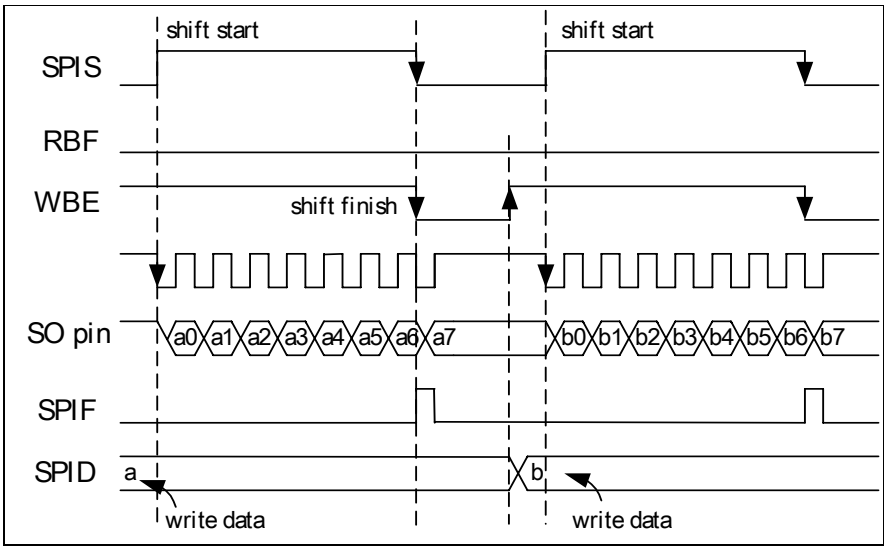


Fig. 5-14 Transmit Mode (8-bit, 1 word)

(b) 8-bit Receive Mode

Setting SPIM0 ~ SPIM1 to receive mode and setting SPIS to "1" to start receiving. The data are input sequentially from the SI pin in synchronous with the serial clock. When the final bit of transfer data has been received, the SPI interrupt is generated and SPIS is cleared to "0" by hardware. In order to receive the next data, the SPIS must be set to "1" again by software. If the current data is not read out from the data buffer, receiving is not started when using internal clock.

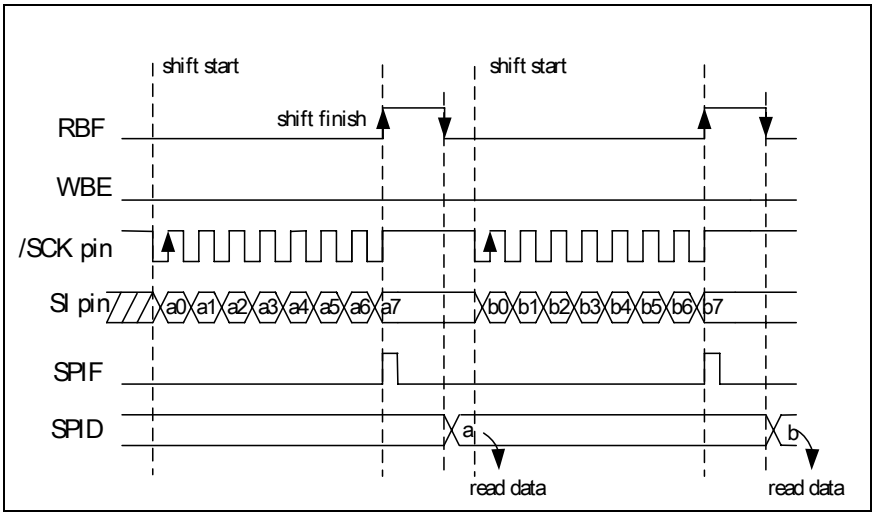


Fig. 5-15 Receive Mode (8-bit, 1 word)

(c) 8-bit Transmit/Receive Mode

Set SPIM0 ~ SPIM1 to transmit/receive mode and write data to data buffer SPID. Set SPIS to "1" to start transferring. The data are output to the SO pin and input from the SI pin sequentially in synchronous with the serial clock. When the number of data words specified has been transferred, the SPI interrupt is generated and SPIS is cleared to "0" by hardware. In order to receive the next data, the SPIS must be set to "1" again by software. Writing data in transmit mode and reading data in receive mode use the same data buffer. If the current data is not read out from the data buffer and then write the data to data buffer, the transfer is not started when using internal clock. Always write the data to be transmitted after reading the received data.

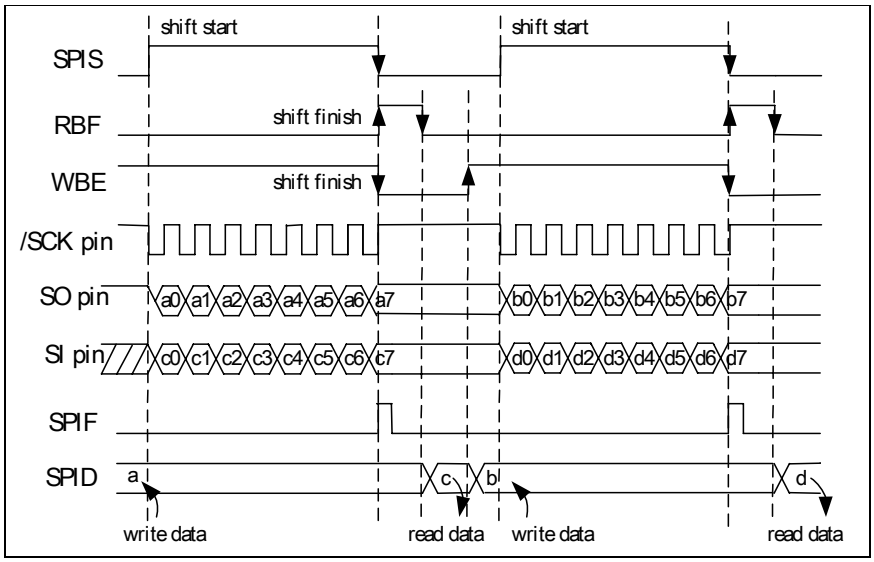


Fig. 5-16 Transmit/Receive Mode (8-bit, 1 word)

(d) Multiple Device Connect (/SS)

When selecting external clock for transfer clock source, the /SS function can be used. This pin (/SS) will be active when the /SS function is enabled, else the /SS pin is a general purpose I/O. Ignore the data on the SDI and SDO pins while /SS is high, since the SDO is no longer driven.

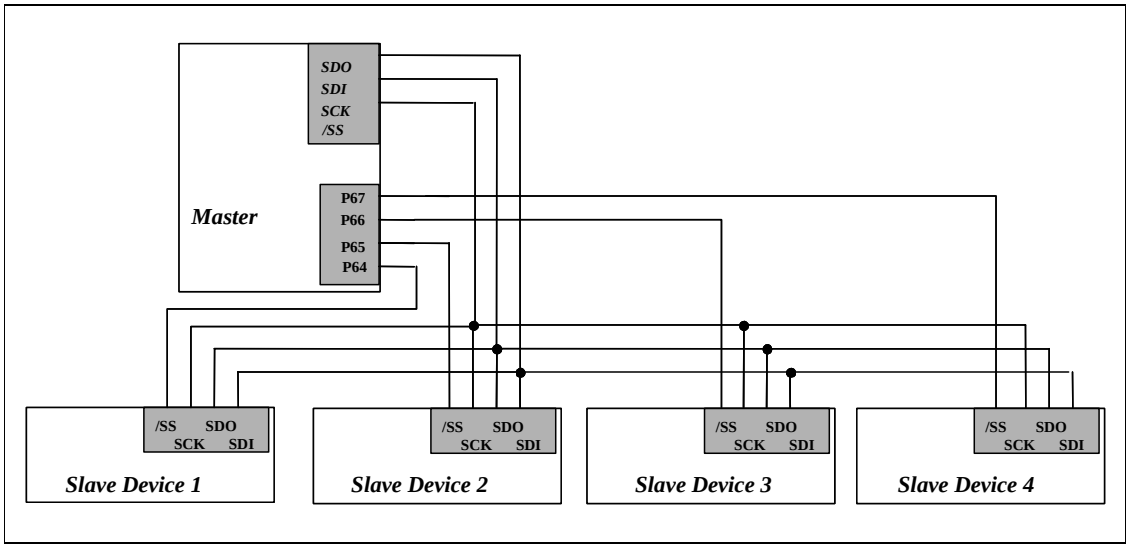


Fig. 5-17 The SPI Configuration Example of Single-Master and Multi-Slaves

5.9 Timer/Counter 2

Registers for Timer/Counter 2 Circuit

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 1	0X08	**TC2CR**	ADD1	ADD0	0	**TC2M**	**TC2S**	**TC2CK2**	**TC2CK1**	**TC2CK0**
			R	R	–	R/W	R/W	R/W	R/W	R/W
Bank 1	0X09	**TC2DH**	**TC2D15**	**TC2D14**	**TC2D13**	**TC2D12**	**TC2D11**	**TC2D10**	**TC2D9**	**TC2D8**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0X0A	**TC2DL**	**TC2D7**	**TC2D6**	**TC2D5**	**TC2D4**	**TC2D3**	**TC2D2**	**TC2D1**	**TC2D0**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x0E	**ISFR1**	EXIF5	**TCIF2**	ADIF	0	EXIF3	TCIF4	SPIF	TCIF3
			R/W	R/W	R/W	–	R/W	R/W	R/W	R/W
SFR	0x0B	**INTCR**	INT1NR	INT0EN	0	INT3ES1	INT3ES0	0	INT1ES	**TC2ES**
			R/W	R/W		R/W	R/W		R/W	R/W
SFR	0x0E	**IMR1**	EXIE5	**TCIE2**	ADIE	0	EXIE3	TCIE4	SPIE	TCIE3
			R/W	R/W	R/W	–	R/W	R/W	R/W	R/W

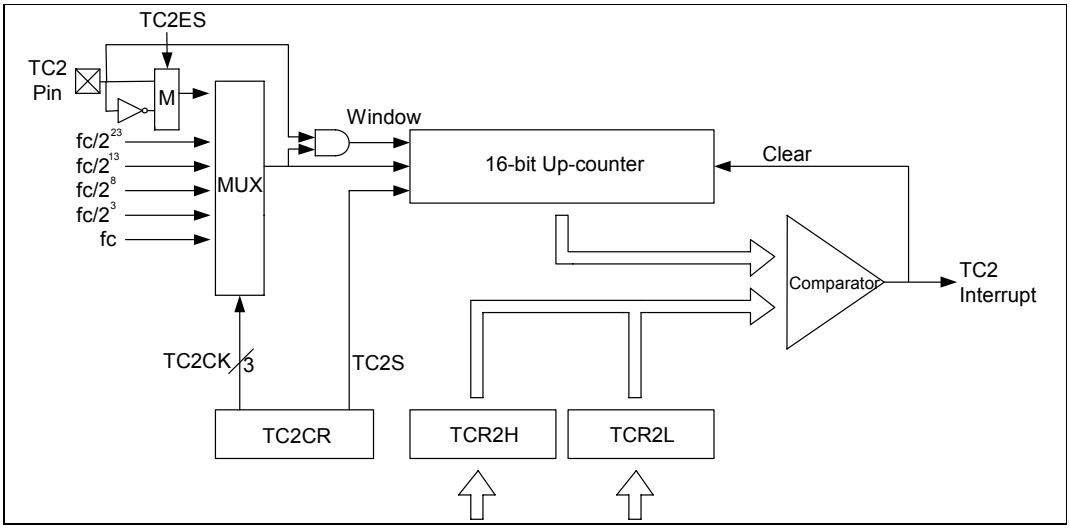


Fig. 5-18 Configuration of Timer/Counter 2

5.9.1 Timer Mode

In Timer mode, counting up is performed using the internal clock. When the contents of the up-counter matched with the TCR2 (TCR2H+TCR2L), then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

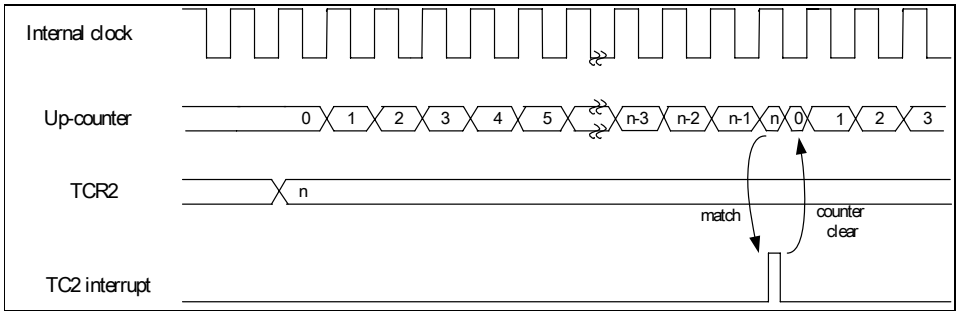


Fig. 5-19 Timer Mode Timing Chart

5.9.2 Counter Mode

In Counter mode, counting up is performed using the external clock input pin (TC2 pin) and **either rising or falling** can be selected by setting TC2ES. When the contents of the up-counter matched with the TCR2 (TCR2H+TCR2L), then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

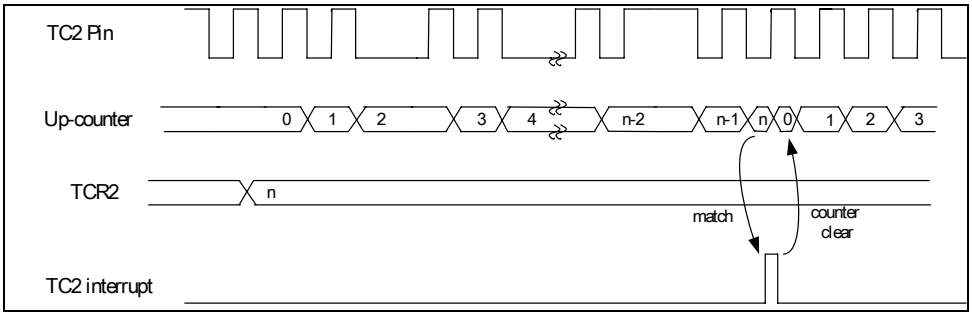


Fig. 5-20 Counter Mode Timing Chart (TC2ES = 1)

5.9.3 Window Mode

In Window mode, counting up is performed on the **rising or falling edge** of the pulse that is logical AND of an internal clock and the TC2 pin (window pulse). When the contents of the up-counter matched with the TCR2 (TCR2H+TCR2L), then interrupt is generated and the counter is cleared. The frequency (window pulse) must be slower than the selected internal clock.

Writing to the TCR2L, the comparison is inhibited until TCR2H is written.

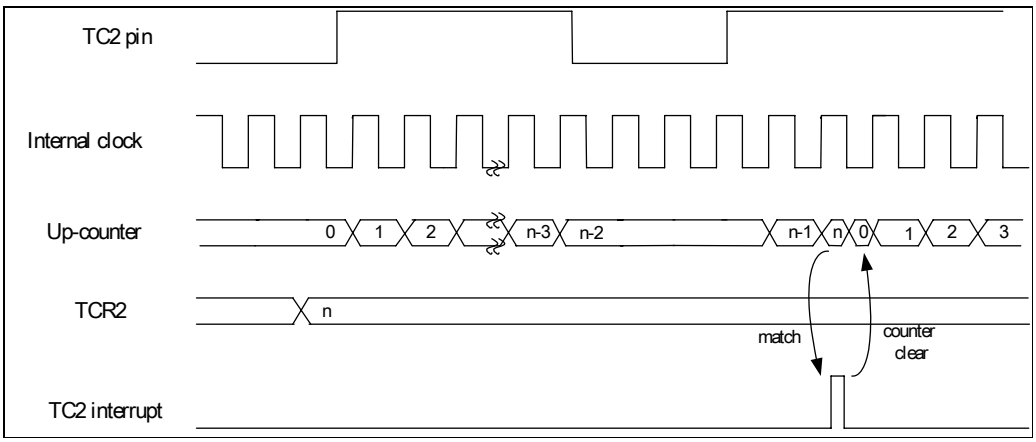


Fig. 5-21 Window Mode Timing Chart

5.10 Timer/Counter 3

Registers for Timer/Counter 3 Circuit

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 1	0X05	**TC3CR**	**TC3CAP**	**TC3S**	**TC3CK1**	**TC3CK0**	**TC3M**	0	0	0
			R/W	R/W	R/W	R/W	R/W	--	--	--
Bank 1	0X06	**TC3DA**	**TC3DA7**	**TC3DA6**	**TC3DA5**	**TC3DA4**	**TC3DA3**	**TC3DA2**	**TC3DA1**	**TC3DA0**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0X07	**TC3DB**	**TC3DB7**	**TC3DB6**	**TC3DB5**	**TC3DB4**	**TC3DB3**	**TC3DB2**	**TC3DB1**	**TC3DB0**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x0E	**ISFR1**	EXIF5	TCIF2	ADIF	0	EXIF3	TCIF4	SPIF	**TCIF3**
			R/W	R/W	R/W	--	R/W	R/W	R/W	R/W
SFR	0x0B	**INTCR**	INT1NR	INT0EN	0	INT3ES1	**INT3ES0**	0	INT1ES	TC2ES
			R/W	R/W	--	R/W	R/W	--	R/W	R/W
SFR	0x0E	**IMR1**	EXIE5	TCIE2	ADIE	0	EXIE3	TCIE4	SPIE	**TCIE3**
			R/W	R/W	R/W	--	R/W	R/W	R/W	R/W

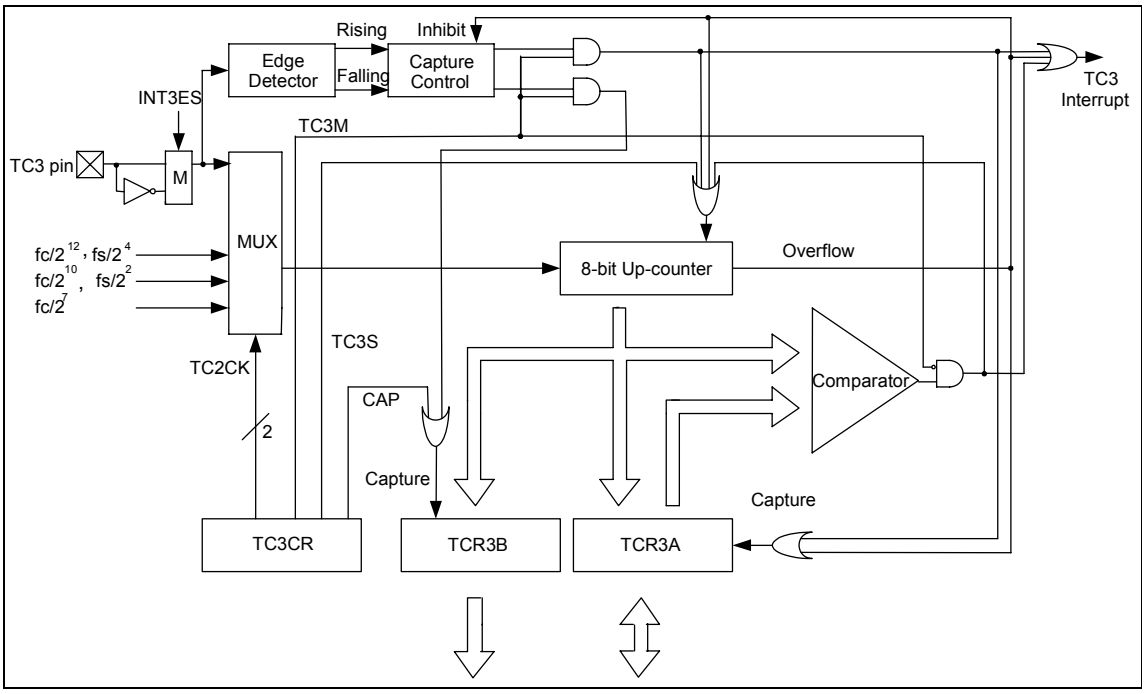


Fig. 5-22 Configuration of Timer/Counter3

5.10.1 Timer Mode

In Timer mode, counting up is performed using the internal clock. When the contents of the up-counter matched with the TCR3DA, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared. The current contents of the up-counter are loaded into the TCR3DB by setting TC3CAP to "1" and the TC3CAP is cleared to "0" after capture automatically.

5.10.2 Counter Mode

In Counter mode, counting up is performed using the external clock input pin (TC3 pin) and **either rising or falling edge** can be selected by INT3ES0 but both edge cannot be used. When the contents of the up-counter matched with the TCR3DA, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared. The current contents of the up-counter are loaded into the TCR3DB by setting TC3CAP to "1" and the TC3CAP is cleared to "0" after capture automatically.

5.10.3 Capture Mode

In Capture mode, the pulse width, period and duty of the TC3 input pin are measured in this mode, which can be used in decoding the remote control signal. The counter is free running by the internal clock. On the rising (falling) edge of TC3 pin input, the contents of the counter is loaded into TCR3DA, then the counter is cleared and interrupt is generated. On the falling (rising) edge of TC3 pin input, the contents of the counter are loaded into TCR3DB. The counter is still counting, on the next rising edge

of the TC3 pin input, the contents of the counter are loaded into TCR3A, counter is cleared and interrupt is generated again. If an overflow before the edge is detected, the FFH is loaded into TCR3DA and an overflow interrupt is generated. During interrupt processing, it can be determined whether or not there is an overflow by checking whether the TCR3DA value is FFH. After an interrupt (capture to TCR3DA or overflow detection) is generated, capture and overflow detection are halted until TCR3DA is read out.

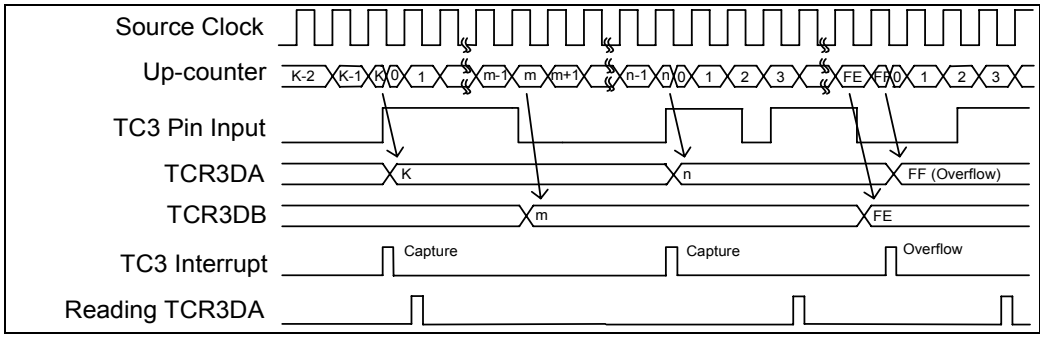


Fig. 5-23 Timing Chart of Capture Mode

5.11 Timer/Counter 4

Registers for Timer 4 Circuit

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0X0B	**TC4CR**	**TC4FF1**	**TC4FF0**	**TC4S**	**TC4CK2**	**TC4CK1**	**TC4CK0**	**TC4M1**	**TC4M0**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0X0C	**TC4D**	**TC4D7**	**TC4D6**	**TC4D5**	**TC4D4**	**TC4D3**	**TC4D2**	**TC4D1**	**TC4D0**
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x0E	**ISFR1**	EXIF5	TCIF2	ADIF	0	EXIF3	**TCIF4**	SPIF	TCIF3
			R/W	R/W	R/W	--	R/W	R/W	R/W	R/W
SFR	0x0E	**IMR1**	EXIE5	TCIE2	ADIE	0	EXIE3	**TCIE4**	SPIE	TCIE3
			R/W	R/W	R/W	--	R/W	R/W	R/W	R/W

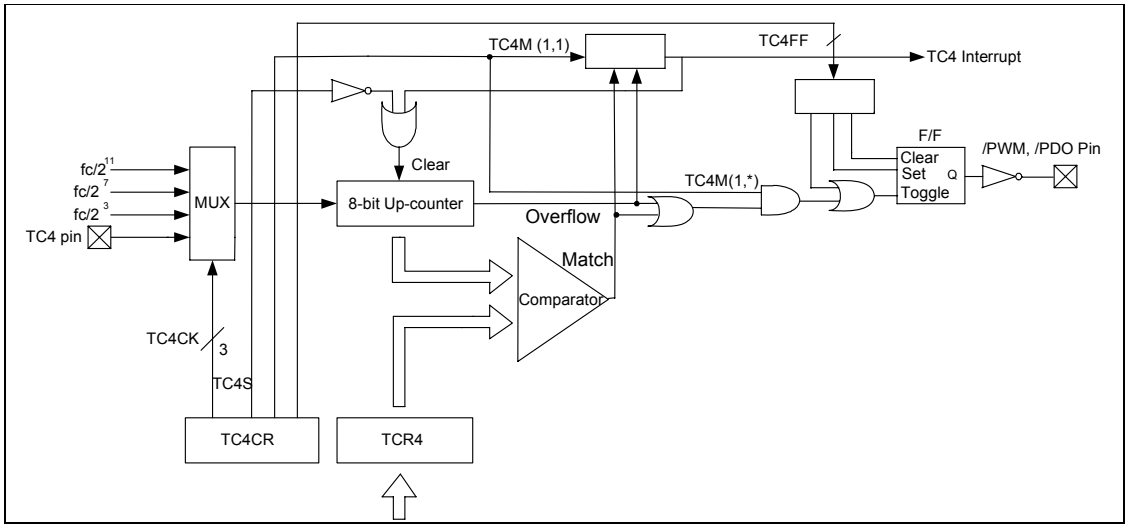


Fig. 5-24 Timer/Counter 4 Configuration

5.11.1 Timer Mode

In Timer mode, counting up is performed using the internal clock. When the contents of the up-counter matched with the TCR4, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

5.11.2 Counter Mode

In Counter mode, counting up is performed on the **rising edge** of the external clock input pin (TC4 pin). When the contents of the up-counter matched with the TCR4, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

5.11.3 PDO Mode

In Programmable Divider Output (PDO) mode, counting up is performed using the internal clock. The contents of TCR4 are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to /PDO pin. This mode can generate 50% duty pulse output. The F/F can be initialized by the program and it is initialized to "0" during a reset. A TC4 interrupt is generated each time the /PDO output is toggled.

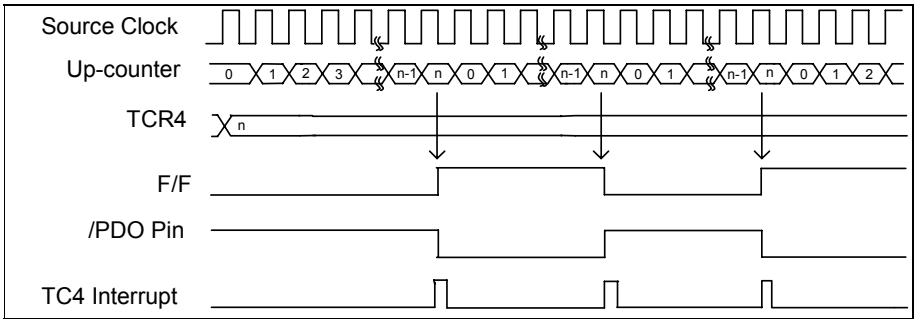


Fig. 5-25 Timing Chart for PDO Mode

5.11.4 PWM Mode

In Pulse Width Modulation (PWM) Output mode, counting up is performed using the internal clock. The contents of the TCR4 are compared with the contents of the up-counter. The F/F is toggled when match is found. The counter is still counting, the F/F is toggled again when the counter overflows, then the counter is cleared. The F/F output is inverted and output to the /PWM pin. A TC4 interrupt is generated each time an overflow occurs. TCR4 is configured as a 2-stage shift register and, during output, will not switch until one output cycle is completed even if TCR4 is overwritten. Therefore, the output can be changed continuously. TRC4 is also shifted the first time by setting TC4S to "1" after data is loaded to TCR4.

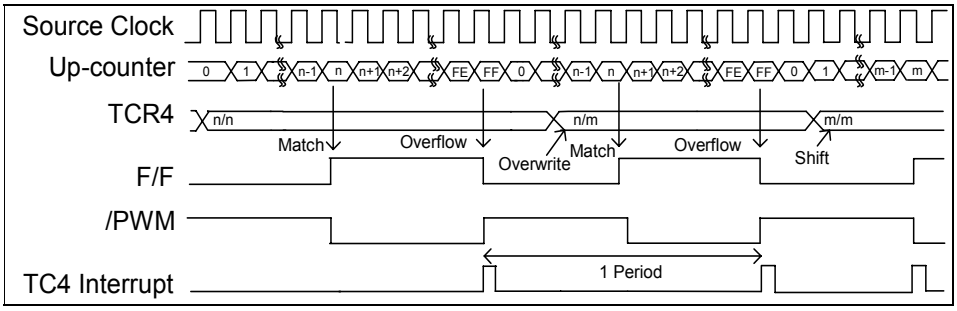


Fig. 5-26 Timing Chart for PWM Mode

5.12 TCC/WDT & Prescaler

An 8-bit counter is available as prescaler for the TCC. The PSR0~PSR2 bits determine the ratio. The prescaler is cleared each time the instruction is written to TCC under TCC mode.

R1 (TCC) is an 8-bit timer/counter. The clock source of TCC is the internal clock. If the TCC signal source is from the internal clock, TCC will increase by 1 at every instruction cycle (without prescaler). CLK=Fosc/2 or CLK=Fosc/4 selection is determined by the CODE Option bit CLK status. CLK=Fosc/2 is used if CLK bit is "0", and CLK=Fosc/4 is used if CLK bit is "1".

The watchdog timer is a free running on-chip RC oscillator. During normal operation mode, a WDT time-out (if enabled) will cause the device to reset or interrupt by setting WDTO. The WDT can be enabled or disabled any time during normal mode by software programming. Without prescaler, the WDT time-out period is approximately 18 ms (default). The WDT can also be used as a timer to generate an interrupt at fixed interval.

5.13 I/O Ports

The I/O registers, Port 6, Port 7, Port 8, and Port 9 are bi-directional tri-state I/O ports. Each I/O pin can be defined as “input” or “output” pin by the I/O control register (IOC6 ~ IOC9). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 6, Port 7, Port 8, and Port 9 are shown in Fig. 5-26.

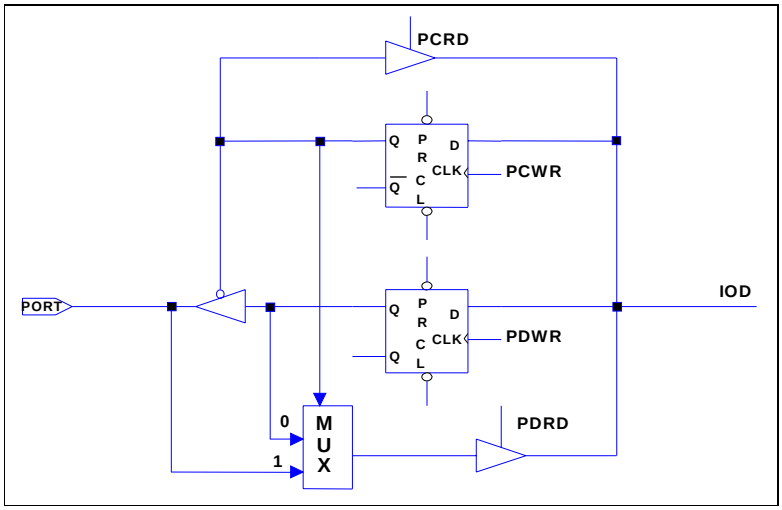


Fig. 5-27 The I/O Port and I/O Control Register Circuit

5.14 Reset and Wake-up

5.14.1 Reset

A reset is initiated by one of the following events:

(1) Power-on reset

(2) /RESET pin input “low”

(3) WDT timeout. (if enabled)

The device is kept in a reset condition for a period of approx. 18ms[1] (one oscillator start-up timer period) after the reset is detected. Once a reset occurs, the following functions are performed.

- The oscillator starts or is running
- The Program Counter (R2) is reset to all “0”.
- When power is switched on, the upper two bits of R3, the upper two bits of R4 and the Bits 6 ~ 4 of R5 are cleared.
- All I/O port pins are configured as input mode (high-impedance state).

[1] **Note:** V_{DD} = 5V, set up time period = 16.2ms ± 30%
V_{DD} = 3V, set up time period = 19.6ms ± 30%

- The Watchdog timer and prescaler are cleared.
- Upon power on, the upper two bits of R3 are cleared.
- Upon power on, the upper two bits of R4 are cleared.
- Upon power on, the upper three bits of R5 are cleared.
- The bits of CONT register are set to all “1” except Bit 6 (INT flag).
- ISFR0, ISFR1, ISFR2 register and IMR1, IMR2 registers are cleared.

The controller has two modes for power saving.

(1) SLEEP mode: R5 (SIS) = 1, SLEP instruction.

The internal oscillator is turned off and all system operation is halted.

(2) Idle mode: R5 (SIS) = 0, SLEP instruction

The CPU core halts but the on-chip peripheral and oscillator circuit remain active.

5.14.2 Wake-up from Sleep Mode

(1) External /SLEEP pin

The controller will be waken up and execute the next instruction after entering Sleep mode. All the registers will maintain their original values before “SLEP” instruction was executed.

(2) /RESET pin pull low

This will reset the controller and starts the program at address zero.

(3) WDT time out

This will reset the controller and run the program at address zero.

5.14.3 Wake-up from Idle Mode

(1) All interrupt

In all these cases, user should always enable the circuit before entering Idle mode. After wake-up, all registers will maintain their original values before entering “SLEP” instruction, then service an interrupt subroutine or proceed with next instruction by setting individual interrupt enable bit. After servicing an interrupt sub-routine (“RETI” instruction), the program will jump from “SLEP” instruction to the next instruction.

(2) /RESET pin pull low

This will reset the controller and run the program at address zero.

(3) WDT time out

This will reset the controller and run the program at address zero.

Table 6. Summary of the Initialized Values for Registers

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x06	IOC6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT time out	1	1	1	1	1	1	1	1
		Wake-up from Sleep, Idle mode	P	P	P	P	P	P	P	P
0x07	IOC7	Bit Name	X	X	X	X	C73	C72	C71	C70
		Power-on	U	U	U	U	1	1	1	1
		/RESET and WDT time out	U	U	U	U	1	1	1	1
		Wake-up from Sleep, Idle mode	U	U	U	U	P	P	P	P
0x08	IOC8	Bit Name	X	X	X	X	X	X	C81	C80
		Power-on	U	U	U	U	U	U	1	1
		/RESET and WDT time out	U	U	U	U	U	U	1	1
		Wake-up from Sleep, Idle mode	U	U	U	U	U	U	P	P
0x09	IOC9	Bit Name	C97	C96	C95	C94	C93	C92	C91	C90
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT time out	1	1	1	1	1	1	1	1
		Wake-up from Sleep, Idle mode	P	P	P	P	P	P	P	P
0x0B	INTCR	Bit Name	INT1NR	INT0EN	X	INT3ES1	INT3ES0	X	INT1ES	TC2ES
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT time out	0	0	0	0	0	0	0	0
		Wake-Up from Sleep, Idle mode	P	P	P	P	P	P	P	P
0x0C	ADOSCR	Bit Name	CALI	SIGN	VOF2	VOF1	VOF0	X	X	X
		Power-on	0	0	0	0	0	U	U	U
		/RESET and WDT time out	0	P	P	P	P	U	U	U
		Wake-up from Sleep, Idle mode	0	P	P	P	P	U	U	U
0x0E	IMR1	Bit Name	EXIE5	TCIE2	ADIE	X	EXIE3	TCIE4	SPIE	TCIE3
		Power-on	0	0	0	U	0	0	0	0
		/RESET and WDT time out	0	0	0	U	0	0	0	0
		Wake-up from Sleep, Idle mode	P	P	P	U	P	P	P	P
0x0F	IMR2	Bit Name	X	UERRIE	URIE	UTIE	TBIE	EXIE1	X	TCIE0
		Power-on	U	0	0	0	0	0	U	0
		/RESET and WDT time out	U	0	0	0	0	0	U	0
		Wake-Up from Sleep, Idle mode	U	P	P	P	P	P	U	P
N/A	CONT	Bit Name	WDT0	/INT	WDTP1	WDTP0	WDTE	PSR2	PSR1	PSR0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT time out	0	0	0	0	0	0	0	0
		Wake-up from Sleep, Idle mode	P	P	P	P	P	P	P	P
0x00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT time out	P	P	P	P	P	P	P	P
		Wake-up from Sleep, Idle mode	P	P	P	P	P	P	P	P
0x01	R1 (TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT time out	0	0	0	0	0	0	0	0
		Wake-up from Sleep, Idle mode	P	P	P	P	P	P	P	P
0x02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT time out	0	0	0	0	0	0	0	0
		Wake-up from Sleep, Idle mode	Jump to interrupt vector or execute next instruction							
0x03	R3 (SR)	Bit Name	RBS1	RBS0	X	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT time out	0	0	0	t	t	P	P	P
		Wake-up from Sleep, Idle mode	P	P	P	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	X	GRBS0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
		Power-on	0	0	U	U	U	U	U	U
		/RESET and WDT time out	0	0	P	P	P	P	P	P
		Wake-Up from Sleep, Idle mode	P	P	P	P	P	P	P	P

Register Bank 0

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05	SCR	Bit Name	X	X	X	PS0	X	X	SIS	REM
		Power-on	U	0	0	0	U	U	0	0
		/RESET and WDT time out	U	0	0	0	U	U	0	0
		Wake-up from Sleep, Idle mode	U	P	P	P	U	U	P	P
0x06	Port 6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT time out	1	1	1	1	1	1	1	1
		Wake-up from Sleep, Idle mode	P	P	P	P	P	P	P	P
0x07	Port 7	Bit Name	X	X	X	X	P73	P72	P71	P70
		Power-on	U	U	U	U	1	1	1	1
		/RESET and WDT time out	U	U	U	U	1	1	1	1
		Wake-up from Sleep, Idle mode	U	U	U	U	P	P	P	P
0x08	Port 8	Bit Name	X	X	X	X	X	X	P81	P80
		Power-on	U	U	U	U	U	U	1	1
		/RESET and WDT time out	U	U	U	U	U	U	1	1
		Wake-up from Sleep, Idle mode	U	U	U	U	U	U	P	P
0x09	Port 9	Bit Name	P97	P96	P95	P94	P93	P92	P91	P90
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT time out	1	1	1	1	1	1	1	1
		Wake-Up from Sleep, Idle mode	P	P	P	P	P	P	P	P
0x0B	TC4CR	Bit Name	TC4FF1	TC4FF0	TC4S	TC4CK2	TC4CK1	TC4CK0	TC4M1	TC4M0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT time out	0	0	0	0	0	0	0	0
		Wake-up from Sleep, Idle mode	P	P	P	P	P	P	P	P
0x0C	TC4D	Bit Name	TC4D7	TC4D6	TC4D5	TC4D4	TC4D3	TC4D2	TC4D1	TC4D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT time out	0	0	0	0	0	0	0	0
		Wake-up from Sleep, Idle mode	P	P	P	P	P	P	P	P
0X0D	ISFR0	Bit Name	X	X	INT3F	INT3R	X	X	WDTIF	EXIF0
		Power-on	U	U	0	0	U	U	0	0
		/RESET and WDT time out	U	U	0	0	U	U	0	0
		Wake-up from Sleep, Idle mode	U	U	P	P	U	U	P	P
0X0E	ISFR1	Bit Name	EXIF5	TCIF2	ADIF	X	EXIF3	TCIF4	SPIF	TCIF3
		Power-on	0	0	0	U	0	0	0	0
		/RESET and WDT time out	0	0	0	U	0	0	0	0
		Wake-up from Sleep, Idle mode	U	P	P	U	P	P	P	P
0X0F	ISFR2	Bit Name	X	UERRIF	RBFF	TBEF	TBIF	EXIF1	X	TCIF0
		Power-on	U	0	0	0	0	0	U	0
		/RESET and WDT time out	U	0	0	0	0	0	U	0
		Wake-up from Sleep, Idle mode	U	P	P	P	P	P	U	P

Register Bank 1

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05	TC3CR	Bit Name	TC3CAP	TC3S	TC3CK1	TC3CK0	TC3M	X	X	X
		Power-on	0	0	0	0	0	U	U	U
		/RESET and WDT time out	0	0	0	0	0	U	U	U
		Wake-up from Sleep, Idle mode	P	P	P	P	P	U	U	U
0x06	TC3DA	Bit Name	TC3DA7	TC3DA6	TC3DA5	TC3DA4	TC3DA3	TC3DA2	TC3DA1	TC3DA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT time out	0	0	0	0	0	0	0	0
		Wake-up from Sleep, Idle mode	P	P	P	P	P	P	P	P
0x07	TC3DB	Bit Name	TC3DB7	TC3DB6	TC3DB5	TC3DB4	TC3DB3	TC3DB2	TC3DB1	TC3DB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT time out	0	0	0	0	0	0	0	0
		Wake-up from Sleep, Idle mode	P	P	P	P	P	P	P	P
0x08	TC2CR/ ADDL	Bit Name	ADD1	ADD0	X	TC2M	TC2S	TC2CK2	TC2CK1	TC2CK0
		Power-on	U	U	U	0	0	0	0	0
		/RESET and WDT time out	P	P	U	0	0	0	0	0
		Wake-up from Sleep, Idle mode	P	P	U	P	0	P	P	P
0x09	TC2DH	Bit Name	TC2D15	TC2D14	TC2D13	TC2D12	TC2D11	TC2D10	TC2D9	TC2D8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT time out	0	0	0	0	0	0	0	0
		Wake-up from Sleep, Idle mode	P	P	P	P	P	P	P	P
0x0A	TC2DL	Bit Name	TC2D7	TC2D6	TC2D5	TC2D4	TC2D3	TC2D2	TC2D1	TC2D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT time out	0	0	0	0	0	0	0	0
		Wake-up from Sleep, Idle mode	P	P	P	P	P	P	P	P
0x0B	ADCR	Bit Name	ADREF	ADRUN	ADCK1	ADCK0	ADP	ADIS2	ADIS1	ADIS0
		Power-on	0	0	0	0	1	0	0	0
		/RESET and WDT time out	0	0	0	0	1	0	0	0
		Wake-up from Sleep, Idle mode	P	(*)	P	P	P	P	P	P
0x0C	ADIC	Bit Name	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT time out	0	0	0	0	0	0	0	0
		Wake-up from Sleep, Idle mode	P	P	P	P	P	P	P	P
0X0D	ADDH	Bit Name	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT time out	P	P	P	P	P	P	P	P
		Wake-up from Sleep, Idle mode	P	P	P	P	P	P	P	P
0X0E	TBKTC	Bit Name	TEN	TCK1	TCK0	X	TBTEN	TBTCK2	TBTCK1	TBTCK0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT time out	0	0	0	0	0	0	0	0
		Wake-up from Sleep, Idle mode	0	P	P	P	0	P	P	P

Register Bank 2

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05	URC1	Bit Name	URTD8	UMODE1	UMODE0	BRATE2	BRATE1	BRATE0	UTBE	TXE
		Power-on	U	0	0	0	0	0	0	0
		/RESET and WDT time out	P	P	P	P	P	P	0	0
		Wake-up from Sleep, Idle mode	P	0	P	P	P	P	P	0
0x06	URC2	Bit Name	X	X	SBIM1	SBIM0	UINVEN	X	X	X
		Power-on	U	U	0	0	0	U	U	U
		/RESET and WDT time out	U	U	P	P	P	U	U	U
		Wake-up from Sleep, Idle mode	U	U	P	P	P	U	U	U
0x07	URS	Bit Name	URRD8	EVEN	PRE	PRERR	OVERR	FMERR	URBF	RXE
		Power-on	U	0	0	0	0	0	0	0
		/RESET and WDT time out	P	P	P	0	0	0	0	0
		Wake-up from Sleep, Idle mode	P	P	P	P	P	P	P	0
0x08	URRD	Bit Name	URRD7	URRD6	URRD5	URRD4	URRD3	URRD2	URRD1	URRD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT time out	P	P	P	P	P	P	P	P
		Wake-up from Sleep, Idle mode	P	P	P	P	P	P	P	P
0x09	URTD	Bit Name	URTD 7	URTD 6	URTD 5	URTD 4	URTD 3	URTD 2	URTD 1	URTD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT time out	P	P	P	P	P	P	P	P
		Wake-up from Sleep, Idle mode	P	P	P	P	P	P	P	P

Register Bank 3

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05	SPIC1	Bit Name	SMP	DCOL	BRS2	BRS1	BRS0	EDS	DORD	WBE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT time out	P	P	P	P	P	P	P	0
		Wake-up from Sleep, Idle mode	P	P	P	P	P	P	P	P
0x06	SPIC2	Bit Name	SPIS	X	X	X	X	SPIM1	SPIM0	RBF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT time out	0	0	0	0	0	P	P	0
		Wake-up from Sleep, Idle mode	0	P	P	P	P	P	P	P
0x07	SPID1	Bit Name	SPID17	SPID16	SPID15	SPID14	SPID13	SPID12	SPID11	SPID10
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT time out	P	P	P	P	P	P	P	P
		Wake-up from Sleep, Idle mode	P	P	P	P	P	P	P	P
0x0A	PHC1	Bit Name	X	X	/PHE81	/PHE80	/PHE63	/PHE62	/PHE61	/PHE60
		Power-on	U	U	1	1	1	1	1	1
		/RESET and WDT time out	U	U	1	1	1	1	1	1
		Wake-up from Sleep, Idle mode	U	U	P	P	P	P	P	P
0x0B	PLC2	Bit Name	X	X	/PLE81	/PLE80	/PLE63	/PLE62	/PLE61	/PLE60
		Power-on	U	U	1	1	1	1	1	1
		/RESET and WDT time out	U	U	1	1	1	1	1	1
		Wake-up from Sleep, Idle mode	U	U	P	P	P	P	P	P
0x0C	PHC2	Bit Name	X	X	X	X	/PHE73	/PHE72	/PHE71	/PHE70
		Power-on	U	U	U	U	1	1	1	1
		/RESET and WDT time out	U	U	U	U	1	1	1	1
		Wake-up from Sleep, Idle mode	U	U	U	U	P	P	P	P
0x0D	PLC2	Bit Name	X	X	X	X	/PLE73	/PLE72	/PLE71	/PLE70
		Power-on	U	U	U	U	1	1	1	1
		/RESET and WDT time out	U	U	U	U	1	1	1	1
		Wake-up from Sleep, Idle mode	U	U	U	U	P	P	P	P

General Purpose Registers

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x10 ~ 0x3F	R10 ~ R3F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT time out	P	P	P	P	P	P	P	P
		Wake-up from Sleep, Idle mode	P	P	P	P	P	P	P	P

Legend: **"x"** = not used **"P"** = previous value before reset
"u" = unknown or don't care **"t"** = check Table 7

5.14.4 The Status of RST, T, and P of the Status Register

The values of T and P are used to verify the event that triggered the processor to wake up. Table 7 shows the events that may affect the status of T and P.

Table 7. The Values of RST, T and P after a reset

Reset Type	T	P
Power on	1	1
/RESET during Operation mode	*P	*P
/RESET wake-up during Sleep mode	*P	*P
/RESET wake-up during Idle mode	*P	*P
WDT during Operation mode	0	*P
WDT wake-up during Sleep mode	0	*P
WDT wake-up during Idle mode	0	*P

*P: Previous status before reset

Table 8 The Events that may affect the T and P Status

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-Up during Sleep mode	*P	*P

*P: Previous value before reset

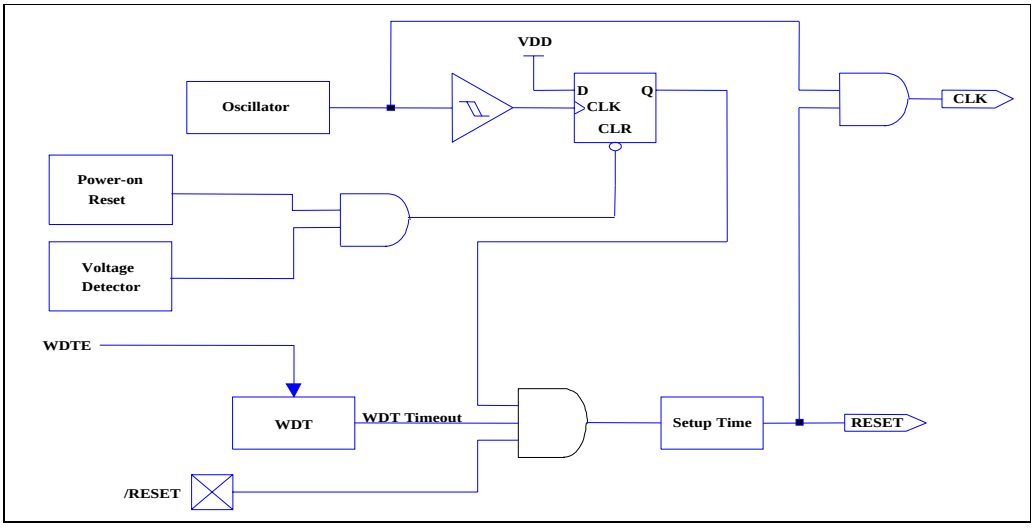


Fig. 5-28 Controller Reset Block Diagram

5.15 Interrupt

The EM78P312N has 15 interrupts (9 external, 6 internal) as listed below:

Table 9 Interrupt Vector

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal / External	Reset	–	–	0000	High 0
Internal	WDT	ENI + WDTEN	WDTIF	0003	1
External	INT0	ENI + INT0EN=1	EXIEF0	0006	2
Internal	TCC	ENI + TCIE0=1	TCIF0	0009	3
External	INT1	ENI + EXIE1=1	EXIF1	000F	4
Internal	TBT	ENI + TBIE=1	TBIF	0012	5
Internal	UART Transmit	ENI + UTIE=1	TBEF	0015	6
Internal	UART Receive	ENI + URIE=1	TBFF	0018	7
Internal	UART Receive error	ENI+UERRIE=1	UERRIF	001B	8
Internal	TC3	ENI + TCIE3=1	TCIF3	0021	9
Internal	SPI	ENI + SPIE=1	SPIF	0024	10
Internal	TC4	ENI + TCIE4=1	TCIF4	0027	11
External	INT3	ENI + EXIE3=1	EXIF3	002A	12
Internal	AD	ENI + ADIE=1	ADIF	0030	13
Internal	TC2	ENI + TCIE2=1	TCIF2	0033	14
External	INT5	ENI + EXIE5=1	EXIF5	0036	Low 15

ISFR0, ISFR1 and ISFR2 are the interrupt status registers that record the interrupt requests in the relative flags/bits. IMR1 and IMR2 are the interrupt mask registers. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (enabled) occurs, the next instruction will be fetched from individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (ISFR 2) is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

5.16 Oscillator

5.16.1 Oscillator Modes

The EM78P312N can operate in two different oscillator modes, i.e., Crystal oscillator mode and External RC oscillator mode (ERC) oscillator mode. User can select which mode by Code Option Register. The maximum limit for operational frequencies of the crystal/resonator under different VDDs is listed below.

Table 10 Oscillator Modes Defined by SDCS and OSC

Mode	OSC	Oscillator
Single Clock	1	High frequency oscillator
	0	ERC

Table 11 The Summary of Maximum Operating Speeds

Condition	VDD	Max. Fxt. (MHz)
High frequency oscillator	3.0	4.0
	5.0	10.0

5.16.2 Crystal Oscillator/Ceramic Resonators (Crystal)

EM78P312N has a clock generator. i.e. fc (high frequency) which can be driven by an external clock signal through the OSCI pin.

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Table 12 provides the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to its specification for appropriate values of C1 and C2. A serial resistor Rs may be necessary for AT strip cut crystal.

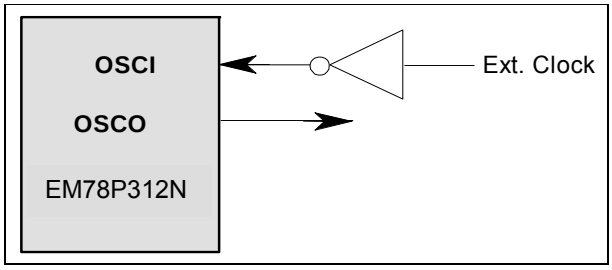


Fig. 5-29 Crystal/Resonator Circuit

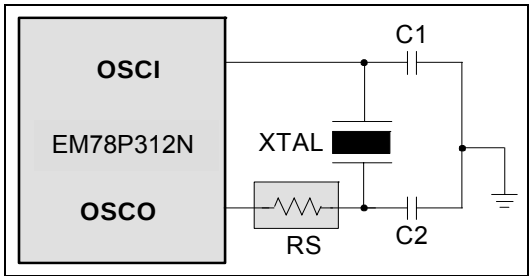


Fig. 5-30 Crystal/Resonator Circuit

Table12. Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonator	HXT	2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	HXT	1.0 MHz	15~30	15~30
		2.0 MHz	15	15
		4.0 MHz	15	15

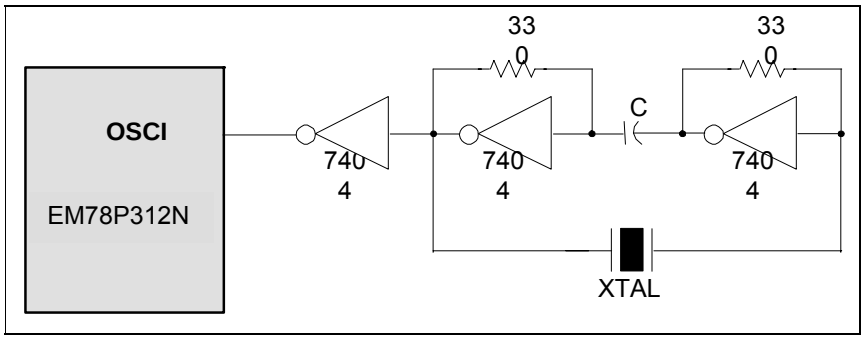


Fig. 5-31 Crystal/Resonator-Series Mode Circuit

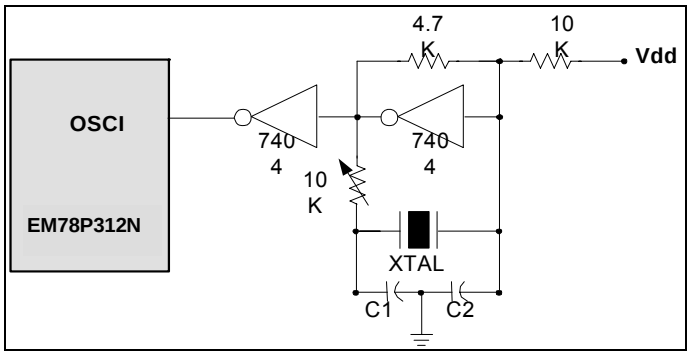


Fig. 5-32 Crystal/Resonator-Parallel Mode Circuit

5.16.3 External RC Oscillator Mode

For applications that do not need very precise timing calculation, the RC oscillator offers a lot of cost savings. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also varies slightly from one chip to another due to the manufacturing process variation.

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and the value of Rext should not be greater than 1 MΩ, otherwise, the frequency is easily affected by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator becomes unstable because the NMOS cannot correctly discharge the current of the capacitance.

Hence, it must be noted that the supply voltage, the operation temperature, the RC oscillator components, the package types, and the PCB layout, will affect the system frequency.

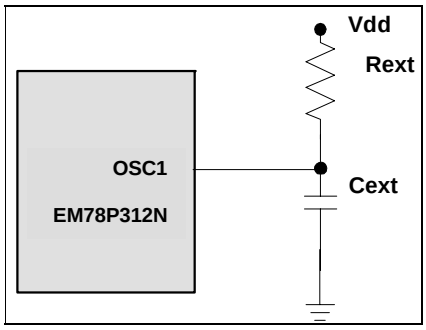


Fig. 5-33 External RC Oscillator Mode Circuit

Table13. RC Oscillator Frequencies

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 pF	3.3k	4.32 MHz	3.56 MHz
	5.1k	2.83 MHz	2.8 MHz
	10k	1.62 MHz	1.57 MHz
	100k	184kHz	187kHz
100 pF	3.3k	1.39 MHz	1.35 MHz
	5.1k	950kHz	930kHz
	10k	500kHz	490kHz
	100k	54kHz	55kHz
300 pF	3.3k	580kHz	550kHz
	5.1k	390kHz	380kHz
	10k	200kHz	200kHz
	100k	21kHz	21kHz

Note: [1]: Measured based on DIP packages.

[2]: The values are for design reference only.

5.17 Code Option Register

The EM78P312N has one CODE option word that is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

Code Option Register and Customer ID Register arrangement distribution:

Word 0	Word 1	Word 2
Bit 12~Bit 0	Bit 12~Bit 0	Bit 12~Bit 0

5.17.1 Code Option Register (Word 0)

Word 0									
Bit 12 ~ 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	CLKS	ENWDTB	CYES	-	OSC	HLP	PR2	PR1	PR0

Bit 12 ~ 9 : Not used

Bit 8 (CLKS) : Instruction period option bit

CLKS = "0" : two oscillator periods

CLKS = "1" : four oscillator periods.

Refer to the Instruction Set section.

Bit 7 (ENWDTB) : Watchdog timer enable bit

ENWDTB = "0" : Enable

ENWDTB = "1" : Disable

Bit 6 (CYES) : Cycle selection for JMP, CALL instruction

CYES = "0" : One cycle

CYES = "1" : Two cycles

Bit 4 (OSC) : Oscillator type selection

OSC = "0" : RC type

OSC = "1" : Crystal type

Bit 3 (HLP) : Power selection

HLP = "0" : Low power

HLP = "1" : High power

Bit 2~0 (PR2~PR0) : Protect Bit

PR2~PR0 are write-protect bits, configured as follows:

PR2	PR1	PR0	Protect
Others			Enable
1	1	1	Disable

5.17.2 Customer ID Register

Word 1
Bit 12~Bit 0
XXXXXXXXXXXXX

Word 2
Bit 12~Bit 0
XXXXXXXXXXXXX

Bits 12 ~ 0: Customer's ID code

5.18 Power-on Considerations

Any microcontroller is not guaranteed to start and operate properly before the power supply maintains at its steady state. The EM78P312N has a built-in Power On Voltage Detector (POVD) with a detecting level of 2.1V. It will work well if V_{DD} rises fast enough (10 ms or less). In many critical applications, however, additional components are required to provide solutions on probable power-up problems.

5.18.1 External Power-on Reset Circuit

The circuit shown in Fig. 5-33 use an external RC to produce the reset pulse. The pulse width (time constant) should be kept long enough for V_{DD} to reach minimum operation voltage. This circuit is used when the power supply has slow rise time. Because the current leakage from the /RESET pin is about ±5μA, it is recommended that R should not be greater than 40K. In this way, the /RESET pin voltage is held below 0.2V. The diode (D) acts as a short circuit at the moment of power down. The capacitor C will discharge rapidly and fully. Rin, the current-limited resistor, will prevent high current or ESD (electrostatic discharge) from flowing to pin /RESET.

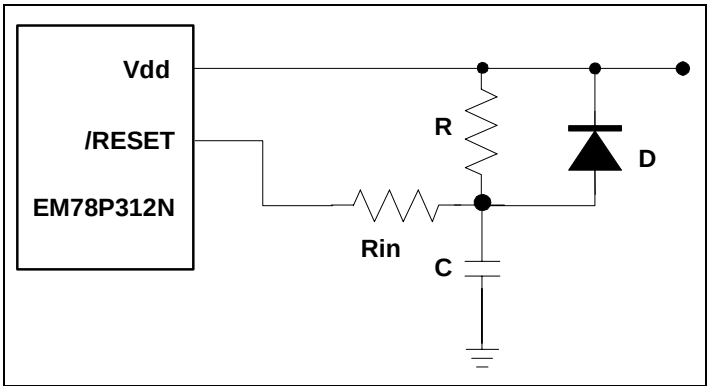


Fig. 5-34 External Power-Up Reset Circuit

5.18.2 Residue-Voltage Protection

When battery is replaced, device power (V_{DD}) is taken off but residue-voltage remains. The residue-voltage may trip below V_{DD} minimum, but not to zero. This condition may cause a poor power-on reset. Fig.35 and Fig. 36 show how to build the residue-voltage protection circuit.

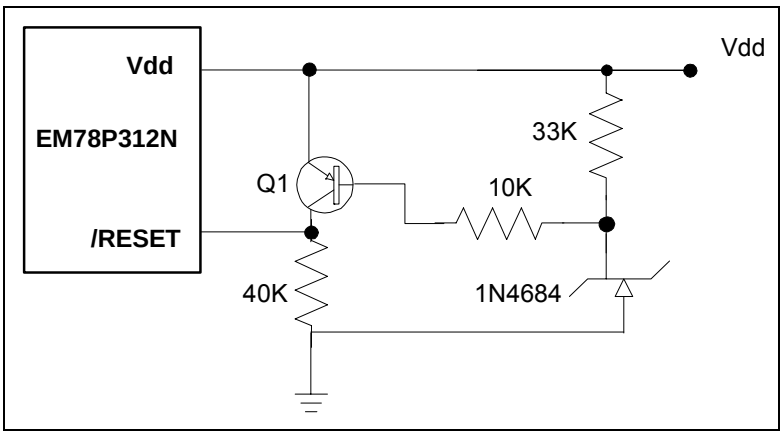


Fig. 5-35 Residue Voltage Protection Circuit 1

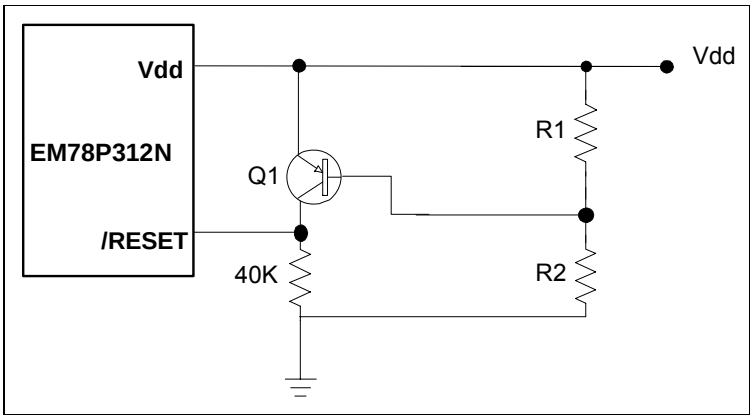


Fig. 5-36 Residue Voltage Protection Circuit 2

5.19 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2", ····). In this case, the execution takes two instruction cycles.

In case the instruction cycle specification is not suitable for certain applications, try to modify the instruction as follows:

(A) Change one instruction cycle to consist of 4 oscillator periods.

(B) The following commands are executed within two instruction cycles; "JMP", "CALL", "RET", "RETL", "RETI", including the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") instructions. In addition, instructions that are written to the program counter are executed within two instruction cycles.

Case (A) is selected by the CODE Option bit, called CLK. One instruction cycle consists of two oscillator clocks if CLK is low, and four oscillator clocks if CLK is high.

Note that once the 4 oscillator periods within one instruction cycle is selected as in Case (A), the internal clock source to TCC should be CLK=Fosc/4, not Fosc/2.

Furthermore, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

Convention:

R = Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None [1]
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None [1]

Binary Instruction				Hex	Mnemonic		Operation	Status Affected
0	0000	01rr	rrrr	00rr	MOV	R, A	A → R	None
0	0000	1000	0000	0080	CLRA		0 → A	Z
0	0000	11rr	rrrr	00rr	CLR	R	0 → R	Z
0	0001	00rr	rrrr	01rr	SUB	A, R	R-A → A	Z,C,DC
0	0001	01rr	rrrr	01rr	SUB	R, A	R-A → R	Z,C,DC
0	0001	10rr	rrrr	01rr	DECA	R	R-1 → A	Z
0	0001	11rr	rrrr	01rr	DEC	R	R-1 → R	Z
0	0010	00rr	rrrr	02rr	OR	A, R	A ∨ R → A	Z
0	0010	01rr	rrrr	02rr	OR	R, A	A ∨ R → R	Z
0	0010	10rr	rrrr	02rr	AND	A, R	A & R → A	Z
0	0010	11rr	rrrr	02rr	AND	R, A	A & R → R	Z
0	0011	00rr	rrrr	03rr	XOR	A, R	A ⊕ R → A	Z
0	0011	01rr	rrrr	03rr	XOR	R, A	A ⊕ R → R	Z
0	0011	10rr	rrrr	03rr	ADD	A, R	A + R → A	Z,C,DC
0	0011	11rr	rrrr	03rr	ADD	R, A	A + R → R	Z,C,DC
0	0100	00rr	rrrr	04rr	MOV	A, R	R → A	Z
0	0100	01rr	rrrr	04rr	MOV	R, R	R → R	Z
0	0100	10rr	rrrr	04rr	COMA	R	/R → A	Z
0	0100	11rr	rrrr	04rr	COM	R	/R → R	Z
0	0101	00rr	rrrr	05rr	INCA	R	R+1 → A	Z
0	0101	01rr	rrrr	05rr	INC	R	R+1 → R	Z
0	0101	10rr	rrrr	05rr	DJZA	R	R-1 → A, skip if zero	None
0	0101	11rr	rrrr	05rr	DJZ	R	R-1 → R, skip if zero	None
0	0110	00rr	rrrr	06rr	RRCA	R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0	0110	01rr	rrrr	06rr	RRC	R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0	0110	10rr	rrrr	06rr	RLCA	R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0	0110	11rr	rrrr	06rr	RLC	R	R(n) → R(n+1), R(7) → (C), C → (R(0)	C
0	0111	00rr	rrrr	07rr	SWAPA	R	R(0-3) → (A(4-7), R(4-7) → (A(0-3)	None
0	0111	01rr	rrrr	07rr	SWAP	R	R(0-3) → (R(4-7)	None
0	0111	10rr	rrrr	07rr	JZA	R	R+1 → A, skip if zero	None
0	0111	11rr	rrrr	07rr	JZ	R	R+1 → R, skip if zero	None
0	100b	bbrr	rrrr	0xxx	BC	R, b	0→ (R(b)	None
0	101b	bbrr	rrrr	0xxx	BS	R, b	1→ (R(b)	None
0	110b	bbrr	rrrr	0xxx	JBC	R, b	if R(b)=0, skip	None
0	111b	bbrr	rrrr	0xxx	JBS	R, b	if R(b)=1, skip	None
1	00kk	kkkk	kkkk	1kkk	CALL	k	PC+1 → [SP], (Page, k) → (PC)	None
1	01kk	kkkk	kkkk	1kkk	JMP	k	(Page, k) → (PC)	None
1	1000	kkkk	kkkk	18kk	MOV	A, k	k → A	None
1	1001	kkkk	kkkk	19kk	OR	A, k	A v k → A	Z
1	1010	kkkk	kkkk	1Akk	AND	A, k	A & k → A	Z
1	1011	kkkk	kkkk	1Bkk	XOR	A, k	A ⊕ k → A	Z
1	1100	kkkk	kkkk	1Ckk	RETL	k	k → A, [Top of Stack] → PC	None
1	1101	kkkk	kkkk	1Dkk	SUB	A, k	k-A → A	Z,C,DC
1	1111	kkkk	kkkk	1Fkk	ADD	A, k	k+A → A	Z,C,DC
1	1110	1000	kkkk	1E8k	PAGE	k	K->R5(6:4)	None
1	1110	1001	kkkk	1E9k	BANK	k	K->R4(7:6)	None

Note: [1] This instruction is applicable to IOC6~IOCA, IMR1, IMR2 only.

6 Absolute Maximum Ratings

6.1 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	-0.3V	to	+6.0V
Output voltage	-0.3V	to	+6.0V
Operating Frequency (2clk)	DC	to	10MHz

6.2 Recommended Operating Conditions

Vss = 0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	Fc = 10MHz	4.0	–	5.5	V
		Fc = 4MHz	2.5	–		
Fc	Crystal: VDD 4.5 to 5.5V	Two cycles with two clocks	1	–	10	MHz
	Crystal: VDD 2.5 to 5.5V		1	–	4	

7 Electrical Characteristics

7.1 DC Electrical Characteristics

Ta= 25 °C, VDD= 5.0V ± 5%, VSS= 0V

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
Fc	Crystal: 4.5V to VDD	Two cycles with two clocks		1	–	10	MHz
ERC	ERC: VDD = 5V	R: 5.1KΩ, C: 100 pF		630	900	1170	kHz
VIHRC	Input High Threshold Voltage (Schmitt Trigger)	OSCI in RC mode		2.8	4	4.5	V
IRC1	Sink current	VI from low to high , VI=5V		15.5	22	28.5	mA
VILRC	Input Low Threshold Voltage (Schmitt Trigger)	OSCI in RC mode		1.3	1.8	2.7	V
IRC2	Sink current	VI from high to low , VI=2V		12	17	22	mA
IIL	Input Leakage Current for input pins	VIN = VDD, VSS		-1	0	1	µA
VIH1	Input High Voltage (Schmitt Trigger)	Ports 6, 7, 8, 9		0.7VDD	–	VDD +0.3V	V
VIL1	Input Low Voltage (Schmitt Trigger)	Ports 6, 7, 8, 9,		-0.3V	–	0.3 VDD	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET, TCC, INT		0.7 VDD	–	VDD +0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET, TCC, INT		-0.3V	–	0.3 VDD	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode		0.7VDD	–	VDD+0.3V	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode		-0.3V	–	0.3VDD	V
IOH1	Output High Voltage (Ports 6, 7, 8, 9)	VOH = VDD-0.4V		-3.5	-5	-6.5	mA
IOL1	Output Low Voltage (Port 9)	VOL = VSS+0.4V		3	5	7	mA
IOL2	Output Low Voltage (Ports 6, Port 7, Port 8)	VOL = VSS+0.4V		12	15	20	mA
IPH	Pull-high current	Pull-high active, input pin at VSS		-50	-75	-100	µA
IPL	Pull-Low current	Pull-high active, input pin at VDD		50	75	100	µA
ISB1	Sleep mode Power down current	All input and I/O pins at VDD, output pin floating	WDT disabled	–	0.8	1.5	µA
ISB2	Sleep mode Power down current		WDT enabled	–	6	10	µA
ICC3	Idle mode Operating supply current at two clocks	VDD=5V, /RESET= 'High', Fc=8MHz, CLKS="0", output pin floating, WDT enabled		–	1.1	1.5	mA
ICC4	Normal mode Operating supply current at two clocks			–	3.0	3.5	mA

Note: * Data in the Minimum, Typical, Maximum (“Min”, “Typ”, ”Max”) columns are based on characterization results at 25°C.

Ta= 25 °C, VDD= 3.0V ± 5%, VSS= 0V

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
Fc	Crystal: 2.5V to VDD	Two cyclea with two clocks		1	–	4	MHz
ERC	ERC: VDD = 3V	R: 5.1KΩ, C: 100 pF		600	850	1100	kHz
VIHRC	Input High Threshold Voltage (Schmitt Trigger)	OSCI in RC mode		1.6	2.3	2.8	V
IRC1	Sink current	VI from low to high , VI=5V		7	9.5	12	µA
VILRC	Input Low Threshold Voltage (Schmitt Trigger)	OSCI in RC mode		0.7	1	1.3	V
IRC2	Sink current	VI from high to low , VI=2V		6	8.5	11	µA
IIL	Input Leakage Current for input pins	VIN = VDD, VSS		-1	0	1	µA
VIH1	Input High Voltage (Schmitt Trigger)	Ports 6,7,8,9,A		0.7VDD	–	VDD+0.3V	V
VIL1	Input Low Voltage (Schmitt Trigger)	Ports 6,7,8,9,A		-0.3V	–	0.3VDD	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	/RESET, TCC		0.7 VDD	–	VDD +0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	/RESET, TCC		-0.3V	–	0.3 VDD	V
VIHX1	Clock Input High Voltage	LOSCI, OSCI in crystal mode		0.7 VDD	–	VDD +0.3V	V
VILX1	Clock Input Low Voltage	LOSCI, OSCI in crystal mode		-0.3V	–	0.3 VDD	V
IOH1	Output High Voltage (Ports 6, 7, 8, 9)	VOH = VDD-0.4V		-2	-3.5	-5	mA
IOL1	Output Low Voltage (Port 9)	VOL = VSS+0.4V		2	3.5	5	mA
IOL2	Output Low Voltage (Ports 6,Port7, Port8)	VOL = VSS+0.4V		10	13	16	mA
IPH	Pull-high current	Pull-high active, input pin at VSS		-15	-23	-31	µA
IPL	Pull-low current	Pull-low active, input pin at VDD		15	23	30	µA
ISB1	Sleep mode Power down current	All input and I/O pins at VDD, output pin floating	WDT disabled	–	0.4	0.8	µA
ISB2	Sleep mode Power down current		WDT enabled	–	1.5	3	µA
ICC3	Idle mode Operating supply current at two clocks	VDD=3V, /RESET= 'High', Fc=4MHz, CLKS="0", output pin floating, WDT enabled		–	0.3	0.5	mA
ICC4	Normal mode Operating supply current at two clocks			–	1.1	1.5	mA

Note: * Data in the Minimum, Typical, Maximum (“Min”, “Typ”, ”Max”) columns are based on characterization results at 25°C.

A/D Converter Characteristic (Vdd =2.5V to 5.5V, Vss=0V, Ta = -40 to 85°C)

Symbol		Parameter	Condition	Min.	Typ.	Max.	Unit
VAREF		Analog reference voltage	VAREF - VASS≧2.5V	2.5	–	V_{DD}	V
VASS				Vss	–	Vss	V
VAI		Analog input voltage	–	VASS	–	VAREF	V
IAI1	IV_{DD}	Analog supply current	V_{DD} =VAREF=5.0V, VASS =0.0V (V reference from V_{DD})	750	850	1000	μA
	Ivref			-10	0	+10	μA
IAI2	IV_{DD}	Analog supply current	V_{DD} =VAREF=5.0V, VASS =0.0V (V reference from VREF)	500	600	820	μA
	IVref			200	250	300	μA
RN		Resolution	V_{DD} =VAREF=5.0V, VASS =0.0V	9	10	–	Bits
LN		Linearity error	V_{DD} = 2.5 to 5.5V Ta=25°C	0	±1	±2	LSB
DNL		Differential nonlinear error	V_{DD} = 2.5 to 5.5V Ta=25°C	0	±0.5	±0.9	LSB
FSE		Full scale error	V_{DD} =VAREF=5.0V, VASS =0.0V	±0	±1	±2	LSB
OE		Offset error	V_{DD} =VAREF=5.0V, VASS =0.0V	±0	±0.5	±1	LSB
ZAI		Recommended impedance of analog voltage source	–	0	8	10	KΩ
TAD		A/D clock period	V_{DD} =VAREF=5.0V, VASS =0.0V	4	–	–	μs
TCN		A/D conversion time	V_{DD} =VAREF=5.0V, VASS =0.0V	14	–	14	TAD
ADIV		A/D input voltage range	V_{DD} =VAREF=5.0V, VASS =0.0V	0	–	VAREF	V
ADOV		A/D output voltage swing	V_{DD} =VAREF=5.0V, VASS =0.0V, RL=10KΩ	0	0.2	0.3	V
				4.7	4.8	5	
PSR		Power Supply Rejection	V_{DD} =5.0V±0.5V	±0		±2	LSB

7.2 AC Electrical Characteristic

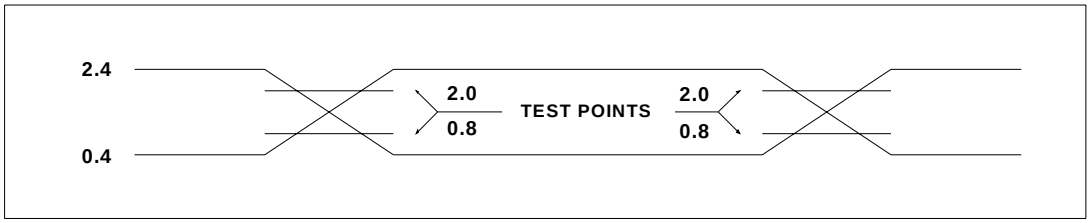
Ta=- 40°C ~ 85 °C, VDD=5V ± 5%, VSS=0V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type (high frequency)	200	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins+20)/ N*	–	–	ns
Tdrh	Device reset hold time	Ta = 25°C	11.3	16.2	21.6	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C	11.3	16.2	21.6	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	Cload=20pF	–	50	–	ns
Tstup1	SDI data setup time	Setup time of SDI data input to SCK↑or SCK↓	–	25	50	ns
Thold1	SDI data hold time	Hold time of SDI data input to SCK↓or SCK↑	–	25	50	ns
Tvalid1	SDO output valid time	SCK↑or SCK↓to SDO data output	–	25	50	ns
Tsckh	SCK input high time	Slave mode (Fmain=8 MHz)	200	–	–	ns
Tsckl	SCK input low time	Slave mode (Fmain=8 MHz)	200	–	–	ns
Tsetup2	Slave mode setup time	/SS↓ to SCK↑or SCK↓(Fmain=8 MHz)	400	–	–	ns
Tdelay1	Slave mode unselect delay time	/SS↑ to SDO output hi-impedance delay time	–	25	50	ns

* N= selected prescaler ratio

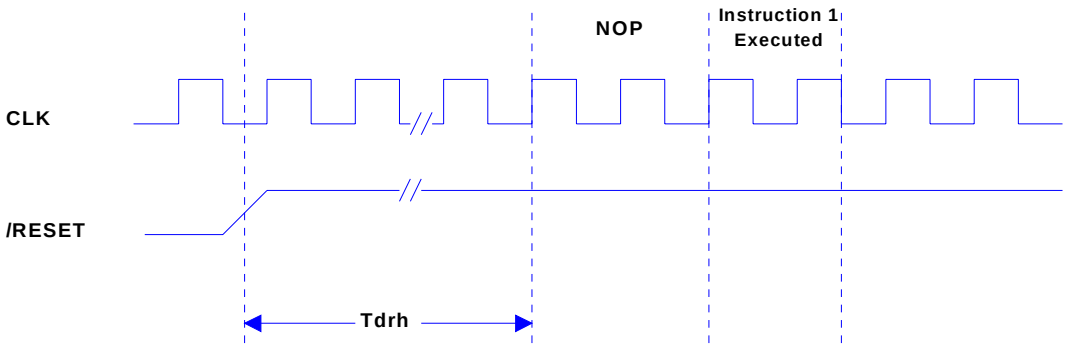
7.3 Timing Diagram

AC Test Input/Output Waveform

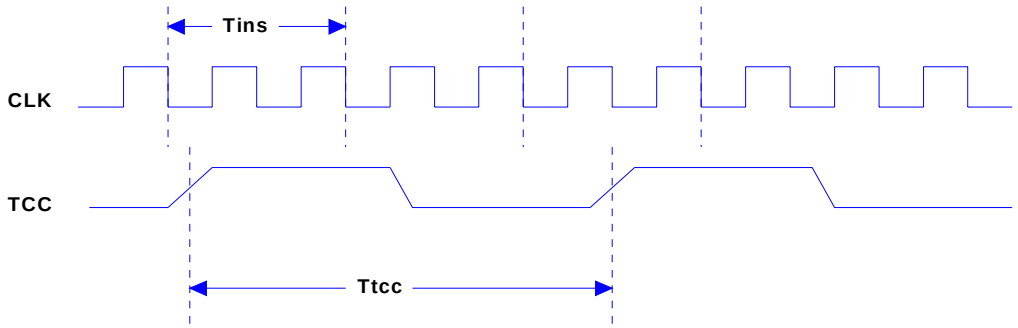


AC Testing : Input is driven at 2.4V for logic "1",and 0.4V for logic "0".Timing measurements are made at 2.0V for logic "1",and 0.8V for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")



APPENDIX

A Package Types:

OTP MCU	Package Type	Pin Count	Package Size
EM78P312NP	DIP	28	600 mil
EM78P312NK	SDIP	28	400 mil
EM78P312NAK	SDIP	28	300 mil
EM78P312NM	SOP	28	300 mil
EM78P312NS	SSOP	28	209 mil

■ Y/S/J：Green product does not contain hazardous substances.

The third edition of Sony SS-00259 standard.

Pb content should be less than 100ppm.

Pb content to fit in with Sony spec.

Part No.	EM78P311SxY	EM78P311SxS/xJ
Electroplate type	Sn/Cu	Pure Tin
Ingredient (%)	Cu:1.0~3.0%	Sn :100%
Melting point(°C)	~227°C	232°C
Electrical resistivity (μΩ-cm)	13	11.4
Hardness (hv)	10~12	8~10
Elongation (%)	40%	>50%