Technical Information Manual

PC 300PL Personal Computer Types 6584 and 6594

> **Note**
>
> Before using this information and the product it supports, be sure to read the general information under Appendix E, "Notices and trademarks" on page 42.

First Edition (October 1999)

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Preface

This *Technical Information Manual* provides information for the IBM® PC 300® Types 6584 and 6594. It is intended for developers who want to provide hardware and software products to operate with these IBM computers and provides an in-depth view of how these IBM computers work. Users of this publication should have an understanding of computer architecture and programming concepts.

Related publications

In addition to this manual, the following IBM publications provide information related to the operation of the IBM PC 300PL Personal Computer:

- *PC 300PL User Guide*
  This publication contains information about configuring, operating, and maintaining the PC 300PL Personal Computer, as well as installing new options in the PC 300PL Personal Computer. Also included are warranty information, instructions for diagnosing and solving problems, and information on how to obtain help and service.

- *Understanding Your Personal Computer*
  This online document includes general information about using computers and detailed information about the features of the PC 300PL Personal Computer.

- *About Your Software*
  This publication (provided only with computers that have IBM-preinstalled software) contains information about the preinstalled software package.

- *Hardware Maintenance Manual*
  This publication contains information for trained service technicians. It is available at http://www.ibm.com/pc/us/cdt/hmm.html on the World Wide Web, and it can also be ordered from IBM. To purchase a copy, see the "Getting Help, Service, and Information" section in *PC 300PL User Guide*.

- *Compatibility Report*
  This publication contains information about compatible hardware and software for the PC 300PL Personal Computer. It is available at http://www.ibm.com/pc/us/cdt on the World Wide Web.

- *Network Administrator's Guide*
  This publication contains information for network administrators who configure and service local area networks (LANs). Look for this publication at http://www.ibm.com/pc/us/cdt on the World Wide Web.

Terminology usage

Attention: The term *reserved* describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

In this manual, some signals are represented in a small, all-capital-letter format (-ACK). A minus sign in front of the signal indicates that the signal is active low. No sign in front of the signal indicates that the signal is active high.

The use of the term *hex* indicates a hexadecimal number.

When numerical modifiers such as K, M, and G are used, they typically indicate powers of 2, not powers of 10. For example, 1 KB equals 1 024 bytes (2^{10}), 1 MB equals 1 048 576 bytes (2^{20}), and 1 GB equals 1 073 741 824 bytes (2^{30}).

When expressing storage capacity, MB equals 1 000 KB (1 024 000). The value is determined by counting the number of sectors and assuming that every two sectors equals 1 KB.

Note: Depending on the operating system and other system requirements, the storage capacity available to the user might vary.

Chapter 1. System overview

PC 300PL Types 6584 and 6594 are computer systems designed to provide state-of-the-art computing power with room for future growth.

Major features

The major features are:

- An Intel® Pentium® III microprocessor with MMX™ technology, streaming single instruction multiple data (SIMD) extensions, and 256 KB L2 cache

- Up to 1 GB of system memory

- Integrated IDE bus master controller, Ultra DMA/66 capable

- EIDE hard disk drive

- System management

    - Wake on LAN® support
    - Desktop Management Interface (DMI) BIOS and DMI software
    - Integrated network protocols
    - Enablement for remote administration
    - Wake on Ring support

- IDE CD-ROM[1] drive, standard on some models

- Asset security

    - Security settings provided by the Configuration/Setup Utility program
        - Power-on and administrator password protection
        - Startup sequence control
        - Hard disk drive and diskette drive access control
        - I/O port control
    - Cover key lock
    - U-bolt and security cabling (optional)
    - Operating system security
    - Diskette write-protection
    - Alert on LAN® support
    - Tamper-detection switch on the chassis

- Accelerated graphics port (AGP) adapter

- Integrated 16-bit stereo audio controller and built-in high-quality speaker in some models (supports SoundBlaster, Adlib, and Microsoft® Windows® Sound System applications)

- Networking

    - IBM 10/100 megabits-per-second (Mbps) PCI Ethernet adapter with Wake on LAN support in some models
    - IBM PCI token ring adapter with Wake on LAN support (optional)

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[1] Variable read rate. Actual playback speed will vary and is often less than the maximum possible.

- Expansion
  Desktop

  - Four drive bays
  - Four PCI expansion slots

  Tower

  - Six drive bays
  - Six PCI expansion slots

- PCI I/O bus compatibility

- EnergyStar compliance (some models only)

- 3.5-inch, 1.44 MB diskette drive

- Input/output features

  - One 25-pin, parallel port with Extended Capabilities Port (ECP)/Extended Parallel Port (EPP) support

  - Two 9-pin, universal asynchronous receiver/transmitter (UART) serial ports

  - Two 4-pin, Universal Serial Bus ports

  - One 6-pin, keyboard port (Windows 95 compatible)

  - One 6-pin, mouse port

  - One 15-pin, DDC2B-compliant monitor port on the AGP adapter

  - Three 3.5-mm audio jacks (line out/headphone, line in, microphone)

Other features

The PC 300PL Personal Computer supports the following features:

Network support

PC 300PL Personal Computer computers are enabled to support management over a network. The following is a list of supported functions:

- Selectable startup sequence
- Selectable automatic power on startup sequence
- POST/BIOS update from network
- Wake on LAN feature
- CMOS Save/Restore utility program
- CMOS setup over LAN
- Wake on Ring

Wake on LAN

The power supply of the computer supports the Wake on LAN feature. With the Wake on LAN feature, the computer can be turned on when a specific LAN frame is passed to the computer over the LAN.

To use the Wake on LAN feature, the computer must be equipped with a network adapter that supports Wake on LAN. Some models come with a network adapter that supports Wake on LAN. You can find the menu for setting the Wake on LAN feature in the Configuration/Setup Utility program.

Wake on Ring

All models can be configured to turn on the computer after a ring is detected from an external or internal modem. The menu for setting the Wake on Ring feature is in the Configuration/Setup Utility program. Two options control this feature:

- **Serial Ring Detect:** Use this option if the computer has an external modem connected to the serial port.

- **Modem Ring Detect:** Use this option if the computer has an internal modem.

Chapter 2. System board features

This section includes information about system board features. For an illustration of the system board, see "System board, Types 6584 and 6594" on page 13.

Pentium III microprocessor with MMX technology

PC 300PL Types 6584 and 6594 come with an Intel Pentium III microprocessor. The microprocessor, which has an attached heat sink, plugs directly into a connector on the system board.

Features

The features of this microprocessor are as follows:

- Optimization for 32-bit software
- 64-bit microprocessor data bus
- 133 MHz front side bus (FSB)
- 256 KB L2 cache integrated into the microprocessor
- 32-bit microprocessor address bus
- Math coprocessor
- MMX technology, which boosts the processing of graphic, video, and audio data
- Cache speed is half of processor core speed
  - 4-way set associative
  - Nonblocking

L2 cache

The Pentium III microprocessor provides 256 KB L2 cache. The L2 cache ECC function is automatically enabled if ECC memory is installed. If non-ECC memory is installed, the L2 cache ECC is disabled. (For information on overriding the ECC memory settings, see the chapter about the Configuration/Setup Utility program, in *PC 300PL User Guide*.) More information on this microprocessor is available at http://www.intel.com on the World Wide Web.

Chip set control

The Intel 820 chip set is the interface between the microprocessor and the following:

- Memory subsystem
- PCI bus
- IDE bus master connection
- High-performance, PCI-to-ISA bridge
- USB ports
- SMBus
- Enhanced DMA controller
- Real-time clock (RTC)

System memory

The system memory interface is controlled by the Intel 820 chip set. Rambus dynamic random access memory (RDRAM) is standard.

The maximum amount of addressable system memory is 1 GB. For memory expansion, the system board provides two Rambus inline memory module (RIMM) connectors. The system board also supports PC700 memory and PC800 memory RIMMs in sizes of 64 MB, 128 MB, 256 MB, and 512 MB. The amount of memory that is preinstalled varies by model.

The following information applies to system memory:

- ECC or non-ECC RDRAM is standard.

- The maximum height of memory modules is 6.35 cm (2.5 in.).

- Each memory connector supports a maximum of 512 MB of memory, when available.

- Install only ECC RIMMS to enable ECC. If you use ECC and non-ECC memory together, all installed memory will function as non-ECC memory.

- RIMM connectors do not support dual inline memory modules (DIMMs).

- Any connector that does not have a RIMM installed must have a *continuity RIMM* (C-RIMM), a module that looks like a RIMM but has no memory on it. A continuity RIMM is used to continue the connection on a RIMM connector that does not have memory installed in it.

- Use PC700 or PC800 RIMMs only.

- Maximum system memory can be auto-detected and auto-configured using serial presence detect and configuration interface (BIOS specific).

The following table shows the possible configuration of RIMMs and continuity RIMMs that can be used in the PC 300PL Personal Computer.

Figure 1. Memory configurations for 133 MHz FSB		
RIMM 1	**RIMM 2**	**Functions as**
PC700	PC700	PC700
PC700	PC800	PC700
PC700	C-RIMM	PC700
PC800	PC800	PC800
PC800	C-RIMM	PC800
C-RIMM	C-RIMM	Invalid
Any RIMM	No RIMM	Invalid
No RIMM	No RIMM	Invalid
No RIMM	C-RIMM	Invalid

For information on the pin assignments for the memory-module connectors, see "Memory connectors" on page 26.

PCI bus

The fully synchronous 33 MHz PCI bus originates in the chip set. Features of the PCI bus are:

- Integrated arbiter with multitransaction PCI arbitration acceleration hooks
- Zero-wait-state, microprocessor-to-PCI write interface for high-performance graphics
- Built-in PCI bus arbiter with support for up to five masters
- Microprocessor-to-PCI memory write posting with 5-Dword-deep buffers
- Conversion of back-to-back sequential microprocessor-to-PCI memory write to PCI burst write
- PCI-to-DRAM posting 18 Dwords
- PCI-to-DRAM up to 100+ MB/sec bandwidth
- Multitransaction timer to support multiple short PCI transactions within one PCI ARB cycle
- PCI 2.2 compliant
- Delayed transaction
- PCI parity checking and generation support

IDE bus master interface

The system board incorporates a PCI-to-IDE interface that complies with the *AT Attachment Interface with Extensions*.

The bus master for the IDE interface is integrated into the I/O hub of the Intel 820 chip set. The chip set is PCI 2.2 compliant. It connects directly to the PCI bus and is designed to allow concurrent operations on the PCI bus and IDE bus. The chip set is capable of supporting PIO mode 0–4 devices and IDE DMA mode 0–3 devices, ATA 66 transfers up to 66 megabytes per second (MBps).

The IDE devices receive their power through a four-position power cable containing +5, +12, and ground voltage. When devices are added to the IDE interface, one device is designated as the master device and another is designated as the slave or subordinate device. These designations are determined by switches or jumpers on each device. There are two IDE ports, one designated Primary and the other Secondary, allowing for up to four devices to be attached. The total number of physical IDE devices is determined by the mechanical package.

For the IDE interface, no resource assignments are given in the system memory or the direct memory access (DMA) channels. For information on the resource assignments, see "Input/output address map" on page 36 and Figure 38 on page 40 (for IRQ assignments).

Two connectors are provided on the riser card for the IDE interface. For information on the connector pin assignments, see "IDE connectors" on page 30.

USB interface

Universal Serial Bus (USB) technology is a standard feature of the computer. The system board provides the USB interface with two connectors integrated into the ICH1 (I/O hub) in the chip set. A USB-enabled device can attach to a connector, and if that device is a hub, multiple peripheral devices can attach to the hub and be used by the system. The USB connectors use Plug and Play technology for installed devices. The speed of the USB is up to 12 MB/sec with a maximum of 127 peripheral devices. The USB is compliant with Universal Host Controller Interface Guide 1.0.

Features provided by USB technology include:

- Support for hot-pluggable devices
- Support for concurrent operation of multiple devices
- Suitability for different device bandwidths
- Support for up to five meters length from host to hub or from hub to hub
- Guaranteed bandwidth and low latencies appropriate for specific devices
- Wide range of packet sizes
- Limited power to hubs

For information on the connector pin assignments for the USB interface, see "USB port connectors" on page 33.

Low pin count bus

The low pin count (LPC) bus allows a connection of the ISA and X-Bus devices such as Super I/O. The PC 300PL Personal Computer uses the National Semiconductor PC87360 Super I/O chip. The PC87360 chip includes the following:

- Floppy disk controller
- Keyboard and mouse controller
- IEEE 1284 parallel port
- Two UART serial ports
- Wake on LAN support
- General purpose input/output (GPIO) ports
- PC98 compliance
- ACPI compliance

Diskette write protection can be enabled or disabled by a programmable setting in the LPC I/O. This setting is accessible through the Configuration/Setup Utility program.

Video subsystem

The PC 300PL Personal Computer comes with one of the following graphics solutions:

- NumberNine S3 Savage4 Accelerated Graphics Port (AGP) 2X adapter with 8 MB 110 MHz SDRAM and a 15-pin SVGA connector

- NumberNine S3 Savage4 Extreme AGP 4X adapter, with 16 MB 166 MHz SDRAM and a converter for a 15-pin VGA displays

The Savage4 graphics accelerator supports the following features:

- 128-bit 2D graphics engine
- High-performance 2D/3D video accelerator
- 3D rendering
- Motion video architecture
- High-speed memory bus
- Flat panel desktop monitor support
- Full software support
- ACPI and PCI power management
- PCI 2.2 bus support, including bus mastering
- 300 MHz RAMDAC with gamma correction
- I2C serial bus and flash ROM support
- 2.5 V core with 3.3V/5V tolerant I/O
- Hardware and BIOS support for VESA timings and DDC monitor communications

Chapter 2. System board features

The video subsystem supports all video graphics array (VGA) modes and is compliant with super video graphics array (SVGA) modes and Video Electronics Standards Association (VESA) 1.2. Some enhanced features include:

- Video subsystem on a chip, including 2D, 3D, and a video port
- 66 MHz AGP system bus interface with 2X or 4X mode
- Sideband signaling (some models only)
- Command list bus mastering support for fast 2D performance
- 64-bit, 125 MHz SDRAM or 166 MHz SGRAM interface
- Plug and Play support
- Advanced Power Management support
- Color space conversion
- Hardware scaling

The integrated graphics memory controller subsystem supports the VESA Display Data Channel (DDC) standard 1.1 and uses DDC1 and DDC2B to determine optimal values during automatic monitor detection.

The video subsystem has the following resource assignments:

Figure 2. Video subsystem resources	
Resource	**Assignment**
ROM	Hex C0000–C7FFF (32KB)
RAM	Hex A0000–BFFFF
I/O (hex)	VGA registers: Attributes 0–14, CRT controller 0–18/22/24/26, CRTC Extension 0-6, DACSTAT, FEAT, GCTL 0-8, INSTS0-1, MISC, Sequencer 0-4, DAC
IRQ	PCI interrupt 1 (automatically assigned to IRQ 0BH by POST or can be disabled in the Configuration/Setup Utility)
DMA	None

For further information on resource assignments, see Appendix B, "System address maps" on page 36 and Appendix C, "IRQ and DMA channel assignments" on page 40.

The PC 300PL Personal Computer supports the following video subsystem modes:

Figure 3. Supported VGA video modes							
Mode (hex)	Display mode	Screen resolution	Colors	Buffer start (hex)	Dot clock (MHz)	Sweep rate (kHz)	Refresh rate (Hz)
00	Text	40 x 25 characters	2	B8000	28.322	31.5	70
01	Text	40 x 25 characters	16	B8000	28.322	31.5	70
02	Text	80 x 25 characters	B/W	B8000	28.322	31.5	70
03	Text	80 x 25 characters	16	B8000	28.322	31.5	70
04	Graphics	320 x 200 pixels	4	B8000	25.175	31.5	70
05	Graphics	320 x 200 pixels	4	B8000	25.175	31.5	70
06	Text	640 x 200 pixels	2	B8000	25.175	31.5	70
07	Text	80 x 25 characters	Mono	B0000	28.322	31.5	70
0D	Graphics	320 x 200 pixels	16	A0000	25.175	31.5	70
0E	Graphics	640 x 200 pixels	16	A0000	25.175	31.5	70
0F	Graphics	640 x 350 pixels	Mono	A0000	25.175	31.5	70
10	Graphics	640 x 350 pixels	16	A0000	25.175	31.5	70
11	Graphics	640 x 480 pixels	2	A0000	25.175	31.5	60
12	Graphics	640 x 480 pixels	16	A0000	25.175	31.5	60
13	Graphics	320 x 200 pixels	256	A0000	25.175	31.5	70

Monitor support

The video subsystem provides a 15-pin monitor connector on the system board. For information on connector pin assignments, see Appendix A, "Connector pin assignments" on page 25.

Video memory

The video memory interface is controlled by an integrated graphics subsystem on the AGP adapter with up to 16 MB video RAM for 2D/3D graphics.

Audio subsystem

The PC 300PL Personal Computer comes with an integrated audio controller. These models are capable of playing and recording sounds and support SoundBlaster, Adlib, and Microsoft Windows Sound System applications.

The device drivers for the preinstalled audio adapter are on the hard disk. The device drivers are also available on the *Product Recovery CD* or *Device Driver and IBM Enhanced Diagnostics CD* that comes with the computer.

If you connect an optional device to the audio adapter, follow the instructions provided by the manufacturer. (Note that device drivers might be required. If necessary, contact the manufacturer for information on these device drivers.)

The following connectors are available on the integrated audio controller:

- *Line/headphone out* port for connecting powered speakers. To hear audio from the adapter you must connect a set of speakers to the Line out port. These speakers must be powered with a built-in amplifier. In general, any powered speakers designed for use with personal computers can be used with the audio subsystem. These speakers are available with a wide range of features and power outputs.

- *Line in* port for connecting musical devices, such as a portable CD player or stereo system.

* *Microphone* for connecting a microphone.

Super input/output controller

Control of the integrated input/output (I/O) and diskette drive controllers is provided by a single module. This module, which supports Plug and Play, controls the following features:

* Diskette drive interface
* Serial port
* Parallel port
* Keyboard and mouse ports
* General-purpose I/O ports

Diskette drive interface

The PC 300PL Personal Computer has four drive bays for installing internal devices. The following is a list of devices that the diskette drive subsystem supports:

* 1.44 MB, 3.5-inch diskette drive
* 1.44 MB, 3.5-inch, 3-mode drive for Japan (no BIOS support for 3-mode drive)
* 1.2 MB, 5.25-inch diskette drive
* 1 Mbps, 500-Kbps, or 250 Kbps internal tape drive

One connector is provided on the system board for diskette drive support. For information on the connector pin assignments, see "Diskette drive connector" on page 31.

Serial ports

Two universal asynchronous receiver/transmitter (UART) serial ports are integrated into the system board. The serial ports include 16-byte data, first-in first-out (FIFO) buffers and have programmable baud rate generators. The serial ports are NS16450 and PC16550A compatible.

For information on the connector pin assignments, see "Serial port connector" on page 34.

Note: Current loop interface is not supported.

The following figure shows the serial port assignments in the configuration.

Figure 4. Serial port assignments		
Port assignment	**Address range (hex)**	**IRQ level**
Serial 1	03F8–03FF	IRQ4
Serial 2	02F8–02FF	IRQ3
Serial 3	03E8–03FF	IRQ4
Serial 4	02E8–02FF	IRQ3

The default setting for the serial port is COM1.

Parallel port

Integrated in the system board is support for extended capabilities port (ECP), enhanced parallel port (EPP), and standard parallel port (SPP) modes. The modes of operation are selected through the Configuration/Setup Utility program with the default mode set to SPP. The ECP and EPP modes are compliant with IEEE 1284.

The following figure shows the parallel port assignments used in the configuration.

Figure 5. Parallel port assignments		
Port assignment	**Address range (hex)**	**IRQ level**
Parallel 1	03BC–03BE	IRQ7
Parallel 2	0378–037F	IRQ5
Parallel 3	0278–027F	IRQ5

The default setting for the parallel port is Parallel 1.

The system board has one connector for the parallel port. For information on the connector pin assignments, see "Parallel port connector" on page 34.

Keyboard and mouse ports

The keyboard and mouse subsystem is controlled by a general purpose 8-bit microcontroller; it is compatible with 8042AH. The controller consists of 256 bytes of data memory and 2 KB of read-only memory (ROM).

The controller has two logical devices: one controls the keyboard and the other controls the mouse. The keyboard has two fixed I/O addresses and a fixed IRQ line and can operate without the mouse. The mouse cannot operate without the keyboard because, although it has a fixed IRQ line, the mouse relies on the addresses of the keyboard for operation. For the keyboard and mouse interfaces, no resource assignments are given in the system memory addresses or DMA channels. For information on the resource assignments, see "Input/output address map" on page 36 and Figure 38 on page 40 (for IRQ assignments).

The system board has one connector for the keyboard port and one connector for the mouse port. For information on the connector pin assignments, see "Mouse and keyboard port connectors" on page 33.

Network connection

Some PC 300PL Personal Computer models are equipped with an Ethernet adapter and some are equipped with a token ring adapter that supports the Wake on LAN feature.

Features of the Ethernet adapter are:

- Operates in shared 10BASE-T or 100BASE-TX environment
- Transmits and receives data at 10 Mbps or 100 Mbps
- Has a RJ-45 connector for LAN attachment
- Operates in symmetrical multiprocessing (SMP) environments
- Supports Wake on LAN
- Supports Alert on LAN
- Supports Remote Program Load (RPL) and Dynamic Host Configuration Protocol (DHCP)

Features of the token-ring adapter are:

- Transmits and receives data at 4 Mbps or 16 Mbps
- Has a RJ-45 and D-shell connectors for LAN attachment
- Supports Wake on LAN
- Supports Alert on LAN
- Supports Remote Program Load (RPL) and Dynamic Host Configuration Protocol (DHCP)

Real-time clock and CMOS

The real-time clock is a low-power clock that provides a time-of-day clock and a calendar. The clock settings are maintained by an external battery source of 3 V dc.

The system uses 242 bytes of complementary metal-oxide semiconductor (CMOS) memory to store data. The CMOS memory is erased if the jumper on the system board is moved.

To locate the battery, see "System board, Types 6584 and 6594" on page 13.

Flash EEPROM

The system board uses 4 Megabits (Mb) of flash electrically erasable, programmable, read-only memory (EEPROM) to store the basic input/output system (BIOS), video BIOS, IBM logo, Configuration/Setup Utility, and Plug and Play data.

If necessary, the EEPROM can be easily updated using a stand-alone utility program that is available on a 3.5-inch diskette.

Expansion adapters

Each PCI-expansion connector is a 32-bit slot. PCI-expansion connectors support the 32-bit 5 V dc, local-bus signalling environment that is defined in *PCI Local Bus Specification 2.1*.

The PC 300PL Personal Computer has four PCI slots to support the addition of adapters. For information on installing adapters, see *PC 300PL User Guide*.

For information on the connector pin assignments, see "PCI connectors" on page 27.

Physical layout

The system board might look slightly different from the one shown.

Note: A diagram of the system board, including switch and jumper settings, is attached to the underside of the computer cover.

System board, Types 6584 and 6594

1 Microprocessor
2 RIMM connector 1
3 RIMM connector 2
4 AGP slot
5 Recovery jumper
6 Battery
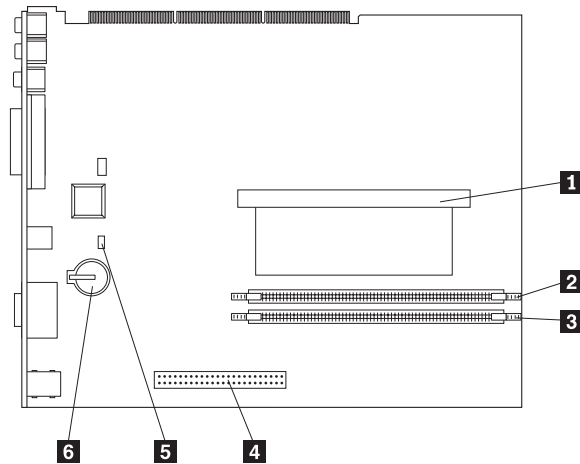
Riser card layouts

The PC 300PL Personal Computer uses a riser card for expansion. The riser card contains expansion slots that connect the adapters to the peripheral component interconnect (PCI) and industry standard architecture (ISA) buses and connectors for the integrated drive electronics (IDE) drives and diskette drives. The following illustrations show the expansion slots on the riser card. The PCI slots are on the front of the riser card, and the power and IDE drive connectors are on the back of the riser card.

PC 300PL — desktop model

Some desktop models have a riser card with four PCI connector slots. The following illustration shows the location of the slots on the PCI riser card.

1 SCSI LED connector
2 Wake on LAN connector
3 Power connector (back)
4 Primary IDE connector (back)
5 Secondary IDE connector (back)
6 Diskette drive connector
7 Fan connector
8 Tamper detector connector
9 Speaker connector
10 RFID connector
11 Power LEDs
12 Alert on LAN connector
13 212-pin connector
14 CD audio connector
15 PCI slot 1
16 PCI slot 2
17 PCI slot 3
18 PCI slot 4
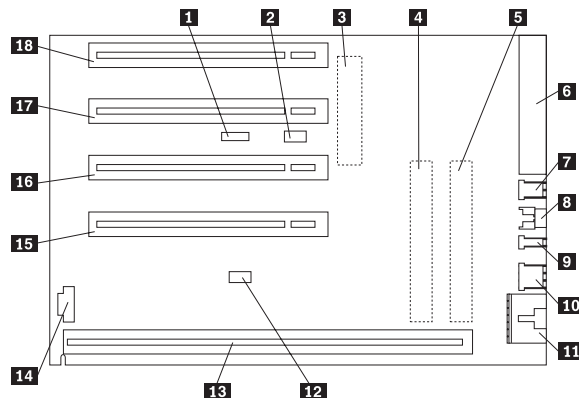
Chapter 2. System board features

Some desktop models have a riser card with two PCI slots, one ISA slot, and one shared PCI/ISA slot. The following illustration shows the location of the slot on the PCI/ISA riser card.

1 PCI slot 3
2 PCI slot 2
3 Alert on LAN connector
4 SCSI LED connector
5 Wake on LAN connector
6 FDD connector
7 Fan connector
8 Tamper detector connector
9 Speaker connector
10 RFID connector
11 Power LEDs
12 ISA slot
13 ISA slot
14 System board connector
15 PCI slot 1
16 CD audio connector
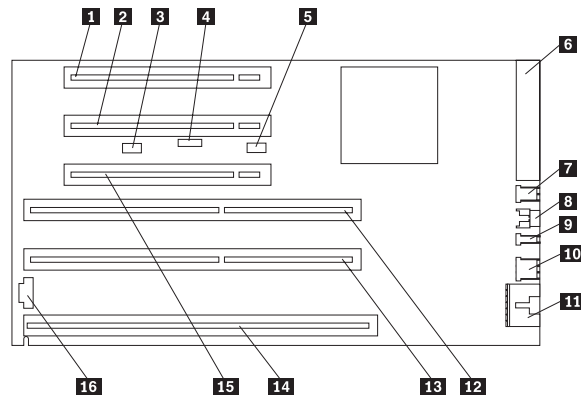
PC 300PL — tower model

The following illustration shows the riser card on the tower model.

1 PCI slots 1-5, lowest to highest
2 Diskette drive connector
3 Hard disk fan 1 connector
4 Hard disk fan 2 connector
5 Front fan connector
6 Wake on LAN connector
7 RFID connector
8 Speaker connector
9 Tamper detector connector
10 SCSI LED connector
11 IDE secondary connector
12 IDE primary connector
13 Power connector
14 Alert on LAN connector
15 212-pin system board connector
16 CD audio connector
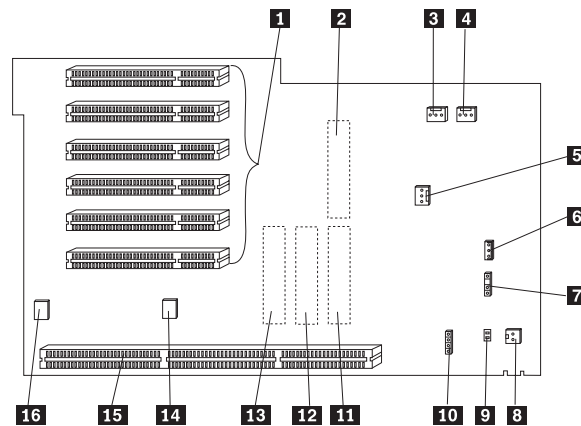
Recovery jumper

The recovery jumper on the system board is used for custom configurations. For the location of the recovery jumper, see the "System board, Types 6584 and 6594" on page 13.

Figure 6. Recovery jumper	
Pins	**Description**
1 and 2	Normal (factory default)
2 and 3	Clear CMOS/password, boot block recovery

Cable connectors

Connections for attaching devices are provided on the back of the computer. The connectors are:

- USB (2)
- Mouse
- Keyboard
- Serial (2)
- Parallel
- Monitor (SVGA or DVI)
- Audio connectors for line in, line/headphone out, and microphone

Connector panel

Each connector for a features that is integrated into the system board can be identified by an icon directly below the connector. A connectors provided by an adapter might not have an identifying icon.

For pin-out details on connectors, see Appendix A, "Connector pin assignments" on page 25.

The following illustration shows the connector panel for the tower model:

1 USB connector 2
2 Serial connector 2
3 Mouse connector
4 SVGA monitor connector
5 DVI monitor connector
6 Keyboard connector
7 Serial connector 1
8 USB connector 1
9 Parallel connector
10 Microphone connector
11 Line in connector
12 Line/headphone out connector
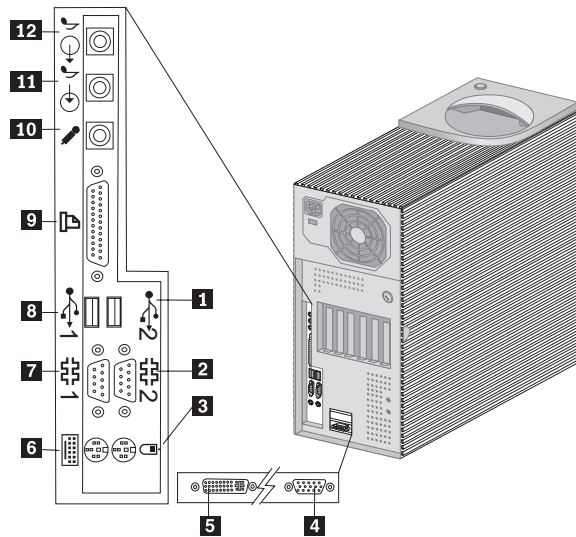
The following illustration shows the connector panel for the desktop model:

1 USB connector 2
2 Serial connector 2
3 SVGA monitor connector
4 DVI monitor connector
5 Mouse connector
6 Keyboard connector
7 Serial connector 1
8 USB connector 1
9 Parallel connector
10 Microphone connector
11 Line in connector
12 Line/headphone out connector
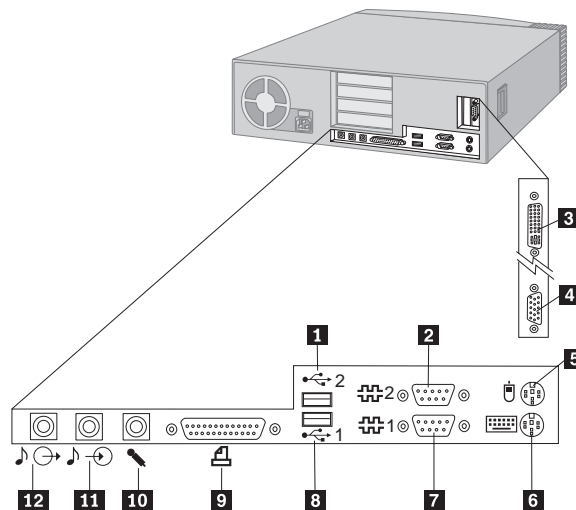
Chapter 3. Physical specifications

This section lists the physical specifications for the PC 300PL Types 6584 and 6594. The PC 300PL Personal Computer desktop model has four expansion slots and four drive bays. The PC 300PL Personal Computer tower model has six expansion slots and six drive bays.

Note: This computer is classified as a Class B digital device. However, this computer includes a built-in network interface controller (NIC) and is considered a Class A digital device when the NIC is in use. The Class A digital device rating and compliance notice are primarily because the inclusion of certain Class A options or Class A NIC cables changes the overall rating of the computer to Class A.

PC 300PL — desktop

Dimensions

- Height: 134 mm (5.3 in.)
- Width: 447 mm (17.6 in.)
- Depth: 450 mm (17.7 in.)

Weight

- Minimum configuration as shipped: 10.0 kg (22 lb)
- Maximum configuration: 11.4 kg (25 lb)

Environment

- Air temperature:
  - System on: 10° to 35°C (50° to 95°F)
  - System off: 10° to 43°C (50° to 110°F)
  - Maximum altitude: 2134 m (7000 ft)

  Note: The maximum altitude, 2133.6 m (7000 ft.), is the maximum altitude at which the specified air temperatures apply. At higher altitudes, the maximum air temperatures are lower than those specified.

- Humidity:
  - System on: 8% to 80%
  - System off: 8% to 80%

Electrical input

- Input voltage:
  - Low range:
    - Minimum: 90 V ac
    - Maximum: 137 V ac
    - Input frequency range: 57–63 Hz
    - Voltage switch setting: 115 V ac
  - High range:
    - Minimum: 180 V ac
    - Maximum: 265 V ac
    - Input frequency range: 47–53 Hz
    - Voltage switch setting: 230 V ac
  - Input kilovolt-amperes (kVA) (approximate):
    - Minimum configuration as shipped: 0.08 kVA
    - Maximum configuration: 0.28 kVA

  Note: Power consumption and heat output vary depending on the number and type of optional features installed and the power management optional features in use.

Heat output

- Approximate heat output in British thermal units (Btu) per hour:
  - Minimum configuration: 245 Btu/hr (70 watts)
  - Maximum configuration: 700 Btu/hr (204 watts)

Airflow

- Approximately 0.56 cubic meter per minute (20 cubic feet per minute) maximum

Acoustical noise-emission values

- Average sound-pressure levels:
  - At operator position:
    - Idle: 37 dBA
    - Operating: 43 dBA
  - At bystander position–1 meter (3.3 ft):
    - Idle: 32 dBA
    - Operating: 36 dBA
- Declared (upper limit) sound-power levels:
  - Idle: 4.7 bels
  - Operating: 5.1 bels

  Note: These levels were measured in controlled acoustical environments according to procedures specified by the American National Standards Institute (ANSI) S12.10 and ISO 7779 and are reported in accordance with ISO 9296. Actual sound-pressure levels in a given location might exceed the average values stated because of room reflections and other nearby noise sources. The declared sound-power levels indicate an upper limit, below which a large number of computers will operate.

PC 300PL — tower

Dimensions

- Height: 492 mm (19.4 in.)
- Width: 200 mm (7.9 in.)
- Depth: 445 mm (17.5 in.)

Weight

- Minimum configuration as shipped: 15 kg (33 lb)
- Maximum configuration: 17.3 kg (38 lb)

Environment

- Air temperature:
  - System on: 10° to 35°C (50° to 95°F)
  - System off: 10° to 43°C (50° to 110°F)
  - Maximum altitude: 2134 m (7000 ft)

  Note: The maximum altitude, 2133.6 m (7000 ft.), is the maximum altitude at which the specified air temperatures apply. At higher altitudes, the maximum air temperatures are lower than those specified.

- Humidity:
  - System on: 8% to 80%
  - System off: 8% to 80%

Electrical input

- Input voltage:
  - Low range:
    - Minimum: 90 V ac
    - Maximum: 137 V ac
    - Input frequency range: 57–63 Hz
    - Voltage switch setting: 115 V
  - High range:
    - Minimum: 180 V ac
    - Maximum: 265 V ac
    - Input frequency range: 47–53 Hz
    - Voltage switch setting: 230 V
  - Input kilovolt-amperes (kVA) (approximate):
    - Minimum configuration as shipped: 0.08 kVA
    - Maximum configuration: 0.38 kVA

  Note: Power consumption and heat output vary depending on the number and type of optional features installed and the power management optional features in use.

Heat output

- Approximate heat output in British thermal units (Btu) per hour:
  - Minimum configuration: 245 Btu/hr (70 watts)
  - Maximum configuration: 969 Btu/hr (285 watts)

Airflow

- Approximately 0.85 cubic meter per minute (30 cubic feet per minute) maximum

Acoustical noise-emission values

- Average sound-pressure levels:
  - At operator position:
    - Idle: 36 dBA
    - Operating: 39 dBA
  - At bystander position–1 meter (3.3 ft):
    - Idle: 33 dBA
    - Operating: 36 dBA
  - Declared (upper limit) sound-power levels:
    - Idle: 4.7 bels
    - Operating: 5.0 bels

  Note: These levels were measured in controlled acoustical environments according to procedures specified by the American National Standards Institute (ANSI) S12.10 and ISO 7779 and are reported in accordance with ISO 9296. Actual sound-pressure levels in a given location might exceed the average values stated because of room reflections and other nearby noise sources. The declared sound-power levels indicate an upper limit, below which a large number of computers will operate.

Cabling requirements for Wake on LAN adapters

The PC 300PL Personal Computer has a 3-pin header on the system board that provides the Auxiliary 5 volts (AUX5) and wake-up signal connections. Newer Wake on LAN adapters have a single 3-pin header that connects to the 3-pin header on the riser card. Some Wake on LAN adapters have two headers: a 3-pin, right-angle header for AUX5, and a 2-pin straight header for the wake-up signal. These Wake on LAN adapter options include a Y-cable that has a 3-pin system board connector on one end and splits into the 3-pin and 2-pin connectors that connect to the adapter.

Chapter 4. Power supply

The power-supply requirements are supplied by 145-watt PC 300PL Personal Computer power supply. The power supply provides 3.3-volt power for the Pentium microprocessor and core chip set and 5-volt power for PCI adapters. Also included is an auxiliary 5-volt (AUX 5) supply to provide power to power-management circuitry and a Wake on LAN adapter. The power supply converts the ac input voltage into four dc output voltages and provides power for the following:

- System board
- Adapters
- Internal drives
- Keyboard and auxiliary devices
- USB devices

A logic signal on the power connector controls the power supply; the front panel switch is not directly connected to the power supply.

The power supply connects to the system board with a 2 x 10 connector.

Power input

The following figure shows the power-input specifications. The power supply has a manual switch to select the correct input voltage.

Figure 7. Power-input requirements	
Specification	**Measurements**
Input voltage, low range	100 (min) to 127 (max) V AC
Input voltage, high range	200 (min) to 240 (max) V AC
Input frequency	50 Hz ± 3 Hz or 60 Hz ± 3 Hz

Power output

The power supply outputs shown in the following figures include the current-supply capability of all the connectors, including system board, DASD, PCI, and auxiliary outputs.

Figure 8. Power-output (145 watts)			
Output voltage	**Regulation**	**Minimum current**	**Maximum current**
+5 volts	+5% to −4%	1.5 A	18.0 A
+12 volts	+5% to −5%	0.2 A	4.2 A
−12 volts	+10% to −9%	0.0 A	0.4 A
+3.3 volts	±2%	0.0 A	10.0 A
−5 volts	±10%	0.0 A	0.3 A
+5 volt (auxiliary)	+5% to −5%	0.0 A	0.02 A

Note: The total combined 3.3 V and 5 V power must not exceed 100 watts.

Figure 9. Power output (200 watts)			
Output voltage	**Regulation**	**Minimum current**	**Maximum current**
+5 volts	+5% to -4%	1.5 A	20.0 A
+12 volts	±5%	0.2 A	8.0 A
−12 volts	+10% to -9%	0.0 A	0.4 A
−5 volts	±10%	0.0 A	0.3 A
+ 3.3 volts	±2%	0.0 A	20.0 A
+5 volts (auxiliary)	±5%	0.005 A	0.72 A

Component outputs

The power supply provides separate voltage sources for the system board and internal storage devices. The following figures show the approximate power that is provided for specific system components. Many components draw less current than the maximum shown.

Figure 10. System board		
Supply voltage	**Maximum current**	**Regulation limits**
+3.3 V dc	3000 mA	+5.0% to −5.0%
+5.0 V dc	4000 mA	+5.0% to −4.0%
+12.0 V dc	25.0 mA	+5.0% to −5.0%
−12.0 V dc	25.0 mA	+10.0% to −9.0%

Figure 11. Keyboard port		
Supply voltage	**Maximum current**	**Regulation limits**
+5.0 V dc	275 mA	+5.0% to −4.0%

Figure 12. PCI-bus adapters (per slot)		
Supply voltage	**Maximum current**	**Regulation limits**
+5.0 V dc	2000 mA	+5.0% to −4.0%
+3.3 V dc	3030 mA	+5.0% to −4.0%

Note: For each PCI connector, the maximum power consumption is rated at 10 watts for +5 V dc and +3.3 V dc combined. Typical power budget assumptions use 7.5 watts per adapter. If maximum power is used, then the overall system configuration will be limited in performance.

Figure 13. USB port		
Supply voltage	**Maximum current**	**Regulation limits**
+5.0 V dc	500 mA	+5.0% to −4.0%

Figure 14. Internal DASD		
Supply voltage	**Maximum current**	**Regulation limits**
+5.0 V dc	1400 mA	+5.0% to −5.0%
+12.0 V dc	1500 mA at startup, 400 mA when active	+5.0% to −5.0%

Note: Some adapters and hard disk drives draw more current than the recommended limits. These adapters and drives can be installed in the system; however, the power supply will shut down if the total power used exceeds the maximum power that is available.

Output protection

The power supply protects against output overcurrent, overvoltage, and short circuits. See the power supply specifications on the previous pages for details.

A short circuit that is placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state, with no damage to the power supply. If this shutdown state occurs, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least one second.

If an overvoltage fault occurs (in the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of the nominal value of the power supply.

Connector description

The power supply for the PC 300PL Personal Computer has four 4-pin connectors for internal devices. The total power used by the connectors must not exceed the amount shown in "Component outputs" on page 19. For connector pin assignments, see Appendix A, "Connector pin assignments" on page 25.

Chapter 5. System software

This section briefly describes some of the system software included with the computer.

BIOS

The computer uses the IBM basic input/output system (BIOS), which is stored in flash electrically erasable programmable read-only memory (EEPROM). Some features of the BIOS are:

- PCI support in accordance with PCI BIOS Specification 2.2
- Microsoft PCI IRQ Routing Table
- Plug and Play support in accordance with Plug and Play BIOS Specification 1.1a
- Advanced Power Management (APM) support according to APM BIOS Interface Specification 1.2
- Wake on LAN support
- Wake on Ring support
- Alert on LAN support
- Remote program load (RPL) and Dynamic Host Configuration Protocol (DHCP)
- Startable CD-ROM support
- Flash-over-LAN support
- Alternate startup sequence
- IBM look and feel, such as screen arrangements
- ACPI (Advanced Configuration and Power Interfaces) 1.0b
- IDE logical block addressing (LBA) support
- LSA 2.0 support
- LS120 support
- DM BIOS 2.1 (DMI 2.0 compliant)
- PC99 compliance

Plug and Play

Support for Plug and Play conforms to the following:

- Plug and Play BIOS Specification 1.1a and 1.0
- Plug and Play BIOS Extension Design Guide 1.0
- Plug and Play BIOS Specification, Errata, and Clarifications 1.0
- Guide to Integrating the Plug and Play BIOS Extensions with system BIOS 1.2
- Plug and Play Kit for DOS and Windows

POST

IBM power-on self-test (POST) code is used. Also, initialization code is included for the on-board system devices and controllers.

POST error codes include text messages for determining the cause of an error. For more information, see Appendix D, "Error codes" on page 41.

Configuration/Setup Utility program

The Configuration/Setup Utility program provides menus for selecting options for devices, I/O ports, date and time, system security, start options, advanced setup, and power management.

More information on using the Configuration/Setup Utility program is provided in *PC 300PL User Guide*.

Advanced Power Management (APM)

The PC 300PL Personal Computer computers come with built-in energy-saving capabilities. Advanced Power Management (APM) is a feature that reduces the power consumption of systems when they are not being used. When enabled, APM initiates reduced-power modes for the monitor, microprocessor, and hard disk drive after a specified period of inactivity.

The BIOS supports APM 1.2. This enables the system to enter a power-managed state, which reduces the power drawn from the ac electrical outlet. Advanced Power Management is enabled through the Configuration/Setup Utility program and is controlled by the individual operating system.

For more information on APM, see *PC 300PL User Guide* and *Understanding Your Personal Computer*.

Advanced Configuration and Power Interface (ACPI)

Automatic Configuration and Power Interface (ACPI) BIOS mode enables the operating system to control the power management features of the computer. Not all operating systems support ACPI BIOS mode. See the operating system documentation to determine if ACPI is supported.

Flash update utility program

The flash update utility program is a stand-alone program to support flash updates. This utility program updates the BIOS code and can change the machine readable information (MRI) to different languages.

The flash update utility program is available on a 3.5-inch diskette.

Diagnostic program

The diagnostic program that comes with the PC 300PL Personal Computer computer is provided on the *Product Recovery CD* and *Device Driver and IBM Enhanced Diagnostics CD*. It runs independently of the operating system. You can use IBM Enhanced Diagnostics to diagnose and repair problems with the computer. You can download the latest version from http://www.ibm.com/pc/support/desktop/desktop_support.html on the World Wide Web. For more information on this diagnostic program, see *PC 300PL User Guide*.

Chapter 6. System compatibility

This chapter discusses some of the hardware, software, and BIOS compatibility issues for the computer. See the *Compatibility Report* for a list of compatible hardware and software options.

Hardware compatibility

This section discusses hardware, software, and BIOS compatibility issues that must be considered when designing application programs.

Many of the interfaces are the same as those used by the IBM Personal Computer AT. In most cases, the command and status organization of these interfaces is maintained.

The functional interfaces are compatible with the following interfaces:

- Intel 8259 interrupt controllers (edge-triggered mode)
- National Semiconductor NS16450 and NS16550A serial communication controllers
- Motorola MC146818 Time of Day Clock command and status (CMOS reorganized)
- Intel 8254 timer, driven from a 1.193 MHz clock (channels 0, 1, and 2)
- Intel 8237 DMA controller, except for the Command and Request registers and the Rotate and Mask functions; the Mode register is partially supported
- Intel 8272 or 82077 diskette drive controllers
- Intel 8042 keyboard controller at addresses hex 0060 and hex 0064
- All video standards using VGA, EGA, CGA, MDA, and Hercules modes
- Parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode

Use this information to develop application programs. Whenever possible, use the BIOS as an interface to hardware to provide maximum compatibility and portability of applications among systems.

Hardware interrupts

Hardware interrupts are level-sensitive for PCI interrupts. The interrupt controller clears its in-service register bit when the interrupt routine sends an End-of-Interrupt (EOI) command to the controller. The EOI command is sent regardless of whether the incoming interrupt request to the controller is active or inactive.

The interrupt-in-progress latch is readable at an I/O-address bit position. This latch is read during the interrupt service routine and might be reset by the read operation or it might require an explicit reset.

Note: For performance and latency considerations, designers might want to limit the number of devices sharing an interrupt level.

With level-sensitive interrupts, the interrupt controller requires that the interrupt request be inactive at the time the EOI command is sent; otherwise, a new interrupt request will be detected. To avoid this, a level-sensitive interrupt handler must clear the interrupt condition (usually by a read or write operation to an I/O port on the device causing the interrupt). After processing the interrupt, the interrupt handler:

1. Clears the interrupt
2. Waits one I/O delay
3. Sends the EOI

    4. Waits one I/O delay

    5. Enables the interrupt through the Set Interrupt Enable Flag command

Hardware interrupt IRQ9 is defined as the replacement interrupt level for the cascade level IRQ2. Program interrupt sharing is implemented on IRQ2, interrupt hex 0A. The following processing occurs to maintain compatibility with the IRQ2 used by IBM Personal Computer products:

1. A device drives the interrupt request active on IRQ2 of the channel.

2. This interrupt request is mapped in hardware to IRQ9 input on the second interrupt controller.

3. When the interrupt occurs, the system microprocessor passes control to the IRQ9 (interrupt hex 71) interrupt handler.

4. This interrupt handler performs an EOI command to the second interrupt controller and passes control to the IRQ2 (interrupt hex 0A) interrupt handler.

5. This IRQ2 interrupt handler, when handling the interrupt, causes the device to reset the interrupt request before performing an EOI command to the master interrupt controller that finishes servicing the IRQ2 request.

Hard disk drives and controller

Reading from and writing to the hard disk is initiated in the same way as in IBM Personal Computer products; however, new functions are supported.

Software compatibility

To maintain software compatibility, the interrupt polling mechanism that is used by IBM Personal Computer products is retained. Software that interfaces with the reset port for the IBM Personal Computer positive-edge interrupt sharing (hex address 02Fx or 06Fx, where x is the interrupt level) does not create interference.

Software interrupts

With the advent of software interrupt sharing, software interrupt routines must daisy chain interrupts. Each routine must check the function value, and if it is not in the range of function calls for that routine, it must transfer control to the next routine in the chain. Because software interrupts are initially pointed to address 0:0 before daisy chaining, check for this case. If the next routine is pointed to address 0:0 and the function call is out of range, the appropriate action is to set the carry flag and do a RET 2 to indicate an error condition.

Machine-sensitive programs

Programs can select machine-specific features, but they must first identify the machine and model type. IBM has defined methods for uniquely determining the specific machine type. The machine model byte can be found through Interrupt 15H, Return System Configuration Parameters function (AH)=C0H).

Appendix A. Connector pin assignments

The following figures show the pin assignments for various system board connectors.

Monitor connector
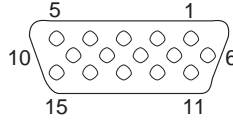
| Pin	Signal	I/O	Pin	Signal	I/O
	Figure 15. Monitor port connector pin assignments—SVGA				
1	Red	O	2	Green	O
3	Blue	O	4	Monitor ID 2 - Not used	I
5	Ground	NA	6	Red ground	NA
7	Green ground	NA	8	Blue ground	NA
9	+5 V, used by DDC2B	NA	10	Ground	NA
11	Monitor ID 0 - Not used	I	12	DDC2B serial data	I/O
13	Horizontal sync	O	14	Vertical sync	O
15	DDC2B clock	I/O			
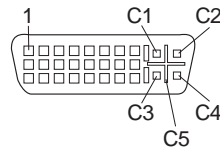
Pin	Signal	I/O	Pin	Signal	I/O
	Figure 16. Monitor port connector pin assignments—DVI main pin field				
1	TMDS data 2+	O	2	TMDS data 2-	O
3	TMDS data 2/4 return	N/A	4	TMDS data 4-*	O
5	TMDS data 4+*	O	6	DDC clock	I/O
7	DDC data	I/O	8	Analog vertical sync	O
9	TMDS data 1-	O	10	TMDS data 1+	O
11	TMDS data 1/3 shield	N/A	12	TMDS data 3+*	O
13	TMDS data 3+*	O	14	+5V power	O
15	Ground	N/A	16	Hot plug detect	O
17	TMDS data 0-	O	18	TMDS data 0+	O
19	Return	N/A	20	TMDS D5*	O
21	TMDS data 5+*	O	22	TMDS clock shield	N/A
23	TMDS clock+	O	24	TMDS clock-	O

Appendix A. Connector pin assignments

| Figure 17. Monitor port connector pin assignments—DVI MicroCross section					
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
C1	Red video out	O	C2	Green video out	O
C3	Analog blue	O	C4	Analog horizontal sync	O
C5	Video/pixel clock return	N/A			

*These are not used on the NumberNine S3 Savage4 AGP card.

Memory connectors
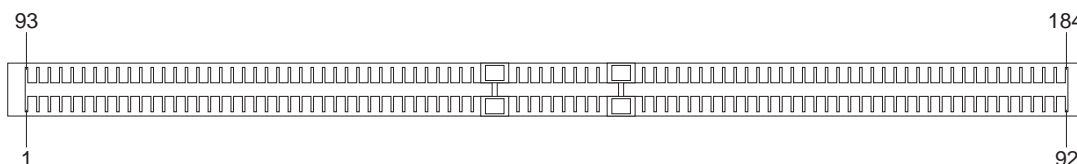
Figure 18 (Page 1 of 2). System memory connector pin assignments							
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
A1	Gnd	B1	Gnd	A47	NC	B47	NC
A2	LDQA8	B2	LDQA7	A48	NC	B48	NC
A3	Gnd	B3	Gnd	A49	NC	B49	NC
A4	LDQA6	B4	LDQA5	A50	NC	B50	NC
A5	Gnd	B5	Gnd	A51	Vref	B51	Vref
A6	LDQA4	B6	LDQA3	A52	Gnd	B52	Gnd
A7	Gnd	B7	Gnd	A53	SCL	B53	SA0
A8	LDQA2	B8	LDQA1	A54	Vdd	B54	Vdd
A9	Gnd	B9	Gnd	A55	SDA	B55	SA1
A10	LDQA0	B10	LCFM	A56	SVdd	B56	SVdd
A11	Gnd	B11	Gnd	A57	SWP	B57	SA2
A12	LCTMN	B12	LCFMN	A58	Vdd	B58	Vdd
A13	Gnd	B13	Gnd	A59	RSCK	B59	RCMD
A14	LCTM	B14	NC	A60	Gnd	B60	Gnd
A15	Gnd	B15	Gnd	A61	RDQB7	B61	RDQB8
A16	NC	B16	LROW2	A62	Gnd	B62	Gnd
A17	Gnd	B17	Gnd	A63	RDQB5	B63	RDQB6
A18	LROW1	B18	LROW0	A64	Gnd	B64	Gnd
A19	Gnd	B19	Gnd	A65	RDQB3	B65	RDQB4
A20	LCOL4	B20	LCOL3	A66	Gnd	B66	Gnd
A21	Gnd	B21	Gnd	A67	RDQB1	B67	RDQB2
A22	LCOL2	B22	LCOL1	A68	Gnd	B68	Gnd
A23	Gnd	B23	Gnd	A69	RCOL0	B69	RDQB0
A24	LCOL0	B24	LDQB0	A70	Gnd	B70	Gnd
A25	Gnd	B25	Gnd	A71	RCOL2	B71	RCOL1
A26	LDQB1	B26	LDQB2	A72	Gnd	B72	Gnd
A27	Gnd	B27	Gnd	A73	RCOL4	B73	RCOL3
A28	LDQB3	B28	LDQB4	A74	Gnd	B74	Gnd

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A29	Gnd	B29	Gnd	A75	RROW1	B75	RROW0
A30	LDQB5	B30	LDQB6	A76	Gnd	B76	Gnd
A31	Gnd	B31	Gnd	A77	NC	B77	RROW2
A32	LDQB7	B32	LDQB8	A78	Gnd	B78	Gnd
A33	Gnd	B33	Gnd	A79	RCTM	B79	NC
A34	LSCK	B34	LCMD	A80	Gnd	B80	Gnd
A3	Vcmos	B35	Vcmos	A81	RCTMN	B81	RCFMN
A36	SOUT	B36	SIN	A82	Gnd	B82	Gnd
A37	Vcmos	B37	Vcmos	A83	RDQA0	B83	RCFM
A38	NC	B38	NC	A84	Gnd	B84	Gnd
A39	Gnd	B39	Gnd	A85	RDQA2	B85	RDQA1
A40	NC	B40	NC	A86	Gnd	B86	Gnd
A41	Vdd	B41	Vdd	A87	RDQA4	B87	RDQA3
A42	Vdd	B42	Vdd	A88	Gnd	B88	Gnd
A43	NC	B43	NC	A89	RDQA6	B89	RDQA5
A44	NC	B44	NC	A90	Gnd	B90	Gnd
A45	NC	B45	NC	A91	RDQA8	B91	RDQA7
A46	NC	B46	NC	A92	Gnd	B92	Gnd

Figure 18 (Page 2 of 2). System memory connector pin assignments

PCI connectors

Pin	Signal	I/O	Pin	Signal	I/O
A1	TRST#	O	B1	−12 V dc	NA
A2	+12 V dc	NA	B2	TCK	O
A3	TMS	O	B3	Ground	NA
A4	TDI	O	B4	TDO	I
A5	+5 V dc	NA	B5	+5 V dc	NA
A6	INTA#	I	B6	+5 V dc	NA
A7	INTC#	I	B7	INTB#	I
A8	+5 V dc	NA	B8	INTD#	I
A9	Reserved	NA	B9	PRSNT1#	I
A10	+5 V dc	NA	B10	Reserved	NA
A11	Reserved	NA	B11	PRSNT2#	I
A12	Ground	NA	B12	Ground	NA
A13	Ground	NA	B13	Ground	NA
A14	3.3 V AUX	NA	B14	3.3 V AUX	NA

Figure 19 (Page 1 of 3). PCI connector pin assignments

Appendix A. Connector pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
	Figure 19 (Page 2 of 3). PCI connector pin assignments				
A15	RST#	O	B15	Ground	NA
A16	+5 V dc (I/O)	NA	B16	CLK	O
A17	GNT#	O	B17	Ground	NA
A18	Ground	NA	B18	REQ#	I
A19	PCI	NA	B19	+5 V dc	NA
A20	Address/data 30	I/O	B20	Address/data 31	I/O
A21	+3.3 V dc	NA	B21	Address/data 29	I/O
A22	Address/data 28	I/O	B22	Ground	NA
A23	Address/data 26	I/O	B23	Address/data 27	I/O
A24	Ground	I/O	B24	Address/data 25	NA
A25	Address/data 24	I/O	B25	+3.3 V dc	NA
A26	IDSEL	O	B26	C/BE 3#	I/O
A27	+3.3 V dc	NA	B27	Address/data 23	I/O
A28	Address/data 22	I/O	B28	Ground	NA
A29	Address/data 20	I/O	B29	Address/data 21	I/O
A30	Ground	I/O	B30	Address/data 19	NA
A31	Address/data 18	I/O	B31	+3.3 V dc	NA
A32	Address/data 16	I/O	B32	Address/data 17	I/O
A33	+3.3 V dc	NA	B33	C/BE 2#	I/O
A34	FRAME#	I/O	B34	Ground	NA
A35	Ground	NA	B35	IRDY#	I/O
A36	TRDY#	I/O	B36	+3.3 V dc	NA
A37	Ground	NA	B37	DEVSEL#	I/O
A38	STOP#	I/O	B38	Ground	NA
A39	+3.3 V dc	NA	B39	LOCK#	I/O
A40	SMBCLK*	I/O	B40	PERR#	I/O
A41	SMBDATA*	I/O	B41	+3.3 V dc	NA
A42	Ground	NA	B42	SERR#	I/O
A43	PAR	NA	B43	+3.3 V dc	NA
A44	Address/data 15	I/O	B44	C/BE 1#	I/O
A45	3.3 V dc	I/O	B45	Address/data 14	I/O
A46	Address/data 13	NA	B46	Ground	NA
A47	Address/data 11	I/O	B47	Address/data 12	I/O
A48	Ground	I/O	B48	Address/data 10	I/O
A49	Address/data 9	NA	B49	Ground	NA
A50	Key	NA	B50	Key	NA
A51	Key	NA	B51	Key	NA
A52	C/BE(0)#	I/O	B52	Address/data 8	I/O
A53	3.3 V dc	I/O	B53	Address/data 7	I/O
A54	Address/data 6	NA	B54	+3.3 V dc	NA
A55	Address/data 4	I/O	B55	Address/data 5	I/O
A56	Ground	I/O	B56	Address/data 3	I/O
A57	Address/data 2	NA	B57	Ground	NA

Figure 19 (Page 3 of 3). PCI connector pin assignments					
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
A58	Address/data 0	I/O	B58	Address/data 1	I/O
A59	+5 V dc	NA	B59	+5 V dc	NA
A60	ACK64#	I/O	B60	ACK64#	I/O
A61	+5 V dc	NA	B61	+5 V dc	NA
A62	+5 V dc	NA	B62	+5 V dc	NA

*These assignments are for PCI connector slot one only; for all other slots, the signal for pin A40 is SDONE and for pin A41 is SBO#.

ISA connectors
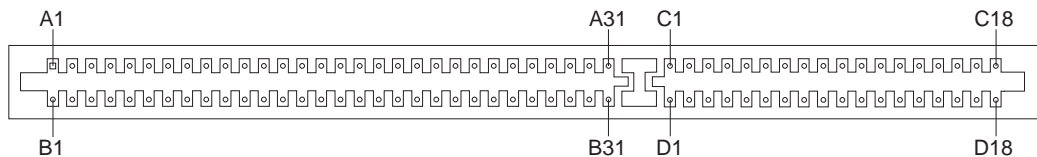
Note: The ISA connectors are on the riser card.

Figure 20 (Page 1 of 2). ISA connector pin assignments					
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
B1	Ground	NA	A1	IOCHCK#	I
B2	RESET DRV	O	A2	SD7	I/O
B3	+5 V dc	NA	A3	SD6	I/O
B4	IRQ2	I	A4	SD5	I/O
B5	-5 V dc	NA	A5	SD4	I/O
B6	DRQ2	I	A6	SD3	I/O
B7	-12 V dc	NA	A7	SD2	I/O
B8	OWS#	I	A8	SD1	I/O
B9	+12 V dc	NA	A9	SD0	I/O
B10	Ground	NA	A10	IOCHRDY	I
B11	SMEMW#	O	A11	AEN	O
B12	SMEMR#	O	A12	SA19	I/O
B13	IOW#	I/O	A13	SA18	I/O
B14	IOR#	I/O	A14	SA17	I/O
B15	DACK3#	O	A15	SA16	I/O
B16	DRQ3	I	A16	SA15	I/O
B17	DACK1#	O	A17	SA14	I/O
B18	DRQ1	I	A18	SA13	I/O
B19	REFRESH#	I/O	A19	SA12	I/O
B20	CLK	O	A20	SA11	I/O
B21	IRQ7	I	A21	SA10	I/O
B22	IRQ6	I	A22	SA9	I/O
B23	IRQ5	I	A23	SA8	I/O
B24	IRQ4	I	A24	SA7	I/O

Appendix A. Connector pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
	Figure 20 (Page 2 of 2). ISA connector pin assignments				
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
B25	IRQ3	I	A25	SA6	I/O
B26	DACK2#	O	A26	SA5	I/O
B27	TC	O	A27	SA4	I/O
B28	BALE	O	A28	SA3	I/O
B29	+5 V dc	NA	A29	SA2	I/O
B30	OSC	O	A30	SA1	I/O
B31	Ground	NA	A31	SA0	I/O
D1	MEMCS16#	I	C1	SBHE#	I/O
D2	IOCS16#	I	C2	LA23	I/O
D3	IRQ10	I	C3	LA22	I/O
D4	IRQ11	I	C4	LA21	I/O
D5	IRQ12	I	C5	LA20	I/O
D6	IRQ15	I	C6	LA19	I/O
D7	IRQ14	I	C7	LA18	I/O
D8	DACK0#	O	C8	LA17	I/O
D9	DRQ0	I	C9	MEMR#	I/O
D10	DACK5#	O	C10	MEMW#	I/O
D11	DRQ5	I	C11	SD8	I/O
D12	DACK6#	O	C12	SD9	I/O
D13	DRQ6	I	C13	SD10	I/O
D14	DACK7#	O	C14	SD11	I/O
D15	DRQ7	I	C15	SD12	I/O
D16	+5 V DC	NA	C16	SD13	I/O
D17	MASTER#	I	C17	SD14	I/O
D18	Ground	NA	C18	SD15	I/O

IDE connectors
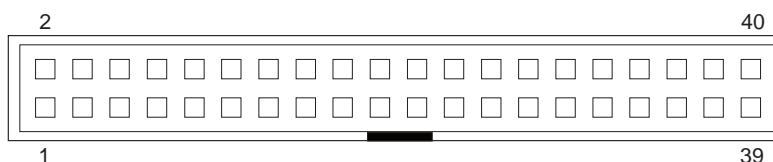
Pin	Signal	I/O	Pin	Signal	I/O
	Figure 21 (Page 1 of 2). IDE connector pin assignments				
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
1	RESET	O	21	NC	NA
2	Ground	NA	22	Ground	NA
3	Data bus bit 7	I/O	23	I/O write	O
4	Data bus bit 8	I/O	24	NC	NA
5	Data bus bit 6	I/O	25	I/O read	O
6	Data bus bit 9	I/O	26	Ground	NA
7	Data bus bit 5	I/O	27	I/O channel ready	I
8	Data bus bit 10	I/O	28	ALE	O

Figure 21 (Page 2 of 2). IDE connector pin assignments					
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
9	Data bus bit 4	I/O	29	NC	NA
10	Data bus bit 11	I/O	30	Ground	NA
11	Data bus bit 3	I/O	31	IRQ	I
12	Data bus bit 12	I/O	32	CS16#	I
13	Data bus bit 2	I/O	33	SA1	O
14	Data bus bit 13	I/O	34	PDIAG#	I
15	Data bus bit 1	I/O	35	SA0	O
16	Data bus bit 14	I/O	36	SA2	O
17	Data bus bit 0	I/O	37	CS0#	O
18	Data bus bit 15	I/O	38	CS1	O
19	Ground	NA	39	Active#	I
20	Key (Reserved)	NA	40	Ground	NA

Diskette drive connector

Figure 22. Diskette drive connector pin assignments					
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
1	Drive 2 installed #	I	2	High density select	O
3	Not connected	NA	4	Not connected	NA
5	Ground	NA	6	Data rate 0	NA
7	Ground	NA	8	Index#	I
9	Reserved	NA	10	Motor enable 0#	O
11	Ground	NA	12	Drive select 1#	O
13	Ground	NA	14	Drive select 0#	O
15	Ground	NA	16	Motor enable 1#	O
17	MSEN1	I	18	Direction in#	O
19	Ground	NA	20	Step#	O
21	Ground	NA	22	Write data#	O
23	Ground	NA	24	Write enable#	O
25	Ground	NA	26	Track0#	I
27	MSEN0	I	28	Write protect#	I
29	Ground	NA	30	Read data#	I
31	Ground	NA	32	Head 1 select#	O
33	Data rate 1	NA	34	Diskette change#	I

Power supply connector

Figure 23 (Page 1 of 2). Power supply connector pin assignments			
Pin	**Signal name**	**Pin**	**Signal name**
1	+3.3 V	11	+3.3 V
2	+3.3 V	12	−12 V

Appendix A. Connector pin assignments

Figure 23 (Page 2 of 2). Power supply connector pin assignments			
Pin	**Signal name**	**Pin**	**Signal name**
3	Ground	13	Ground
4	+5 V	14	ON/OFF
5	Ground	15	Ground
6	+5 V	16	Ground
7	Ground	17	Ground
8	PWR GOOD	18	–5 V
9	+5 V standby	19	+5 V
10	+12 V	20	+5 V

Wake on LAN connectors

Figure 24. Wake on LAN connector pin assignments	
Pin	**Description**
1	+5 V standby
2	Ground
3	Wake on LAN

Alert on LAN connectors

Figure 25. Alert on LAN connector pin assignments	
Pin	**Description**
1	SMB Data
2	SMB Clock
3	Intrusion

Tamper detection switch

Figure 26. Tamper switch pin assignments	
Pin	**Description**
1	Ground
2	Tamper switch

Radio frequency ID

Figure 27. Radio frequency identification (RFID) pin assignments	
Pin	**Description**
1	RFID Ant 1
2	Key
3	Ground
4	RFID Ant 2

## SCSI high frequency LED connectors

Figure 28. SCSI high frequency LED connector pin assignments	
Pin	**Description**
1	Not connected
2	to LED
3	to LED
4	Not connected

CD audio connector

Figure 29. CD audio connector pin assignments	
Pin	**Description**
1	CD in left
2	CD in Ground
3	CD in Ground
4	CD in Right

USB port connectors
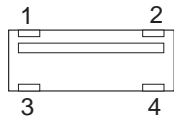
Figure 30. USB port connector pin assignments	
Pin	**Signal**
1	VCC
2	-Data
3	+Data
4	Ground

Mouse and keyboard port connectors
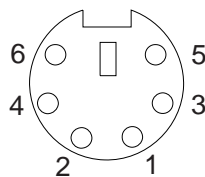
Figure 31 (Page 1 of 2). Mouse port connector pin assignments					
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
1	Data	I/O	2	Reserved	I/O
3	Ground	NA	4	+5 V dc	NA

Appendix A. Connector pin assignments

	Figure 31 (Page 2 of 2). Mouse port connector pin assignments				
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
5	Clock	I/O	6	Reserved	NA

	Figure 32. Keyboard port connector pin assignments				
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
1	Keyboard data	I/O	2	Mouse data	I/O
3	Ground	NA	4	+5 V dc	NA
5	Keyboard clock	I/O	6	Mouse clock	I/O

Serial port connector
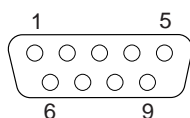
	Figure 33. Serial port connector pin assignments				
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
1	Data carrier detect	I	2	Receive data#	I
3	Transmit data#	O	4	Data terminal read	O
5	Ground	NA	6	Data set ready	I
7	Request to send	O	8	Clear to send	I
9	Ring indicator	I			

Parallel port connector
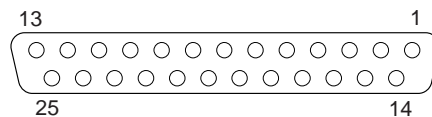
	Figure 34 (Page 1 of 2). Parallel port connector pin assignments				
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
1	STROBE#	I/O	2	Data bit 0	I/O
3	Data bit 1	I/O	4	Data bit 2	I/O
5	Data bit 3	I/O	6	Data bit 4	I/O
7	Data bit 5	I/O	8	Data bit 6	I/O
9	Data bit 7	I/O	10	ACK#	I
11	BUSY	I	12	PE	I
13	SLCT	I	14	AUTO FD XT#	O
15	ERROR#	I	16	INIT#	O
17	SLCT IN#	O	18	Ground	NA
19	Ground	NA	20	Ground	NA
21	Ground	NA	22	Ground	NA
23	Ground	NA	24	Ground	NA

Figure 34 (Page 2 of 2). Parallel port connector pin assignments					
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
25	Ground	NA			

Appendix B. System address maps

System memory map

The first 640 KB of system board RAM is mapped starting at address hex 0000000. A 256 byte area and a 1 KB area of this RAM are reserved for BIOS data areas. Memory can be mapped differently if POST detects an error.

Figure 35. System memory map			
Address range (decimal)	**Address range (hex)**	**Size**	**Description**
0 K – 512 K	00000–7FFFF	512 KB	Conventional
512 K – 639 K	80000–9FBFF	127 KB	Extended conventional
639 K – 640 K	9FC00–9FFFF	1 KB	Extended BIOS data
640 K – 767 K	A0000–BFFFF	128 KB	Dynamic video memory display cache
768 K – 800 K	C0000 to C7FFF	32 KB	Video ROM BIOS (shadowed)
800 K – 896 K	C8000–DFFFF	96 KB	PCI space, available to adapter ROMs
896 K – 1 MB	E0000–FFFFF	128 KB	System ROM BIOS (main memory shadowed)
1 MB – 16 MB	100000–FFFFFF	15 MB	PCI space
16 MB – 4095.872 MB	1000000–FFDFFFF	4079.8 MB	PCI space (positive decode)
	FFFE0000 – FFFFFFFF	128 KB	System ROM BIOS

Input/output address map

The following figure lists resource assignments for the I/O address map. Any addresses that are not shown are reserved.

Figure 36 (Page 1 of 3). I/O address map		
Address (Hex)	**Size**	**Description**
0000–000F	16 bytes	DMA 1
0010–001F	16 bytes	General I/O locations — available to PCI bus
0020–0021	2 bytes	Interrupt controller 1
0022–003F	30 bytes	General I/0 locations — available to PCI bus
0040–0043	4 bytes	Counter/timer 1
0044–00FF	28 bytes	General I/0 locations — available to PCI bus
0060	1 byte	Keyboard controller byte - reset IRQ
0061	1 byte	PIIX4, system port B
0064	1 byte	Keyboard controller, CMD/STAT byte
0070, bit 7	1 bit	Enable NMI
0070, bits 6:0	1 bit	Real-time clock, address
0071	1 byte	Real-time clock, data
0072–007F	14 bytes	General I/O locations — available to PCI bus
0080	1 byte	POST checkpoint register during POST only
008F	1 byte	Refresh page register

Figure 36 (Page 2 of 3). I/O address map		
Address (Hex)	**Size**	**Description**
0080–008F	16 bytes	ICH1, DMA page registers
0090–0091	15 bytes	General I/O locations — available to PCI bus
0092	1 byte	PS/2 keyboard controller registers
0093–009F	15 bytes	General I/O locations
00A0–00A1	2 bytes	Interrupt controller 2
00A2–00BF	30 bytes	APM control
00C0–00DF	31 bytes	DMA 2
00E0–00EF	16 bytes	General I/O locations — available to PCI bus
00F0	1 byte	BX, Coprocessor Error register
00F1–016F	127 bytes	General I/O locations — available to PCI bus
0170–0177	8 bytes	Secondary IDE channel
01F0–01F7	8 bytes	Primary IDE channel
0200–0207	8 bytes	Available
0220–0227	8 bytes	SMC 37C673, Serial port 3 or 4
0228–0277	80 bytes	General I/O locations — available to PCI bus
0278–027F	8 bytes	SMC 27C673, LPT3
0280–02E7	102 bytes	Available
02E8–02EF	8 bytes	SMC PC37C673, Serial port 3 or 4
02F8–02FF	8 bytes	COM2
0338–033F	8 bytes	SMC PC37C673, serial port 3 or 4
0340–036F	48 bytes	Available
0370–0371.	2 bytes	SMC SIO system board Plug and Play index/data registers
0372–0375	4 bytes	Available
0376–0377	2 bytes	IDE channel 1 command
0378–037F	8 bytes	LPT2
0380–03B3	52 bytes	Available
03B4–03B7	4 bytes	Video
03BA	1 byte	Video
03BC–03BE	16 bytes	LPT1
03C0–03CF	16 bytes	Video
03D4–03D7	4 bytes	Video
03DA	1 byte	Video
03D0–03DF	11 bytes	Available
03E0–03E7	8 bytes	Available
03E8–03EF	8 bytes	COM3 or COM4
03F0–03F5	6 bytes	Diskette channel 1
03F6	1 byte	Primary IDE channel command port
03F7 (Write)	1 byte	Diskette channel 1 command
03F7, bit 7	1 bit	Diskette disk change channel
03F7, bits 6:0	7 bits	Primary IDE channel status port
03F8–03FF	8 bytes	COM1
0400–047F	128 bytes	Available
0480–048F	16 bytes	DMA channel high page registers

Appendix B. System address maps

Figure 36 (Page 3 of 3). I/O address map		
Address (Hex)	**Size**	**Description**
0490–0CF7	1912 bytes	Available
0CF8–0CFB	4 bytes	PCI Configuration address register
0CFC–0CFF	4 bytes	PCI Configuration data register
LPT*n* + 400h	8 bytes	ECP port, LPT*n* base address + hex 400
0CF9	1 byte	Turbo and reset control register
0D00–FFFF	62207 bytes	Available

DMA I/O address map

The following figure lists resource assignments for the DMA address map. Any addresses that are not shown are reserved.

Figure 37 (Page 1 of 2). DMA I/O address map			
Address (hex)	**Description**	**Bits**	**Byte pointer**
0000	Channel 0, Memory Address register	00–15	Yes
0001	Channel 0, Transfer Count register	00–15	Yes
0002	Channel 1, Memory Address register	00–15	Yes
0003	Channel 1, Transfer Count register	00–15	Yes
0004	Channel 2, Memory Address register	00–15	Yes
0005	Channel 2, Transfer Count register	00–15	Yes
0006	Channel 3, Memory Address register	00–15	Yes
0007	Channel 3, Transfer Count register	00–15	Yes
0008	Channels 0–3, Read Status/Write Command register	00–07	
0009	Channels 0–3, Write Request register	00–02	
000A	Channels 0–3, Write Single Mask register bits	00–02	
000B	Channels 0–3, Mode register (write)	00–07	
000C	Channels 0–3, Clear byte pointer (write)	N/A	
000D	Channels 0–3, Master clear (write)/temp (read)	00–07	
000E	Channels 0–3, Clear Mask register (write)	00–03	
000F	Channels 0–3, Write All Mask register bits	00–03	
0081	Channel 2, Page Table Address register [2]	00–07	
0082	Channel 3, Page Table Address register [2]	00–07	
0083	Channel 1, Page Table Address register [2]	00–07	
0087	Channel 0, Page Table Address register [2]	00–07	
0089	Channel 6, Page Table Address register [2]	00–07	
008A	Channel 7, Page Table Address register [2]	00–07	
008B	Channel 5, Page Table Address register [2]	00–07	
008F	Channel 4, Page Table Address/Refresh register	00–07	
00C0	Channel 4, Memory Address register	00–15	Yes
00C2	Channel 4, Transfer Count register	00–15	Yes
00C4	Channel 5, Memory Address register	00–15	Yes
00C6	Channel 5, Transfer Count register	00–15	Yes
00C8	Channel 6, Memory Address register	00–15	Yes

Figure 37 (Page 2 of 2). DMA I/O address map			
Address (hex)	**Description**	**Bits**	**Byte pointer**
00CA	Channel 6, Transfer Count register	00–15	Yes
00CC	Channel 7, Memory Address register	00–15	Yes
00CE	Channel 7, Transfer Count register	00–15	Yes
00D0	Channels 4–7, Read Status/Write Command register	00–07	
00D2	Channels 4–7, Write Request register	00–02	
00D4	Channels 4–7, Write Single Mask register bit	00–02	
00D6	Channels 4–7, Mode register (write)	00–07	
00D8	Channels 4–7, Clear byte pointer (write)	N/A	
00DA	Channels 4–7, Master clear (write)/temp (read)	00–07	
00DC	Channels 4–7, Clear Mask register (write)	00–03	
00DE	Channels 4–7, Write All Mask register bits	00–03	
00DF	Channels 5–7, 8- or 16-bit mode select	00–07	

PCI configuration space map

Bus number (hex)	Device number (hex)	Function number (hex)	Description
00	00	00	Intel 84440BX (host bridge)
00	01	00	Intel 84440BX (PCI/AGP)
00	1E	0	Intel 82371AB Hub interface to PCI bridge registers
00	1F	01	Intel 82371AB IDE bus master
00	1F	02	Intel 82371AB USB
00	1F	0	Intel 82371AB Interface bridge registers
00	1F	5	AC '97 audio controller
02	X	00	PCI connectors

---

2 Upper byte of memory address register.

Appendix C. IRQ and DMA channel assignments

The following figures list the interrupt request (IRQ) and direct memory access (DMA) channel assignments.

Figure 38. IRQ channel assignments	
IRQ	**System resource**
NMI	Critical system error
SMI	System management interrupt — power management
0	Reserved (interval timer)
1	Reserved (keyboard)
2	Reserved, cascade interrupt from slave PIC
3	COM2 [3]
4	COM1 [3]
5	LPT2/audio (if present)
6	Diskette controller
7	LPT1 [3]
8	Real-time clock
9	Video
10	Available to user
11	Available to user
12	Mouse port
13	Reserved (math coprocessor)
14	Primary IDE (if present)
15	Secondary IDE (if present)

Figure 39. DMA channel assignments		
DMA channel	**Data width**	**System resource**
0	8 bits	Open
1	8 bits	Open
2	8 bits	Diskette drive
3	8 bits	Parallel port (for ECP or EPP)
4	–	Reserved (cascade channel)
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

---

[3] Default, can be changed to another IRQ.

Appendix D. Error codes

A complete list of POST error codes is provided in the *PC 300PL User Guide* and in the *Hardware Maintenance Manual*.

POST error codes

POST error messages appear when POST finds problems with the hardware during power-on or when a change in the hardware configuration is found. POST error messages are 3-, 4-, 5-, 8-, or 12-character alphanumeric messages.

Beep codes

A complete list of beep codes is provided in the *Hardware Maintenance Manual*.

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  Source: Intel Corporation

- *AT Attachment Interface with Extensions*
  Source: American National Standard of Accredited Standards Committee

- *Extended Capabilities Port: Specification Kit*
  Source: Microsoft Corporation

- *Intel Microprocessor and Peripheral Component Literature*
  Source: Intel Corporation

- *PCI BIOS Specification 2.0*
  Source: PCI Special Interest Group

- *PCI Local Bus Specification 2.1*
  Source: PCI Special Interest Group

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  Source: Microsoft Corporation; available at *http://www.microsoft.com/hwdev*

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  Source: Microsoft Corporation

- *Universal Serial Bus Specifications*
  Source: *http://www.usb.org*

- *Video Electronics Standards Association 1.2*
  Source: *http://www.vesa.org*

- *AT24RF08A- PCID Specification*

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