

CMX58886CX cpuModules™



User's Manual

BDM-61000050 Revision A

PRELIMINARY

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CMX58886CX *cpuModules*™ User's Manual

RTD Document Number: BDM-610000050 Revision A

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Revision History

Revision	Date	Reason for Change
A	06/30/06	Initial release

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Chapter 1 Introduction

This manual provides comprehensive hardware and software information for users developing with the CMX58886CX PC/104-Plus cpuModule.



Note Read the specifications beginning on page 10 prior to designing with the cpuModule.

This manual is organized as follows:

- Chapter 1** **Introduction**
introduces main features and specifications
- Chapter 2** **Getting Started**
provides abbreviated instructions to get started quickly
- Chapter 3** **Connecting the cpuModule**
provides information on connecting the cpuModule to peripherals
- Chapter 4** **Using the cpuModule**
provides information to develop applications for the cpuModule, including general cpuModule information, detailed information on storing both applications and system functions, and using utility programs
- Appendix A** **Hardware Reference**
lists jumper locations and settings, physical dimensions, and processor thermal management
- Appendix B** **Troubleshooting**
offers advice on debugging problems with your system
- Appendix C** **IDAN™ Dimensions and Pinout**
provides connector pinouts for the cpuModule installed in an RTD Intelligent Data Acquisition Node (IDAN) frame
- Appendix D** **Additional Information**
lists sources and websites to support the cpuModule installation and configuration
- Appendix E** **Limited Warranty**

CMX58886CX cpuModules

RTD's CMX58886CX cpuModule represents the latest in high-performance embedded computing solutions. It includes 400 MHz source-synchronous Front Side Bus (FSB), on-die 512kB L2 cache, and data pre-fetch logic. It uses a 333MHz DDR-SDRAM controller that can support up to 2.7 G-Bytes per second of memory bandwidth. All memory chips are soldered directly onto the board.

The video interface is provided by an Analog SVGA output and an LVDS flat panel output. The two outputs are independent, and can display separate images and display timings. Maximum resolution is 2048 x 1536.

High-speed peripheral connections include USB 2.0, with up to 480 Mb/sec data throughput. An ATA-100/66/33 IDE controller provides a fast connection to the hard drive. Network connectivity is provided by an integrated 10/100 Mbps Ethernet controller. Other features include two RS-232/422/485 COM ports, Parallel Port, and AC97 audio.

RTD has gone the extra mile to include additional advanced features for maximum flexibility. These include an ATA/IDE Disk Chip socket that allows a true IDE drive to be attached to the board, either socketed or soldered. A MultiPort can be configured as a standard EPP/ECP parallel port, a floppy drive port, or an Advanced Digital I/O (aDIO) port. An Advanced Watchdog Timer is provided that can generate and interrupt or reset when the timer expires. The DDR-SDRAM controller uses Error-Correcting-Codes (ECC) to correct single bit memory errors, and detect two-bit memory errors, providing for a more robust memory system. SDRAM is soldered directly to the board for high vibration resistance. The CMX58886CX is also available in a rugged, fanless IDAN enclosure.

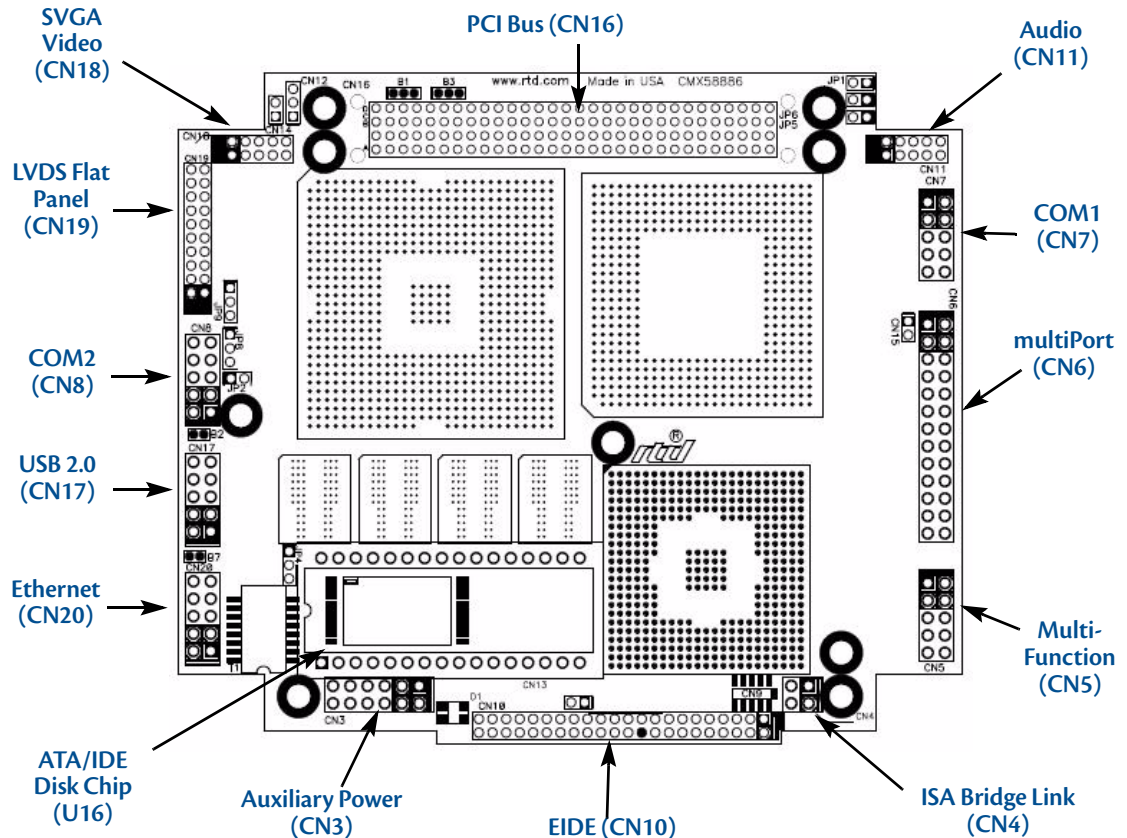


Figure 1 CMX58886CX cpuModule (top view)

Thermal Monitor and Thermal Throttling

The Intel® Thermal Monitor is a feature on the CMX58886CX that automatically throttles the CPU when the CPU exceeds its thermal limit. The maximum temperature of the processor is defined as the temperature that the Thermal Monitor is activated. The thermal limit and duty cycle of the Thermal Monitor cannot be modified. The Thermal Monitor can be disabled by the BIOS for applications where deterministic speed is more important than device failure due to thermal runaway. In addition to the Thermal Monitor, conventional Thermal Throttling is also provided. This forces the CPU to skip clock cycles when it exceeds a thermal limit. The thermal limit and duty cycle of thermal throttling can be modified in the BIOS.

Error-Correction Codes

The Graphics and Memory Controller Hub (GMCH) may be configured in the BIOS setup to operate in an Error-Correction-Code (ECC) data integrity mode. ECC mode allows multiple bit error detection and single bit error correction. The GMCH generate an 8-bit code word for each 64-bit Qword of memory, and performs a full Qword write at a time so that an 8-bit code is sent with each write. Since the code word covers a full Qword, writes of less than a Qword require a read-merge-write operation. Consider a Dword write to memory. In this case, when in ECC mode, GMCH will read the Qword where the addressed Dword will be written, merge in the new Dword, generate a code covering the new Qword and finally write the entire Qword and code back to memory. Any correctable (single-bit) errors detected during the initial Qword read are corrected before merging the new Dword.

Memory with ECC enabled requires additional system memory resources. This will cause the integrated graphics engine to have less memory bandwidth for access to the graphics frame buffer. Because of this, the display may flicker at high resolutions when the graphics processor is fully utilized and ECC is enabled. ECC memory is supported with internal graphics only.

aDIO with Wake-on-aDIO

RTD's exclusive multiPort™ allows the parallel port to be configured as an Advanced Digital I/O (aDIO™), ECP/EPP parallel port, or a floppy drive. aDIO™ is 16 digital bits configured as 8 bit-direction programmable and 8-bit port-direction programmable I/O giving you any combination of inputs and outputs. Match, event, and strobe interrupt modes mean no more wasting valuable processor time polling digital inputs. Interrupts are generated when the 8 bit-direction programmable digital inputs match a pattern or on any value change event. Bit masking allows selecting any subgroup of eight bits. The strobe input latches data into the bit-programmable port and generates an interrupt. Any of the interrupt modes can be used to generate a wake event from any standby/powerdown mode.

Ordering Information

The CMX58886CX cpuModule is available with a 1.0 GHz processor and 256 or 512 MB of DDR SDRAM. The cpuModule can also be purchased as part of an Intelligent Data Acquisition Node (IDAN™) building block, which consists of the cpuModule and a milled aluminum IDAN frame. The IDAN building block can be used in just about any combination with other IDAN building blocks to create a simple but rugged PC/104 stack. Refer to Appendix C, *IDAN™ Dimensions and Pinout*, for more information. The CMX58886CX cpuModule can also be purchased as part of a custom-built RTD HiDAN™ or HiDAN*plus* High Reliability Intelligent Data Acquisition Node. Contact RTD for more information on its high reliability PC/PCI-104 systems.

CMX58886CX Model Options

The basic cpuModule model options are shown below. Refer to the RTD website (www.rtd.com) for more detailed ordering information.

Table 1 CMX58886CX cpuModule Model Options

Part Number	Description
CMX58886CX1000ER-512	1.0 GHz, 512MB DDR-SDRAM cpuModule
CMX58886CX1000ER-256	1.0 GHz, 256MB DDR-SDRAM cpuModule

Cable Kits and Accessories

For maximum flexibility, RTD does not provide cables with the cpuModule. You may wish to purchase the CMX58886CX cpuModule cable kit (P/N XK-CM65), which contains:

- Multi-function utility harness (keyboard socket, battery, reset, speaker)
- Two serial port cables (DIL-10 to DSUB-9)
- Parallel port cable (DIL-26 to DSUB-25)
- Two IDE cables
- VGA monitor cable (DIL-10 to high density 15-pin DSUB)
- Power cable (DIL-12 to wire leads)
- Two USB cables (5-pin SIL to USB A)
- Audio Cable (DIL-10 to three Mini-Jacks)
- One Ethernet cable (DIL-10 to RJ-45)

A floppy drive cable kit (P/N XK-CM49) is also available for connecting to the multiPort. This cable kit comes with:

- 3.5" HDD Floppy Drive with a multiPort interface board
- Two floppy cables

For additional accessories, refer to the RTD website.

Board Features

- 1.0 GHz Intel Celeron M with thermal throttling
 - 400 MHz, source-synchronous Front Side Bus
 - Math coprocessor
 - Supports MMX and SSE2 instructions
 - Internal Cache
 - L1 - 32KB of instruction and 32KB data; L2 - 512kB
- 256 or 512 Mbytes BGA DDR SDRAM
 - Up to 333 MHz Data Rate
 - ECC corrects single-bit memory errors and detects 2-bit errors
- Stackable 120-pin PCI bus
 - 4 Bus master add-on cards capable
 - 3.3V or 5V PCI bus signaling
- Advanced Thermal Management
 - Thermal Throttling reduces clock speed to prevent thermal runaway
 - Auto Fan Control only runs fan when needed
 - SMBus Temperature Monitor for CPU and board temperature
 - Mini Fan Heatsink with Auto Fan control
 - Passive Structural Heatsink & Heatpipes in IDAN and HiDAN System Configurations
- Advanced Programmable Interrupt Controller (APIC)
 - High resolution 100 MHz APIC timer
 - 24 interrupt channels with APIC enabled (15 in legacy PIC mode)
- Advanced Configuration and Power Interface (ACPI)
 - ACPI 1.0 Compliant
 - Supported power down modes: S1 (Power On Suspend), S3 (Suspend to RAM), S4 (Hibernate), and S5 (Soft-Off)
 - CPU Clock Throttling and Clock Stop for C0 to C3 Support
 - Wake events include:
 - aDIO Interrupt
 - Wake-on-LAN
 - Real Time Clock
 - COM port Ring
 - Power Switch
 - etc.
- Three (3) counter/timers (Intel 8254 compatible)
- Seven (7) DMA channels (Intel 8237 compatible)
- Y2K compliant Real-Time Clock (external battery required)
- Nonvolatile storage of CMOS settings without battery
- Watchdog timer
- Complete PC-compatible Single Board Computer

I/O

- AC97 Audio Support
 - Selectable Headphone or Line level output
 - Line level input
 - Microphone input
- Fast Ethernet
 - Ethernet Controller
 - Intel 82562 Fast Ethernet PCI Controller
 - Integrated 3KByte Transmit and 3Kbyte Receive FIFOs
 - Physical Layer
 - 100Base-Tx and 10Base-T
 - Full Duplex support
 - Easy to Use
 - Low Power Features
 - LED Status
 - Software configuration
- 855GME SVGA controller Onboard with 3D Acceleration
 - DirectX & OpenGL 3D Accelerator
 - Analog SVGA Output
 - LVDS Flat Panel output
 - Resolution up to 2048 x 1536 pixels with 32K colors
 - VGA, SVGA, XGA, SXGA, UXGA
 - Up to 16 million colors
 - 64-bit AGP Hardware graphics-accelerator
 - 1MB to 64MB of shared DDR high-performance memory
- Software-configurable RS-232/422/485 serial ports
 - 16550 compatible UARTs for high-speed
 - Termination resistors for RS-422/485
- multiPort function connector
 - Parallel port
 - SPP, PS/2 bi-directional, EPP & ECP
 - Advanced Digital I/O (aDIO)
 - One 8-bit port programmable as input or output
 - Eight bit-programmable I/O with Advanced Digital Interrupt Modes
 - Event Mode Interrupt generates an interrupt when any input bit changes
 - Match Mode Interrupt generates an interrupt when input bits match a preset value
 - External Strobe Mode latches 8 data inputs and generates an interrupt
 - Two Strobes can be configured as readable inputs
 - Floppy controller interface
 - Interfaces with RTD's multiPort Floppy Drive and Cable Kit
 - ESD protection

- Two USB 2.0 (Universal Serial Bus) Ports
 - Supports 480 Mb/s (high-speed), 12Mb/s (full-speed), and 1.5Mbs (low speed) peripherals
 - 500 mA @ 5 Vdc provided per port
 - USB Boot capability
- UltraDMA-100 / 66 / 33 Master Mode PCI EIDE Controller
 - Transfer rate up to 100MB/sec using UltraDMA
 - Increased reliability using UltraDMA-66 transfer protocols
 - Support ATAPI compliant devices including DVD drives
 - 48-bit LBA support for hard drives larger than 137GB
- 32 pin ATA/IDE Disk Chip Socket
 - Miniature ATA/IDE Flash Disk Chip
 - Capacities up to 4GB
 - Natively supported by all major operating systems
- Utility port
 - PC/AT compatible keyboard port
 - PS/2 Mouse Port
 - Speaker port (0.1W output)
 - Hardware Reset input
 - Battery input for Real Time Clock
 - Soft Power Button input
- Power I/O
 - Access to PCI-104 Bus pins
 - Power ground, ± 12 , 5 & 3.3 VDC

BIOS

- RTD Enhanced AMI BIOS
- User-configurable using built-in Setup program
- Nonvolatile storage of CMOS settings without battery
- Boot Devices
 - Standard Devices (floppy disk, hard disk, etc.)
 - ATA/IDE Disk Chip
 - USB Device
 - Network
 - Fail Safe Boot ROM
 - Surface-mount Flash chip that holds ROM-DOS™
- Quick Boot mode

Block Diagram

The next figure shows a simplified block diagram of the CMX58886CX cpuModule.

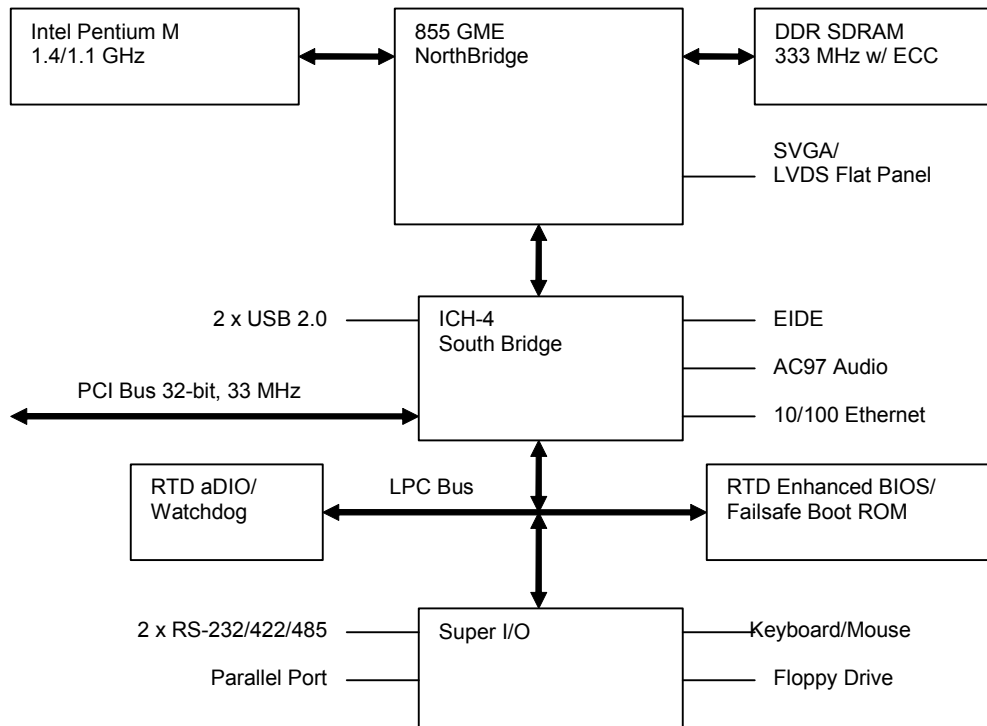


Figure 2 CMX58886CX cpuModule Simplified Block Diagram

You can easily customize the cpuModule by stacking PCI-104 modules such as video controllers, modems, LAN controllers, or analog and digital data acquisition modules. Stacking PCI-104 modules onto the cpuModule avoids expensive installations of backplanes and card cages, and preserves the module's compactness.

The cpuModule uses the RTD Enhanced AMI BIOS. Drivers in the BIOS allow booting from floppy disk, hard disk, ATA/IDE Disk Chip, or boot block flash, thus enabling the system to be used with traditional disk drives or nonmechanical drives. Boot from USB devices and network are also supported.

The cpuModule and BIOS are also compatible with most real-time operating systems for PC compatible computers, although these may require creation of custom drivers to use the aDIO and watchdog timer.

Specifications

Physical Characteristics

- Dimensions: 117mm L x 97mm W x 15mm H (4.6"L x 3.8"W x 0.6"H)
- Weight: Approximately 0.19 Kg (0.40 lbs.)
- PCB: 14-layer, mixed surface-mount and thru-hole

Power Consumption

Exact power consumption depends on the actual application. Table 2 lists power consumption for typical configurations and clock speeds.

Table 2 cpuModule Power Consumption

Module	Speed	RAM	Power, typ.	Power, Max.
CMX58886CX	1.0 GHz	256 or 512 MB	10.9 W	12.2 W

Operating Conditions

Table 3 Operating Conditions

Symbol	Parameter	Test Condition	Min.	Max.
V _{CC5}	5V Supply Voltage		4.75V	5.25V
V _{CC3}	3.3V Supply Voltage		3.1V ¹	n/a
V _{CC12}	12V Supply Voltage		n/a ²	n/a
V _{CC-12}	-12V Supply Voltage		n/a ²	n/a
V _{CCSTBY}	5V Standby Voltage ³		4.75V	5.25V
I _{CCSTBY}	5V Standby Current ³		-	500mA
T _a	Ambient Operating Temperature	Standard ⁴	-40C	+75C
T _a	Ambient Operating Temperature	Extended ⁴	-40C	+85C
T _s	Storage Temperature		-40C	+85C
Rh	Humidity	Non-Condensing	0	90%
MTBF	Mean Time Before Failure	23 C	110,000 hours	

1. Because the cpuModule has an onboard +3.3V supply, an external +3.3V supply is not required. However, if a +3.3 V supply is installed in the system to power PC/104-Plus or PCI-104 expansion boards, it will be monitored by the CPU at power up.
2. The 12V and -12V rails are not used by the cpuModule. They are only connected between the bus connector and the power connector. Any requirements on these signals are driven by other components in the system.
3. 5V Standby is used to power the board when the main supply is turned off (power down modes S3-S5). It is not required for board operation.
4. With proper cooling (See *Thermal Management* on page 65)

Electrical Characteristics

The table below lists the Electrical Characteristics of the CMX58886CX. Operating outside of these parameters may cause permanent damage to the cpuModule.

Table 4 Electrical Characteristics

Symbol	Parameter	Test Condition	Min.	Max.
PCI				
V_{OH}	Output Voltage High	$I_{OH} = -0.5 \text{ mA}$	2.9 V	3.3 V
V_{OL}	Output Voltage Low	$I_{OL} = 6.0 \text{ mA}$	0.0 V	0.55 V
V_{IH}	Input Voltage High	—	1.8 V	5.5 V
V_{IL}	Input Voltage Low	—	-0.5 V	0.9
Bridge Link (CN4)				
V_{OH}	Output Voltage High	$I_{OH} = -0.5 \text{ mA}$	2.4 V	3.3 V
V_{OL}	Output Voltage Low	$I_{OL} = 6.0 \text{ mA}$	0.0 V	0.55 V
V_{IH}	Input Voltage High	—	2.0 V	5.5 V
V_{IL}	Input Voltage Low	—	-0.5 V	0.8 V
IDE & ATA/IDE Disk Chip Socket¹				
V_{OH}	Output Voltage High	$I_{OH} = -6.0 \text{ mA}$	2.8 V	3.3 V
V_{OL}	Output Voltage Low	$I_{OL} = 6.0 \text{ mA}$	0.0 V	0.51 V
V_{IH}	Input Voltage High	—	2.0 V	5.5 V
V_{IL}	Input Voltage Low	—	-0.5 V	0.8 V
Ethernet				
V_{OH}	Output Voltage High	$I_{OH} = -4.0 \text{ mA}$		
V_{OL}	Output Voltage Low	$I_{OL} = 8.0 \text{ mA}$		
V_{IH}	Input Voltage High	—		
V_{IL}	Input Voltage Low	—		
USB Ports				
I_{oc}	Overcurrent Limit	Total of both ports	1.8A	2.6A
LVDS Port				
V_{OD}	Differential Output Voltage		250 mV	450 mV
V_{os}	Offset Voltage		1.125 V	1.375 V
I_{VCC}	Supply Current for Panel Electronics	—	0	2 A
I_{BKLT}	Supply Current for Backlight	—	0	2 A
V_{OH}	Output Voltage High DDC_*, FP_ENABLK	$I_{OH} = -1.0 \text{ mA}$	2.97 V	3.3 V
V_{OL}	Output Voltage Low DDC_*, FP_ENABLK	$I_{OL} = 1.0 \text{ mA}$	0	0.33 V
V_{IH}	Input Voltage High DDC_*	—	2.0	3.6 V
V_{IL}	Input Voltage Low DDC_*	—	-0.3	0.8 V

Table 4 Electrical Characteristics

Symbol	Parameter	Test Condition	Min.	Max.
SVGA Port				
V_{OH}	Output Voltage High HSYNC, VSYNC	$I_{OH} = -32.0 \text{ mA}$	3.8 V	5.0 V
V_{OL}	Output Voltage Low HSYNC, VSYNC	$I_{OL} = 32.0 \text{ mA}$	0.0 V	0.55 V
V_{OH}	Output Voltage High DDC_*	$I_{OH} = -4.0 \text{ mA}$	2.4 V	3.3 V
V_{OL}	Output Voltage Low DDC_*	$I_{OL} = 8.0 \text{ mA}$	0.0 V	0.4 V
V_{IH}	Input Voltage High DDC_*	—	2.0 V	5.5 V
V_{IL}	Input Voltage Low DDC_*	—	-0.3 V	0.8 V
I_{DDCvcc}	Supply Current for DDC Electronics	—	0	2 A
Serial Ports - RS-232				
V_{OH}	Output Voltage High	$R_L = 3 \text{ k}$	5.0 V	10.0 V
V_{OL}	Output Voltage Low	$R_L = 3 \text{ k}$	-10.0 V	-5.0 V
V_{IH}	Input Voltage High	—	2.4 V	25 V
V_{IL}	Input Voltage Low	—	-25 V	0.8 V
Serial Ports - RS-422/485				
V_{OD1}	Differential Output	$R_L = 50 \text{ Ohm}$	2.0 V	6.0 V
V_{OD2}	Differential Output	$R_L = 27 \text{ Ohm}$	1.5 V	6.0 V
V_{OC}	Common Mode Output	$R_L = 27 \text{ or } 50 \text{ Ohm}$	0.0 V	3.0 V
V_{TH}	Differential Input Threshold	$-7V < V_{CM} < 7V$	-0.3 V	0.3 V
V_I	Absolute Max Input Voltage	—	-25 V	25 V
multiPort - all modes				
V_{OH}	Output Voltage High	$I_{OH} = -4.0 \text{ mA}$	2.4 V	3.3 V
V_{OL}	Output Voltage Low	$I_{OL} = 8.0 \text{ mA}$	0.0 V	0.4 V
V_{IH}	Input Voltage High ²	—	2.0 V	5.5 V
V_{IL}	Input Voltage Low ²	—	-0.5 V	0.8 V
RTC Battery Voltage				
V_{RTC}	Input RTC Voltage ³	—	2.0V	3.6 V
External Power Management (CN12) - PME#				
V_{IH}	Input Voltage High	—	2.0 V	3.3 V
V_{IL}	Input Voltage Low	—	-0.5 V	0.8 V

1. Applies to modes up to UltraDMA Mode 4 (ATA/66)
2. Maximum DC undershoot below ground must be limited to either 0.5V or 10mA. During transitions, the device pins may undershoot to -2.0V or overshoot to 7.0V, provided it is less than 10ns, with the forcing current limited to 200 mA.
3. Only required to maintain date and time when power is completely removed from the system. Not required for board operation.

Contact Information

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techsupport@rtd.com

Internet: <http://www.rtd.com>



Chapter 2 Getting Started

For many users, the factory configuration of the CMX58886CX cpuModule can be used to get a PC/104 system operational. You can get your system up and running quickly by following the simple steps described in this chapter, which are:

1. Connect power.
2. Connect the utility harness.
3. Connect a keyboard.
4. Default BIOS configuration.
5. Fail Safe Boot ROM.
6. Connect a VGA monitor to the SVGA connector.

Refer to the remainder of this chapter for details on each of these steps.

Connector Locations

Figure 3 shows the connectors and the ATA/IDE Disk Chip socket of the CMX58886CX cpuModule.

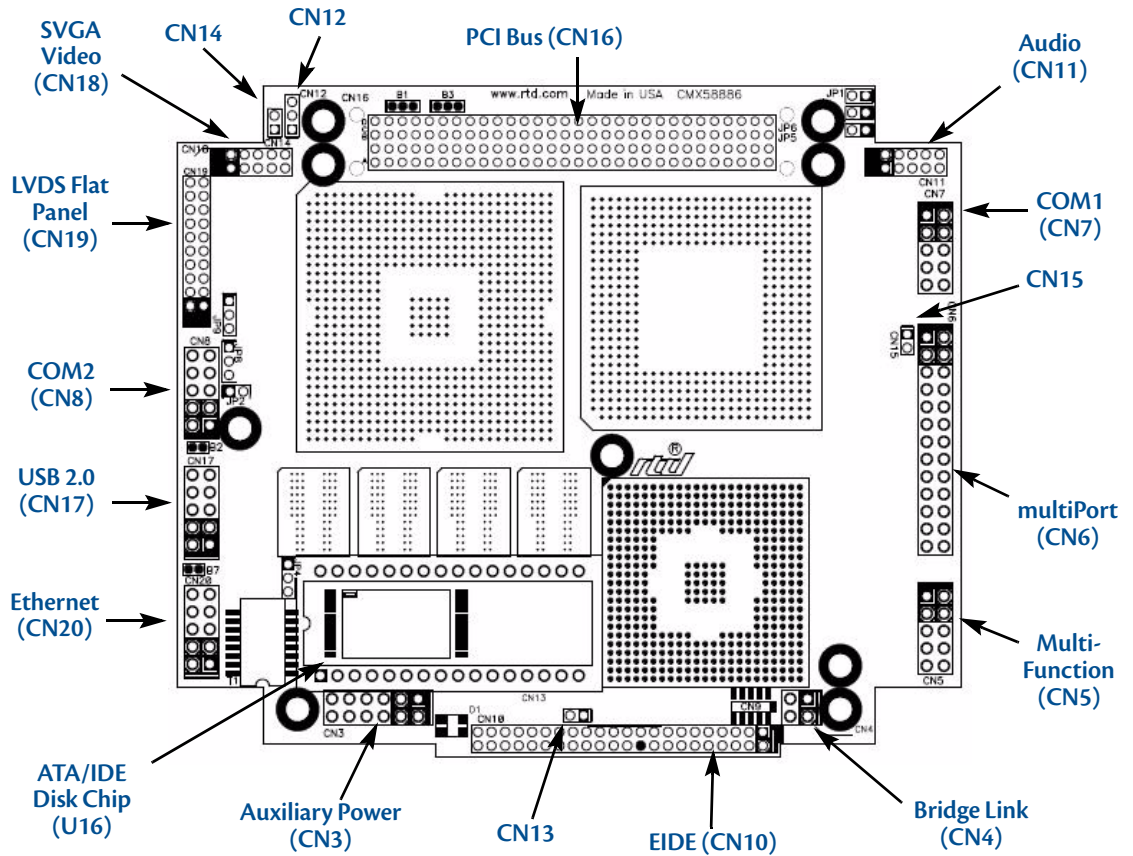


Figure 3 CMX58886CX Connector Locations



Note Pin 1 of each connector is indicated by a white silk-screened square on the top side of the board and a square solder pad on the bottom side of the board. Pin 1 of the bus connectors match when stacking PC104-Plus or PCI-104 modules.

Table 5 CMX58886CX Basic Connectors

Connector	Function	Size
CN3	Auxiliary Power	12-pin
CN4	Bridge Link	4-pin
CN5	Utility Port	10-pin
CN6	multiPort	26-pin
CN7	Serial Port 1 (COM1)	10-pin
CN8	Serial Port 2 (COM2)	10-pin
CN9	Reserved	10-pin
CN10	EIDE Connector	44-pin
CN11	Audio Connector	10-pin
CN12	External Power Management	3-pin
CN13	RTC Battery Input (optional)	2-pin
CN14	Fan Power (+5V)	2-pin
CN15	Fan Power (switched)	2-pin
CN16	PC/104-Plus (PCI) Bus	120-pin
CN17	USB 2.0	10-pin
CN18	Video (SVGA)	10-pin
CN19	Flat Panel Video (LVDS)	30-pin
CN20	Ethernet	10-pin
U16	ATA/IDE Disk Chip Socket	32-pin



WARNING *If you connect power incorrectly, the module will almost certainly be damaged or destroyed. Such damage is not covered by the RTD warranty! Please verify connections to the module before applying power.*

Power is normally supplied to the cpuModule through the PCI bus connectors (**CN16**). If you are placing the cpuModule onto a PC/104-Plus or PCI-104 stack that has a power supply, you do not need to make additional connections to supply power.

If you are using the cpuModule without a PCI-104 or PC/104-Plus stack or with a stack that does not include a power supply, refer to *Auxiliary Power (CN3)* on page 24 for more details.

Some PCI-104 and PC/104-Plus expansion cards may require +3.3V supplied on the PC/104-Plus (PCI) connector (**CN16**). To learn how to supply this voltage, refer to *Auxiliary Power (CN3)* on page 24 and *Jumper Settings and Locations* on page 80.

Connecting the Utility Cable

The multi-function connector (**CN5**) implements the following interfaces:

- PC/AT compatible keyboard
- PS/2 mouse port
- Speaker port (0.1W output)
- Hardware Reset input
- Battery input for Real Time Clock
- Soft Power Button input

To use these interfaces, you must connect to the utility port connector (**CN5**). The utility harness from the RTD cable kit provides a small speaker, two connectors for the keyboard and mouse, a push-button for resetting the PC/104-Plus or PCI-104 system, and a lithium battery to provide backup power for the real time clock.

Refer to *Utility Port Connector (CN5)* on page 26 to connect devices to the utility port connector .

Connecting a Keyboard

You may plug a PC/AT compatible keyboard directly into the circular DIN connector of the utility harness in the cable kit.



Note Many keyboards are switchable between PC/XT and AT operating modes, with the mode usually selected by a switch on the back or bottom of the keyboard. For correct operation with this cpuModule, you must select AT mode.

Connecting to the PC/104-Plus (PCI) Bus

Other PC/104-Plus or PCI-104 expansion boards may be connected to the cpuModule's PC/104-Plus (PCI) bus connector. To connect expansion modules to the PC/104-Plus bus, follow the procedure below to ensure that stacking of the modules does not damage connectors or electronics.



WARNING Do not force the module onto the stack! Wiggling the module or applying too much pressure may damage it. If the module does not readily press into place, remove it, check for bent pins or out-of-place keying pins, and try again.

1. Turn off power to the PC/104-Plus or PCI-104 system or stack.
2. Select and install stand-offs to properly position the cpuModule on the stack.
3. Touch a grounded metal part of the rack to discharge any buildup of static electricity.
4. Remove the cpuModule from its anti-static bag.
5. Check that keying pins in the bus connector are properly positioned.
6. Check the stacking order; if a PCI to ISA bridge card is used to connect any PC/104 modules, make sure an XT bus card will not be placed between two AT bus cards or it will interrupt the AT bus signals.
7. Hold the cpuModule by its edges and orient it so the bus connector pins line up with the matching connector on the stack.
8. Gently and evenly press the cpuModule onto the PC/104-Plus or PCI-104 stack.

There are three additional considerations to make when using the PCI bus:

- Slot selection switches on add-in boards

- PCI bus expansion card power
- PCI bus signaling levels

Slot Selection Switches

Unlike PC/104 cards, PC/104-Plus and PCI-104 expansion cards have a "slot" selection switch or jumpers. In total, there are 4 PCI cards that can be stacked onto the cpuModule with switch positions 0 through 3. The distance from the CPU determines these switch settings. The card closest to the CPU is said to be in slot 0, the next closest slot 1 and so on to the final card as slot 3.



Note This requirement means that all PC/104-Plus and PCI-104 cards must be stacked either on the top or the bottom of the CPU, not on both sides.

The "slot" setting method may vary from manufacturer to manufacturer, but the concept is the same. The CPU is designed to provide the correct delay to the clock signals to compensate for the bus length. The correct switch setting ensures the proper clock delay setting, interrupt assignment, and bus grant/request channel assignment. Refer to the expansion board's manual for the proper settings. Each expansion card must be in a different slot.

PCI Bus Expansion Card Power

+5 Volt DC

The +5 V power pins on the PC/104-Plus (PCI) bus are connected directly to the +5 V pins on the auxiliary power connector, **CN3** (pins 2 and 8).

+3.3 Volt DC

The factory default configuration is to connect the +3.3 V pins on the PCI bus to the auxiliary power connector (**CN3**) by soldering pins 1–2 on solder blob, **B3** (see Table 58 on page 82 for solder blob settings). This is to ensure that the cpuModule's onboard +3.3V supply will not supply power to the PC/104-Plus connector while a PC/104-Plus or PCI-104 power supply is already powering the +3.3V pins.

To supply +3.3V to PC/104-Plus or PCI-104 expansion boards with the onboard +3.3 V power supply, change **B3** from pins 1–2 to pins 2–3. In this configuration, the current limit of the +3.3V connection to the PCI +3.3V via **B3** should not be exceeded (see Table 58 on page 82 for current limitation).

PCI Bus Signaling Levels

The PCI bus can operate at +3.3 V or +5 V signaling levels. The signaling levels for the I/O pins on a PCI bus card are determined by solder blob **B1**. The default is +3.3 V. Refer to Table 58 on page 82 for solder blob settings.



WARNING You will have to ensure that all your expansion cards can operate together at a single signaling level.

Booting the CMX58886CX cpuModule for the First Time

You can now apply power to the cpuModule. You will see:

- A greeting message from the VGA BIOS (if the VGA BIOS has a sign-on message)
- The cpuModule BIOS version information
- A message requesting you press **Delete** to enter the Setup program

If you don't press **Delete**, the cpuModule will try to boot from the current settings. If you press **Delete**, the cpuModule will enter Setup. Once you have configured the cpuModule using Setup, save your changes and reboot.



Note You may miss the initial sign-on messages if your monitor takes a while to power on.

Note By default, cpuModules are shipped with Fail Safe Boot ROM enabled. When Fail Safe Boot ROM is enabled, the system will boot to it exclusively.



Chapter 3 Connecting the cpuModule

This chapter provides information on all CMX58886CX cpuModule connectors.

- Connector Locations* — page 22
- Auxiliary Power (CN3)* — page 24
- Utility Port Connector (CN5)* — page 26
- SVGA Video Connector (CN18)* — page 29
- LVDS Flat Panel Video Connector (CN19)* — page 31
- EIDE Connector (CN10)* — page 32
- ATA/IDE Disk Chip Socket (U16)* — page 33
- Serial Port 1 (CN7) and Serial Port 2 (CN8)* — page 34
- multiPort™ (CN6)* — page 37
- USB 2.0 Connector (CN17)* — page 40
- Ethernet (10/100Base-T and -TX) Connector (CN20)* — page 41
- Audio (CN11)* — page 42
- PC/104-Plus PCI Bus (CN16)* — page 43
- Bridge Link (CN4)* — page 46
- External Power Management (CN12)* — page 47
- Optional RTC Battery Input (CN13)* — page 47
- Fan Power, +5 V (CN14)* — page 47
- Fan Power, Switched (CN15)* — page 48

Connector Locations

Figure 4 shows the connectors and the ATA/IDE Disk Chip socket of the CMX5886CX cpuModule.

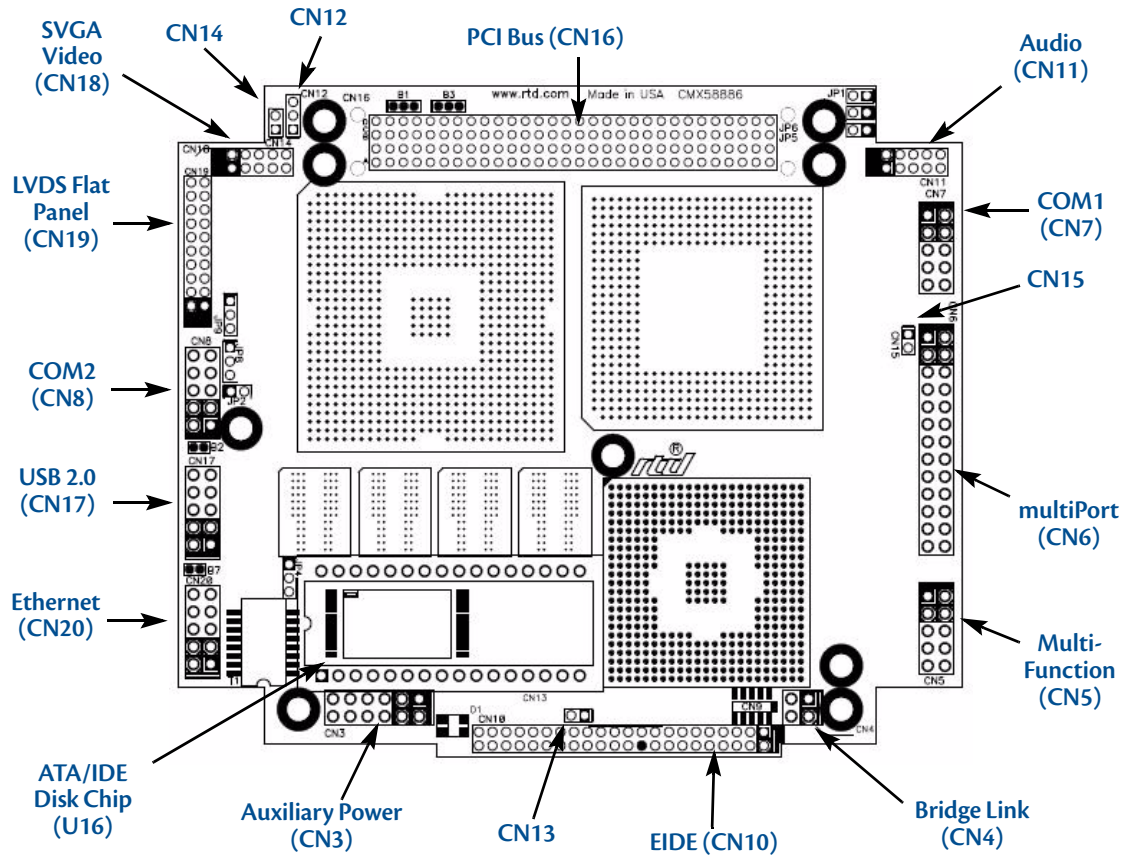


Figure 4 CMX5886CX Connector Locations



Note Pin 1 of each connector is indicated by a white silk-screened square on the top side of the board and a square solder pad on the bottom side of the board. Pin 1 of the bus connectors match when stacking PC104-Plus or PCI-104 modules.

Table 6 CMX58886CX Basic Connectors

Connector	Function	Size
CN3	Auxiliary Power	12-pin
CN4	Bridge Link	4-pin
CN5	Utility Port	10-pin
CN6	multiPort	26-pin
CN7	Serial Port 1 (COM1)	10-pin
CN8	Serial Port 2 (COM2)	10-pin
CN9	Reserved	10-pin
CN10	EIDE Connector	44-pin
CN11	Audio Connector	10-pin
CN12	External Power Management	3-pin
CN13	RTC Battery Input (optional)	2-pin
CN14	Fan Power (+5 V)	2-pin
CN15	Fan Power (switched)	2-pin
CN16	PC/104-Plus (PCI) Bus	120-pin
CN17	USB 2.0	10-pin
CN18	Video (SVGA)	10-pin
CN19	Flat Panel Video (LVDS)	30-pin
CN20	Ethernet	10-pin
U16	ATA/IDE Disk Chip Socket	32-pin

Auxiliary Power (CN3)



WARNING If you connect power incorrectly, the module will almost certainly be destroyed. Please verify power connections to the module before applying power.

Power can be conveyed to the module either through the PCI-104-Plus bus (**CN16**) or through the Auxiliary Power connector (**CN3**). The cpuModule only requires +5 VDC and ground for operation; however, other modules in the system may require +12 VDC, -12 VDC, and -5 VDC. In these instances, the corresponding inputs on the Auxiliary Power Connector (**CN3**) may be used to supply these voltages.

Insufficient current supply will prevent your cpuModule from booting. The gauge and length of the wire used for connecting power to the cpuModule must be taken into consideration. Some power connectors have clip leads on them and may have significant resistance. Make sure that the input voltage does not drop below +4.8 V at the +5 V power pins. (Refer to Table 2 on page 10 for the cpuModule's power requirements). A good rule of thumb is to use wire that can supply twice the power required by the system.



Note Connect two separate wires to the +5V pins (2 and 8) on the power connector to ensure a good power supply connection. We recommend that no less than 18 gauge wire be used and the length of this wire should not exceed 3 ft. Always measure the voltage drop from your power supply to the power pins on the cpuModule. The voltage at pins (2 and 8) should be +5V.

Table 7 Auxiliary Power Connector (CN3)¹

Pin	Signal	Function
1	GND	Ground
2	+5 V	+5 Volts DC
3	+5V_STDBY	+5V Standby (ATX)
4	+12 V	+12 Volts DC
5	Reserved	Reserved
6	-12 V	-12 Volts DC
7	GND	Ground
8	+5 V	+5 Volts DC
9	GND	Ground
10	+3.3 V	See note below
11	PSON#	Power Supply On (ATX)
12	+3.3 V	See note below

1. For more information on the ATX style signals, +5V Standby and PSON#, refer to the *Power Management* section in Chapter 4, *Using the cpuModule*.



Note The +3.3 V pins (10 and 12) on the auxiliary power connector (**CN3**) are connected to the +3.3 V pins on the PC-104-Plus bus by default. These pins be configured to supply power to PC/104-Plus or PCI-104 expansion. If +3.3 V is supplied to the PC/104-Plus connector from the onboard power supply, the +3.3V pins (10 and 12) are not connected. Refer to the **B3** description in Table 58 on page 82 for more information.

Facing the connector pins, the pinout of the Auxiliary Power connector is:

11	9	7	5	3	1
PSON#	GND	GND	Reserved	+5V_STDBY	GND
+3.3 V	+3.3 V	+5 V	-12 V	+12 V	+5 V
12	10	8	6	4	2

Power Supply Protection

The cpuModule has protection circuitry that helps prevent damage due to problems with the +5 V supply, such as reversed polarity, overvoltage, and overcurrent.

Utility Port Connector (CN5)

The utility port connector implements the following functions:

- PC/AT compatible keyboard port
- PS/2 mouse port
- Speaker port (0.1W output)
- Hardware Reset input
- Battery input for Real Time Clock
- Soft Power Button input

Table 8 provides the pinout of the multi-function connector.

Table 8 Utility Port Connector (CN5)

Pin	Signal	Function	In/Out
1	SPKR+	Speaker Output (open collector)	out
2	PWR	+5 V	out
3	RESET	Manual Push-Button Reset	in
4	PWRSW	Soft Power Button	in
5	KBD	Keyboard Data	in/out
6	KBC	Keyboard Clock	out
7	GND	Ground	—
8	MSC	Mouse Clock	out
9	BAT	RTC Battery Input	in
10	MSD	Mouse Data	in/out

Facing the connector pins, the pinout is:

9	7	5	3	1
BAT	GND	KBD	RESET	SPKR+
MSD	MSC	KBC	PWRSW	PWR
10	8	6	4	2

Speaker

A speaker output is available on pins 1 and 2 of the multi-function connector. These outputs are controlled by a transistor to supply 0.1 W of power to an external speaker. The external speaker should have 8 Ω impedance and be connected between pins 1 and 2.

Keyboard

A PS/2 compatible keyboard can be connected to the multi-function connector. Usually PC keyboards come with a cable ending with a 5-pin male PS/2 connector. Table 9 lists the relationship between the multi-function connector pins and a standard PS/2 keyboard connector.

Table 9 Keyboard Connector Pins (CN5)

Pin	Signal	Function	PS/2
5	KBD	Keyboard Data	1
6	KBC	Keyboard Clock	5
7	GND	Ground	3
2	PWR	Keyboard Power (+5 V)	4

To ensure correct operation, check that the keyboard is either an AT compatible keyboard or a switchable XT/AT keyboard set to AT mode. Switchable keyboards are usually set by a switch on the back or bottom of the keyboard.

Mouse

A PS/2 compatible mouse can be connected to the multi-function connector. Table 10 lists the relationship between the multi-function connector pins and a standard PS/2 mouse connector.

Table 10 Mouse Connector Pins (CN5)

Pin	Signal	Function	PS/2
10	MSD	Mouse Data	1
8	MSC	Mouse Clock	5
7	GND	Ground	3
2	PWR	Keyboard Power (+5 V)	4

System Reset

Pin 3 of the multi-function connector allows connection of an external push-button to manually reset the system. The push-button should be normally open, and connect to ground when pushed.

Soft Power Button

Pin 4 of the multi-function connector allows connection of an external push-button to send a soft power signal to the system. The push-button should be normally open, and connect to ground when pushed. For more information on the modes of the Soft Power Button, refer to the *Power Management* section in Chapter 4, *Using the cpuModule*.

Battery

Pin 9 of the multi-function connector is the connection for an external backup battery. This battery is used by the cpuModule when system power is removed in order to preserve the date and time in the real time clock.

Connecting a battery is only required to maintain time when power is completely removed from the cpuModule. A battery is not required for board operation.



WARNING *The optional RTC battery input connector (CN13) should be left unconnected if the multi-function connector (CN5) has a battery connected to pin 9.*

SVGA Video Connector (CN18)

Table 11 provides the pinout of the video connector.

Table 11 SVGA Video Connector (CN18)

Pin	Signal	Function	In/Out
1	VSYNC	Vertical Sync	out
2	HSYNC	Horizontal Sync	out
3	DDCSCL	Monitor Communications Clock	out
4	RED	Red Analog Output	out
5	DDCSDA	Monitor Communications Data	bidirectional
6	GREEN	Green Analog Output	out
7	PWR	+5 V	out
8	BLUE	Blue Analog Output	out
9	GND	Ground	out
10	GND	Ground	out

Facing the connector pins of the SVGA Video connector (**CN18**), the pinout is:

9	7	5	3	1
GND	PWR	DDCSDA	DDCSCL	VSYNC
GND	BLUE	GREEN	RED	HSYNC
10	8	6	4	2

The following table lists the supported video resolutions.

Table 12 SVGA Video Resolutions

Resolution	Colors	Refresh Rates
640 x 480	16, 256, 64k, 16M	60, 70, 72, 75, 85, 100, 120 Hz
720 x 480	256, 64k, 16M	60 Hz
720 x 576	256, 64k, 16M	50 Hz
800 x 600	16, 256, 64k, 16M	60, 70, 72, 75, 85, 100, 120 Hz
960 x 540	256, 64k, 16M	60 Hz
1024 x 768	256, 64k, 16M	60, 70, 75, 85, 100, 120 Hz
1152 x 864	256, 64k, 16M	60, 70, 72, 75, 85, 100 Hz
1280 x 720	256, 64k, 16M	60, 75, 85, 100 Hz
1280 x 768	256, 64k, 16M	60, 75, 85 Hz
1280 x 960	256, 64k, 16M	60, 75, 85 Hz
1280 x 1024	256, 64k, 16M	60, 70, 72, 75, 85, 100, 120 Hz
1400 x 1050	256, 64k, 16M	60, 75, 85 Hz
1600 x 900	256, 64k, 16M	60, 75, 85, 100, 120 Hz
1600 x 1200	256, 64k, 16M	60, 65, 70, 72, 75, 85, 100, 120 Hz
1856 x 1392	256, 64k, 16M	60, 75 Hz
1920 x 1080	256, 64k, 16M	50, 60, 75, 85, 100 Hz
1920 x 1200	256, 64k, 16M	60, 75 Hz
1920 x 1440	256, 64k, 16M	60, 75, 85 Hz
2048 x 1536	256, 64k, 16M	60, 75 Hz

LVDS Flat Panel Video Connector (CN19)

Table 13 provides the pinout of the Flat Panel Video connector (**CN19**). FP_VCC can be either +5 V or +3.3 V, and is selected with jumper **JP8**. FP_VBKLT can be either +5 V or +12 V, and can be selected with **JP9**. See *Jumper Settings and Locations* on page 80 for more details.

Table 13 Flat Panel Video Connector (CN19)

Pin	Signal	Function	In/Out
1	Y0P	LVDS Data 0+	out
2	Y0M	LVDS Data 0-	out
3	DDC_CLK	Panel Detection Clock	out
4	GND	Ground	GND
5	Y1P	LVDS Data 1+	out
6	Y1M	LVDS Data 1-	out
7	DDC_DATA	Panel Detection Data	in/out
8	GND	Ground	GND
9	Y2P	LVDS Data 2+	out
10	Y2M	LVDS Data 2-	out
11	GND	Ground	GND
12	GND	Ground	GND
13	YCP	LVDS Clock+	out
14	YCM	LVDS Clock-	out
15	Y3P	LVDS Data 3+	out
16	Y3M	LVDS Data 3-	out
17	GND	Ground	GND
18	FP_VCC	Power for flat panel electronics	out
19	FP_VBKLT	Power for flat panel backlight	out
20	FP_ENABLK	Enable for Backlight Power	out

Table 14 lists several LVDS panels that were tested with this cpuModule. When evaluating a panel to be used with this cpuModule, review the specifications of the tested panels to assure compatibility.

Table 14 Tested LVDS Panels

Manufacturer	Model Number	Resolution	Color Depth
Optrex	T-51756D121J-FW-A-AA	1024 x 768	18 bit
Optrex	T-51639D084JU-FW-A-AB	1024 x 768	24 bit

EIDE Connector (CN10)

The EIDE connector is a 44-pin, 2 mm connector that can connect to a variety of EIDE or IDE devices. The connector provides all signals and power needed to use a 2.5-inch form factor (laptop) hard drive. Also, the first 40 pins of the connector provide all of the signals needed to interface to a 3.5-inch or 5-inch form factor hard drive, CD-ROM drive, or other EIDE device. The larger form factors use a 40-pin, 0.1 inch spacing connector, so an adapter cable or adapter board is needed to connect to **CN10**.

Table 15 EIDE Connector (CN10)¹

Pin	Signal	Pin	Signal
1	RESET#	2	GND
3	DD7	4	DD8
5	DD6	6	DD9
7	DD5	8	DD10
9	DD4	10	DD11
11	DD3	12	DD12
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	GND	20	N/C
21	DMARQ	22	GND
23	DIOW#:STOP	24	GND
25	DIOR#:HDMARDY#:HSTROBE	26	GND
27	IORDY:DDMARDY#:DSTROB	28	GND
29	DMACK#	30	GND
31	INTRQ	32	N/C
33	DA1	34	PDIAG
35	DA0	36	DA2
37	CS0#	38	CS1#
39	DASP#	40	GND
41	+5 V (logic)	42	+5 V (motor)
43	GND	44	N/C

1. Signals marked with (#) are active low.

ATA/IDE Disk Chip Socket (U16)

The ATA/IDE Disk Chip socket is a 32-pin socket that supports +3.3V or +5V miniature ATA/IDE flash disk chips. The socket allows a true IDE device to be attached to the board with either a socketed or soldered connection. Such true IDE devices are supported by all major operating systems, and do not require special drivers. The socket supports ATA/IDE flash disk chips with capacities up to 4GB..



WARNING Before installing a device in the ATA/IDE Disk Chip socket, the system must be configured in the correct mode. For details on configuring the socket, refer to Chapter 4, Using the cpuModule.

WARNING The ATA/IDE Disk Chip socket does not support conventional SSD memory devices or devices that install as a BIOS extension (such as the M-Systems DiskOnChip®). If such a device is installed, the cpuModule and device will almost certainly be destroyed.

Table 16 ATA/IDE Disk Chip Socket (U16)¹

Pin	Signal	Pin	Signal
1	RESET#	32	VDD ²
2	D7	31	D8
3	D6	30	D9
4	D5	29	D10
5	D4	28	D11
6	D3	27	D12
7	D2	26	D13
8	D1	25	D14
9	D0	24	D15
10	DMARQ/WP#	23	IOWR#
11	IORD#	22	DMACK/CSEL
12	INTRQ	21	IOCS16#
13	A1	20	PDIAG#
14	A0	19	A2
15	CS1FX#	18	CS3FX#
16	GND	17	DASP#

1. Signals marked with (#) are active low.
2. VDD may be set to +3.3 V or +5 V with jumper JP4

Serial Port 1 (CN7) and Serial Port 2 (CN8)

Serial Port 1 (COM1) is implemented on connector **CN7**, and Serial Port 2 is implemented on connector **CN8**. The serial ports are normally configured as PC compatible full-duplex RS-232 ports, but you may use the Setup program to reconfigure these ports as half-duplex RS-422 or full-duplex RS-422 or RS-485. If you reconfigure the ports, you must also select the I/O address and corresponding interrupt using Setup. Table 17 provides the available I/O addresses and corresponding interrupts.

Table 17 Serial Port Settings

I/O Address (hex)	IRQ
03F8	IRQ4
02F8	IRQ3
03E8	IRQ4
02E8	IRQ3

Serial Port UART

The serial ports are implemented with a 16550-compatible UART (Universal Asynchronous Receiver/Transmitter). This UART is capable of baud rates up to 115.2 kbaud in 16450 and 16550A compatible mode, and includes a 16-byte FIFO. Refer to any standard PC-AT hardware reference for the register map of the UART. For more information about programming UARTs, refer to the Appendix.

RS-232 Serial Port (Default)

The default serial port mode is full-duplex RS-232. With this mode enabled, the serial port connectors must be connected to RS-232 compatible devices. Table 18 provides the serial port connector pinout and shows how to connect to an external DB-25 or DB-9 compatible serial connector.

Table 18 Serial Port in RS-232 Mode

Pin	Signal	Function	In/Out	DB-25	DB-9
1	DCD	Data Carrier Detect	in	8	1
2	DSR	Data Set Ready	in	6	6
3	RXD	Receive Data	in	3	2
4	RTS	Request To Send	out	4	7
5	TXD	Transmit Data	out	2	3
6	CTS	Clear To Send	in	5	8
7	DTR	Data Terminal Ready	out	20	4
8	RI	Ring Indicate	in	22	9
9,10	GND	Signal Ground	—	7	5

Facing the serial port's connector pins, the pinout is:

9	7	5	3	1
GND	DTR	TXD	RXD	DCD
GND	RI	CTS	RTS	DSR
10	8	6	4	2

RS-422 or RS-485 Serial Port

You may use Setup to configure the serial ports as RS-422 or RS-485. In this case, you must connect the serial port to an RS-422 or RS-485 compatible device.

When using RS-422 or RS-485 mode, you can use the serial ports in either half-duplex (two-wire) or full-duplex (four-wire) configurations. For half-duplex (2-wire) operation, you must connect RXD+ to TXD+, and connect RXD- to TXD-.



Note The *cpuModule* has a 120 Ω termination resistor. Termination is usually necessary on all RS-422 receivers and at the ends of the RS-485 bus.

Note If required, the termination resistor can be enabled by closing jumper **JP1** for Serial Port 1 (COM1) or **JP2** for Serial Port 2 (COM2).

When using full-duplex (typically in RS-422 mode), connect the ports as shown in Table 19.

Table 19 Full-Duplex Connections

Port 1	Port 2
RXD+	TXD+
TXD+	RXD+
RXD-	TXD-
TXD-	RXD-

When using half-duplex in RS-485 mode, connect the ports as shown in Table 20.

Table 20 Half-Duplex RS-485 Mode

From	To
Port 1 TXD+	Port 1 RXD+
Port 1 TXD-	Port 1 RXD-
Port 1 TXD+	Port 2 RXD+
Port 1 RXD-	Port 2 TXD-

RS-422 and RS-485 Mode Pinout

Table 21 provides the serial port connector pinout when RS-422 or RS-485 modes are enabled.

Table 21 Serial Port in RS-422/485 Mode

Pin	Signal	Function	In/Out	DB-9
1	—	Data Carrier Detect	—	1
2	—	Data Set Ready	—	6
3	RXD-	Receive Data (-)	in	2
4	TXD+	Transmit Data (+)	out	7
5	TXD-	Transmit Data (-)	out	3
6	RXD+	Receive Data (+)	in	8
7	—	Reseved	—	4
8	—	Reseved	—	9
9,10	GND	Signal Ground	out	5

Facing the serial port connector, the pinout is:

9	7	5	3	1
GND	Rsvd	TXD-	RXD-	Rsvd
GND	Rsvd	RXD+	TXD+	Rsvd
10	8	6	4	2



Note When using the serial port in RS-485 mode, the serial transmitters are enabled and disabled under software control. The transmitters are enabled by manipulating the Request To Send (RTS*) signal of the serial port controller. This signal is controlled by writing bit 1 of the Modem Control Register (MCR) as follows:

- If MCR bit 1 = 1, then RTS* = 0, and serial transmitters are disabled
- If MCR bit 1 = 0, then RTS* = 1, and serial transmitters are enabled

Note For more information on the serial port registers, including the MCR, refer to the Serial Port Programming reference on page 99.

multiPort™ (CN6)

RTD's exclusive multiPort can be configured as an Advanced Digital I/O (aDIO™), a parallel port, or a floppy drive. Refer to Chapter 4, *Using the cpuModule*, to configure the multiPort.

multiPort Configured as an Advanced Digital I/O (aDIO™) Port

The multiPort connector (CN6) can be configured as an aDIO port. aDIO is 16 digital bits configured as 8-bit programmable and 8-bit port programmable I/O, providing any combination of inputs and outputs. Match, event, and strobe interrupt modes mean no more wasting valuable processor time polling digital inputs. Interrupts are generated when the 8-bit programmable digital inputs match a pattern, or on any value change event. Bit masking allows selecting any subgroup of 8 bits. The strobe input latches data into the bit programmable port and generates an interrupt. Refer to *multiPort: Advanced Digital I/O Ports (aDIO™)* on page 56 for information on programming the multiPort.

Table 22 multiPort aDIO Pinout

CN6 Pin	Function	CN6 Pin	Function
1	strobe 0	2	P0-4
3	P1-0	4	P0-5
5	P1-1	6	P0-6
7	P1-2	8	P0-7
9	P1-3	10	strobe 1
11	P1-4	12	GND
13	P1-5	14	GND
15	P1-6	16	GND
17	P1-7	18	GND
19	P0-0	20	GND
21	P0-1	22	GND
23	P0-2	24	GND
25	P0-3	26	+5 V

multiPort Configured as a Parallel Port

The parallel port is available on connector **CN6**. Make sure the multiPort in the BIOS Setup is configured to parallel port. You can use the BIOS Setup to select the parallel port's address and associated interrupt, and choose between its operational modes (SPP, ECP, EPP 1.7, and EPP 1.9).

The pinout of the connector enables a ribbon cable to be connected directly to a DB-25 connector, thus providing a standard PC compatible port.



Note For correct operation, keep the length of the cable connecting the cpuModule and parallel device less than 3 meters (10 feet).

Table 23 lists the parallel port signals and explains how to connect it to a DB-25 connector to obtain a PC compatible port.

Table 23 multiPort Connector (CN6) as a Parallel Port

CN6 Pin	Signal	Function	In/Out	DB-25
1	STB	Strobe Data	out	1
2	AFD	Autofeed	out	14
3	PD0	Printer Data 0 (LSB)	out	2
4	ERR	Printer Error	in	15
5	PD1	Parallel Data 1	out	3
6	INIT	Initialize Printer	out	16
7	PD2	Printer Data 2	out	4
8	SLIN	Select Printer	out	17
9	PD3	Printer Data 3	out	5
10	GND	Signal Ground	—	18
11	PD4	Printer Data 4	out	6
12	GND	Signal Ground	—	19
13	PD5	Printer Data 5	out	7
14	GND	Signal Ground	—	20
15	PD6	Printer Data 6	out	8
16	GND	Signal Ground	—	21
17	PD7	Printer Data 7 (MSB)	out	9
18	GND	Signal Ground	—	22
19	ACK	Acknowledge	in	10
20	GND	Signal Ground	—	23
21	BSY	Busy	in	11
22	GND	Signal Ground	—	24
23	PE	Paper End	in	12
24	GND	Signal Ground	—	25
25	SLCT	Ready To Receive	in	13
26	—	+5 V	—	—

multiPort Configured as a Floppy Drive Controller

The multiPort (CN6) can be configured to be a floppy drive controller. This can be configured in the BIOS Setup under Integrated Peripherals. For more information on configuring the multiPort in the BIOS Setep, refer to page 60

Table 24 shows the pin assignments to connect a floppy drive to the multiPort.

Table 24 multiPort Connector Floppy Pinout (CN6)¹

CN6 Pin	Function	DB-25	Floppy Drive Pin
1	DS0#	1	14
2	DR0	14	2
3	INDEX#	2	8 ²
4	HDSEL#	15	32
5	TRK0#	3	26 ²
6	DIR#	16	18
7	WRTPRT#	4	28 ²
8	STEP#	17	20
9	RDATA#	5	30 ²
10	GND	18	—
11	DSKCHG	6	34 ²
12	GND	19	odd pins
13	—	7	—
14	GND	20	odd pins
15	MTR0#	8	10
16	GND	21	odd pins
17	—	9	—
18	GND	22	odd pins
19	DS1#	10	12
20	GND	23	odd pins
21	MTR1#	11	16
22	GND	24	odd pins
23	WDATA#	12	22
24	GND	25	odd pins
25	WGATE#	13	24
26	+5 V	—	—

1. Signals marked with (#) are active low.
2. These signals must be pulled to 5V with separate 470 Ohm resistors.

USB 2.0 Connector (CN17)

Two USB 2.0 compliant connectors are available on connector, **CN17**. Table 25 provides the pinout of the USB connector.

Table 25 USB Connector (CN17)

Pin	Signal	Function	In/Out
1	VCC1	Supply +5 V to USB1	out
2	VCC2	Supply +5 V to USB2	out
3	DATA1-	Bidirectional data line for USB1	in/out
4	DATA2-	Bidirectional data line for USB2	in/out
5	DATA1+	Bidirectional data line for USB1	in/out
6	DATA2+	Bidirectional data line for USB2	in/out
7	GND	Ground	out
8	GND	Ground	out
9	GND	Ground	out
10	GND	Ground	out

Facing the connector pins, the pinout is:

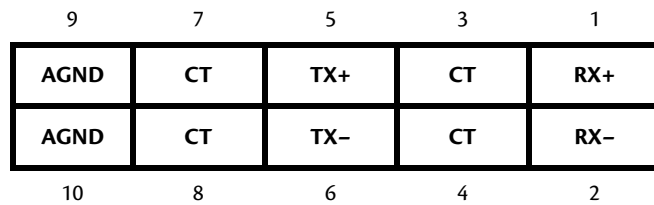
9	7	5	3	1
GND	GND	DATA1+	DATA1-	VCC1
GND	GND	DATA2+	DATA2-	VCC2
10	8	6	4	2

Ethernet (10/100Base-T and -TX) Connector (CN20)

The functionality of the Ethernet port is based on the Intel 82562 Fast Ethernet PCI controller. Table 27 provides the pinout of the Ethernet connector.

Table 26 Ethernet Connector (CN20)

RJ-45 Pin	10-Pin DIL Pin	Signal	Function	In/Out
3	1	RX+	Receive+	in
6	2	RX-	Receive-	in
1	5	TX+	Transmit+	out
2	6	TX-	Transmit-	out
4	3	CT	Termination connected to pin 4	—
5	4	CT	Termination connected to pin 3	—
7	7	CT	Termination connected to pin 8	—
8	8	CT	Termination connected to pin 7	—
—	9	AGND	Ground	—
—	10	AGND	Ground	—



Audio (CN11)

A full featured AC97 compliant audio port is available on CN11. It provides a mono microphone input, stereo line level input, and a stereo output that can be configured as line level or headphone level. The output is configured in the BIOS setup utility. When used as a headphone output, it will drive 32 Ohm speaker at 50mW.

Table 27 Audio Connector (CN11)

10-Pin DIL Pin	Signal	Function	In/Out
1	MIC_VREF	2.2V Supply to bias microphones. 5mA max.	out
2	MIC_IN	Microphone input. 1V RMS or 0.1V RMS.	in
3	GND	Signal GND	GND
4	LINE_IN_LEFT	Line level input for left channel. 1V RMS nominal.	in
5	GND	Signal GND	GND
6	LINE_IN_RIGHT	Line level input for right channel. 1V RMS nominal.	in
7	GND	Signal GND	GND
8	OUTPUT_LEFT	Left channel output. Selectable as line level (1V RMS) or headphone.	out
9	GND	Signal GND	GND
10	OUTPUT_RIGHT	Left channel output. Selectable as line level (1V RMS) or headphone.	out

9	7	5	3	1
GND	GND	GND	GND	MIC_VREF
OUTPUT_RIGHT	OUTPUT_LEFT	LINE_IN_RIGHT	LINE_IN_LEFT	MIC_IN
10	8	6	4	2

PC/104-Plus PCI Bus (CN16)

Connector **CN16** carries the signals of the PC/104-Plus PCI bus. These signals match definitions of the PCI Local Bus specification Revision 2.1. Table 28 list the pinouts of the PC/104-Plus bus connector.

Table 28 PC/104-Plus Bus Signal Assignments¹

Pin	A	B	C	D
1	GND	Reserved/+5V_STDBY ²	+5 V	AD00
2	VIO	AD02	AD01	+5 V
3	AD05	GND	AD04	AD03
4	C/BE0#	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VIO	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3 V	C/BE1#	AD15	+3.3 V
9	SERR#	GND	Reserved / PSON# ²	PAR
10	GND	PERR#	+3.3 V	Reserved / PME# ²
11	STOP#	+3.3 V	LOCK#	GND
12	+3.3 V	TRDY#	GND	DEVSEL#
13	FRAME#	GND	IRDY#	+3.3 V
14	GND	AD16	+3.3 V	C/BE2#
15	AD18	+3.3 V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3 V	AD23	AD22	+3.3 V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3#	VIO	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5 V	AD28	AD27
22	+5 V	AD30	GND	AD31
23	REQ0#	GND	REQ1#	VIO
24	GND	REQ2#	+5 V	GNT0#
25	GNT1#	VIO	GNT2#	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5 V	CLK3	GND
28	GND	INTD#	+5 V	RST#
29	+12 V	INTA#	INTB#	INTC#
30	-12V	REQ3#	GNT3#	GND

1. Signals marked with (#) are active low.

2. Optional signals for ATX power management

PC/104-Plus PCI Bus Signals

The following are brief descriptions of the PC/104-Plus PCI bus signals.

Address and Data

AD[31:00] — Address and Data are multiplexed. A bus transaction consists of an address cycle followed by one or more data cycles.

C/BE[3:0]# — Bus Command/Byte Enables are multiplexed. During the address cycle, the command is defined. During the Data cycle, they define the byte enables.

PAR — Parity is even on AD[31:00] and C/BE[3:0]# and is required.

Interface Control Pins

FRAME# — Frame is driven by the current master to indicate the start of a transaction and will remain active until the final data cycle.

TRDY# — Target Ready indicates the selected device's ability to complete the current data cycle of the transaction. Both IRDY# and TRDY# must be asserted to terminate a data cycle.

IRDY# — Initiator Ready indicates the master's ability to complete the current data cycle of the transaction.

STOP# — Stop indicates the current selected device is requesting the master to stop the current transaction.

DEVSEL# — Device Select is driven by the target device when its address is decoded.

IDSEL[3:0] — Initialization Device Select is used as a chip-select during configuration.

LOCK# — Lock indicates an operation that may require multiple transactions to complete.

Error Reporting

PERR# — Parity Error is for reporting data parity errors.

SERR# — System Error is for reporting address parity errors.

Arbitration (Bus Masters Only)

REQ[3:0]# — Request indicates to the arbitrator that this device desires use of the bus.

GNT[3:0]# — Grant indicates to the requesting device that access has been granted.

System

CLK — Clock provides timing for all transactions on the PCI bus.

RST# — Reset is used to bring PCI-specific registers to a known state.

Interrupts

INTA# — Interrupt A is used to request Interrupts.

INTB# — Interrupt B is used to request Interrupts only for multi-function devices.

INTC# — Interrupt C is used to request Interrupts only for multi-function devices.

INTD# — Interrupt D is used to request Interrupts only for multi-function devices.

Power Supplies and VIO

+5 V — +5 V supply connected to PC/104 bus and auxiliary power connector (**CN3**) +5 V supplies.

+12 V — +12 V supply connected to PC/104 bus and auxiliary power connector (**CN3**) +12 V supplies.

-12 V — -12 V supply connected to PC/104 bus and auxiliary power connector (**CN3**) -12 V supplies.

+3.3 V — The +3.3 V pins on the PC/104-Plus (PCI) connector may be supplied by the onboard +3.3V power supply, however this is not the the default configuration. To supply +3.3V to PC/104-Plus or PCI-104 expansion cards via these pins, solder blob **B3** must be modified. For more information refer to Table 58 on page 82.

VIO — This signal is typically the I/O power to the bus drivers on a PCI bus card. Signaling level is determined by solder blob **B1**. The default is +3.3 V. Refer to Table 58 on page 82 for solder blob settings.

ATX Power Management Signals (optional)

If an ATX power supply is connected to the system, the following signals listed below may be used to wake the system from low power modes. For more information on these signals, refer to the *Power Management* section on page 66.

+5V_STDBY — Some low power modes require that +5 V standby power is applied to the cpuModule during the wake event. This signal is an input to the CPU.

PME# — Power Management Event input

PSON# — This is an active low open-drain output used to turn the power supply on when the system is exiting a low power state.



Note Use of these signals will require board customization. For more information, contact the factory.

Bridge Link (CN4)

The Bridge Link connector allows devices that requires Legacy/ISA interrupts to interface with the cpuModule. When ISA devices are installed in the system (via a PCI to ISA bridge card), the Bridge Link connector provides Legacy/ISA DMA request signals, as well as a serial interrupt signal which permits access to all available system interrupts.

Multiple devices may utilize the serial interrupt signal, SERIRQ, which is decoded on the cpuModule. Only one device may use the DMA request and grant signal pair.

Table 29 Bridge Link (CN4)

Pin	Signal	Function
1	GND	Ground
2	DMAREQ	Legacy/ISA DMA Request
3	SERIRQ	Serial Interrupt Request
4	DMAGNT	Legacy/ISA DMA Grant

Facing the connector pins, the pinout is:

3	1
SERIRQ	GND
DMAGNT	DMAREQ
4	2

External Power Management (CN12)

An external power management connector (CN12) is available for external devices to wake the system from low power states. Some low power modes require that +5 V standby power is applied to the cpuModule during the wake event.

For more information on power management, including a description of the board's supported wake options, refer to the *Power Management* section on page 66.

Table 30 External Power Management (CN12)

Pin	Signal	Function
1	+5V_STDBY	+5 V standby Power
2	GND	Ground
2	PME#	Powerment Management Event input

Optional RTC Battery Input (CN13)

The optional RTC battery input is the connection for an external backup battery. This battery is used by the cpuModule when system power is removed in order to preserve the date and time in the real time clock.

Connecting a battery is only required to maintain time when power is completely removed from the cpuModule. A battery is not required for board operation.

Table 31 Optional RTC Battery Input (CN13)

Pin	Signal	Function
1	BAT	RTC Battery Input
2	GND	Ground



WARNING This optional RTC battery connector (CN13) should be left unconnected if the utility port connector (CN5) has a battery connected.

Fan Power, +5 V (CN14)

If a fan is required to cool the cpuModule, it can be wired to CN14, which provides a continuous connection to +5 V and ground.

Table 32 Fan Power, +5 V (CN14)

Pin	Signal	Function
1	+5V	+5 Volts DC
2	GND	Ground



Note To utilize the thermal fan mode feature in the BIOS, the fan must be connected to CN15

Fan Power, Switched (CN15)

The switched fan power connector (CN15) is an optional fan connector which allows the system to power the fan only when the processor temperature reaches high temperatures.

To utilize this connector, refer to the *Thermal Management* section on page 65.

Table 33 Fan Power, Switched (CN15)

Pin	Signal	Function
1	CPU_FAN_PWM	+5 Volts DC, switched
2	GND	Ground



Chapter 4 Using the cpuModule

This chapter provides information for users who wish to develop their own applications programs for the CMX58886CX cpuModule.

This chapter includes information on the following topics:

- The RTD Enhanced AMI BIOS* — page 50
- Memory Map* — page 53
- I/O Address Map* — page 54
- Hardware Interrupts* — page 55
- multiPort: Advanced Digital I/O Ports (aDIO™)* — page 56
- multiPort: Parallel Port Control* — page 60
- multiPort: Floppy Drive* — page 60
- AC'97 Audio* — page 60
- Ethernet (10/100Base-T and -TX)* — page 60
- IDE Controller Configuration* — page 61
- Real Time Clock Control* — page 63
- Watchdog Timer Control* — page 64
- Thermal Management* — page 65
- Power Management* — page 66
- Multi-Color LED* — page 69
- Reset Status Register* — page 71
- User EEPROM* — page 73
- Features and Settings That Can Affect Boot Time* — page 74
- System Recovery* — page 75
- Basic Interrupt Information for Programmers* — page 76

The RTD Enhanced AMI BIOS

The RTD Enhanced AMI BIOS is software that interfaces hardware-specific features of the cpuModule to an operating system (OS). Physically, the BIOS software is stored in a Flash EPROM on the cpuModule. Functions of the BIOS are divided into two parts.

The first part of the BIOS is known as POST (power-on self-test) software, and it is active from the time power is applied until an OS boots (begins execution). POST software performs a series of hardware tests, sets up the machine as defined in Setup, and begins the boot of the OS.

The second part of the BIOS is known as the CORE BIOS. It is the normal interface between cpuModule hardware and the OS which is in control. It is active from the time the OS boots until the cpuModule is turned off. The CORE BIOS provides the system with a series of software interrupts to control various hardware devices.

Configuring the RTD Enhanced AMI BIOS

The cpuModule Setup program allows you to customize the cpuModule's configuration. Selections made in Setup are stored on the board and are read by the BIOS at power-on.

Entering the BIOS Setup

You can run Setup by rebooting the cpuModule and repeatedly pressing the **Delete** key. When you are finished with Setup, save your changes and exit. The system will automatically reboot.

Field Selection

To move between fields in Setup, use the keys listed below.

Table 34 Setup Keys

Key	Function
→, ←, ↓, ↑	Move between fields
+, -, PgUp, PgDn	Selects next/previous values in fields
Enter	Go to the submenu for the field
Esc	To previous menu then to exit menu

Main Menu Setup Fields

The following is a list of Main Menu Setup fields.

Table 35 Main Menu Setup Fields

Field	Active Keys	Selections
Main	Press Enter to select	Access system information such as BIOS version, EPLD version, and CMOS time and date settings
Advanced	Press Enter to select	Setup advanced cpuModule features
PCIPnP	Press Enter to select	Set PnP and PCI options and control system resources
Boot	Press Enter to select	Set the system boot sequence
Security	Press Enter to select	Setup the supervisor and user access passwords or enable boot sector virus protection
Power	Press Enter to select	Control power management settings, including power supply type, and system wake functions
Thermal	Press Enter to select	Monitor the cpuModule temperature, or activate thermal or fan modes.
Exit	Press Enter to select	Save or discard changes and exit the BIOS, or load the default BIOS settings



Note Future BIOS versions may have slightly different setup menus and options.

Power On Self Test (POST) Codes

Each POST Code represents a series of events that take place in a system during the POST. If the POST fails during a particular POST Code, the system will not boot as expected.

The BIOS uses I/O port 80h to store the active POST Code. A POST Code board is a tool that is used to display the POST Codes on I/O port 80h. This is usually accomplished with two 7-segment LEDs. Such a board is useful for debugging a system that is unable to boot.

Booting to Boot Block Flash with Fail Safe Boot ROM



Note Boards are shipped with Fail Safe Boot ROM enabled. When Fail Safe Boot ROM is enabled, the system will boot to it exclusively.

The Fail Safe Boot ROM is a minimal build of ROM-DOS™ located inside a surface-mounted Boot Block Flash chip. Boot Block Flash is a write-protected flash device that contains the BIOS and extra room where the Fail Safe Boot ROM is stored. Additionally, Fail Safe Boot ROM is an emergency interface accessible by an external computer. The ROM DISK contains utilities for remote access to the system's disk drives. Due to the size of the flash chip, Fail Safe Boot ROM contains an abbreviated selection of the ROM-DOS™ utilities; however, the complete ROM-DOS™ is contained on a CD shipped with the cpuModule.

The purpose of the Fail Safe Boot ROM is to make the cpuModule bootable upon receipt. The Fail Safe Boot ROM can be used as an indicator of the module's functionality when booting problems arise with another operating system. This test can be accomplished by enabling the Fail Safe Boot ROM in the Boot section of the BIOS Setup Utility. Enabling this option forces the cpuModule to boot to Fail Safe Boot ROM.

To boot to the Fail Safe Boot ROM, install jumper **JP5**, and apply power to the system.



Note If power is applied to the system while **JP5** is installed, the multi-color LED will turn red.

Memory Map

The ISA portion of the cpuModule addresses memory using 24 address lines. This allows a maximum of 2^{24} locations, or 16 MB of memory.

Table 36 shows how memory in the first megabyte is allocated in the system.

Table 36 First Megabyte Memory Map

Address (hex)	Description
C0000–FFFFFh ROM	256 KB BIOS in Flash EPROM, shadowed into DRAM during runtime.
C0000–EFFFFh	Run time user memory space. Usually, memory between C0000h and CFFFFh is used for the BIOS of add-on VGA video cards.
A0000–BFFFFh	Normally used for video RAM as follows: EGA/VGA 0A0000–0AFFFFh Monochrome 0B0000–0B7FFFh CGA 0B8000–0BFFFFh
00502–9FFFFh	DOS reserved memory area
00400–00501h	BIOS data area
00000–003FFh	Interrupt vector area

Memory beyond the first megabyte can be accessed in real mode by using EMS or a similar memory manager. See your OS or programming language references for information on memory managers.

I/O Address Map

As with all standard PC/104 boards, the I/O space is addressed by 10 address lines (SA0–SA9). This allows 2^{10} or 1024 distinct I/O addresses. Any add-on modules you install must therefore use I/O addresses in the range of 0–1023 (decimal) or 000–3FF (hex).



Note If you add any PC/104 modules or other peripherals to the system you must ensure they do not use reserved addresses listed below, or malfunctions will occur. The exception to this is if the resource has been released by the user.

Table 37 lists I/O addresses reserved for the CMX58886CX cpuModule.

Table 37 I/O Addresses Reserved for the CMX58886CX cpuModule

Address Range (hex)	Bytes	Device
000–00Fh	16	DMA Controller
010–01Fh	16	Reserved for CPU
020–021h	2	Interrupt Controller 1
022–02Fh	13	Reserved
040–043h	4	Timer
060–064h	5	Keyboard Interface
070–071h	2	Real Time Clock Port
080–08Fh	16	DMA Page Register
0A0–0A1h	2	Interrupt Controller 2
0C0–0DFh	32	DMA Controller 2
0F0–0FFh	16	Math Coprocessor
100–101h	2	Video Initialization
1F0–1FFh	16	Hard Disk ¹
200–201h	2	Reserved
238–23Bh	4	Bus Mouse ²
2E8–2EFh	8	Serial Port ³
2F8–2FFh	8	Serial Port ³
3E8–3EFh	8	Serial Port ³
3F0–3F7h	8	Floppy Disk ¹
3F8–3FFh	8	Serial Port ³
450–453h	4	aDIO ⁴
455h	1	Watchdog Timer ⁵
456–45F	9	EPLD

1. If a floppy or IDE controller is not connected to the system, the I/O addresses listed will not be occupied.
2. If a PS/2 mouse is not connected to the system, the I/O addresses listed will not be occupied.
3. Only one of the I/O addresses shown for a serial port is active at any time. You can use Setup to select which one is active or to disable it entirely.
4. If aDIO is disabled, the I/O addresses listed will not be occupied.
5. If watchdog timer is disabled, the I/O addresses listed will not be occupied.

Hardware Interrupts



Note If you add any expansion modules or other peripherals to the system, you must ensure they do not use interrupts needed by the `cpuModule`, or malfunctions will occur.

The CMX58886CX `cpuModule` supports the standard PC interrupts listed in Table 38. Interrupts not in use by hardware on the `cpuModule` itself are listed as available. Similarly, if the operating system is using APIC, more IRQs will be available.

Table 38 Hardware Interrupts Used on the CMX58886CX `cpuModule`

Interrupt	Normal Use
0	Timer 0
1	Keyboard
2	Cascade of IRQ 8–15
3	COM2
4	COM1
5	Available
6 ¹	Floppy
7	Printer
8	Real Time Clock
9	Available, routed to IRQ 2
10	Available
11	Available
12	Bus Mouse
14 ²	Primary IDE hard disk ³
15	ATA/IDE Disk Chip socket

1. Floppy disk interrupt, INT6, is available for use if no floppy disk is present in the system and floppy disk is disabled in Setup.
2. Hard disk interrupt, INT14, is available for use if no hard disk drive is present in the system and hard disk is disabled in Setup.
3. IRQs 14 and 15 may be available if the IDE controller is configured in Native Mode (refer to *IDE Controller Configuration* — page 61)



Note The `cpuModule` has onboard PCI devices that will claim IRQ lines. In some instances, a PCI device will claim an IRQ line that is required by a legacy device. To reserve an IRQ for a legacy device, refer to the PnP/PCI Configuration Setup fields in the BIOS.

For external devices that require Legacy/ISA interrupts, a serial interrupt signal is available which permits access to the CPU's hardware interrupts. One pair of Legacy/ISA DMA request/grant signals are also available. For more information on the serial interrupt signal, and the DMA request/grand pair, refer to *Bridge Link (CN4)* in Chapter 3, *Connecting the `cpuModule`*

multiPort: Advanced Digital I/O Ports (aDIO™)

Ensure that the BIOS setup has the multiPort set to aDIO mode. This board supports 16 bits of TTL/CMOS compatible digital I/O (TTL signaling). Use the BIOS setup to set the multiPort into its aDIO mode. These I/O lines are grouped into two ports, Port 0 and Port 1. Port 0 is bit programmable; Port 1 is byte programmable. Port 0 supports RTD's Advanced Digital Interrupt modes. The two modes are match and event. Match mode generates an interrupt when an 8-bit pattern is received in parallel that matches the match mask register. Event mode generates an interrupt when a change occurs on any bit. In either mode, masking can be used to monitor selected lines.

When the CPU boots, all digital I/O lines are programmed as inputs, meaning that the digital I/O line's initial state is undetermined. If the digital I/O lines must power up to a known state, an external 10 kΩ resistor must be added to pull the line high or low.

The 8-bit control read/write registers for the digital I/O lines are located from I/O address 450h to 453h. These registers are written to zero upon power up. From 450h to 453h, the name of these registers are **Port 0 data**, **Port 1 data**, **Multi-Function**, and **DIO-Control** register.



Note RTD provides drivers that support the aDIO interface on popular operating systems. RTD recommends using these drivers instead of accessing the registers directly.

Digital I/O Register Set

Table 39 Port 0 Data I/O Address 450h

D7	D6	D5	D4	D3	D2	D1	D0
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Port 0 Data register is a read/write bit direction programmable register. A particular bit can be set to input or output. A read of an input bit returns the value of port 0. A read of an output bit returns the last value written to Port 0. A write to an output bit sends that value to port 0.

Table 40 Port 1 Data I/O Address 451h

D7	D6	D5	D4	D3	D2	D1	D0
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Port 1 Data register is a read/write byte direction programmable register. A read on this register when it is programmed to input will read the value at the multiPort connector. A write on this register when it is programmed as output will write the value to the multiPort connector. A read on this register when it is set to output will read the last value sent to the multiPort connector.

Table 41 Multi-Function I/O Address 452h

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

The multi-function register is a read/write register whose contents are set by the DIO-Control register. See the DIO-Control register description for a description of this register.

Table 42 DIO-Control I/O Address 453h—Read Access

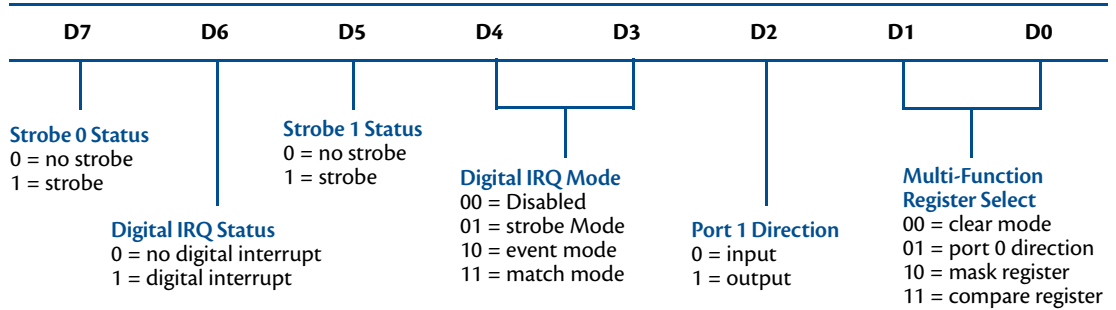


Table 43 DIO-Control I/O Address 453h—Write Access

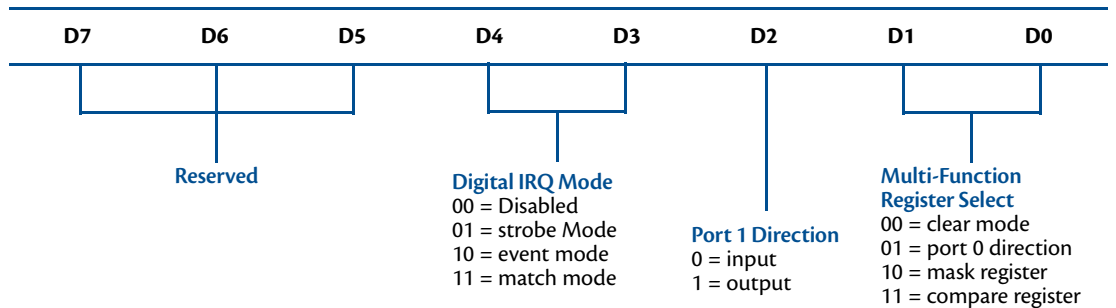


Table 44 Multi-Function at Address 452h¹

read/write	00 clear	X	X	X	X	X	X	X	X
0 in, 1 out	01 Port 0 direction	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
0 no mask, 1 mask	10 DIO mask	M7	M6	M5	M4	M3	M2	M1	M0
read/write	11 compare	C7	C6	C5	C4	C3	C2	C1	C0

1. Contents based on bits D0 and D1 of DIO-Control.

Clear Register:

A read to this register Clears the IRQs and a write to this register sets the DIO-Compare, DIO- Mask, DIO-Control, Port 1, and Port 0 to zeros. A write to this register is used to clear the board.

Port 0 Direction Register:

Writing a zero to a bit in this register makes the corresponding pin of the multiPort connector an input. Writing a one to a bit in this register makes the corresponding pin of the multiPort connector an output.

Mask Register:

Writing a zero to a bit in this register will not mask off the corresponding bit in the DIO-Compare register. Writing a one to a bit in this register masks off the corresponding bit in the DIO-Compare register. When all bits are masked off the aDIOs comparator is disabled. This condition means Event and Match mode will not generate an interrupt. This register is used by Event and Match modes.

Compare Register:

A Read/Write register used for Match Mode. Bit values in this register that are not masked off are compared against the value on Port 0. A Match or Event causes bit 6 of DIO-Control to be set and if the aDIO is in Advanced interrupt mode, the Match or Event causes an interrupt.

Table 45 Wake Control I/O Address 451h

D7	D6	D5	D4	D3	D2	D1	D0
Reserved						Int Mask	Wake Enable
						1 = Interrupt is masked 0=Interrupt is enabled	1=Interrupt triggers a Wake Event 0=Interrupt does not trigger a wake event.

Port 1 Data register is a read/write byte direction

Interrupts

In order to use an interrupt with aDIO, the interrupt must first be selected in the BIOS setup utility under **Advanced, I/O Devices, aDIO Configuration, aDIO Interrupt**. The Digital I/O can use interrupts 3, 5, 6, 7, 10, 11, and 12. The interrupt must also be reserved so that it is not assigned to PCI devices. To reserve the interrupt, enter the BIOS under **PCIPnP** and change the interrupt you wish to use to “Reserved.” Then, select the appropriate interrupt mode in the DIO Control register. Also, verify that the Int Mask bit is cleared in the Wake Control register

Advanced Digital Interrupts

There are three Advanced Digital Interrupt modes available. These three modes are Event, Match, and Strobe. The use of these three modes is to monitor state changes at the multiPort connector. One way to enable interrupts is to set bit 4 of the DIO-Control register to a 1 and select Event or Match mode. The other way to enable interrupts is explained in *Strobe Mode*.

Event Mode

When this mode is enabled, Port 0 is latched into the DIO-Compare register at 8.33 MHz. The aDIO circuitry includes deglitching logic. The deglitching requires pulses on Port 0 to be at least 120 ns in width. As long as changes are present longer than that, the event is guaranteed to register. Pulses as small as 60 ns can register as an event, but they must occur between the rising and falling edge of the 8.33 MHz clock. To enter Event mode, set bits [4:3] of the DIO-Control register to “10”.

Match Mode

When this mode is enabled, Port 0 is latched into the DIO-Compare register at 8.33 MHz. The aDIO circuitry includes deglitching logic. The deglitching requires pulses on Port 0 to be at least 120 ns in width. As long as changes are present longer than that, the match is guaranteed to register. Pulses as small as 60 ns can register as a match, but they must occur between the rising and falling edge of the 8.33 MHz clock. To enter Match mode, set bits [4:3] of the DIO-Control register to “11”.



Note Make sure bit 3 is set BEFORE writing the DIO-Compare register. If you do not set bit 3 first, the contents of the DIO-Compare register could be lost because the Event mode latches in Port 0 into the DIO-Compare register at an 8.33 MHz rate.

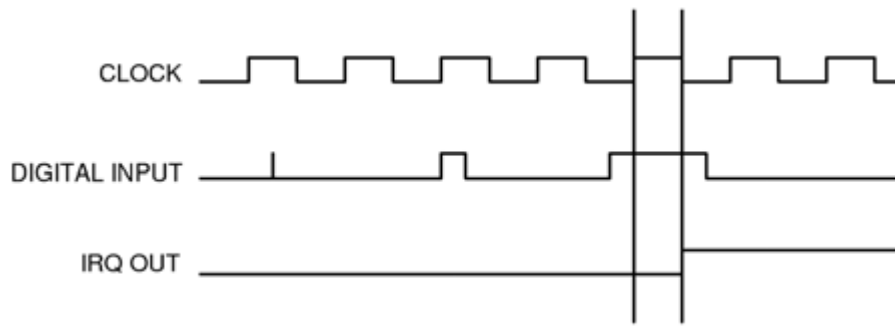


Figure 5 aDIO Match Mode

Strobe Mode

Another interrupt mode supported by aDIO is Strobe mode. This allows the strobe pin of the DIO connector to trigger an interrupt. A low to high transition on the strobe pin will cause an interrupt request. The request will remain high until the Clear Register is read from. Additionally, the Compare Register latched in the value at Port 0 when the Strobe pin made a low to high transition. No further strobes will be available until a read of the Compare Register is made. You must read the Compare Register, and then clear interrupts so that the latched value in the compare register is not lost. To enter Strobe mode, set bits [4:3] of the DIO-Control register to "01".

Wake-on-aDIO

The aDIO Strobe, Match and Event interrupt can be used to generate a wake event. This event can wake the CPU from any power-down mode, including Soft-Off (S5). Wake from aDIO will work as long as +5V Standby power is applied to the board. To use the aDIO to wake the system, Wake from aDIO must first be enabled in the BIOS setup utility. Then the aDIO is configured in the appropriate interrupt mode. The "Wake Enable" bit is then set in the Wake Control Register at 0x454. The CPU can then be placed in a standby mode, and the aDIO interrupt will wake the system.

During system standby, a 32kHz clock is used for the aDIO instead of an 8.33 MHz clock. Therefore, transitions must be at least 30 us in order to trigger a wake event.

If the aDIO is to be used for a wake event only, and not an interrupt, the "Int Mask" bit can be set in the Wake Control Register. This will block the interrupt, but still allow a wake event to occur. The various settings for "Wake Enable" and "Int Mask" are shown in Table 46 below.

Table 46 Interrupt and Wake Event Generation

WakeEnable	Int Mask	Function
0	0	No Interrupt or Wake event is generated
0	1	Interrupt Only
1	0	Wake Event Only
1	1	Interrupt and Wake Event

multiPort: Parallel Port Control

The parallel port may be operated in SPP (output-only), EPP (bidirectional), and ECP (extended capabilities) modes. The mode may be selected in the BIOS, or by application software.

To configure the parallel port in the BIOS, enter the BIOS, and follow the steps below:

1. Under the “Advanced” menu in the BIOS, select the “I/O Device Configuration” submenu
2. Set the multiPort mode to “Parallel Port”
3. When a new “Parallel Port Configuration” appears, select it and configure the parallel port base address, parallel port mode, and IRQ

multiPort: Floppy Drive

The multiPort connector can be configured as a floppy drive. To utilize the floppy controller, the multiPort mode must be first be set to Floppy Drive in the BIOS. The complete process for setting up the multiPort as a floppy drive is described below.

1. With the system powered off, attach a floppy drive with an adapter board to **CN6**.
2. Power on the system and enter the BIOS setup screen by pressing the delete key as the system boots.
3. Set Drive B to **1.44 MB** in the Standard CMOS Settings section of BIOS Setup.
4. Set the multiPort to **Floppy** in the BIOS Setup.
5. If booting to the floppy drive is required, set the first boot device in the boot sequence to floppy drive

When the floppy drive is enabled, a special cable and adapter board is required. For more information about this cable kit, refer to the *Cable Kits and Accessories* section in page 5.

AC'97 Audio

To use the CPU's onboard audio, it must first be enabled in the BIOS. Two signaling levels are supported, so a line out connection can be used for powered speakers, as well as a headphone connection for non-powered speakers.

Once enabled, two audio output modes can be selected:

- **Line Out:** This signaling level should be used for powered speakers.
- **Headphone:** This signaling level should be used for non-powered speakers.

Ethernet (10/100Base-T and -TX)

To use the onboard 10/100 Ethernet controller, Ethernet must first be enabled in the BIOS.

When enabled, the multi-color LED will blink to indicate an Ethernet connection. For more information, refer to the *Multi-Color LED* section on page 69.

IDE Controller Configuration

The CPU's onboard EIDE connector (**CN10**) supports several different drive speed modes, which are BIOS configurable. Supported drive modes will depend on whether a 40-conductor or 80-conductor cable is connecting the EIDE device. The modes and cable detection schemes described below may be set in the BIOS Setup. Similarly, the ATA/IDE Disk Chip socket (**U16**) is BIOS configurable.

Cable Modes

There are two types of cables that may be used for connecting drives to the EIDE connector: 40 conductor cables or 80 conductor cables. Depending on the cable used, different drive speeds are supported. A 40 conductor cable can be used for speeds up to UDMA Mode 2 (Ultra ATA/33).

In order to use drive speeds faster than UDMA Mode 2 (Ultra ATA/33), an 80 conductor cable is required. The BIOS can be configured to detect the presence of an 80 conductor cable. The 80 conductor cable adds a ground wire between each signal, and uses standard 40 pin connectors, therefore an adapter board is required to connect an 80 conductor cable to **CN10**.

Cable Detection

Every time the cpuModule is powered on or a hardware reset is issued, the BIOS will automatically detect the presence of a 80 conductor cable connecting a device to **CN10**. The user selectable cable detection modes are described below.

Device and Host Mode

This method involves a capacitor on the PDIAG signal, which has a pull-up connection to a logic 1 voltage. To determine if the connected cable is 40 conductor or 80 conductor, the CPU first sends a command to the attached device. When the device receives the command, it asserts the PDIAG signal low, forcing the capacitor to discharge. The device then deasserts the PDIAG signal, and monitors the charging of the pulled-up capacitor.

If a 40-conductor cable is connected, the signal will still be low when sampled by the device. If an 80-conductor cable is connected, the capacitor will charge before the device samples PDIAG, and thus read a logic 1. Once the cable is determined, the device reports the type of cable to the CPU.

Host Determination of Cable Type

For this method of detection, the CPU reads the CPBLID pin, which determines if a 40-conductor or 80-conductor cable is connected between the CPU and device. The CPBLID signal is pulled low on the CPU end of the connection by default, indicating that a 40-conductor cable is used if the signal is not driven.

If an 80-conductor cable is connected, the device is able to drive CPBLID high, and the CPU can determine that an 80-conductor cable is connected. When a 40-conductor cable is used, this pin is not connected, and the CPU cannot read the the signal driven by the device.

Device Detect

For device detect mode, the CPU issues a command to the device, which tells the CPU the fastest drive speed mode it can use. The CPU then sets the transfer mode to the fastest speed supported by the device.



WARNING When this cable detection method is enabled, the highest transfer speed supported by the device will be used regardless of whether a 40-conductor or 80-conductor cable is used. If the device speed does not match the cable, data corruption and unexpected behaviors may occur. This mode should not be selected unless the user knows the cable type and the modes supported by the connected EIDE device.

Legacy Mode and Native Mode IDE

The onboard EIDE controller may be configured as either a Legacy or Native Mode IDE controller in the BIOS Setup. However, the operating system must support the selected mode for the device to operate correctly. The default configuration for the controller is Legacy Mode, as this is supported by most operating systems.

Legacy Mode

Legacy mode is the default configuration of the onboard EIDE controller. When in this mode, the controller will be fixed to use two interrupts: IRQs 14 and 15. Similarly, the I/O address of the controller will be fixed in the system. When in Legacy Mode, only a primary and secondary channel may be used in the system.

Native Mode

Native Mode allows more flexibility, as the system resources used by the IDE controller may be modified. When in Native Mode, the IDE controller only requires a single IRQ. Unlike Legacy Mode, this IRQ may be changed by the user or the operating system for better distribution of the system IRQs. When IRQs in the system are more evenly distributed, interrupt latency is minimized. The base address of the controller may also be modified.

Configuring the ATA/IDE Disk Chip Socket

The cpuModule was designed to be used in embedded computing applications. In such environments, magnetic media like hard disks and floppy disks are not very desirable. It is possible to eliminate magnetic storage devices by placing your operating system and application software into the cpuModule's ATA/IDE Disk Chip socket.

Before installing a device in the ATA/IDE Disk Chip socket, it is highly recommended to first configure the secondary IDE controller and device mode in the BIOS setup.

The secondary IDE controller must be enabled in the BIOS to allow read and write access to the device. When a device is installed in the socket, it will always appear as a master on the cpuModule's secondary IDE controller.

From the BIOS setup screen, the user can also configure whether the socket contains a DMA mode or PIO mode device.

- **DMA Mode:** DMA mode will reduce CPU overhead. This mode can be set to use multi-word DMA.
- **PIO Mode:** When the socket is in PIO mode, PIO transfers are supported. PIO Mode supports write protection.

Real Time Clock Control

The cpuModule is equipped with a real time clock (RTC) which provides system date and time functions, and also provides 128 nonvolatile memory locations. The contents of these memory locations are retained whenever an external backup battery is connected, whether or not system power is connected.

You may access the RTC date, time, and memory using an index and data register at I/O addresses 70h and 71h. Address 70h is the Index register. It must be written with the number of the register to read or write. Refer to the map below for valid choices for the index. Data is then written to or read from the selected register by writing or reading (respectively) the data register at address 71h.



WARNING Do NOT change values stored in the RTC registers listed as RESERVED in the table below. Doing so will interfere with proper cpuModule operation.

Registers of the RTC are shown below.

Table 47 Real Time Clock Registers

Registers (hex)	Registers (decimal)	Number of Bytes	Function
00h	0	1	BCD Seconds
02h	2	1	BCD Minutes
04h	4	1	BCD Hours
06h	6	1	Day of Week
07h	7	1	Day of Month
08h	8	1	Month
09h	9	1	Year
0A–0Dh	10–13	4	RTC Control Registers
0E–31h	14–49	36	RESERVED—Do not modify!
32h	50	1	BCD Century
33–3Fh	51–63	13	RESERVED—Do not modify!
40–7Fh	64–127	64	User RAM

Watchdog Timer Control

The cpuModule includes a watchdog timer, which provides protection against programs "hanging", or getting stuck in an execution loop where they cannot respond correctly. When enabled, the watchdog timer must be periodically reset by your application program. If it is not refreshed before the time-out period expires, it will cause a hardware reset of the cpuModule.

The watchdog time-out period is typically 1.1 seconds, but can vary between 550 ms and 1.65 seconds. Because of operating system latency, it is recommended that the watchdog be refreshed at half of the period, or every 275 ms.

Before using the Watchdog timer, it must be enabled in the BIOS setup utility. When it is disabled in the BIOS, the watchdog register does not appear in I/O space and it will not generate an a reset.



Note Enabling the watchdog timer in the BIOS does not actually arm it. The watchdog timer can be armed by accessing I/O address 455h, a explained below.

Three functions have been implemented on the cpuModule for controlling watchdog timer control. These are:

- **Arm:** The watchdog timer can be enabled by writing a 1 to bit 7 of I/O port 0x455. To ensure compatability with future designs, you should read the register and only change the bit you need to change.
- **Disarm:** The watchdog timer is disabled by writing a 0 to bit 7 of I/O port 0x455. To ensure compatability with future designs, you should read the register and only change the bit you need to change.
- **Refresh:** The watchdog timer is refreshed by reading from I/O port 0x455. After you enable the watchdog timer, you must refresh it at least once every 550 ms.

Table 48 Wake Control I/O Address 455h

D7	D6	D5	D4	D3	D2	D1	D0
Watchdog Enable	Reserved						
1=Watchdog timer is disabled and will not generate an interrupt							
0=Watchdog Timer is enabled and needs to be refreshed							

Thermal Management

The cpuModule has several thermal features which can be used to monitor and control the board's temperature when extreme operating conditions are prevalent.

Thermal Monitor and Thermal Throttling

The Intel® Thermal Monitor is a feature on the CMX58886CX that automatically throttles the CPU when the CPU exceeds its thermal limit. The maximum temperature of the processor is defined as the temperature that the Thermal Monitor is activated. The thermal limit and duty cycle of the Thermal Monitor cannot be modified. The Thermal Monitor can be disabled by the BIOS for applications where deterministic speed is more important than device failure due to thermal runaway.

In addition to the Thermal Monitor, conventional Thermal Throttling is also provided. This forces the CPU to skip clock cycles when it exceeds a thermal limit. The thermal limit and duty cycle of thermal throttling can be modified in the BIOS, where both the PCB and CPU temperature can be set to activate thermal throttling. The CPU and PCB temperature are displayed in the *Thermal* section of the BIOS setup..



Note The CPU and PCB temperatures displayed in the BIOS are approximate and should not be used to validate a cooling solution.

Fan Mode

The CPU fan can be controlled by the CPU when connected to the switched fan power connector (**CN15**). Two fan modes are supported, which can be toggled in the BIOS setup.

- **Always On:** When in this mode, the fan is always powered by the CPU.
- **Auto:** This mode allows the system to keep the fan turned off until the CPU is hot. When the fan mode is set to auto, the CPU's power consumption is reduced.



Note If the CPU fan is connected to the continuous +5 V fan connector (**CN14**), changing the fan mode options in the BIOS will not affect the fan, as it will always be turned on.

Further Temperature Reduction

The cpuModule's temperature is directly related to power consumption. Reducing the power consumption of the CPU will have an effect on the CPU's temperature. Suggested methods for reducing the CPU's power consumption can be found in the *Power Management* section on page 66.

Power Management

The CMX58886CX cpuModule supports various powering mechanisms which allow the cpuModule to monitor power consumption and temperature, and achieve minimal power consumption states. These unique features include thermal monitoring and thermal throttling, as well as low power modes including APM and ACPI configurations. Various wake options are also available to resume normal system power when power modes are no longer necessary for the application.

Advanced Power Management (APM)

Legacy Advanced Power Management (APM 1.2) options such as setting suspend and standby timeout intervals, can be configured in the BIOS on the cpuModule.

Advanced Configuration and Power Interface (ACPI)

The cpuModule supports several different ACPI low power modes, including the S1, S3, S4, and S5 sleeping states. Suspend modes S1 and S3 can be enabled in the BIOS, where the soft power button on the utility port (**CN5**) can be setup as a suspend button (see *Power Button Modes*). Sleep modes S4 and S5 are typically setup by the operating system.

The cpuModule's ACPI suspend modes are described below

- **S1 (Power on Suspend):** The S1 low power state consumes the most power of all supported ACPI sleep modes. In this mode, the CPU stops executing instructions, but power to the CPU and RAM is maintained.
- **S3 (Suspend to RAM):** Everything in the system is powered off except for the system memory. When the system wakes from this mode, operating systems typically allow applications to resume where they left off, as the state of the application is preserved in memory.
- **S4 (Hibernate):** When the system enters this state, the operating system will typically save the current state of applications and relevant data to disk, thus allowing the system RAM to be powered down.
- **S5 (Soft-Off):** The system is in a soft off state, and must be rebooted when it wakes.

Power Button Modes

The soft power button input of the utility port connector (**CN5**) can be configured as a suspend button to send a soft power signal to the system. The power buttons function can be changed to a suspend button in the BIOS. When configured in suspend mode, if S1 or S3 are enabled, pressing the power button will force the system into the specified sleep state.

Low-Power Wake Options

The cpuModule supports several methods of waking from a low power state. Several of these wake options are BIOS configurable, and can be accessed directly from the "Power" menu in the BIOS setup:

- **Resume on Ring:** While in a low power mode, the ring indicator input of either COM port may be used to wake the system.
- **Resume on aDIO:** This option allows the system to use an aDIO Strobe, Match, or Event interrupt to generate a wake event. This event can wake the CPU from any power-down mode, including Soft-Off (S5). For more information, refer to the section titled *Wake-on-aDIO* on page 59.
- **Resume on PME#:** When enabled, the system can wake when a signal is applied to the External Power Management connector (**CN12**). This includes wake-up on onboard LAN controller. The PME# signal is also available on the PC/104-Plus (PCI) bus connector.

- **Resume on RTC Alarm:** The RTC Alarm allows the system to turn on at a certain time every day. This option is BIOS configurable.

AT vs. ATX Power Supplies

Both AT and ATX power supplies may be used with the CMX58886CX cpuModule, however AT power supplies do not provide any standby power to the cpuModule. When an AT power supply is used to power the system, low power modes that require a standby power to wake the system will not be fully supported.

ATX power supplies do provide a standby power, thus allowing the system to utilize all low power modes supported by the hardware. When an ATX supply is used to power the cpuModule, lower power modes can be achieved. During these low power modes, the standby power from the ATX power supply provides power to a small circuit on the CPU, which is used to watch for a system wake event.

ATX Power Supply Signals

The auxiliary power connector (**CN3**) provides two ATX style signals., +5V Standby and PSON#. The +5V Standby rail is used to power certain parts of the cpuModule when the main power supply is turned off, i.e. during Suspend-to-RAM (S3), Hibernate (S4), or Soft-Off (S5) power modes. The PSON# signal is an active low open-drain output that signals the power supply to turn on. Use of these signals allows the power consumption to drop to below 1W during standby modes, and still enable any of the wake events.

The CPU monitors power supply inputs, and also generates the ATX Power Good signal.

Reducing Power Consumption

In addition to the CPU's low power modes, power consumption can further be reduced by making some modifications to the BIOS setup. When the following features are modified, the CPU's power consumption will decrease:

- **Memory Speed:** Changing the DDR DRAM clock frequency will reduce power consumption, however memory performance will also be reduced.
- **Ethernet:** Can be disabled in the BIOS
- **Serial Ports:** Can be disabled in the BIOS
- **LVDS Flat Panel:** If an LVDS panel is not connected to the cpuModule while using a VGA monitor, setting the BIOS to use only a CRT (VGA) monitor will reduce power consumption.
- **Fan Mode:** Set the fan to auto mode so it is used only when the processor reaches high temperatures. This option will only effect the fan if it is connected to the switched fan power connector (**CN15**).
- **Multi-Color LED:** Can be disabled in the BIOS

Multi-Color LED

The CMX58886CX has a Multi-Color LED located beside the EIDE connector (**CN10**) which can be enabled or disabled in the BIOS setup screen. The color of the LED indicates the status of the board, as shown in Table 49.

Table 49 LED Colors

Color	Description
Green	Normal Operation
Blue	On Board IDE Activity
Red	cpuModule is in reset ¹
Yellow (Red + Green)	cpuModule is in Standby
White (R+G+B)	cpuModule is approaching thermal limit (CPU is throttled if enabled)
Cyan (Blue + Green)	Ethernet Link at 10 Mbps
Magenta (Blue + Red)	Ethernet Link at 100 Mbps
Blink	Ethernet Activity

1. If power is applied to the cpuModule while jumper **JPS** is installed, the LED will be red. This does not indicate that the board is in reset

The LED can also be controlled manually by writing to I/O Port 456h, as shown in Table 50 and Table 51.

Table 50 Multi-Color LED I/O Address 456h

D7	D6	D5	D4	D3	D2	D1	D0
User EEPROM	User EEPROM	User EEPROM	Reserved	Reserved	Multi-Color LED		



Note When writing to I/O Port 456h, only the lower three bits of the register should be modified. Modifying the upper bits will effect the User EEPROM

The following table lists the color displayed and the value written.

Table 51 Manual LED Colors

I/O Port 456h Value	Color
0x00	Automatic (see Table 49)
0x08	Off ¹
0x09	Blue
0x0A	Green
0x0B	Cyan (Green + Blue)
0x0C	Red
0x0D	Magenta (Red + Blue)
0x0E	Yellow (Red + Green)
0x0F	White (Red + Green + Blue)

1. Disabling the LED will reduce system power consumption.

Reset Status Register

The cpuModule has several different signals on board which can cause a system reset. If a reset occurs, the reset status register can be used to see which reset or resets have been asserted on the cpuModule.

The user has the ability to see which resets have been asserted. Resets can also be cleared.

- **Examine Resets:** Reading from I/O port 0x457 will indicate if a reset has been asserted. If a 1 is read, the corresponding reset has been asserted. If a 0 is read from the bit, the reset has not been asserted
- **Clear Reset:** Each reset can be cleared by writing a 1 to the selected bit of I/O port 0x457.

Table 52 Reset Status I/O Address 457h - Read Access

D7	D6	D5	D4	D3	D2	D1	D0
Main Power (+5V) 0 = reset asserted 1 = no reset	CPU Core Power 0 = reset asserted 1 = no reset	Non-Standby Power 0 = reset asserted 1 = no reset	Memory Power 0 = reset asserted 1 = no reset	Standby Power 0 = reset asserted 1 = no reset	Reserved	PCI Reset 0 = reset asserted 1 = no reset	Utility Reset 0 = reset asserted 1 = no reset

Table 53 Reset Status I/O Address 457h - Write Access

D7	D6	D5	D4	D3	D2	D1	D0
Main Power (+5V) 1 = clear reset	CPU Core Power 1 = clear reset	Non-Standby Power 1 = clear reset	Memory Power 1 = clear reset	Standby Power 1 = clear reset	Reserved	PCI Reset 1 = clear reset	Utility Reset 1 = clear reset

Table 54 Reset Status Description and Priorities

I/O Address 457h	Reset Signal	Reset Priority ¹	Description
D7	Main Power (+5V)	2	Main input power to cpuModule (+5V)
D6	CPU Core Power	3	CPU core powers supply
D5	Non-Standby Power	3	Power supplies that are not for standby power
D4	Memory Power	3	Power to onboard memory banks
D3	Standby Power	1	Standby power supplies
D2	Reserved	-	Reserved
D1	PCI Reset	4	PCI bus reset signal
D0	Utility Reset	-	Utility connector push button reset ²

1. When a reset is asserted, all resets with a higher reset priority will also be asserted. For example, if the standby power reset is asserted, all other resets will also be asserted.
2. The BIOS allows the user to change the function of the utility connector's push button reset. If the push button is not configured as a reset, this bit will always read a 0 (asserted) when the reset button has been pushed.

User EEPROM

A 512kB serial EEPROM (Atmel AT93C66) is available on the cpuModule for the user to save nonvolatile parameters on the cpuModule. The EEPROM can be accessed by reading and writing to I/O address 456h, as shown in the following table.

Table 55 User EEPROM I/O Address 456h

D7	D6	D5	D4	D3	D2	D1	D0
CS	SK	DI	DO	Reserved	(Multi-Color LED)		

Table 56 EEPROM Register Description

Bit	Signal	Function	Read / Write
D7	CS	Chip Select	Read / Write
D6	SK	Serial Data Clock	Read / Write
D5	DI	Serial Data Input	Read / Write
D4	DO	Serial Data Output	Read Only
D3		Reserved	
D2		(Multi-Color LED)	
D1		(Multi-Color LED)	
D0		(Multi-Color LED)	

Features and Settings That Can Affect Boot Time

The boot time of a system is dependent upon numerous system settings as well as devices attached to a system.. This section addresses some devices and settings that can increase or decrease a system's boot time.

Quick Boot

The BIOS contains a Quick Boot option that minimizes the boot time of the system. Quick Boot eliminates the exhaustive tests that are performed during Power On Self Test (POST) while maintaining the functionality of the board (see note 1 below). By enabling the Quick Boot feature, your system can achieve 5-second boot times.

Add-On Cards With BIOS Extensions

Some add-on cards have an integrated BIOS extension. The most common examples are SCSI controllers and network cards with boot ROMs. During POST, the BIOS executes the card's extension code. This extension code is third-party code, which is beyond RTD's control. The BIOS extension will most likely increase the boot time. Exactly how much it increases boot time will depend on the particular card and firmware version.

VGA Controller

VGA controllers have a VGA BIOS that must be initialized during POST. It can take some time to initialize the VGA BIOS. Exactly how long will depend on the particular VGA controller and BIOS version.

Hard Drive Type

During IDE initialization, each IDE device must be probed. Some devices take longer to probe. 2.5-inch hard drives tend to take longer than 3.5-inch ones, because they spin at a lower RPM.

Monitor Type

Some monitors take a while to power on. Desktop flat panels are especially slow. This does not affect the actual boot time of the CPU. However, the CPU may boot before the monitor powers on.

NVRAM Updates

System configuration data is stored in the onboard NVRAM. When the system configuration changes, this information must be updated. If an update is necessary, it will happen at the end of POST (the BIOS will display an "Updating NVRAM..." message). The NVRAM update takes a few seconds and increases the boot time. Once the NVRAM is updated, boot times will return to normal.

NVRAM updates only happen when the system configuration changes. They do not happen spuriously. They are usually triggered by adding or removing a PCI device from a stack. Updates can also be triggered by altering the Plug-n-Play configuration of the BIOS.

Boot Device Order

The BIOS contains a list of devices to try booting from. If you wish to boot to a particular device (for example, a hard drive), make sure that it is first in the boot order. This will speed up boot times.

System Recovery

Loading Default BIOS Settings

The default BIOS can be restored either by using the “Load Defaults” option in the BIOS, or by installing jumper **JP5** (see Figure 6 on page 81). In most cases, the easiest way to load default settings is by setting them in the BIOS. For other unique cases, jumper **JP5** provides an alternative method of restoring the BIOS settings.

To restore the default BIOS settings with jumper **JP5**, follow the procedure below.

1. Remove power from the system.
2. Install **JP5**.
3. Apply power to the system. The cpuModule will then load its default settings. Note that the multi-color LED will be red if power is applied while **JP5** is installed.
4. Reboot and press **Delete** to enter BIOS Setup.
5. Save the BIOS settings and exit, allowing the system to boot to the FSBR.
6. The next time the system is powered, the BIOS Setup will be configured to use the default settings.

Booting to the Fail Safe Boot ROM (FSBR)

If your system is in configuration that will not allow it to boot, the Fail Safe Boot ROM is a minimal build of ROM-DOS which can be booted to for system debugging. To boot to the FSBR, follow the instructions below.

1. Remove power from the system.
2. Install **JP5**. This will force the cpuModule to boot using the default BIOS configuration.
3. Apply power to the system. The cpuModule will then boot to the Fail Safe Boot ROM image. Note that the multi-color LED will be red if power is applied while **JP5** is installed.
4. Press the {Del.} key to enter Setup, or allow the cpuModule to boot to Failsafe

Basic Interrupt Information for Programmers

An interrupt is a subroutine called asynchronously by external hardware (usually an I/O device) during the execution of another application. The CPU halts execution of its current process by saving the system state and next instruction, and then jumps to the interrupt service routine, executes it, loads the saved system state and saved next instruction, and continues execution. Interrupts are good for handling infrequent events such as keyboard activity. Interrupts on this `cpuModule` are controlled by two Intel 8259-equivalent interrupt controllers containing 13 available interrupt request lines.

What happens when an interrupt occurs?

An `IRQx` pin on the PC/104 bus makes a low to high transition while the corresponding interrupt mask bit is unmasked and the PIC determines that the IRQ has priority, that is, the PIC interrupts the processor. The current code segment (CS), instruction pointer (IP), and flags are pushed onto the stack. The CPU then reads the 8-bit vector number from the PIC, and a new CS and IP are loaded from a vector—indicated by the vector number—from the interrupt vector table that exists in the lowest 1024 bytes of memory. The processor then begins executing instructions located at CS:IP. When the interrupt service routine is completed the CS, IP, and flags that were pushed onto the stack are popped from the stack into their appropriate registers and execution resumes from the point where it was interrupted.

How long does it take to respond to an interrupt?

A DOS system can respond to an interrupt between 6 and 15 μ s. A Windows system can take a much longer time when a service routine has been installed by a device driver implemented as a DLL—from 250 to 1500 μ s or longer. The time the CPU spends in the interrupt depends on the efficiency of the code in the ISR. These numbers are general guidelines and will fluctuate depending on operating system and version. Minimum time between two IRQ requests is 125 ns per ISA specification.

Interrupt Request Lines

To allow different peripheral devices to generate interrupts on the same computer, the ISA bus has eight different interrupt request (IRQ) lines. On the ISA bus, a transition from low to high on one of these lines generates an interrupt request, which is handled by the PC's interrupt controller. On the PCI bus, an interrupt request is level-triggered.

The interrupt controller checks to see if interrupts are to be acknowledged from that IRQ and, if another interrupt is already in progress, it decides if the new request should supersede the one in progress or if it has to wait until the one in progress is done. This prioritizing allows an interrupt to be interrupted if the second request has a higher priority. The priority level is based on the number of the IRQ; IRQ0 has the highest priority, IRQ1 is second-highest, and so on through IRQ7, which has the lowest. Many of the IRQs are used by the standard system resources. IRQ0 is used by the system timer, IRQ1 is used by the keyboard, IRQ3 by COM2, IRQ4 by COM1, and IRQ6 by the disk drives. Therefore, it is important to know which IRQ lines are available in your system for use by the `cpuModule`.

Intel 8259 Programmable Interrupt Controller

The chip responsible for handling interrupt requests in the PC is the Intel 8259 Programmable Interrupt Controller. To use interrupts, you need to know how to read and set the Intel 8259's interrupt mask register (IMR) and how to send the end-of-interrupt (EOI) command to the Intel 8259.

Each bit in the IMR contains the mask status of an IRQ line; bit 0 is for IRQ0, bit 1 is for IRQ1, and so on. If a bit is set (1), then the corresponding IRQ is masked and will not generate an interrupt. If a bit is clear (0), then the corresponding IRQ is unmasked and can generate interrupts. The IMR is programmed through port 21h.



Note When in APIC mode, the PIC is programmed differently, and IRQ routing behaves differently. For more information, refer to the APIC datasheets and specifications provided by Intel.

PCI Interrupts

PCI devices can share interrupts. The BIOS or operating system may assign multiple PCI devices to the same IRQ line. Any interrupt service routine (ISR) written for PCI devices must be able to handle shared interrupts. Refer to *Interrupt-Driven PC System Design* (ISBN: 0-929392-50-7) for more information on PCI interrupts.

Writing an Interrupt Service Routine (ISR)

The first step in adding interrupts to your software is to write the ISR. This is the routine that will automatically be executed each time an interrupt request occurs on the specified IRQ. An ISR is different than standard routines that you write. First, on entrance, the processor registers should be pushed onto the stack BEFORE you do anything else. Second, just before exiting your ISR, you must clear the interrupt status flag and write an end-of-interrupt command to the Intel 8259 controller. Finally, when exiting the ISR, in addition to popping all the registers you pushed on entrance, you must use the IRET instruction and not a plain RET. The IRET automatically pops the flags, CS, and IP that were pushed when the interrupt was called.

Most C compilers allow you to identify a procedure (function) as an interrupt type and will automatically add these instructions to your ISR, with one important exception: most compilers do not automatically add the end-of-interrupt command to the procedure; you must do this yourself. Other than this and the few exceptions discussed below, you can write your ISR just like any other routine. It can call other functions and procedures in your program and it can access global data. If you are writing your first ISR, RTD recommends focusing on the basics, such as incrementing a global variable.

Most operating systems have restrictions on what instructions can be called in your ISR. Consult your OS documentation for details on writing your ISR.



Note A complete explanation of interrupt programming is beyond the scope of this manual. For more information on interrupts, refer to the Appendix.

Sample Code

RTD's drivers provide examples of ISR's and interrupt handling. Refer to them as working examples. These drivers were shipped with your cpuModule, but they can also be downloaded from RTD's website (www.rtd.com).



Appendix A Hardware Reference

This appendix provides information on CMX58886CX cpuModule hardware, including:

Jumper Settings and Locations — page 80

Onboard PCI Devices — page 83

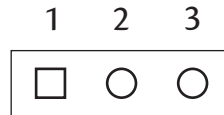
Physical Dimensions — page 84

Jumper Settings and Locations

Many cpuModule options are configured by positioning jumpers. Jumpers are labeled on the board as **JP** followed by a number.

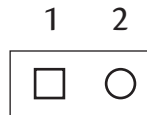
Some jumpers have three pins, allowing three settings:

- Pins 1 and 2 connected (indicated as “1–2”)
- Pins 2 and 3 connected (indicated as “2–3”)
- No pins connected



Some jumpers have two pins, allowing two settings:

- Pins 1 and 2 connected (indicated as “closed”)
- Pins 1 and 2 unconnected (indicated as “open”)



Solder jumpers are located on the cpuModule’s bottom side. Solder blobs are factory-set and rarely changed. Contact RTD Technical Support for further information.

Figure 6 shows the jumper and solder blob locations that are used to configure the cpuModule. In both top and bottom figures, the PC/104 bus connector is at the six o'clock position. Table 57 lists the jumpers and their settings. Table 58 lists the solder blobs and their settings.

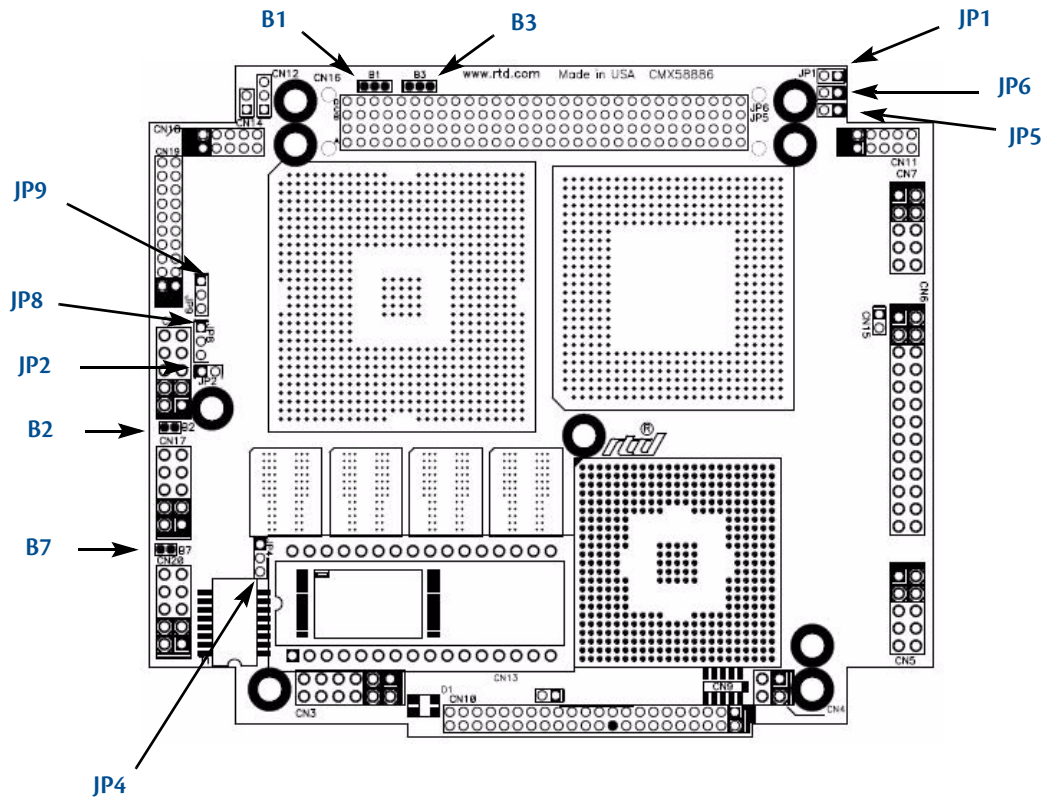


Figure 6 CMX5886CX Jumper and Solder Blob Locations (top side)

Table 57 CMX5886CX Jumpers

Jumper	Pins	Function	Default
JP1	2	Enable/disable 120 Ω series termination to COM1 (CN7) in RS-422/485 modes	open
JP2	2	Enable/disable 120 Ω series termination to COM2 (CN8) in RS-422/485 modes	open
JP4	3	Select power for the ATA/IDE Disk Chip pins 1–2: +5 V pins 2–3: +3.3 V	pins 2–3
JP5	2	Install to load the default BIOS settings (for more information, refer to the following section of the manual: <i>System Recovery</i> — page 75). Note that the multi-color LED will be red if JP5 is installed.	open
JP6	2	Reserved	open
JP8	3	Select power for the flat panel electronics pins 1–2: +3.3 V pins 2–3: +5 V	pins 1–2
JP9	3	Select power for flat panel backlight pins 1–2: +12 V pins 2–3: +5 V	pins 2–3

Table 58 CMX58886CX Solder Blobs

Solder Blob	Positions	Function	Default
B1	3	Connect the PCI VI/O to either +3.3 V or +5 V positions 1–2: +5 V positions 2–3: +3.3 V	pins 2–3
B2	2	Solder closed to connect USB ground to frame ground	open
B3	3	Solder jumper B3 can connect +3.3 V on the PCI bus to either the onboard +3.3V or to the board's +3.3 V supply pins on the auxiliary power connector (CN3). positions 1–2: connect PCI +3.3 V to CN3 , pins 10 and 12 positions 2–3: connect PCI +3.3 V to onboard +3.3 V for powering <i>PC/104-Plus</i> or PCI-104 expansion cards (current should not exceed 1A)	pins 1–2
B7	2	Solder closed to connect Ethernet ground to frame ground	open

Onboard PCI Devices

The CMX58886CX cpuModule has several onboard PCI devices, all of which are listed in the table below.

Table 59 Onboard PCI Devices

Device ID	Vendor ID	Description
103E	8086	LAN Controller
244E	8086	Hub to PCI Bridge
24C0	8086	PCI to LPC Bridge
24C2	8086	USB UHCI Controller
24C3	8086	SMBus Controller
24C5	8086	AC'97 Audio Controller
24CB	8086	IDE Controller
24CD	8086	USB EHCI Controller
3580	8086	Host-Hub
3582	8086	Graphics Device
3584	8086	Main Memory
3585	8086	Config Process
-	-	PCI Slot 1
-	-	PCI Slot 2
-	-	PCI Slot 3
-	-	PCI Slot 4

Physical Dimensions

Figure 7 shows the mechanical dimensions of the CMX58886CX cpuModule.

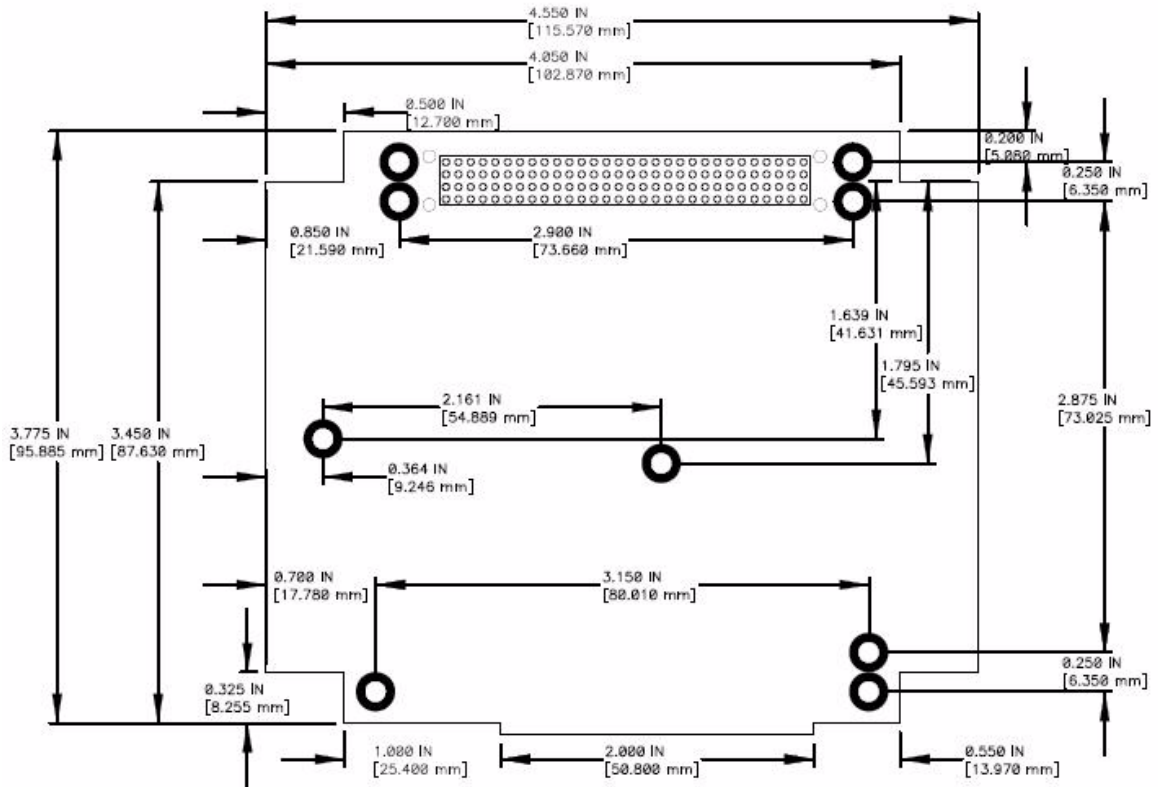


Figure 7 CMX58886CX Physical Dimensions (± 0.005 inches)



Appendix B Troubleshooting

Many problems you may encounter with operation of your CMX58886CX cpuModule are due to common errors. This appendix includes the following sections to help you get your system operating properly.

- Common problems and solutions
- Troubleshooting a PC/104-Plus system
- How to obtain technical support

Common Problems and Solutions

Table 60 lists some of the common problems you may encounter while using your CMX58886CX cpuModule, and suggests possible solutions.

If you are having problems with your cpuModule, review this table before contacting RTD Technical Support.

Table 60 Troubleshooting

Problem	Cause	Solution
cpuModule "will not boot"	no power or wrong polarity	<ul style="list-style-type: none"> check for correct power on PC/104 bus connectors
	incorrect Setup	<ul style="list-style-type: none"> reboot and press Delete to run Setup
	defective or misconnected device on bus	<ul style="list-style-type: none"> check for misaligned bus connectors remove other cards from stack
	cable connected backwards	<ul style="list-style-type: none"> verify all cables are connected correctly
	SSD installed backwards	<ul style="list-style-type: none"> check for an SSD memory installed in socket backwards
cpuModule keeps rebooting	problem with power supply	<ul style="list-style-type: none"> check for correct power on PC/104 bus connector
	reset switch is on	<ul style="list-style-type: none"> check that the reset button is not pushed in
	watchdog timer is not being serviced quickly enough	<ul style="list-style-type: none"> verify that the watchdog timer is being refreshed before it times out
cpuModule will not boot from particular drive or device	device not bootable	<ul style="list-style-type: none"> use sys command on drive or reformat the device using the /s switch
	device not formatted	<ul style="list-style-type: none"> format drive using /s switch
	power not connected to boot drive	<ul style="list-style-type: none"> connect power cable to floppy or hard drive
erratic operation	excessive bus loading	<ul style="list-style-type: none"> reduce number of PC/104 modules in stack remove termination components from bus signals remove any power supply bus terminations
	power supply noise	<ul style="list-style-type: none"> examine power supply output with oscilloscope glitches below 4.75 VDC will trigger a reset add bypass caps
	power supply limiting	<ul style="list-style-type: none"> examine power supply output with oscilloscope check for voltage drop below 4.75 VDC when hard drive or floppy drive starts add bypass caps
	insufficient cabling through power connector	<ul style="list-style-type: none"> increase wire gauge to connector power through bus connectors
	temperature too high	<ul style="list-style-type: none"> add fan, processor heatsink, or other cooling device(s) See <i>Thermal Management</i> on page 65
	memory address conflict	<ul style="list-style-type: none"> check for two hardware devices (e.g. Ethernet, SSD, Arcnet, PCMCIA) trying to use the same memory address check for two software devices (e.g. EMM386, PCMCIA drivers, etc.) trying to use the same memory addresses check for hardware and software devices trying to use the same memory address check for an address range shadowed (see Advanced Setup screen) while in use by another hardware or software device
	I/O address conflict	<ul style="list-style-type: none"> check for another module trying to use I/O addresses reserved for the cpuModule between 010h and 01Fh check for two modules (e.g. dataModules, PCMCIA cards, Ethernet) trying to use the same I/O addresses

Table 60 Troubleshooting (cont'd)

Problem	Cause	Solution
keyboard does not work	keyboard interface damaged by misconnection	<ul style="list-style-type: none"> • check if keyboard LEDs light
	wrong keyboard type	<ul style="list-style-type: none"> • verify keyboard is an "AT" type or switch to "AT" mode
floppy drive light always on	cable misconnected	<ul style="list-style-type: none"> • check for floppy drive cable connected backwards
two hard drives will not work, but one does	both drives configured for master	<ul style="list-style-type: none"> • set one drive for master and the other for slave operation (consult drive documentation)
floppy does not work	"data error" due to drive upside down	<ul style="list-style-type: none"> • orient drive properly (upright or on side)
will not boot when video card is removed	illegal calls to video controller	<ul style="list-style-type: none"> • look for software trying to access nonexistent video controller for video, sound, or beep commands
abnormal video	flat panel is enabled	<ul style="list-style-type: none"> • disable the flat panel in the BIOS
can only use 640 x 480 resolution in Windows	flat panel is enabled	<ul style="list-style-type: none"> • disable the flat panel in the BIOS
	video drivers not installed	<ul style="list-style-type: none"> • install the video drivers
will not boot from PCMCIA hard drive	booting from PCMCIA is not supported	<ul style="list-style-type: none"> • boot from SSD, use autoexec.bat to load PCMCIA drivers, run application from PCMCIA card
COM port will not work in RS-422 or RS-485 modes	not configured for RS-422/485	<ul style="list-style-type: none"> • correctly configure serial port in Setup program
COM port will not transmit in RS-422 or RS-485 mode	not enabling transmitters	<ul style="list-style-type: none"> • control RTS* bit of Modem Control Register to enable transmitters; see Serial Port descriptions
date and time not saved when power is off	no backup battery	<ul style="list-style-type: none"> • connect a backup battery to the multi-function connector
cannot enter BIOS	quick boot enabled with no hard drives	<ul style="list-style-type: none"> • install JP5, reboot, and run qboot.exe and reboot.
screen flickers at high resolutions when processor is fully utilized	memory with ECC enabled requires additional system memory resources; the integrated graphics engine has less memory bandwidth for access to the graphics frame buffer	<ul style="list-style-type: none"> • disable ECC

Troubleshooting a PC/104-Plus System

If you have reviewed the preceding table and still cannot isolate the problem with your CMX58886CX cpuModule, please try the following troubleshooting steps. Even if the resulting information does not help you find the problem, it will be very helpful if you need to contact technical support.

1. **Simplify the system.** Remove items one at a time and see if one particular item seems to cause the problem.
2. **Swap components.** Try replacing items in the system one-at-a-time with similar items.

How to Obtain Technical Support

If after following the above steps, you still cannot resolve a problem with your CMX58886CX cpuModule, please gather the following information:

- cpuModule model, BIOS version, and serial number
- List of all boards in system
- List of settings from cpuModule Setup program
- Printout of autoexec.bat and config.sys files (if applicable)
- Description of problem
- Circumstances under which problem occurs

Then contact RTD Technical Support:

Phone: 814-234-8087

Fax: 814-234-5218

E-mail: techsupport@rtd.com

Appendix C IDAN™ Dimensions and Pinout

cpuModules, like all other RTD PC/PCI-104 modules, can be packaged in Intelligent Data Acquisition Node (IDAN) frames, which are milled aluminum frames with integrated heat sinks and heat pipes for fanless operation. RTD modules installed in IDAN frames are called building blocks. IDAN building blocks maintain the simple but rugged PC/104 stacking concept. Each RTD module is mounted in its own IDAN frame and all I/O connections are brought to the walls of each frame using standard PC connectors. No connections are made from module to module internal to the system other than through the PC/104 and PC/104-Plus bus, enabling quick interchangeability and system expansion without hours of rewiring and board redesign.

The CMX58886CX cpuModule can also be purchased as part of a custom-built RTD HiDAN™ or HiDANplus™ High Reliability Intelligent Data Acquisition Node. This appendix provides the dimensions and pinouts of the CMX58886CX installed in an IDAN frame. Contact RTD for more information on high reliability IDAN, HiDAN, and HiDANplus PC/PCI-104 systems.



IDAN—Adhering to the PC/104 stacking concept, IDAN allows you to build a customized system with any combination of RTD modules.

IDAN Heat Pipes—Advanced heat pipe technology maximizes heat transfer to heat sink fins.

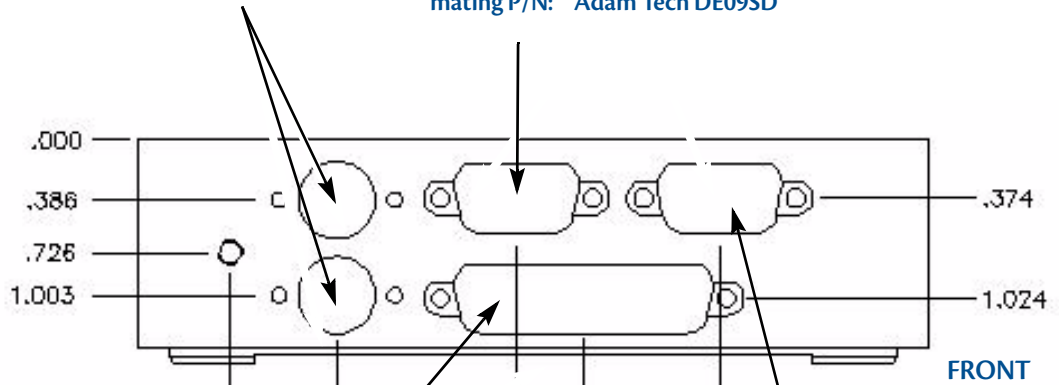


HiDANplus—Integrating the modularity of IDAN with the ruggedization of HiDAN, HiDANplus enables connectors on all system frames, with signals running between frames through a dedicated stack-through raceway.

IDAN Dimensions and Connectors

6-pin mini-DIN (female)
 module P/N: Adam Tech MDE006W
 mating P/N: Adam Tech MDP006

9-pin D (male)
 module P/N: Adam Tech DE09PD
 mating P/N: Adam Tech DE09SD

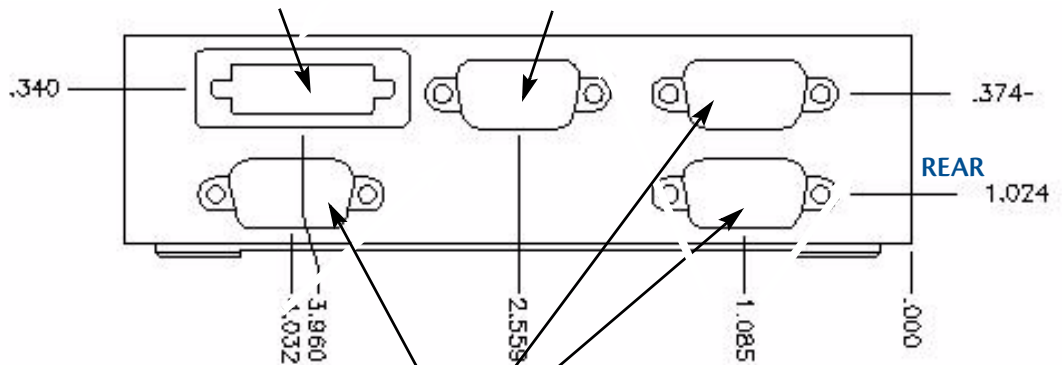


25-pin D (female)
 module P/N: Adam Tech DB25SD
 mating P/N: Adam Tech DB25PD

9-pin D (female)
 module P/N: Adam Tech DE09SD
 mating P/N: Adam Tech DE09PD

20-pin mini D (female)
 module P/N: 3M 10220-6212VC
 mating P/N: 3M 10120-3000VE

15-pin high-density D (female)
 module P/N: Adam Tech HDT15SD
 mating P/N: Adam Tech HDT15PD



9-pin D (male)
 module P/N: Adam Tech DE09PD
 mating P/N: Adam Tech DE09SD

Figure 8 IDAN-CMX5886CX Connectors

External I/O Connections

Table 61 PS/2 Mouse — 6-Pin mini-DIN Connector (female)

IDAN Pin #	Signal	Function
1	MDAT	Mouse Data
2	Reserved	—
3	GND	Ground
4	+5 V	+5 Volts
5	MCLK	Mouse Clock
6	Reserved	—

Table 62 Keyboard — 6-Pin mini-DIN Connector (female)

IDAN Pin #	Signal	Function
1	KDAT	Keyboard Data
2	Reserved	—
3	GND	Ground
4	+5 V	+5 V
5	KCLK	Keyboard Clock
6	Reserved	—

Table 63 COM1/COM2 (RS-232) — 9-Pin D Connector (male)

IDAN Pin #	Signal	Function	Mode
1	DCD	Data Carrier Detect	Input
2	RXD	Receive Data	Input
3	TXD	Transmit Data	Output
4	DTR	Data Terminal Ready	Output
5	GND	Ground	—
6	DSR	Data Set Ready	Input
7	RTS	Request To Send	Output
8	CTS	Clear To Send	Input
9	RI	Ring Indicator	Input

Table 64 COM1/COM2 (RS-422/485) — 9-Pin D Connector (male)

IDAN Pin #	Signal	Function	Mode
1	Reserved	—	—
2	RXD-	Receive Data -	Input
3	TXD-	Transmit Data -	Output
4	Reserved	—	—
5	GND	Ground	—
6	Reserved	—	—
7	TXD+	Transmit Data +	Output
8	RXD+	Receive Data +	Input
9	Reserved	—	—

Table 65 multiPort — 25-Pin D Connector (female)

IDAN Pin #	aDIO Port	Parallel Port	Floppy Port	CPU Pin #
1	strobe 0	STB	—	1
2	P1-0	PD0	INDEX#	3
3	P1-1	PD1	TRK0#	5
4	P1-2	PD2	WRTPRT#	7
5	P1-3	PD3	RDATA#	9
6	P1-4	PD4	DSKCHG	11
7	P1-5	PD5	—	13
8	P1-6	PD6	—	15
9	P1-7	PD7	—	17
10	P0-0	ACK	DS1#	19
11	P0-1	BSY	MTR#	21
12	P0-2	PE	WDATA#	23
13	P0-3	SLCT	WGATE#	25
14	P0-4	AFD	DR0#	2
15	P0-5	ERR	HDSEL#	4
16	P0-6	INIT	DIR#	6
17	P0-7	SLIN	STEP#	8
18	strobe 1	GND	GND	10
19	GND	GND	GND	12
20	GND	GND	GND	14
21	GND	GND	GND	16
22	GND	GND	GND	18
23	GND	GND	GND	20
24	GND	GND	GND	22
25	GND	GND	GND	24

Table 66 Panel — 25-Pin mini D Connector (female)

IDAN Pin #	Signal Name	CPU Pin #
1	LVDS_YAP0	1
2	LVDS_DDCPCLK	3
3	LVDS_YAP1	5
4	LVDS_DDCPDATA	7
5	LVDS_YAP2	9
6	GND	11
7	LVDS_CLKAP	13
8	LVDS_YAP3	15
9	GND	17
10	FP_BKLT	19
11	LVDS_YAM0	2
12	GND	4
13	LVDS_YAM1	6
14	GND	8
15	LVDS_YAM2	10
16	GND	12
17	LVDS_CLKAM	14
18	LVDS_YAM3	16
19	FP_VCC	18
20	LVDS_BKLTCTL	20

Table 67 SVGA — 15-Pin High Density D Connector (female)

IDAN Pin #	Signal	Function	CPU Pin #
1	Red	Red Analog Output	4
2	Green	Green Analog Output	6
3	Blue	Blue Analog Output	8
4	DDC CLK	Monitor Clock	3
5	GND	Ground	9
6	GND	Ground	9
7	GND	Ground	9
8	GND	Ground	10
9	Reserved	Reserved	—
10	GND	Ground	10
11	+5 V	+ 5 Volts	7
12	DDC Data	Monitor data	5
13	HSYNC	Horizontal Sync	2
14	VSYNC	Vertical Sync	1
15	Reserved	Reserved	—

Table 68 USB — 9-Pin D Connector (male)

IDAN Pin #	Signal	Function	Mode
1	VCC1	+5 V to USB1	output
2	Data USB1-	USB1 Data-	input/output
3	Data USB1+	USB1 Data+	input/output
4	GND	Ground	—
5	GND	Ground	—
6	VCC2	+5 V to USB2	output
7	Data USB2-	USB2 Data-	input/output
8	Data USB2+	USB2 Data+	input/output
9	GND	Ground	—

Table 69 Ethernet — 9-Pin D Connector (female)

IDAN Pin #	10Base-T Adapter Pin #	Signal	CPU Pin #
1	1	Receive +	1
2	2	Reserved	3
3	3	Transmit +	5
4	4	Reserved	7
5	5	Ground	9
6	6	Receive -	2
7	7	Reserved	4
8	8	Transmit -	6
9	—	Reserved	8

Table 70 Audio — 9-Pin D Connector (female)

IDAN Pin #	Signal	CPU Pin #
5	MIC_VREF	1
4	GND	3
3	LINE_IN_GND	5
2	GND	7
2	GND	9
9	MIC_IN	2
8	LINE_IN_LEFT	4
7	LINE_IN_RIGHT	6
6	OUTPUT_LEFT	8
1	OUTPUT_RIGHT	10



Appendix D Additional Information

Application Notes

RTD offers many application notes that provide assistance with the unique feature set of the CMX58886CX cpuModule. For the latest application notes, refer to the RTD website.

Drivers and Example Programs

To obtain the latest versions of drivers and example programs for this cpuModule, refer to the RTD website.

Interrupt Programming

For more information about interrupts and writing interrupt service routines, refer to the following book:

Interrupt-Driven PC System Design
by Joseph McGivern
ISBN: 0929392507

Serial Port Programming

For more information about programming serial port UARTs, consult the following book:

Serial Communications Developer's Guide
by Mark Nielson
ISBN: 0764545701

PC/104 and PC/104-Plus Specifications

A copy of the latest PC/104 and PC/104-Plus specifications can be found on the webpage for the PC/104 Embedded Consortium:

<http://www.pc104.org>



Appendix E Limited Warranty

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