Active Receive Mixer
LF to 500 MHz

AD8342

FEATURES

- **Broadband RF port: LF to 500 MHz**
- **Conversion gain: 3.7 dB**
- **Noise figure: 12.2 dB**
- **Input IP3: 22.7 dBm**
- **Input P_{1dB}: 8.3 dBm**
- **LO drive: 0 dBm**
- **Differential high impedance RF input port**
- **Single-ended, 50 Ω LO input port**
- **Single-supply operation: 5 V @ 98 mA**
- **Power-down mode**
- **Exposed paddle LFCSP: 3 mm × 3 mm**

APPLICATIONS

- **Cellular base station receivers**
- **ISM receivers**
- **Radio links**
- **RF instrumentation**

FUNCTIONAL BLOCK DIAGRAM

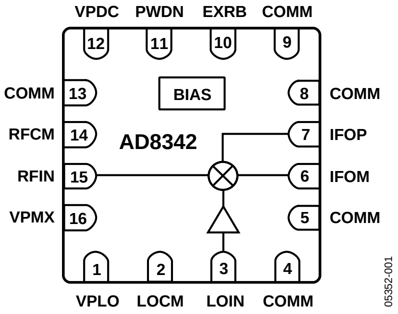


Figure 1.

GENERAL DESCRIPTION

The AD8342 is a high performance, broadband active mixer. It is well suited for demanding receive-channel applications that require wide bandwidth on all ports and very low intermodulation distortion and noise figure.

The AD8342 provides a typical conversion gain of 3.7 dB with an RF frequency of 238 MHz. The integrated LO driver presents a 50 Ω input impedance with a low LO drive level, helping to minimize the external component count.

The differential high impedance broadband RF port allows for easy interfacing to both active devices and passive filters. The RF input accepts input signals as large as 1.6 V p-p or 8 dBm (relative to 50 Ω) at P_{1dB}.

The open-collector differential outputs provide excellent balance and can be used with a differential filter or IF amplifier, such as the AD8369 or AD8351. These outputs can also be converted to a single-ended signal through the use of a matching network or a transformer (balun). When centered on the VPOS supply voltage, the outputs may swing ±2 V differentially.

The AD8342 is fabricated on an Analog Devices proprietary, high performance SiGe IC process. The AD8342 is available in a 16-lead LFCSP. It operates over a −40°C to +85°C temperature range. An evaluation board is also available.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

4/05—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, f_{RF} = 238 MHz, f_{LO} = 286 MHz, LO power = 0 dBm, Z_O = 50 Ω, R_{BIAS} = 1.82 kΩ, RF termination = 100 Ω, IF terminated into 100 Ω through a 2:1 ratio balun, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
RF INPUT INTERFACE					
Return Loss	Hi-Z input terminated with 100 Ω off-chip resistor		10		dB
Input Impedance	Frequency = 238 MHz (measured at RFIN with RFCM ac-grounded)		1‖0.4		kΩ‖pF
DC Bias Level	Internally generated; port must be ac-coupled		2.4		V
OUTPUT INTERFACE					
Output Impedance	Differential impedance, frequency = 48 MHz		10‖0.5		kΩ‖pF
DC Bias Voltage	Supplied externally	4.75	V_S	5.25	V
Power Range	Via a 2:1 impedance ratio transformer			13	dBm
LO INTERFACE					
Return Loss			10		dB
DC Bias Voltage	Internally generated; port must be ac-coupled		V_S − 1.6		V
POWER-DOWN INTERFACE					
PWDN Threshold			3.5		V
PWDN Response Time	Device enabled, IF output to 90% of its final level		0.4		µs
	Device disabled, supply current <5 mA		4		µs
PWDN Input Bias Current	Device enabled		−80		µA
	Device disabled		+100		µA
POWER SUPPLY					
Positive Supply Voltage		4.75	5	5.25	V
Quiescent Current					
VPDC	Supply current for bias cells		5		mA
VPMX, IFOP, IFOM	Supply current for mixer, R_{BIAS} = 1.82 kΩ		58		mA
VPLO	Supply current for LO limiting amplifier		35		mA
Total Quiescent Current	V_S = 5 V	85	98	113	mA
Power-Down Current	Device disabled		500		µA

AC PERFORMANCE

V_S = 5 V, T_A = 25°C, LO power = 0 dBm, Z_O = 50 Ω, R_{BIAS} = 1.82 kΩ, RF termination 100 Ω, IF terminated into 100 Ω via a 2:1 ratio balun, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
RF FREQUENCY RANGE[1]		50		500	MHz
LO FREQUENCY RANGE[1]	High side LO	60		850	MHz
IF FREQUENCY RANGE[1]		10		350	MHz
CONVERSION GAIN	f_{RF} = 460 MHz, f_{LO} = 550 MHz, f_{IF} = 90 MHz		3.2		dB
	f_{RF} = 238 MHz, f_{LO} = 286 MHz, f_{IF} = 48 MHz		3.7		dB
SSB NOISE FIGURE	f_{RF} = 460 MHz, f_{LO} = 550 MHz, f_{IF} = 90 MHz		12.5		dB
	f_{RF} = 238 MHz, f_{LO} = 286 MHz, f_{IF} = 48 MHz		12.2		dB
INPUT THIRD-ORDER INTERCEPT	f_{RF1} = 460 MHz, f_{RF2} = 461 MHz, f_{LO} = 550 MHz, f_{IF1} = 90 MHz, f_{IF2} = 89 MHz each RF tone −10 dBm		22.2		dBm
	f_{RF1} = 238 MHz, f_{RF2} = 239 MHz, f_{LO} = 286MHz, f_{IF1} = 48MHz, f_{IF2} = 47MHz each RF tone −10 dBm		22.7		dBm
INPUT SECOND-ORDER INTERCEPT	f_{RF1} = 460 MHz, f_{RF2} = 410 MHz, f_{LO} = 550 MHz, f_{IF1} = 90 MHz, f_{IF2} = 140 MHz		50		dBm
	f_{RF1} = 238 MHz, f_{RF2} = 188 MHz, f_{LO} = 286 MHz, f_{IF1} = 48MHz, f_{IF2} = 98 MHz		44		dBm
INPUT 1 dB COMPRESSION POINT	f_{RF} = 460 MHz, f_{LO} = 550 MHz, f_{IF} = 90 MHz		8.5		dBm
	f_{RF} = 238 MHz, f_{LO} = 286 MHz, f_{IF} = 48 MHz		8.3		dBm
LO TO IF OUTPUT LEAKAGE	LO power = 0 dBm, f_{LO} = 286 MHz		−27		dBc
LO TO RF INPUT LEAKAGE	LO power = 0 dBm, f_{LO} = 286 MHz		−55		dBc
2× LO TO IF OUTPUT LEAKAGE	LO power = 0 dBm, f_{RF} = 238 MHz, f_{LO} = 286 MHz IF terminated into 100 Ω and measured with a differential probe		−47		dBm
RF TO IF OUTPUT LEAKAGE	RF power = −10 dBm, f_{RF} = 238 MHz, f_{LO} = 286 MHz		−32		dBc
IF/2 SPURIOUS	RF power = −10 dBm, f_{RF} = 238 MHz, f_{LO} = 286 MHz		−70		dBc

[1] Frequency ranges are those that were extensively characterized; this device can operate over a wider range. See the High IF Applications section for details.

SPUR TABLE

V_S = 5 V, T_A = 25°C, RF and LO power = 0 dBm, f_{RF} = 238MHz, f_{LO} = 286MHz, Z_O = 50 Ω, R_{BIAS} = 1.82 kΩ, RF termination 100 Ω, IF terminated into 100 Ω via a 2:1 ratio balun.

Note: Measured using standard test board. Typical noise floor of measurement system = −100 dBm.

Table 3.

		m														
	$nf_{RF} - mf_{LO}$	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
n	0	<−100	−25	−54	−28	−45	−35	−39	−36	−42	−57	−44	−42	−41	−46	−59
	1	−39	3.5	−42	−6	−48	−16	−50	−28	−57	−37	−68	−45	−54	−37	−61
	2	−52	−47	−51	−49	−54	−56	−56	−62	−62	−66	−71	−80	−80	−67	−79
	3	−81	−57	−79	−61	−82	−61	−74	−69	−94	−85	−89	−86	−86	−90	−81
	4	−78	−70	−80	−79	−80	−85	−87	−92	−93	−96	−95	<−100	−97	<−100	−95
	5	−98	−79	−95	−87	−96	−94	−95	−88	−98	−94	<−100	<−100	<−100	<−100	<−100
	6	<−100	<−100	<−100	−99	<−100	−96	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	7	<−100	<−100	<−100	<−100	−96	<−100	−98	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100
	8	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	−97	<−100	<−100	<−100	<−100	<−100	<−100
	9	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	−99	<−100	<−100	<−100
	10	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	−99	<−100	<−100	<−100	<−100
	11	<−100	<−100	<−100	<−100	<−100	<−100	<−100	−96	<−100	−97	<−100	−96	<−100	<−100	<−100
	12	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	−99	<−100	−98	<−100	<−100	<−100	<−100
	13	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	−97	<−100	−97	−99	<−100	<−100
	14	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	−98	−98	<−100	<−100	<−100
	15	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage, V_S	5.5 V
RF Input Level	12 dBm
LO Input Level	12 dBm
PWDN Pin	V_S + 0.5 V
IFOP, IFOM Bias Voltage	5.5 V
Minimum Resistor from EXRB to COMM	1.8 kΩ
Internal Power Dissipation	650 mW
θ_{JA}	77°C/W
Maximum Junction Temperature	135°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

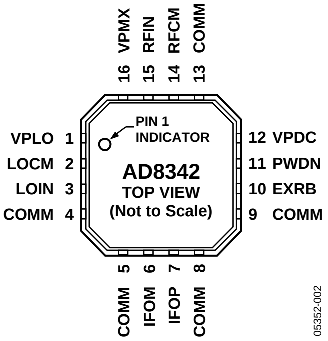


Figure 2. 16-Lead LFCSP

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	VPLO	Positive Supply Voltage for the LO Buffer: 4.75 V to 5.25 V.
2	LOCM	AC Ground for Limiting LO Amplifier. Internally biased to Vs − 1.6 V. AC-couple to ground.
3	LOIN	LO Input. Nominal input level 0 dBm. Input level range −10 dBm to +4 dBm (relative to 50 Ω). Internally biased to Vs − 1.6 V. AC-couple.
4, 5, 8, 9, 13	COMM	Device Common (DC Ground).
6, 7	IFOM, IFOP	Differential IF Outputs (Open Collectors). Each requires dc bias of 5.00 V (nominal).
10	EXRB	Mixer Bias Voltage. Connect resistor from EXRB to ground. Typical value of 1.82 kΩ sets mixer current to nominal value. Minimum resistor value from EXRB to ground = 1.8 kΩ. Internally biased to 1.17 V.
11	PWDN	Connect to Ground for Normal Operation. Connect pin to V_S for disable mode.
12	VPDC	Positive Supply Voltage for the DC Bias Cell: 4.75 V to 5.25 V.
14	RFCM	AC Ground for RF Input. Internally biased to 2.4 V. AC-couple to ground.
15	RFIN	RF Input. Internally biased to 2.4 V. Must be ac-coupled.
16	VPMX	Positive Supply Voltage for the Mixer: 4.75 V to 5.25 V.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, RF power = −10 dBm, LO power = 0 dBm, Z_O = 50 Ω, R_{BIAS} = 1.82 kΩ, RF termination 100 Ω, IF terminated into 100 Ω via a 2:1 ratio balun, unless otherwise noted.

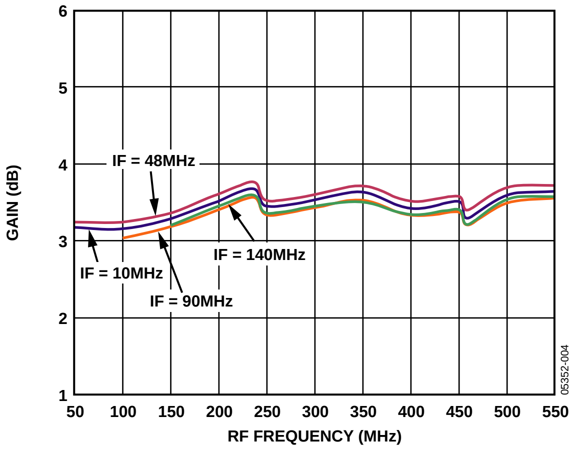


Figure 3. Conversion Gain vs. RF Frequency

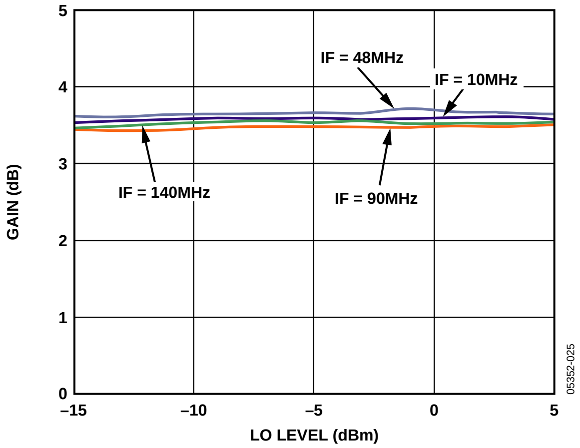


Figure 4. Gain vs. LO Level, RF Frequency = 238 MHz

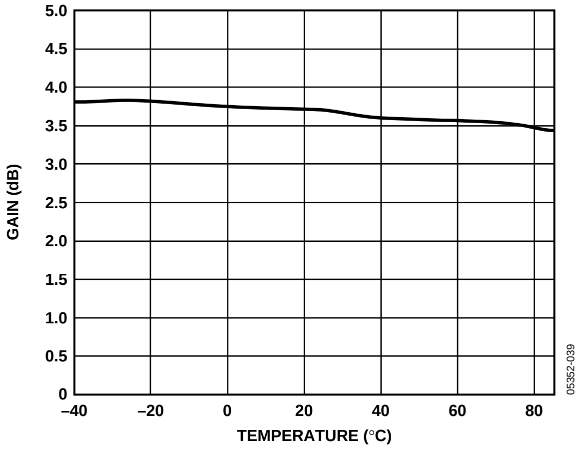


Figure 5. Gain vs. Temperature, f_{RF} = 238 MHz, f_{LO} = 286 MHz

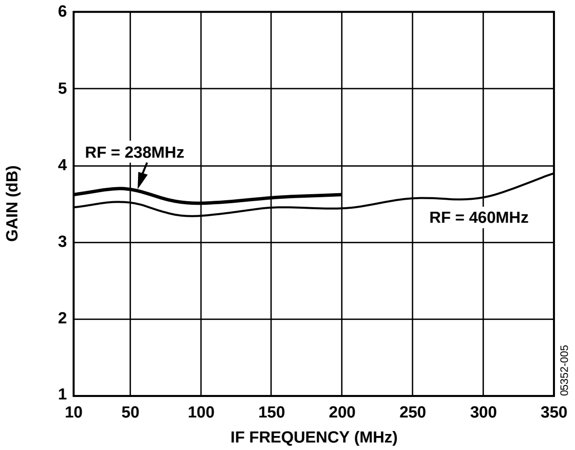


Figure 6. Conversion Gain vs. IF Frequency

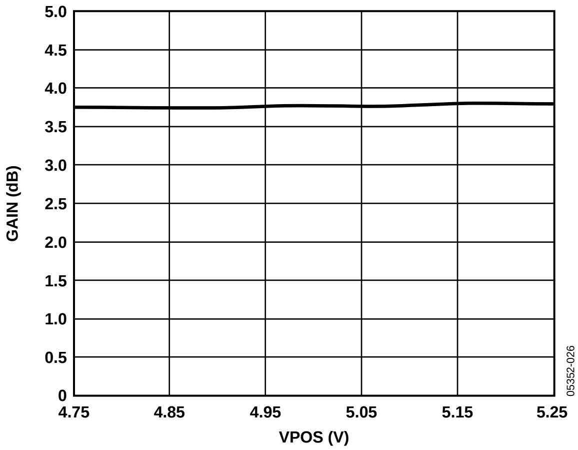


Figure 7. Gain vs. Vpos, f_{RF} = 238 MHz, f_{LO} = 286 MHz

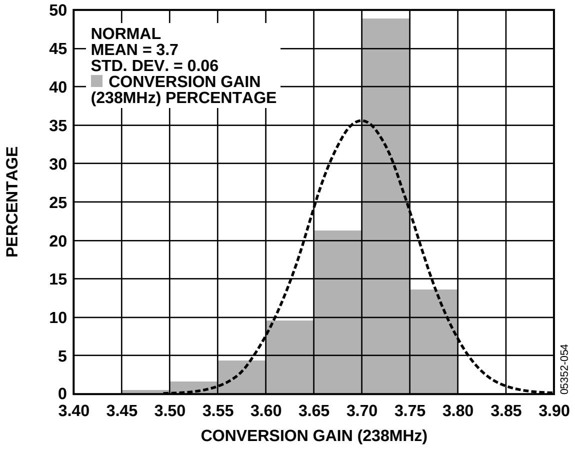


Figure 8. Conversion Gain Distribution, f_{RF} = 238 MHz, f_{LO} = 286 MHz

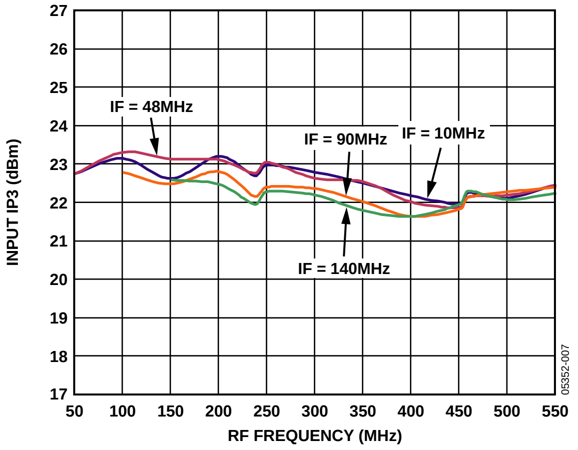


Figure 9. Input IP3 vs. RF Frequency

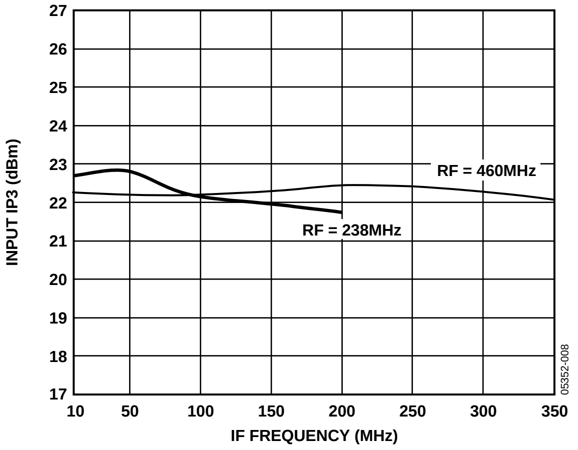


Figure 12. Input IP3 vs. IF Frequency

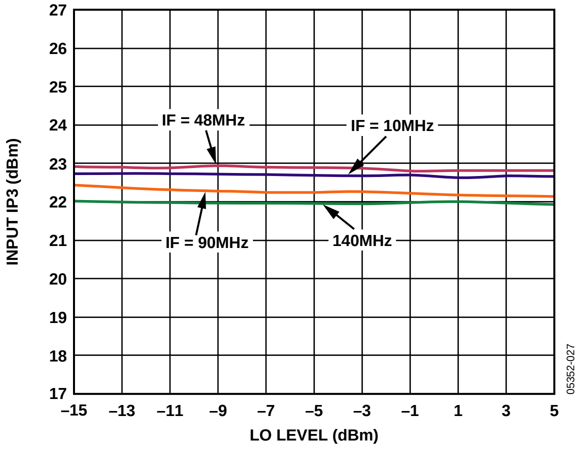


Figure 10. Input IP3 vs. LO Level, f_{RF1} = 238 MHz, f_{RF2} = 239 MHz

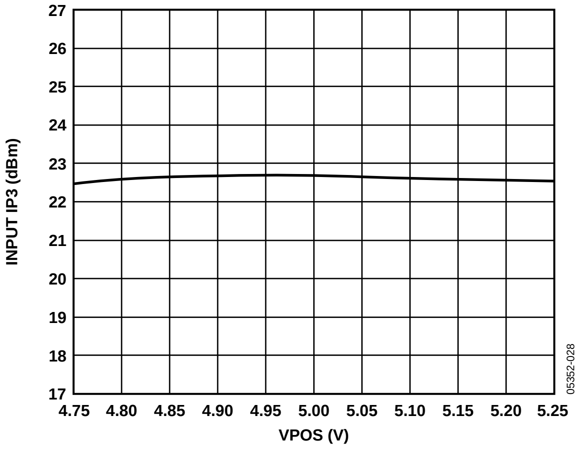


Figure 13. Input IP3 vs. Vpos, f_{RF} = 238 MHz, f_{RF2} = 239 MHz LO Frequency = 286 MHz

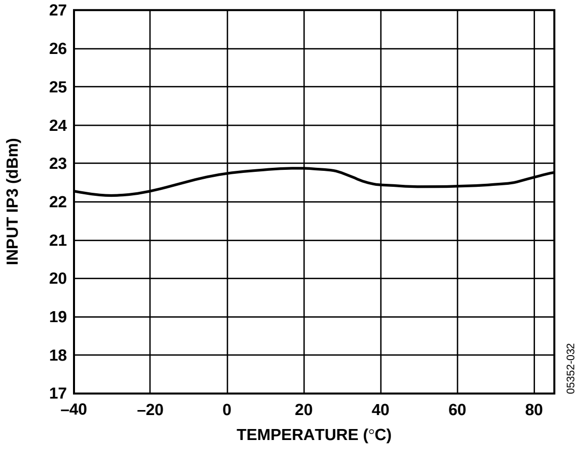


Figure 11. Input IP3 vs. Temperature, f_{RF1} = 238 MHz, f_{RF2} = 239 MHz, f_{LO} = 286 MHz

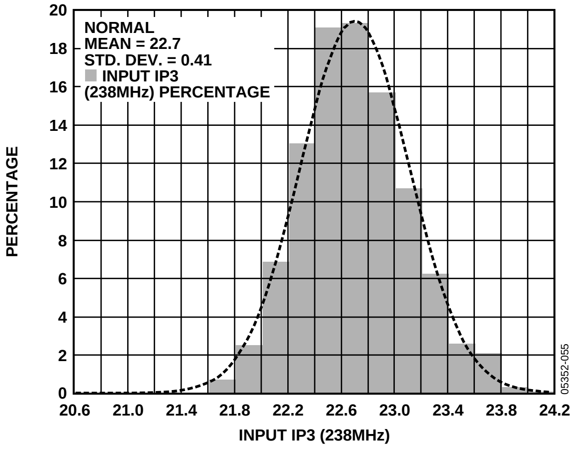


Figure 14. Input IP3 Distribution, f_{RF} = 238 MHz, f_{LO} = 286 MHz

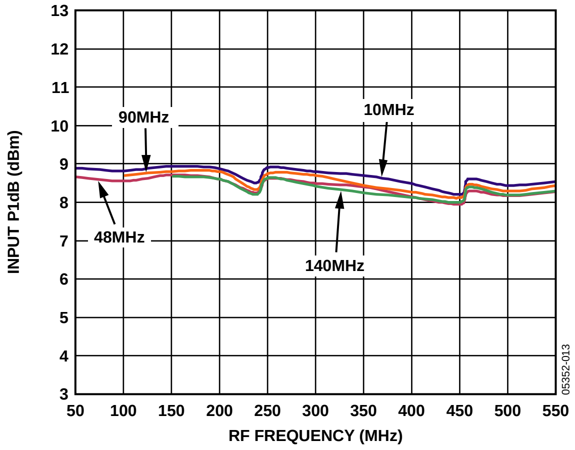


Figure 15. Input P1dB vs. RF Frequency

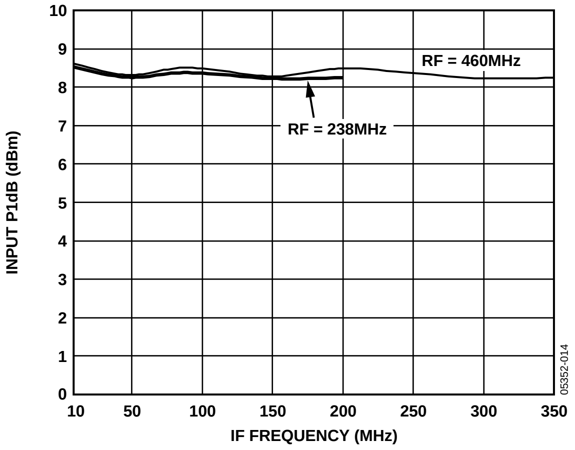


Figure 18. Input P1dB vs. IF Frequency

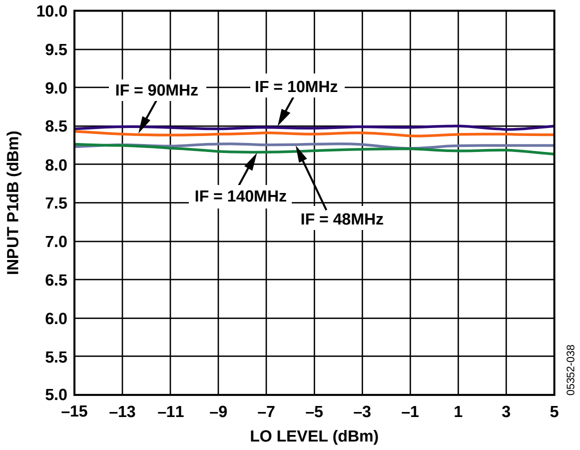


Figure 16. Input P1dB vs. LO Level, f_{RF} = 238 MHz

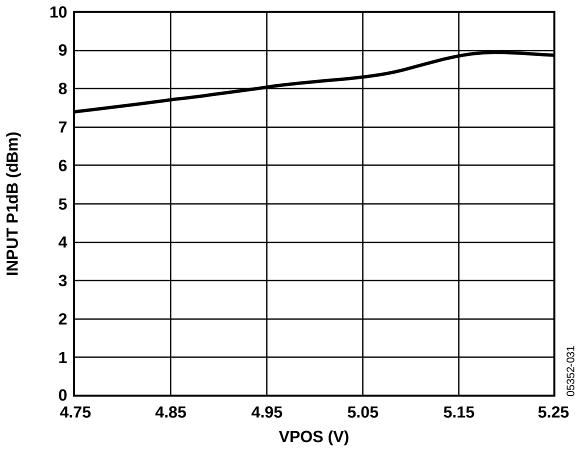


Figure 19. Input P1dB vs. Vpos, f_{RF} = 238 MHz, f_{LO} = 286 MHz

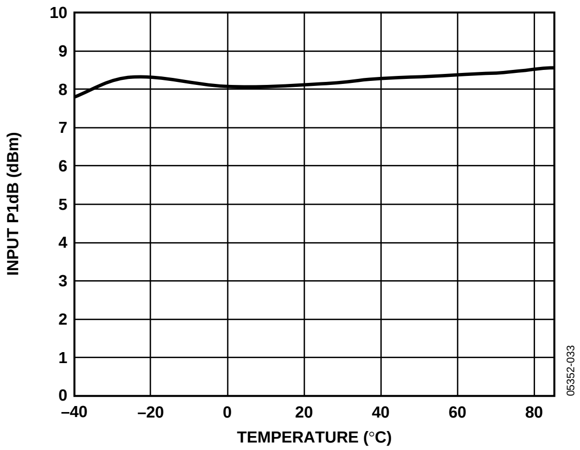


Figure 17. Input P1dB vs. Temperature, f_{RF} = 238 MHz, f_{LO} = 286 MHz

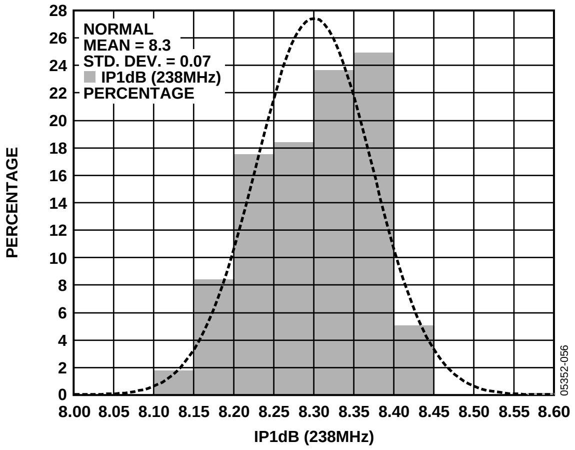


Figure 20. Input IP3 Distribution, f_{RF} = 238 MHz, f_{LO} = 286 MHz

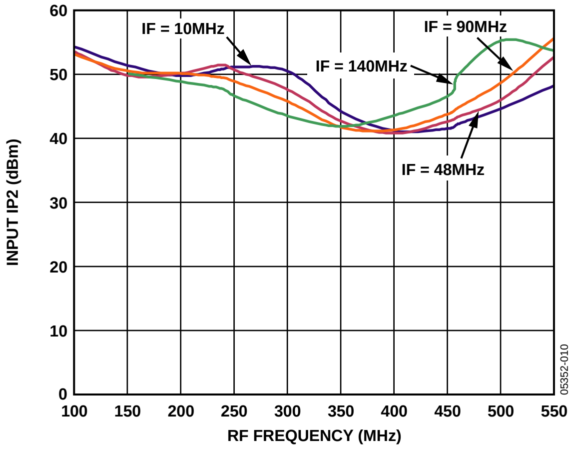


Figure 21. Input IP2 vs. RF Frequency (Second RF = R F - 50 MHz)

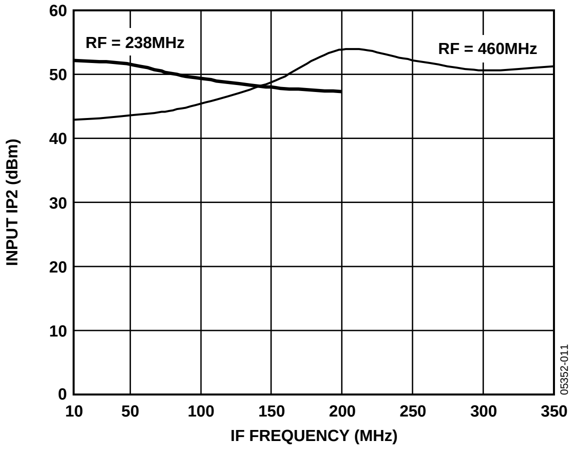


Figure 24. Input IP2 vs. IF Frequency (Second RF = R F - 50 MHz)

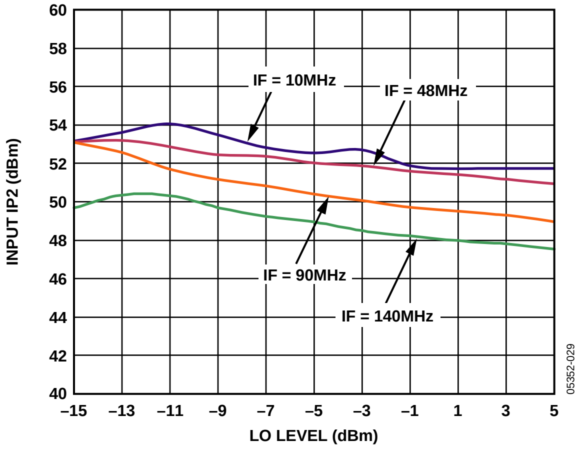


Figure 22. Input IP2 vs. LO Level, f_{RF} = 238 MHz, ,f_{RF2} =188MHz

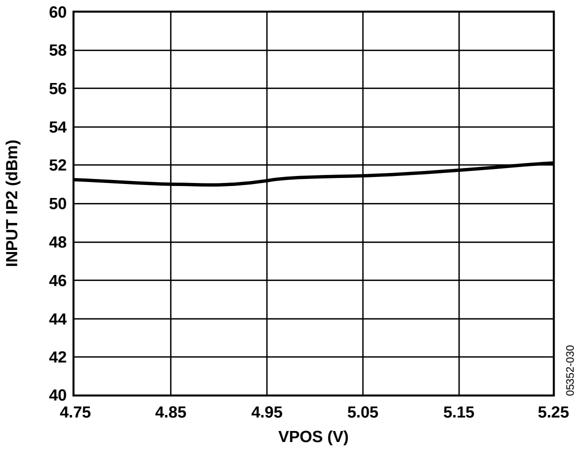


Figure 25. Input IP2 vs. Vpos, f_{RF1} = 238 MHz, f_{RF2} = 188 MHz, f_{LO} = 286 MHz

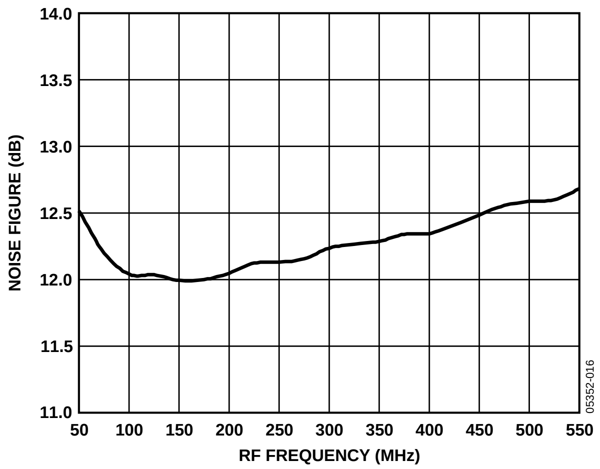


Figure 23. Noise Figure vs. RF Frequency, IF Frequency = 48 MHz

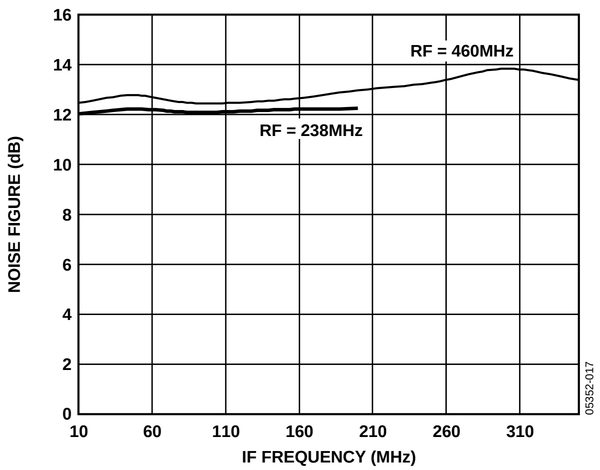


Figure 26. Noise Figure vs. IF Frequency

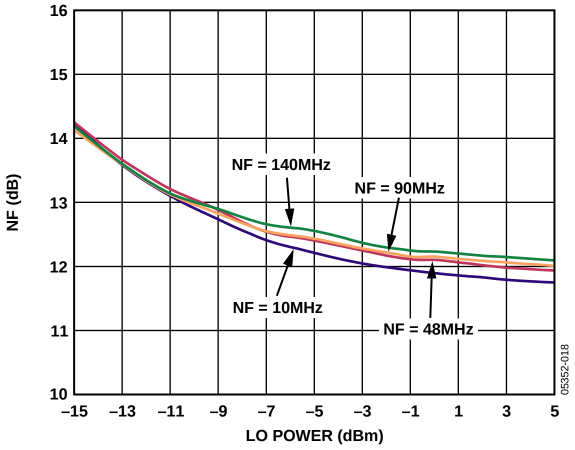


Figure 27. Noise Figure vs. LO Power, f_{RF} = 238 MHz

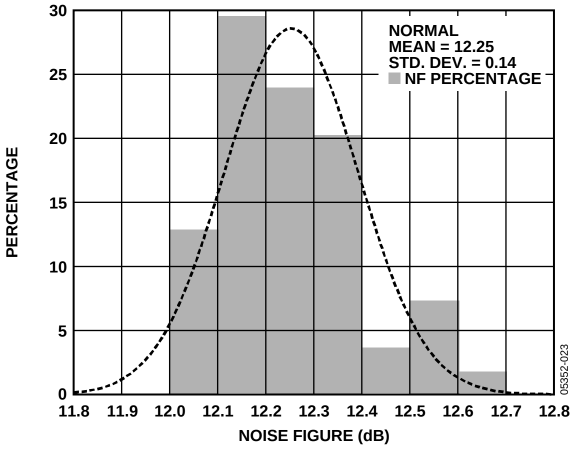


Figure 30. Noise Figure Distribution, f_{RF} = 238 MHz, f_{LO} = 286 MHz

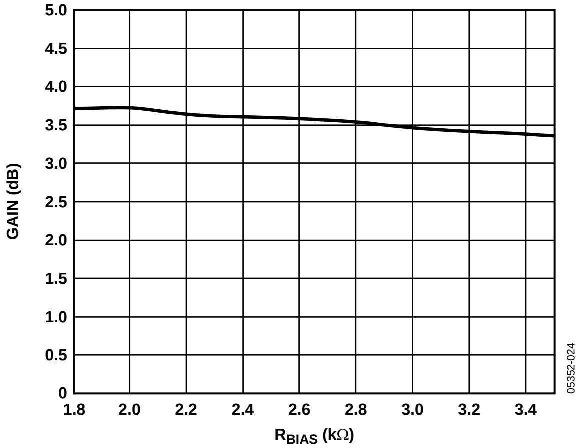


Figure 28. Gain vs. R_{BIAS}, RF Frequency = 238 MHz, LO Frequency = 286MHz

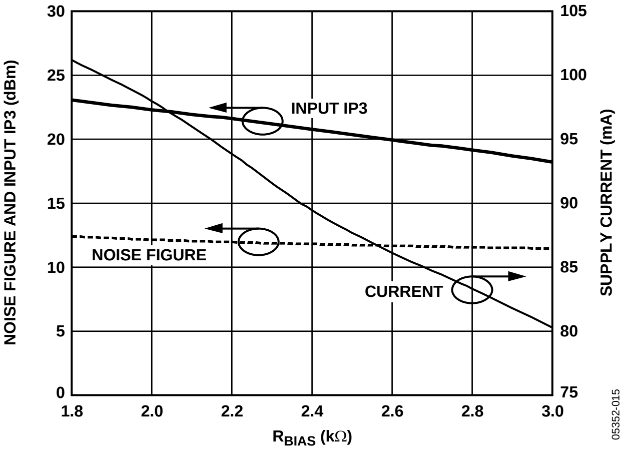


Figure 31. Noise Figure, Input IP3 and Supply Current vs. R_{BIAS}, f_{RF1} = 238 MHz, f_{RF2} = 239 MHz, f_{LO} = 286 MHz

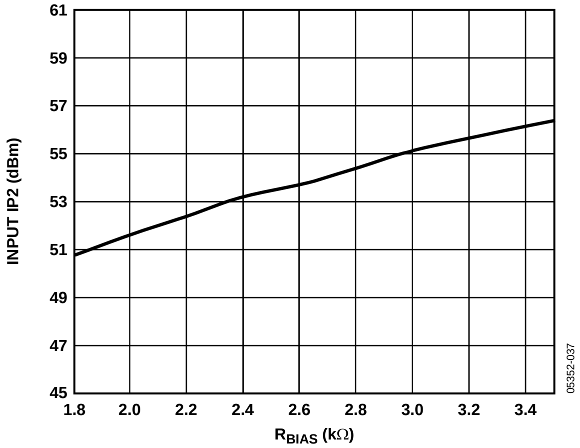


Figure 29. Input IP2 vs. R_{BIAS}, f_{RF} = 238 MHz (Second RF = RF – 50MHz), f_{LO} = 286 MHz

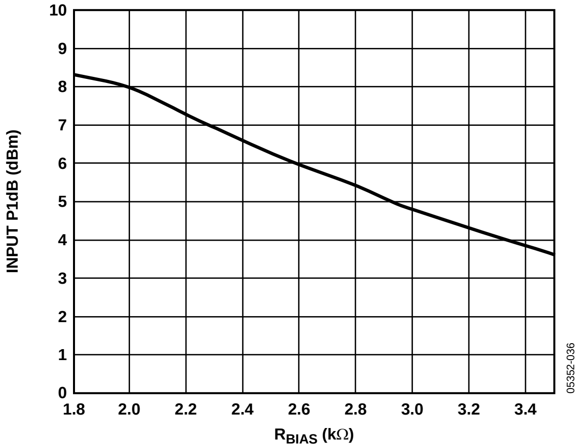


Figure 32. Input P1dB vs. R_{BIAS}, f_{RF} = 238 MHz, f_{LO} = 286 MHz

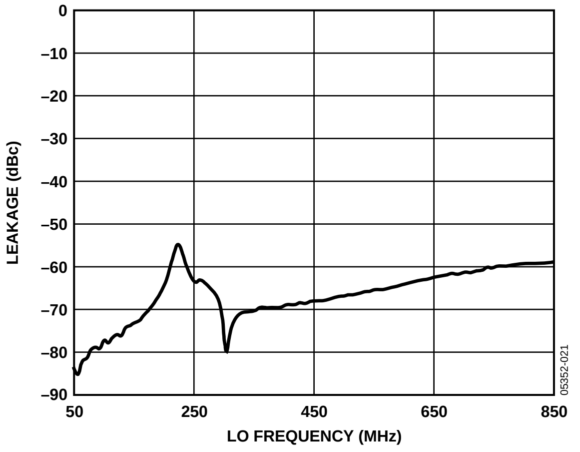


Figure 33. LO to RF Leakage vs. LO Frequency, LO Power = 0 dBm

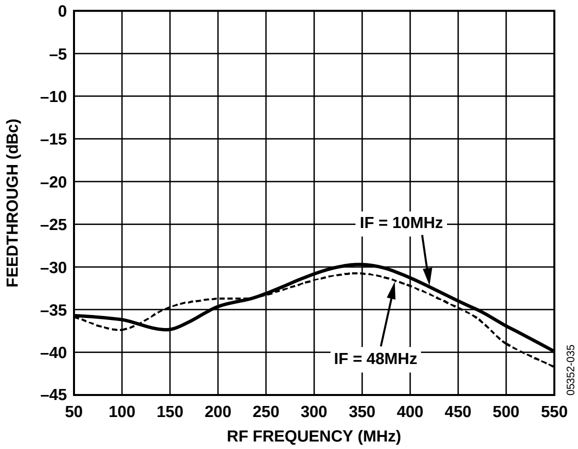


Figure 34. RF to IF Feedthrough, RF Power = –10 dBm

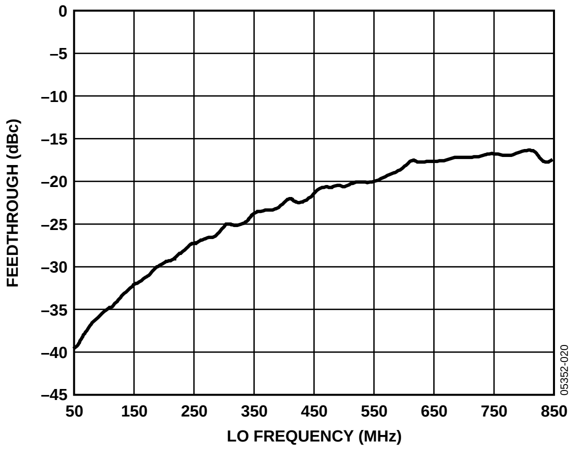


Figure 35. LO to IF Feedthrough vs. LO Frequency, LO Power = 0 dBm

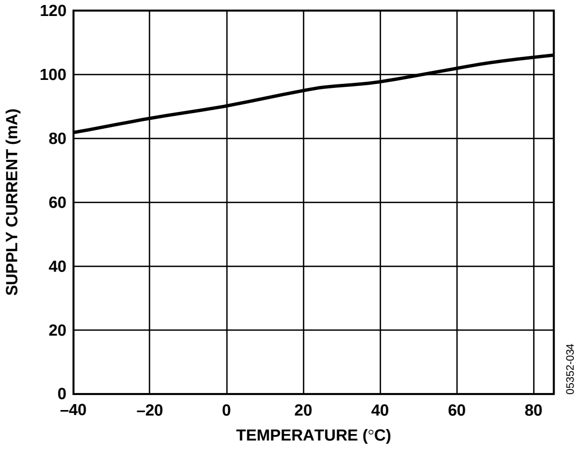


Figure 36. Supply Current vs. Temperature

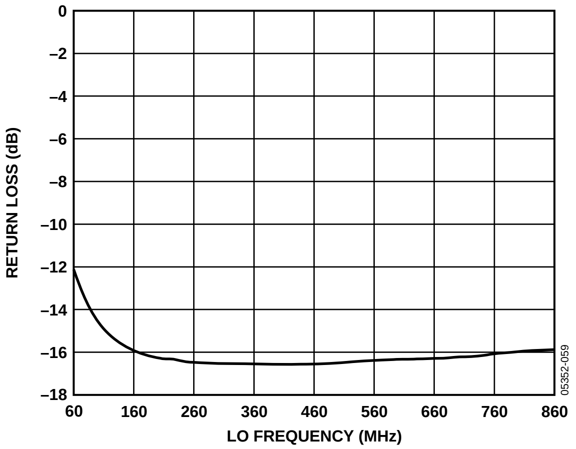


Figure 37. LO Return Loss vs. LO Frequency

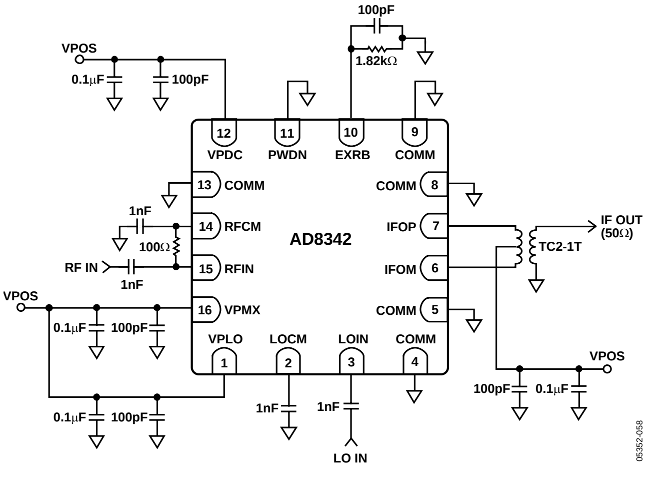


Figure 38. Characterization Circuit Used to Measure TPC Data

CIRCUIT DESCRIPTION

The AD8342 is an active mixer optimized for operation within the input frequency range of near dc to 500 MHz. It has a differential, high impedance RF input that can be terminated or matched externally. The RF input can be driven either single-ended or differentially. The LO input is a single-ended 50 Ω input. The IF outputs are differential open-collectors. The mixer current can be adjusted by the value of an external resistor to optimize performance for gain, compression, and intermodulation, or for low power operation. Figure 39 shows the basic blocks of the mixer, including the LO buffer, RF voltage-to-current converter, bias cell, and mixing core.

The RF voltage to RF current conversion is done via a resistively degenerated differential pair. To drive this port single-ended, the RFCM pin should be ac-grounded while the RFIN pin is ac-coupled to the signal source. The RF inputs can also be driven differentially. The voltage-to-current converter then drives the emitters of a four-transistor switching core. This switching core is driven by an amplified version of the local oscillator signal connected to the LO input. There are three limiting gain stages between the external LO signal and the switching core. The first stage converts the single-ended LO drive to a well-balanced differential drive. The differential drive then passes through two more gain stages, which ensures a limited signal drives the switching core. This affords the user a lower LO drive requirement, while maintaining excellent distortion and compression performance. The output signal of these three LO gain stages drives the four transistors within the mixer core to commutate at the rate of the local oscillator frequency. The output of the mixer core is taken directly from its open collectors. The open collector outputs present a high impedance at the IF frequency. The conversion gain of the mixer depends directly on the impedance presented to these open collectors. In characterization, a 100 Ω load was presented to the part via a 2:1 impedance transformer.

The device also features a power-down function. Application of a logic low at the PWDN pin allows normal operation. A high logic level at the PWDN pin shuts down the AD8342. Power consumption when the part is disabled is less than 10 mW.

The bias for the mixer is set with an external resistor (R_{BIAS}) from the EXRB pin to ground. The value of this resistor directly affects the dynamic range of the mixer. The external resistor should not be lower than 1.82 kΩ. Permanent damage to the part could result if values below 1.8 kΩ are used. This resistor sets the dc current through the mixer core. The performance effects of changing this resistor can be seen in the Typical Performance Characteristics section.

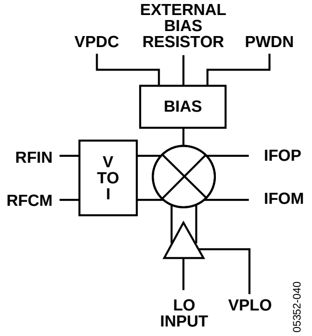


Figure 39. Simplified Schematic Showing the Key Elements of the AD8342

As shown in Figure 40, the IF output pins, IFOP and IFOM, are directly connected to the open collectors of the NPN transistors in the mixer core so the differential and single-ended impedances looking into this port are relatively high—on the order of several kΩ. A connection between the supply voltage and these output pins is required for proper mixer core operation.

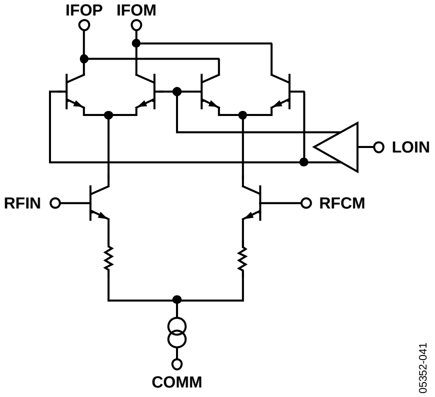


Figure 40. AD8342 Simplified Schematic

The AD8342 has three pins for the supply voltage: VPDC, VPMX, and VPLO. These pins are separated to minimize or eliminate possible parasitic coupling paths within the AD8342 that could cause spurious signals or reduced interport isolation. Consequently, each of these pins should be well bypassed and decoupled as close to the AD8342 as possible.

AC INTERFACES

The AD8342 is designed to downconvert radio frequencies (RF) to lower intermediate frequencies (IF) using a high or low-side local oscillator (LO). The LO is injected into the mixer core at a frequency higher or lower than the desired input RF. The difference between the LO and the RF , $f_{LO} – f_{RF,}$ (high side) or $f_{RF} – f_{LO}$ (low side) is the intermediate frequency, f_{IF}. In addition to the desired RF signal, an RF image is downconverted to the desired IF frequency. The image frequency is at $f_{LO} + f_{IF}$ when driven with a high side LO . When using a broadband load, the conversion gain of the AD8342 is nearly constant over the specified RF input band (see Figure 3).

The AD8342 is designed to operate over a broad frequency range. It is essential to ac-couple RF and LO ports to prevent dc offsets from skewing the mixer core in an asymmetrical manner, potentially degrading noise figure and linearity.

The RF input of the AD8342 is high impedance, 1 kΩ across the frequency range shown in Figure 41. The input capacitance decreases with frequency due to package parasitics.

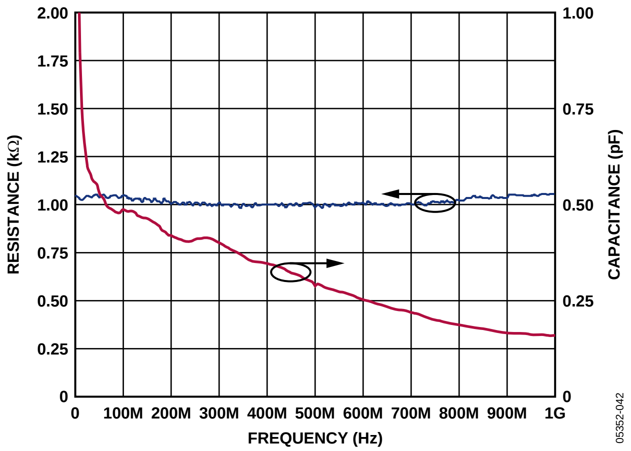


Figure 41. RF Input Impedance

The matching or termination used at the RF input of the AD8342 has a direct effect on its dynamic range. The characterization circuit, as well as the evaluation board, uses a 100 Ω resistor to terminate the RF port. This termination resistor in shunt with the input stage results in a return loss of better than −10 dBm (relative to 50 Ω). Table 4 shows gain, IP3, P1dB, and noise figure for four different input networks. This data was measured at an RF frequency of 250 MHz and at an LO frequency of 300 MHz.

Table 4. Dynamic Performance for Various Input Networks

Input Network	50 Ω Shunt	100 Ω Shunt	500 Ω Shunt	Matched (Fig. 40)
Gain (dB)	0.66	3.5	5.3	9.3
IIP3 (dBm)	25.4	22.9	20. 6	18.5
P1dB (dBm)	10.8	8.4	6.3	2.3
NF (dB)	14	12.5	10.2	10.5

The RF port can also be matched using an LC circuit, as shown in Figure 42.

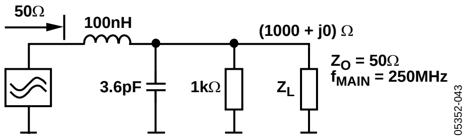
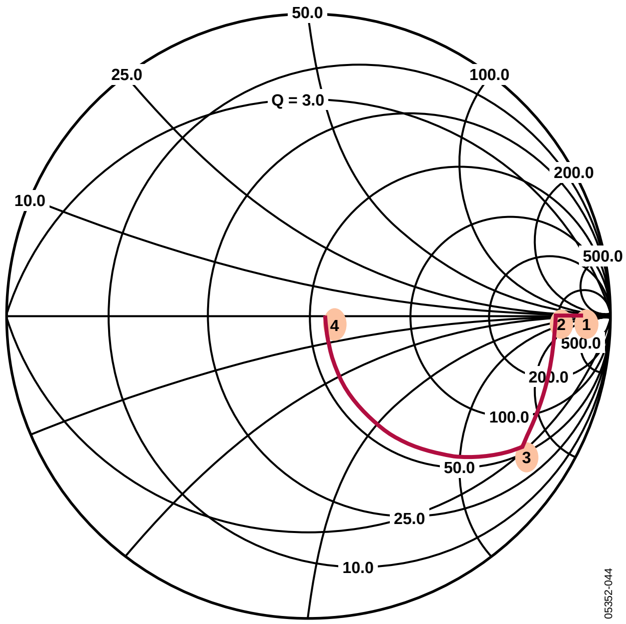


Figure 42. Matching Circuit

Impedance transformations of greater than 10:1 result in a higher Q circuit and thus a narrow RF input bandwidth. A 1 kΩ resistor is placed across the RF input of the device in parallel with the device internal input impedance, creating a 500 Ω load. This impedance is matched to as close as possible to 50 Ω for the source, with standard components using a shunt C, series L matching circuit (see Figure 43).



Point 1(1000.0 + j0.0)Ω Q = 0.0 at 250.000 MHz

Point 2(500.0 + j0.0)Ω Q = 0.0 at 250.000 MHz

Point 3(55.6 – j157.2)Ω Q = 2.8 at 250.000 MHz

Point 4(55.6 – j0.1)Ω Q = 0.0 at 250.000 MHz

Figure 43. LC Matching Example

IF PORT

The IF port comprises open-collector differential outputs. The NPN open collectors can be modeled as current sources that are shunted with resistances of ~10 kΩ in parallel with capacitances of ~1 pF.

The specified performance numbers for the AD8342 were measured with 100 Ω differential terminations. However, different load impedances may be used where circumstances dictate. In general, lower load impedances result in lower conversion gain and lower output P1dB. Higher load impedances result in higher conversion gain for small signals, but lower IP3 values for both input and output.

If the IF signal is to be delivered to a remote load, more than a few millimeters away at high output frequencies, avoid unintended parasitic effects due to the intervening PCB traces. One approach is to use an impedance transforming network or transformer located close to the AD8342. If very wideband output is desired, a nearby buffer amplifier may be a better choice, especially if IF response to dc is required. An example of such a circuit is presented in Figure 45, in which the AD8351 differential amplifier is used to drive a pair of 75 Ω transmission lines. The gain of the buffer can be independently set by appropriate choice of the value for the gain resistor, R_G.

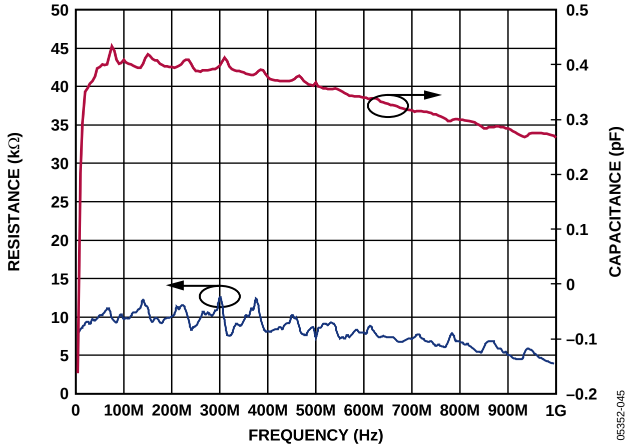


Figure 44. IF Port Impedance

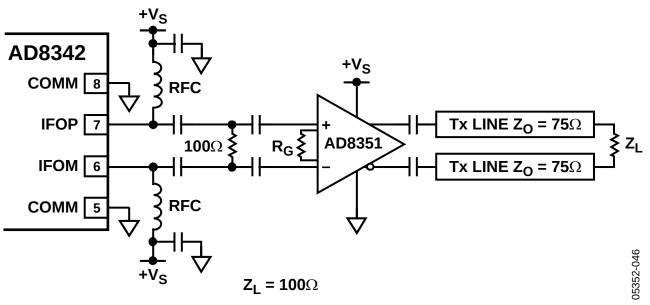


Figure 45. AD8351 Used as Transmission Line Driver and Impedance Buffer

The high input impedance of the AD8351 allows for a shunt differential termination to provide the desired 100 Ω load to the AD8342 IF output port.

It is necessary to bias the open-collector outputs using one of the schemes presented in Figure 47 and Figure 48. Figure 47 illustrates the application of a center tapped impedance transformer. The turns ratio of the transformer should be selected to provide the desired impedance transformation. In the case of a 50 Ω load impedance, a 2-to-1 impedance ratio transformer should be used to transform the 50 Ω load into a 100 Ω differential load at the IF output pins. Figure 48 illustrates a differential IF interface where pull-up choke inductors are used to bias the open-collector outputs. The shunting impedance of the choke inductors used to couple dc current into the mixer core should be large enough at the IF operating frequency so it does not load down the output current before reaching the intended load. Additionally, the dc current handling capability of the selected choke inductors needs to be at least 45 mA. The self-resonant frequency of the selected choke should be higher than the intended IF frequency. A variety of suitable choke inductors are commercially available from manufacturers such as Murata and Coilcraft. Figure 46 shows the loading effects when using nonideal inductors. An impedance transforming network may be required to transform the final load impedance to 100 Ω at the IF outputs. There are several good reference books that explain general impedance matching procedures, including:

- Chris Bowick, *RF Circuit Design*, Newnes, Reprint Edition, 1997.
- David M. Pozar, *Microwave Engineering*, Wiley Text Books, Second Edition, 1997.
- Guillermo Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*, Prentice Hall, Second Edition, 1996.

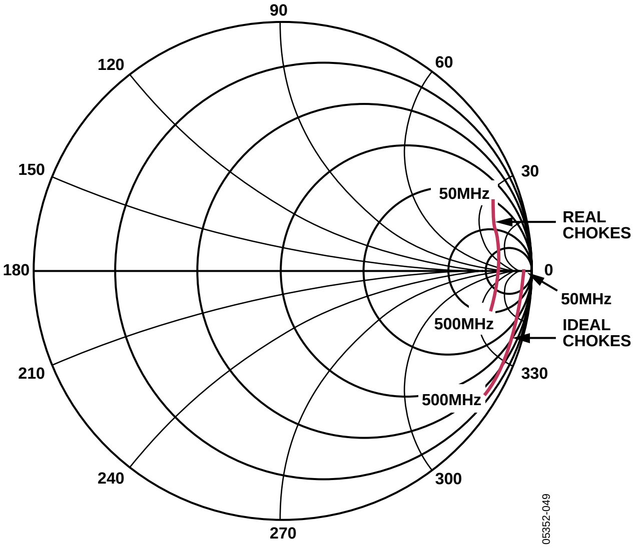


Figure 46. IF Port Loading Effects Due to Finite Q Pull-Up Inductors (Murata BLM18HD601SN1D Chokes)

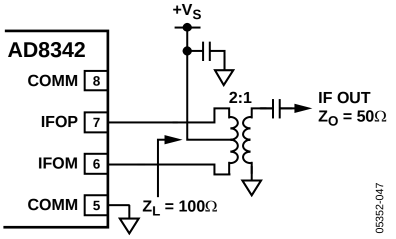


Figure 47. Biasing the IF Port Open-Collector Outputs Using a Center-Tapped Impedance Transformer

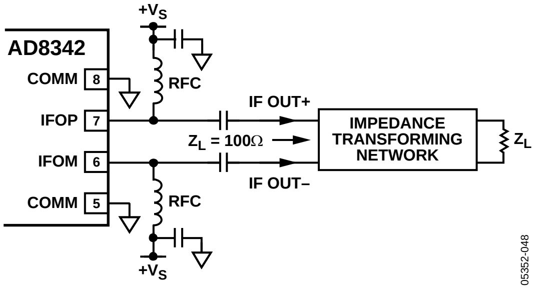


Figure 48. Biasing the IF Port Open-Collector Outputs Using Pull-Up Choke Inductors

The AD8342 is optimized for driving a 100 Ω load. Although the device is capable of driving a wide variety of loads, to maintain optimum distortion and noise performance, it is advised that the presented load at the IF outputs is close to 100 Ω. The linear differential voltage conversion gain of the mixer can be modeled as

$$Av = G_m \times R_{LOAD}$$

where:

$$G_m = \frac{1}{\pi}\frac{g_m}{1 + g_m R_e}$$

R_{LOAD} is the single-ended load impedance.

g_m is the transistor transconductance and is equal to 1810/R_{BIAS}.

R_e is 15 Ω.

The external R_{BIAS} resistor is used to control the power dissipation and dynamic range of the AD8342. Because the AD8342 has internal resistive degeneration, the conversion gain is primarily determined by the load impedance and the on-chip degeneration resistors. Figure 49 shows how gain varies with IF load. The external R_{BIAS} resistor has only a small effect. The most direct way to affect conversion gain is by varying the load impedance. Small loads result in lower gains while larger loads increase the conversion gain. If the IF load impedance is too large it causes a decrease in linearity (P1dB, IP3). In order to maintain positive conversion gain and preserve SFDR performance, the differential load presented at the IF port should remain in the range of ~ 100 Ω to 250 Ω.

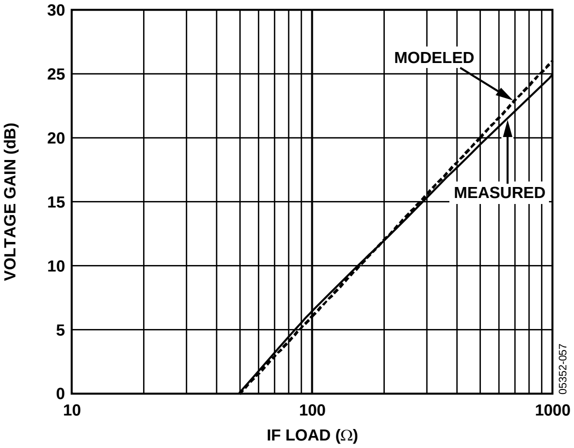


Figure 49. Voltage Conversion Gain vs. IF Loading

LO CONSIDERATIONS

The LOIN port provides a 50 Ω load impedance with common-mode decoupling on LOCM. Again, common-grade ceramic capacitors provide sufficient signal coupling and bypassing of the LO interface.

The LO signal needs to have adequate phase noise characteristics and low second-harmonic content to prevent degradation of the noise figure performance of the AD8342. An LO plagued with poor phase noise can result in reciprocal mixing, a mechanism that causes spectral spreading of the downconverted signal, limiting the sensitivity of the mixer at frequencies close-in to any large input signals. The internal LO buffer provides enough gain to hard-limit the input LO and provide fast switching of the mixer core. Odd harmonic content present on the LO drive signal should not impact mixer performance; however, even-order harmonics cause the mixer core to commutate in an unbalanced manner, potentially degrading noise performance. Simple lumped element low-pass filtering can be applied to help reject the harmonic content of a given local oscillator, as shown in Figure 50. The filter depicted is a common 3-pole Chebyshev, designed to maintain a 1-to-1 source-to-load impedance ratio with no more than 0.5 dB of ripple in the pass band. Other filter structures can be effective as long as the second harmonic of the LO is filtered to negligible levels, for example, ~30 dB below the fundamental.

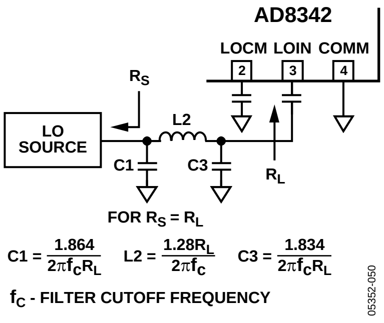


Figure 50. Using a Low-Pass Filter to Reduce LO Second Harmonic

HIGH IF APPLICATIONS

In some applications it may be desirable to use the AD8342 as an up-converting mixer. The AD8342 is a broadband mixer capable of both up and down conversion. Unlike other mixers that rely on on-chip reactive circuitry to optimize performance over a specific band, the AD8342 is a versatile general-purpose device that can be used from arbitrarily low frequencies to several GHz. In general, the following considerations help to ensure optimum performance:

- Minimize ac loading impedance of IF port bias network.
- Maximize power transfer to the desired ac load.
- For maximum conversion gain and the lowest noise performance reactively match the input as described in the IF Port section.
- For maximum input compression point and input intercept points resistively terminate the input as described in the IF Port section.

As an example, Figure 51 shows the AD8342 as an up-converting mixer for a WCDMA single-carrier transmitter design. For this application, it was desirable to achieve −65 dBc adjacent channel power ratio (ACPR) at a −13 dBm output power level. The ACPR is a measure of both distortion and noise carried into an adjacent frequency channel due to the finite intercept points and noise figure of an active device.

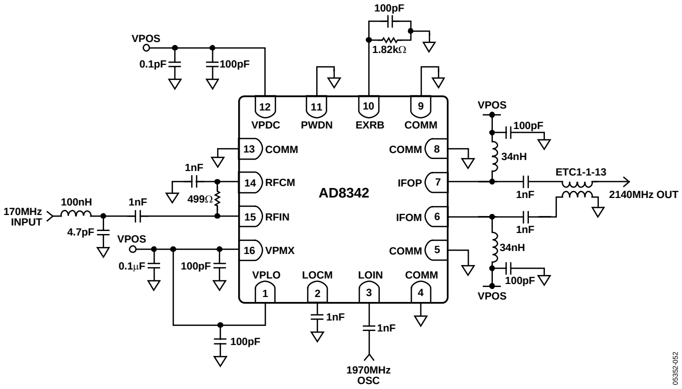


Figure 51. WCDMA Tx Up-Conversion Application Circuit

Because a WCDMA channel encompasses a bandwidth of almost 5 MHz, it is necessary to keep the Q of the matching circuit low enough so that phase and magnitude variations are below an acceptable level over the 5 MHz band. It is possible to use purely reactive matching to transform a 50 Ω source to match the raw ~1 kΩ input impedance of the AD8342. However, the L and C component variations could present production concerns due to the sensitivity of the match. For this application, it is advantageous to shunt down the ~1 kΩ input impedance using an external shunt termination resistor to allow for a lower Q reactive matching network. The input is terminated across the RFIN and RFCM pins using a 499 Ω termination. The termination should be as close to the device as possible to minimize standing wave concerns. The RFCM is bypassed to ground using a 1 nF capacitor. A dc blocking capacitor of 1 nF is used to isolate the dc input voltage present on the RFIN pin from the source. A step-up impedance transformation is realized using a series L shunt C reactive network. The actual values used need to accommodate for the series L and stray C parasitics of the connecting transmission line segments. When using the customer evaluation board with the components specified in Figure 51, the return loss over a 5 MHz band centered at 170 MHz was better than 10 dB.

External pull-up choke inductors are used to feed dc bias into the open-collector outputs. It is desirable to select pull-up choke inductors that present high loading reactance at the output frequency. Coilcraft 0302CS series inductors were selected due to their very high self-resonant frequency and Q. A 1:1 balun was ac-coupled to the output to convert the differential output to a single-ended signal and present the output with a 50 Ω ac loading impedance.

The performance of the circuit is shown in Figure 52. The average ACPR of the adjacent and alternate channels is presented vs. output power. The circuit provides a 65 dBc ACPR at −13 dBm output power. The optimum ACPR power level can be shifted to the right or left by adjusting the output loading and the loss of the input match.

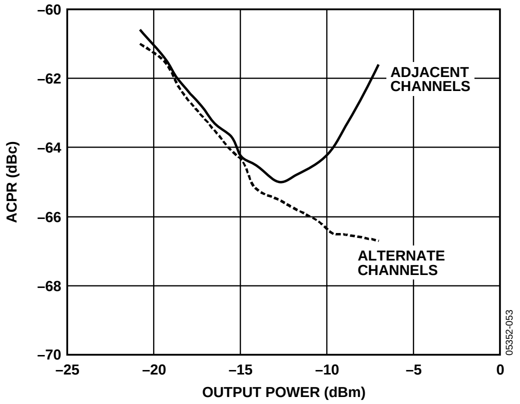


Figure 52. Single Carrier WCDMA ACPR Performance of Tx Up-Conversion Circuit (Test Model 1_64)

EVALUATION BOARD

An evaluation board is available for the AD8342. The evaluation board is configured for single-ended signaling at the IF output port via a balun transformer. The schematic for the evaluation board is presented in Figure 53.

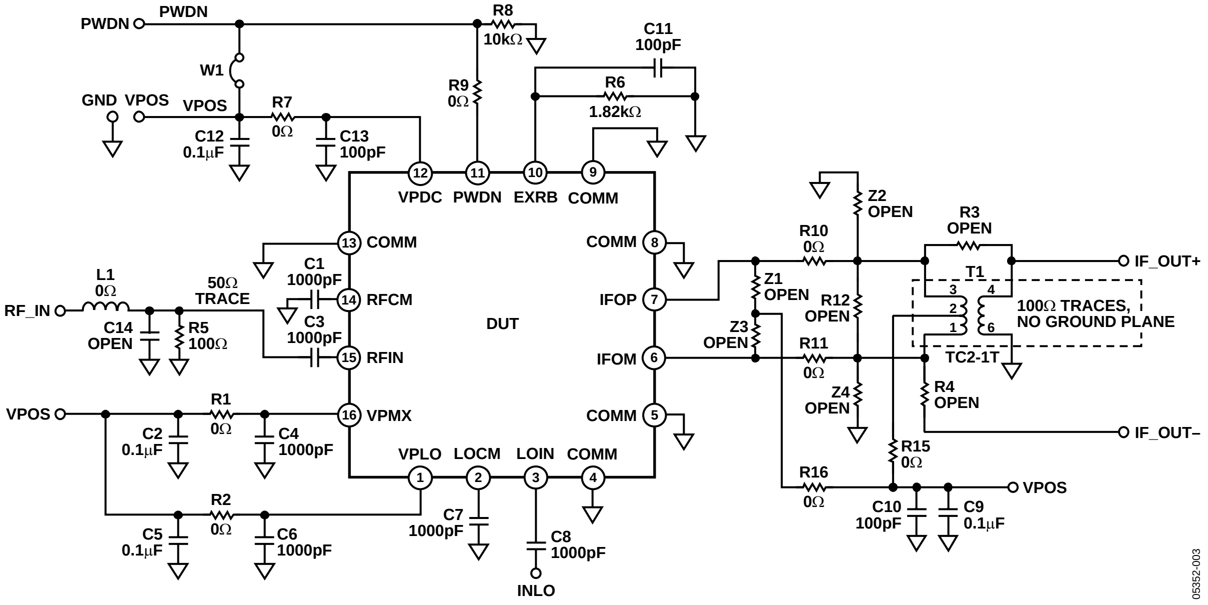
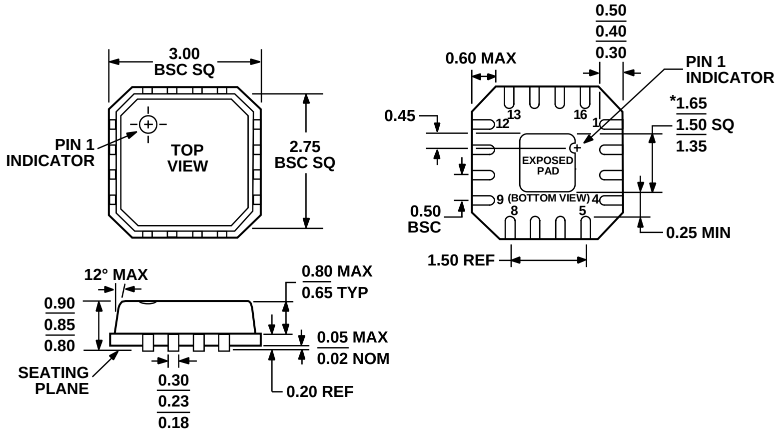


Figure 53. Evaluation Board

Table 6. Evaluation Board Configuration Options

Component	Function	Default Conditions
R1, R2, R7, C2, C4, C5, C6, C10 C12, C13, C14, C9	Supply decoupling. Shorts or power supply decoupling resistors and filter capacitors.	R1, R2, R7 = 0 Ω C4, C6 = 1000 pF C10, C13 = 100 pF C2, C5, C12, C9 = 0.1 µF
R3, R4	Options for single-ended IF output circuit.	R3, R4 = Open Ω
R15, 16		R15, R16 = 0 Ω
R6, C11	R_{BIAS} resistor that sets the bias current for the mixer core. The capacitor provides ac bypass for R6.	R6 = 1.82 kΩ C11 = 100 pF
R8	Pull down for the PWDN pin.	R8 = 10 kΩ
R9	Link to PWDN pin.	R9 = 0 Ω
C3, R5, C16, L1	RF input. C3 provides dc block for RF input. R5 provides a resistive input termination. C16 and L1 are provided for reactive matching the input.	C3 = 1000 pF R5 = 100 Ω C14 = Open L1 = 0 Ω
C1	RF common ac coupling. Provides dc block for RF input common connection.	C1 = 1000 pF
C8	LO input ac coupling. Provides dc block for the LO input.	C7, C8 = 1000 pF
C7	LO common ac coupling. Provides dc block for LO input common connection.	
W1	Power down. The part is on when the PWDN is connected to ground via a 10 kΩ resistor. The part is disabled when PWDN is connected to the positive supply (V_S) via W1.	
T1, R12, R11, Z3, Z4, Z1, Z2, R10	IF output interface. T1 converts a differential high impedance IF output to single-ended. When loaded with 50 Ω, this balun presents a 100 Ω load to the mixers collectors. The center tap of the primary is used to supply the bias voltage (V_S) to the IF output pins.	T1 = TC2-1T, 2:1 (Mini-Circuits) R12 = Open Ω R10, R11 = 0 Ω Z3, Z4 = Open Z1, Z2 = Open

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-220-VEED-2
EXCEPT FOR EXPOSED PAD DIMENSION.

Figure 54. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm x 3 mm Body, Very Thin Quad
(CP-16-3)
Dimensions in millimeters

ORDERING GUIDE

Models	Temperature Package	Package Description	Package Outline	Branding	Transport Media, Quanity
AD8342ACPZ-REEL7[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-3	Q01	1,500, Reel
AD8342ACPZ-R2[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-3	Q01	250, Reel
AD8342ACPZ-WP[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-3	Q01	50, Waffle Pack
AD8342-EVAL		Evaluation Board			1

[1] Z = Pb-free part.

D05352–0–4/05(0)