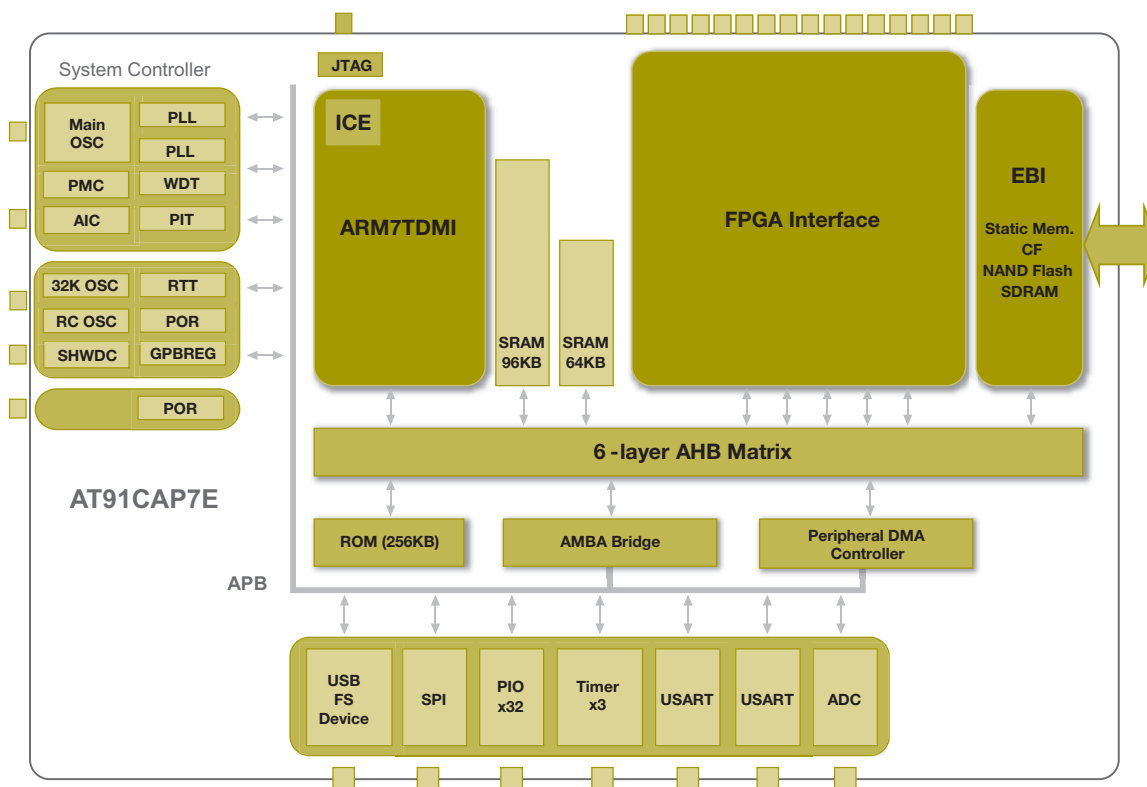# ⬈ AT91CAP7E

AT91CAP7E is an ARM7™-based MCU with a direct FPGA interface, six-layer advanced high-speed bus (AHB), peripheral DMA controller and 160 Kbytes of on-chip SRAM. It offers seamless migration to AT91CAP7 customizable MCUs for ARM7-plus-FPGA designs. It includes on-chip peripherals such as USB 2.0 full speed device, SPI master and slave, two USARTs, three 16-bit timer counters, an 8-channel/10-bit analog to digital converter, plus a full-functioned system controller including interrupt and power control and supervisory functions.

The FPGA interface on the AT91CAP7E provides the FPGA with direct access to the AT91CAP7E's on-chip AHB and peripheral DMA controller. This architecture eliminates FPGA-induced bus contention, off-loads MCU-to-FPGA communications from the CPU, and frees up the external bus interface for external memory access.

Interfacing an ARM7-based MCU to an FPGA has traditionally been done through the external bus interface (EBI) or programmable I/O. Either arrangement requires that the CPU transfer data to and from


the FPGA one word-at-a-time, basically stealing CPU cycles that should be conserved for processing and limiting access to external memory during FPGA operations.

The FPGA interface on Atmel's AT91CAP7E provides the FPGA with two AHB masters, four AHB slaves, a special direct AHB slave interface to an external RAM through the FPGA, and a programmable ROM that remaps the external RAM to emulate and debug the ROM code. Fourteen advanced peripheral bus (APB) slaves, two full-duplex DMA channels and 32-bit programmable I/O may be hardware selected to share I/O. An on-chip priority interrupt controller provides up to 13 encoded interrupts and two additional un-encoded interrupts for DMA transfers.

Atmel provides FPGA logic that decodes and encodes the bus traffic that flows between the FPGA and the AT91CAP7E microcontroller. The logic blocks inside the FPGA are connected to the AT91CAP7E via the AHB master and slave channels.

The AT91CAP7E is a standard microcontroller with an FPGA interface that makes the FPGA look and work like it is on the internal bus on the MCU. Customers who are considering the AT91CAP7 customizable MCU for their designs, frequently need a two-chip, no-NRE, FPGA-plus ARM7 solution as they are gaining market momentum. The AT91CAP7E provides such a solution and offers an engineering-free migration path to a lower cost, lower power customizable MCU when volume justifies it. The AT91CAP7E is available in a 225 LFBGA package (13 x 13 x 1.4mm).

CAP7E

CAP7E to FPGA Interface
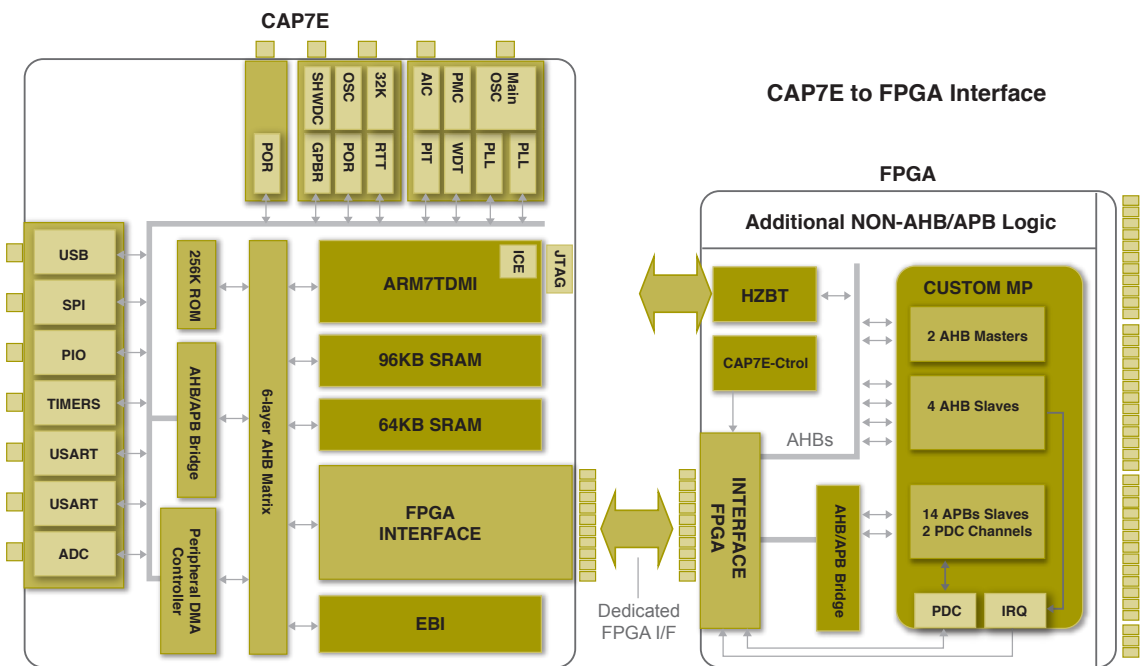
AT91CAP7 Customizable MCUs

Atmel's AT91CAP7 customizable MCU is an ARM7-based microcontroller with a metal-programmable (MP) block with 450K gates or the equivalent of 56K FPGA logic cells (LC). Any functionality that has been implemented in an FPGA may be migrated directly to a CAP7 device with no special EDA tools or customer-side engineering. Standard FPGA software tools are all that is necessary to implement functions such as LCD controllers, DSP algorithms (e.g. GPS correlators, FFTs, FIR filters), and proprietary customer IP. A AT91CAP7 implementation delivers as much as 8X better performance, consumes 98% less static power, and costs about 30% less than the FPGA-plus-MCU implementation. The AT91CAP7 is available in multiple packages.

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