

## Features

- Very high speed: 45 ns
- Temperature ranges
  - Industrial: -40°C to +85°C
  - Automotive-A: -40°C to +85°C
  - Automotive-E: -40°C to +125°C
- Voltage range: 4.5V to 5.5V
- Pin compatible with CY62128B
- Ultra low standby power
  - Typical standby current: 1  $\mu$ A
  - Maximum standby current: 4  $\mu$ A (Industrial)
- Ultra low active power
  - Typical active current: 1.3 mA at f = 1 MHz
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Offered in standard Pb-free 32-pin STSOP, 32-pin SOIC, and 32-pin TSOP I packages

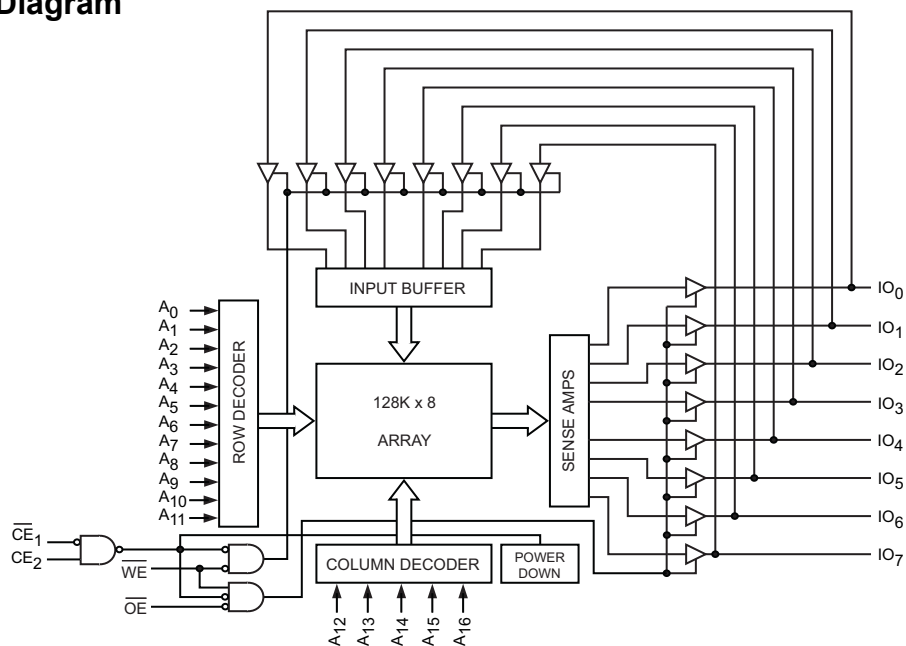
## Functional Description

The CY62128E<sup>[1]</sup> is a high performance CMOS static RAM organized as 128K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW). The eight input and output pins (IO<sub>0</sub> through IO<sub>7</sub>) are placed in a high impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or a write operation is in progress ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH and  $\overline{WE}$  LOW)

To write to the device, take Chip Enable ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight IO pins (IO<sub>0</sub> through IO<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>).

To read from the device, take Chip Enable ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the IO pins.

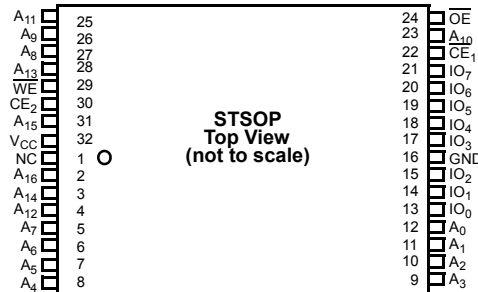
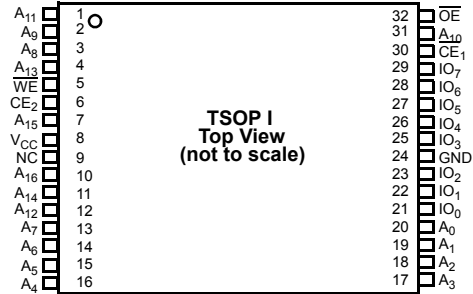
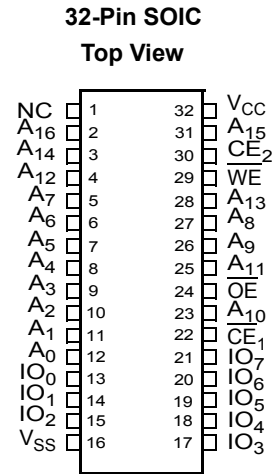
## Logic Block Diagram



### Note

1. For best practice recommendations, refer to the Cypress application note "System Design Guidelines" at <http://www.cypress.com>.

### Pin Configuration<sup>[2]</sup>



### Product Portfolio

Product	Range	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
						Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
						f = 1MHz		f = f <sub>max</sub>			
Min	Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max			
CY62128ELL	Ind'l/Auto-A	4.5	5.0	5.5	45 <sup>[4]</sup>	1.3	2	11	16	1	4
CY62128ELL	Auto-E	4.5	5.0	5.5	55	1.3	4	11	35	1	30

**Notes**

- NC pins are not connected on the die.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25°C.
- When used with a 100 pF capacitive load and resistive loads as shown on page 4, access times of 55 ns (t<sub>AA</sub>, t<sub>ACE</sub>) and 25 ns (t<sub>DOE</sub>) are guaranteed.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied .....	-55°C to +125°C
Supply Voltage to Ground Potential.....	-0.5V to 6.0V ( $V_{CC(max)}$ + 0.5V)
DC Voltage Applied to Outputs in High-Z State <sup>[5, 6]</sup> .....	-0.5V to 6.0V ( $V_{CC(max)}$ + 0.5V)
DC Input Voltage <sup>[5, 6]</sup> .....	-0.5V to 6.0V ( $V_{CC(max)}$ + 0.5V)

Output Current into Outputs (LOW).....	20 mA
Static Discharge Voltage.....	> 2001V (MIL-STD-883, Method 3015)
Latch up Current.....	> 200 mA

## Operating Range

Device	Range	Ambient Temperature	$V_{CC}$ <sup>[7]</sup>
CY62128ELL	Ind'I/Auto-A	-40°C to +85°C	4.5V to 5.5V
	Auto-E	-40°C to +125°C	

## Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	45 ns (Ind'I/Auto-A)			55 ns (Auto-E)			Unit
			Min	Typ <sup>[3]</sup>	Max	Min	Typ <sup>[3]</sup>	Max	
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -1$ mA	2.4			2.4			V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 2.1$ mA			0.4			0.4	V
$V_{IH}$	Input HIGH Voltage	$V_{CC} = 4.5V$ to 5.5V	2.2		$V_{CC} + 0.5$	2.2		$V_{CC} + 0.5$	V
$V_{IL}$	Input LOW voltage	$V_{CC} = 4.5V$ to 5.5V	-0.5		0.8	-0.5		0.8	V
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		+1	-4		+4	$\mu$ A
$I_{OZ}$	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-1		+1	-4		+4	$\mu$ A
$I_{CC}$	$V_{CC}$ Operating Supply Current	$f = f_{max} = 1/t_{RC}$ $V_{CC} = V_{CC(max)}$		11	16		11	35	mA
		$f = 1$ MHz $I_{OUT} = 0$ mA CMOS levels		1.3	2		1.3	4	
$I_{SB2}$ <sup>[8]</sup>	Automatic CE Power down Current—CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0$ , $V_{CC} = V_{CC(max)}$		1	4		1	30	$\mu$ A

## Capacitance (For all Packages)<sup>[9]</sup>

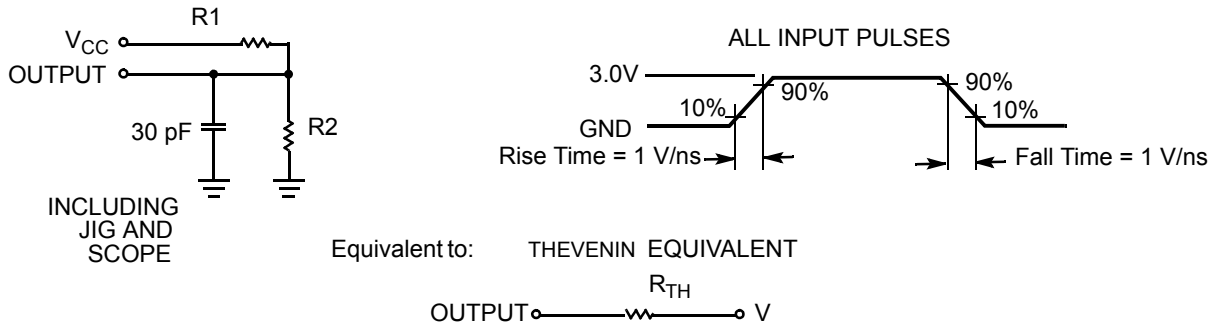
Parameter	Description	Test Conditions	Max	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ C$ , $f = 1$ MHz, $V_{CC} = V_{CC(typ)}$	10	pF
$C_{OUT}$	Output Capacitance		10	pF

### Notes

- $V_{IL(min)}$  = -2.0V for pulse durations less than 20 ns.
- $V_{IH(max)}$  =  $V_{CC} + 0.75V$  for pulse durations less than 20 ns.
- Full device AC operation assumes a 100  $\mu$ s ramp time from 0 to  $V_{CC(min)}$  and 200  $\mu$ s wait time after  $V_{CC}$  stabilization.
- Only chip enables ( $\overline{CE}_1$  and  $CE_2$ ) must be at CMOS level to meet the  $I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating.
- Tested initially and after any design or process changes that may affect these parameters.

**Thermal Resistance<sup>[9]</sup>**

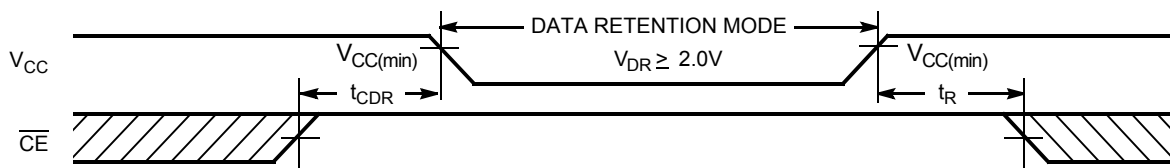
Parameter	Description	Test Conditions	SOIC Package	STSOP Package	TSOP Package	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	48.67	32.56	33.01	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		25.86	3.59	3.42	°C/W

**AC Test Loads and Waveform**


Parameters	Value	Unit
R1	1800	Ω
R2	990	Ω
R <sub>TH</sub>	639	Ω
V <sub>TH</sub>	1.77	V

**Data Retention Characteristics (Over the Operating Range)**

Parameter	Description	Conditions	Min	Typ <sup>[3]</sup>	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		2			V
I <sub>CCDR</sub> <sup>[8]</sup>	Data Retention Current	V <sub>CC</sub> = V <sub>DR</sub> , $\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V			4	μA
		Ind'I/Auto-A			30	μA
t <sub>CDR</sub> <sup>[9]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[10]</sup>	Operation Recovery Time		t <sub>RC</sub>			ns

**Data Retention Waveform<sup>[11]</sup>**

**Notes**

10. Full device AC operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> ≥ 100 μs or stable at V<sub>CC(min)</sub> ≥ 100 μs.

11.  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and CE<sub>2</sub>. When  $\overline{CE}_1$  is LOW and CE<sub>2</sub> is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or CE<sub>2</sub> is LOW,  $\overline{CE}$  is HIGH.

**Switching Characteristics** (Over the Operating Range)<sup>[12]</sup>

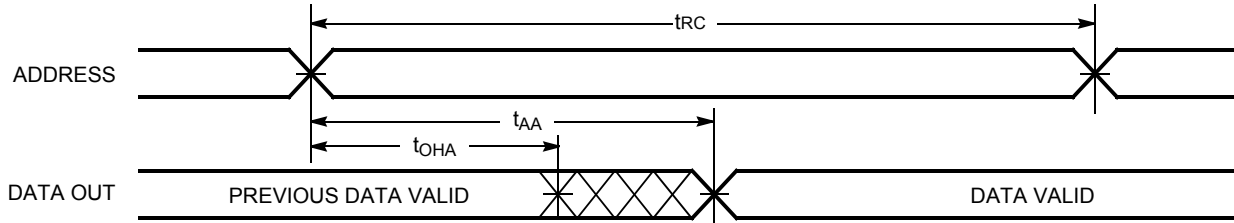
Parameter	Description	45 ns (Ind'l/Auto-A)		55 ns (Auto-E)		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
$t_{RC}$	Read Cycle Time	45		55		ns
$t_{AA}$	Address to Data Valid		45		55	ns
$t_{OHA}$	Data Hold from Address Change	10		10		ns
$t_{ACE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Data Valid		45		55	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		22		25	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low-Z <sup>[13]</sup>	5		5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High-Z <sup>[13, 14]</sup>		18		20	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Low-Z <sup>[13]</sup>	10		10		ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH or $CE_2$ LOW to High-Z <sup>[13, 14]</sup>		18		20	ns
$t_{PU}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Power Up	0		0		ns
$t_{PD}$	$\overline{CE}_1$ HIGH or $CE_2$ LOW to Power Down		45		55	ns
<b>Write Cycle<sup>[15]</sup></b>						
$t_{WC}$	Write Cycle Time	45		55		ns
$t_{SCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Write End	35		40		ns
$t_{AW}$	Address Setup to Write End	35		40		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Setup to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	35		40		ns
$t_{SD}$	Data Setup to Write End	25		25		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z <sup>[13, 14]</sup>		18		20	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z <sup>[13]</sup>	10		10		ns

**Notes**

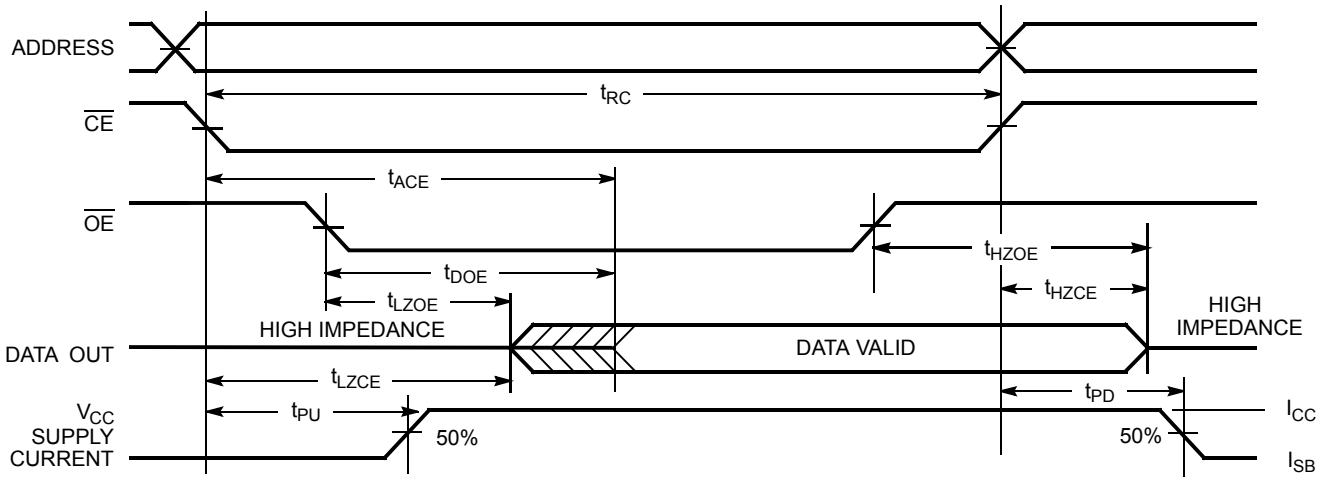
12. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3ns (1V/ns) or less, timing reference levels of 1.5V, input pulse levels of 0 to 3V, and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the "™" on page 4.
13. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
14.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
15. The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $CE = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

### Switching Waveforms

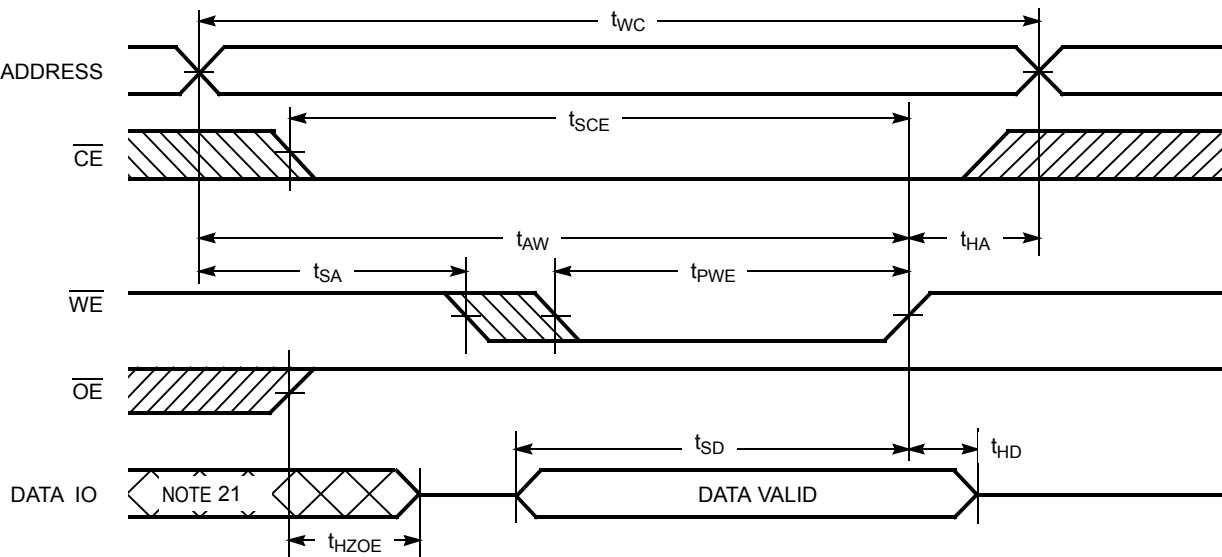
**Figure 1. Read Cycle 1 (Address Transition Controlled)** [16, 17]



**Figure 2. Read Cycle No. 2 ( $\overline{OE}$  Controlled)** [11, 17, 18]



**Figure 3. Write Cycle No. 1 ( $\overline{WE}$  Controlled)** [11, 15, 19, 20]



**Notes:**

- 16. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
- 17. WE is HIGH for read cycle.
- 18. Address valid before or similar to  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.
- 19. Data IO is high impedance if  $\overline{OE} = V_{IH}$ .
- 20. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in high impedance state.
- 21. During this period, the IOs are in output state and input signals must not be applied.

Switching Waveforms (continued)

Figure 4. Write Cycle No. 2 ( $\overline{CE1}$  or  $CE2$  Controlled) [11, 15, 19, 20]

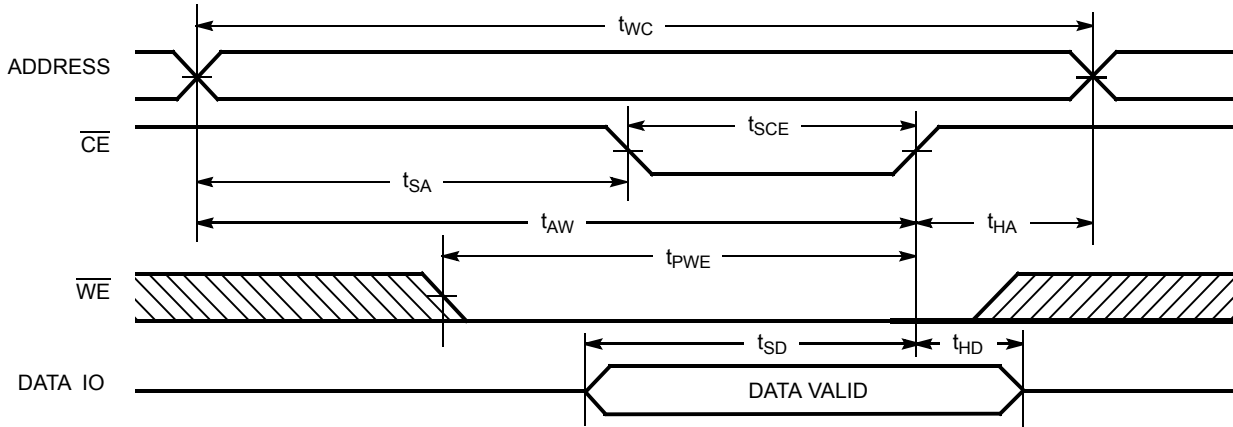
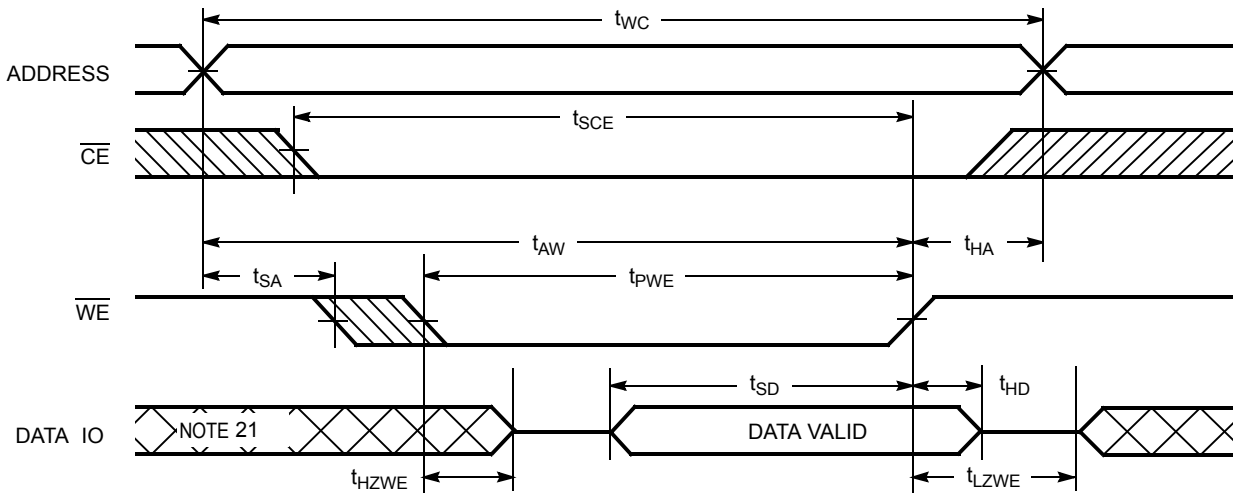


Figure 5. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [11, 20]



Truth Table

$CE_1$	$CE_2$	$WE$	$OE$	Inputs/Outputs	Mode	Power
H	X	X	X	High-Z	Deselect/Power down	Standby ( $I_{SB}$ )
X	L	X	X	High-Z	Deselect/Power down	Standby ( $I_{SB}$ )
L	H	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	H	L	X	Data In	Write	Active ( $I_{CC}$ )
L	H	H	H	High-Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

### Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62128ELL-45SXI	51-85081	32-pin 450-Mil SOIC (Pb-free)	Industrial
	CY62128ELL-45ZAXI	51-85094	32-pin STSOP (Pb-free)	
	CY62128ELL-45ZXI	51-85056	32-pin TSOP Type I (Pb-free)	
45	CY62128ELL-45SXA	51-85081	32-pin 450-Mil SOIC (Pb-free)	Automotive-A
	CY62128ELL-45ZXA	51-85056	32-pin TSOP Type I (Pb-free)	
55	CY62128ELL-55SXE	51-85081	32-pin 450-Mil SOIC (Pb-free)	Automotive-E
	CY62128ELL-55ZAXE	51-85094	32-pin STSOP (Pb-free)	

Contact your local Cypress sales representative for availability of these parts.

### Package Diagrams

Figure 6. 32-pin (450 Mil) Molded SOIC (51-85081)

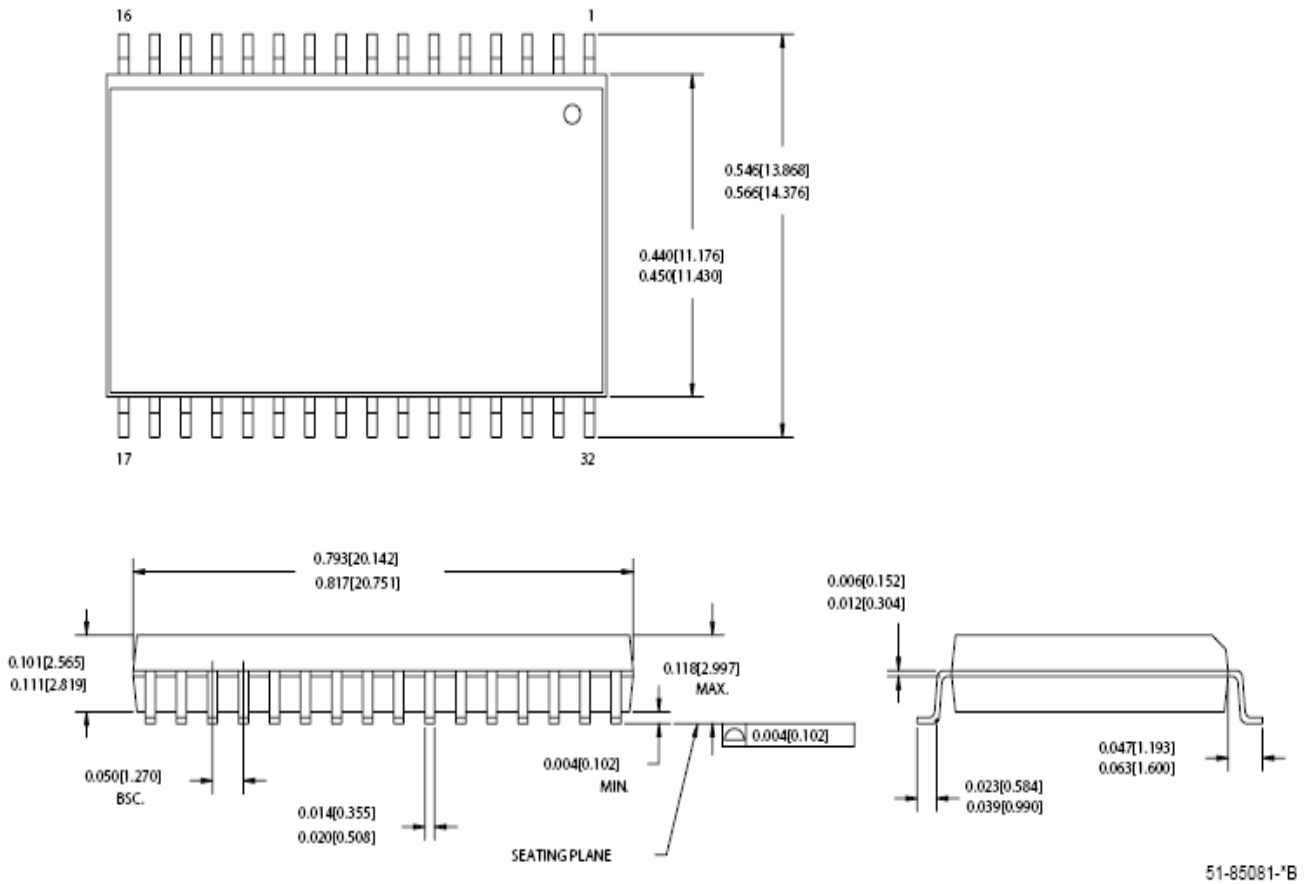




Figure 7. 32-pin Shrunk Thin Small Outline Package (8 x 13.4 mm) (51-85094)

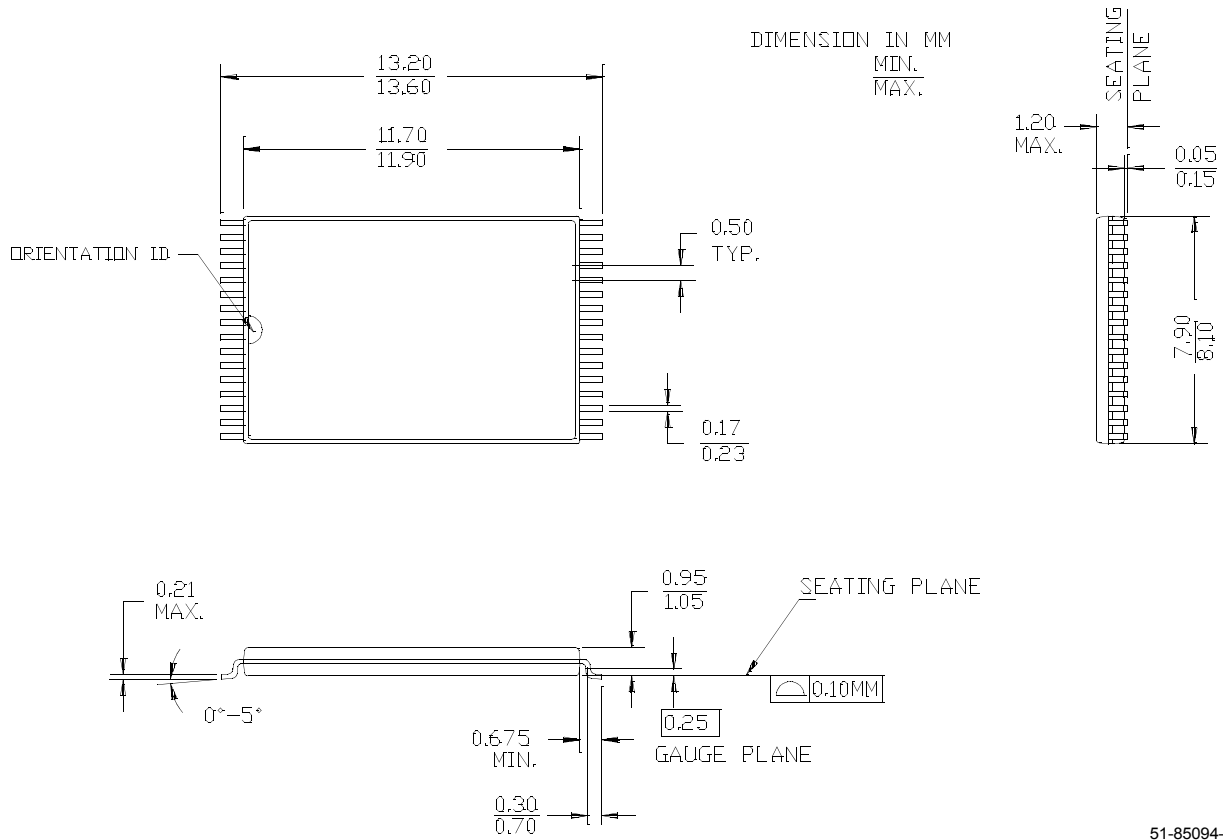
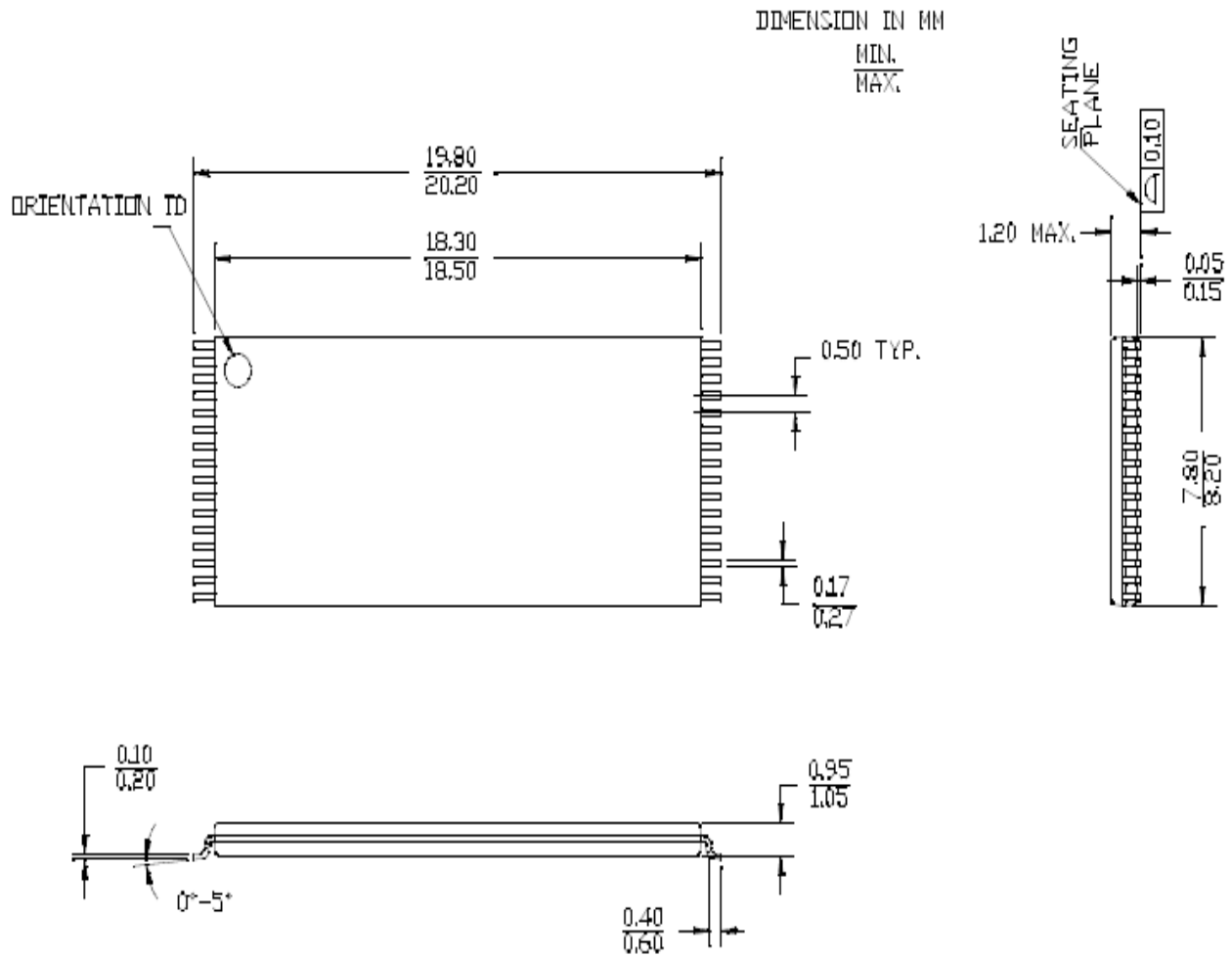


Figure 8. 32-pin Thin Small Outline Package Type I (8 x 20 mm) (51-85056)



51-85056-1U

**Document History Page**

Document Title: CY62128E MoBL <sup>®</sup> 1-Mbit (128K x 8) Static RAM				
Document Number: 38-05485				
Revision	ECN	Submission Date	Orig. of Change	Description of Change
**	203120	See ECN	AJU	New data sheet
*A	299472	See ECN	SYT	Converted from Advance Information to Preliminary Changed $t_{OHA}$ from 6 ns to 10 ns for both 35 ns and 45 ns, respectively Changed $t_{DOE}$ from 15 ns to 18 ns for 35 ns speed bin Changed $t_{HZOE}$ , $t_{HZWE}$ from 12 and 15 ns to 15 and 18 ns for the 35 and 45 ns speed bins, respectively Changed $t_{HZCE}$ from 12 and 15 ns to 18 and 22 ns for the 35 and 45 ns speed bins, respectively Changed $t_{SCE}$ from 25 and 40 ns to 30 and 35 ns for the 35 and 45 ns speed bins, respectively Changed $t_{SD}$ from 15 and 20 ns to 18 and 22 ns for the 35 and 45 ns speed bins, respectively Added Pb-free package information Added footnote #9 Changed operating range for SOIC package from Commercial to Industrial Modified signal transition time from 5 ns to 3 ns in footnote #11 Changed max of $I_{SB1}$ , $I_{SB2}$ and $I_{CCDR}$ from 1.0 $\mu$ A to 1.5 $\mu$ A
*B	461631	See ECN	NXR	Converted from Preliminary to Final Included Automotive Range and 55 ns speed bin Removed 35 ns speed bin Removed "L" version of CY62128E Removed Reverse TSOP I package from Product offering Changed $I_{CC(Typ)}$ from 8 mA to 11 mA and $I_{CC(max)}$ from 12 mA to 16 mA for $f = f_{max}$ Changed $I_{CC(max)}$ from 1.5 mA to 2.0 mA for $f = 1$ MHz Removed $I_{SB1}$ DC Specs from Electrical characteristics table Changed $I_{SB2(max)}$ from 1.5 $\mu$ A to 4 $\mu$ A Changed $I_{SB2(Typ)}$ from 0.5 $\mu$ A to 1 $\mu$ A Changed $I_{CCDR(max)}$ from 1.5 $\mu$ A to 4 $\mu$ A Changed the AC Test load Capacitance value from 100 pF to 30 pF Changed $t_{LZOE}$ from 3 to 5 ns Changed $t_{LZCE}$ from 6 to 10 ns Changed $t_{HZCE}$ from 22 to 18 ns Changed $t_{PWE}$ from 30 to 35 ns Changed $t_{SD}$ from 22 to 25 ns Changed $t_{LZWE}$ from 6 to 10 ns Updated the Ordering Information Table
*C	464721	See ECN	NXR	Updated the Block Diagram on page # 1
*D	563144	See ECN	AJU	Added footnote 4 on page 2
*E	1024520	See ECN	VKN	Added Automotive-A information Converted Automotive-E specs to final Added footnote #9 related to $I_{SB2}$ and $I_{CCDR}$ Updated Ordering Information table
*F	2548575	08/05/08	NXR	Corrected typo error in Ordering Information table

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