# 4-Mbit (256K x 16) Static RAM

## Features

■ Very high speed: 45 ns

■ Wide voltage range: 4.5V–5.5V

■ Ultra low standby power
  ❏ Typical standby current: 1 $\mu$A
  ❏ Maximum standby current: 7 $\mu$A

■ Ultra low active power
  ❏ Typical active current: 2 mA at f = 1 MHz

■ Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features

■ Automatic power down when deselected

■ CMOS for optimum speed and power

■ Available in Pb-free 44-pin TSOP II package

## Functional Description

The CY62146E is a high performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that reduces power consumption when a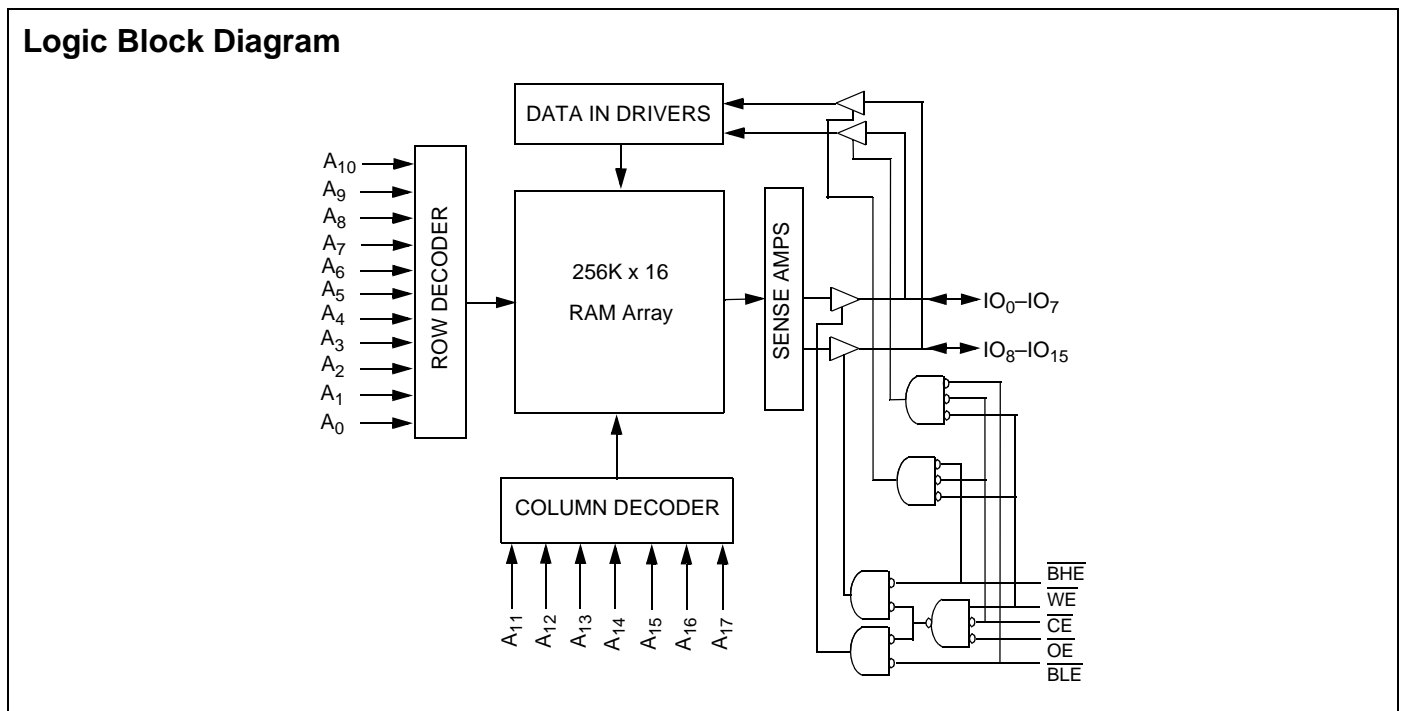ddresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ($\overline{CE}$ HIGH). The input and output pins ($IO_0$ through $IO_{15}$) are placed in a high impedance state when:

■ Deselected ($\overline{CE}$ HIGH)

■ Outputs are disabled ($\overline{OE}$ HIGH)

■ Both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH)

■ Write operation is active ($\overline{CE}$ LOW and $\overline{WE}$ LOW)

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from IO pins ($IO_0$ through $IO_7$) is written into the location specified on the address pins ($A_0$ through $A_{17}$). If Byte High Enable ($\overline{BHE}$) is LOW, then data from IO pins ($IO_8$ through $IO_{15}$) is written into the location specified on the address pins ($A_0$ through $A_{17}$).
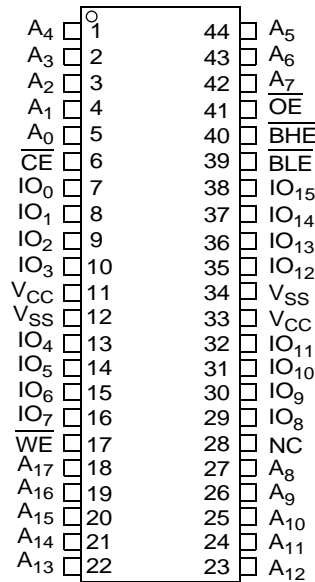
To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on $IO_0$ to $IO_7$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on $IO_8$ to $IO_{15}$. See Table 1 for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

## Logic Block Diagram

[+] Feedback

## Pin Configuration

**Figure 1.  44-Pin TSOP II (Top View)** [1]

```
A4   [ 1      44 ]  A5
A3   [ 2      43 ]  A6
A2   [ 3      42 ]  A7
A1   [ 4      41 ]  OE
A0   [ 5      40 ]  BHE
CE   [ 6      39 ]  BLE
IO0  [ 7      38 ]  IO15
IO1  [ 8      37 ]  IO14
IO2  [ 9      36 ]  IO13
IO3  [ 10     35 ]  IO12
VCC  [ 11     34 ]  VSS
VSS  [ 12     33 ]  VCC
IO4  [ 13     32 ]  IO11
IO5  [ 14     31 ]  IO10
IO6  [ 15     30 ]  IO9
IO7  [ 16     29 ]  IO8
WE   [ 17     28 ]  NC
A17  [ 18     27 ]  A8
A16  [ 19     26 ]  A9
A15  [ 20     25 ]  A10
A14  [ 21     24 ]  A11
A13  [ 22     23 ]  A12
```

## Product Portfolio

| Product | Range | V$_{CC}$ Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| | | | | | | Operating I$_{CC}$, (mA) | | | | Standby, I$_{SB2}$ ($\mu$A) | |
| | | | | | | f = 1 MHz | | f = f$_{max}$ | | | |
| | | Min | Typ[2] | Max | | Typ [2] | Max | Typ [2] | Max | Typ [2] | Max |
| CY62146ELL | Ind'l/Auto-A | 4.5 | 5.0 | 5.5 | 45 | 2 | 2.5 | 15 | 20 | 1 | 7 |

**Notes**
1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A$ = 25°C.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ................................. −65°C to +150°C

Ambient Temperature with
Power Applied ........................................... −55°C to +125°C

Supply Voltage to Ground Potential .................. −0.5V to 6.0V

DC Voltage Applied to Outputs
in High-Z State [3, 4] ........................................... −0.5V to 6.0V

DC Input Voltage [3, 4] ...................................... −0.5V to 6.0V

Output Current into Outputs (LOW) ............................ 20 mA

Static Discharge Voltage ......................................... >2001V
(MIL-STD-883, Method 3015)

Latch up Current ..................................................... >200 mA

## Operating Range

| Device | Range | Ambient Temperature | $V_{CC}$ [5] |
|---|---|---|---|
| CY62146ELL | Ind'l/Auto-A | −40°C to +85°C | 4.5V–5.5V |

## Electrical Characteristics

Over the Operating Range

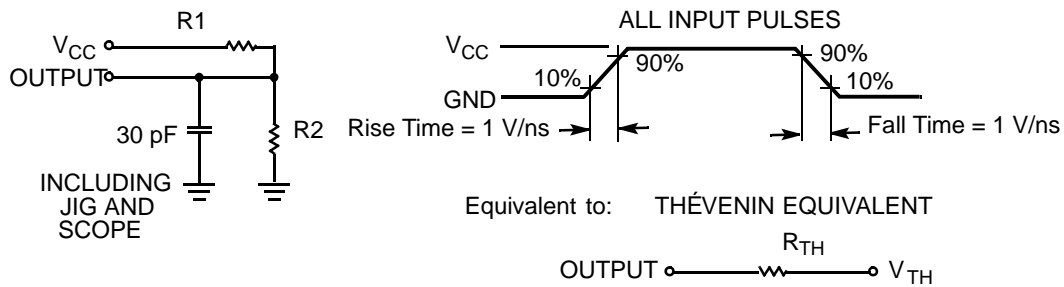| Parameter | Description | Test Conditions | | 45 ns (Ind'l/Auto-A) | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ [2] | Max | |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -1.0$ mA | | 2.4 | | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL} = 2.1$ mA | | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | $4.5 \leq V_{CC} \leq 5.5$ | | 2.2 | | $V_{CC} + 0.5$ | V |
| $V_{IL}$ | Input LOW Voltage | $4.5 \leq V_{CC} \leq 5.5$ | | −0.5 | | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | $GND \leq V_I \leq V_{CC}$ | | −1 | | +1 | µA |
| $I_{OZ}$ | Output Leakage Current | $GND \leq V_O \leq V_{CC}$, Output Disabled | | −1 | | +1 | µA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | $f = f_{max} = 1/t_{RC}$ | $V_{CC} = V_{CCmax}$ | | 15 | 20 | mA |
| | | $f = 1$ MHz | $I_{OUT} = 0$ mA, CMOS levels | | 2 | 2.5 | |
| $I_{SB2}$ [6] | Automatic CE Power down Current — CMOS Inputs | $\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0$, $V_{CC} = V_{CC(max)}$ | | | 1 | 7 | µA |

## Capacitance

Tested initially and after any design or process changes that may affect these parameters.

| Parameter | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A = 25°C$, $f = 1$ MHz, $V_{CC} = V_{CC(typ)}$ | 10 | pF |
| $C_{OUT}$ | Output Capacitance | | 10 | pF |

## Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

| Parameter | Description | Test Conditions | TSOP II | Unit |
|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 3 × 4.5 inch, two layer printed circuit board | 77 | °C/W |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case) | | 13 | °C/W |

**Notes**
3. $V_{IL}$(min) = −2.0V for pulse durations less than 20 ns for I < 30 mA.
4. $V_{IH}$(max) = $V_{CC}$ + 0.75V for pulse durations less than 20 ns.
5. Full Device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC}$ (min) and 200 µs wait time after $V_{CC}$ stabilization.
6. Only chip enable (CE) and byte enables (BHE and BLE) is tied to CMOS levels to meet the $I_{SB2}$ / $I_{CCDR}$ spec. Other inputs are left floating.

### Figure 2. AC Test Loads and Waveforms



| Parameters | 5.0V | Unit |
|---|---|---|
| R1 | 1800 | Ω |
| R2 | 990 | Ω |
| R$_{TH}$ | 639 | Ω |
| V$_{TH}$ | 1.77 | V |

## Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|---|
| V$_{DR}$ | V$_{CC}$ for Data Retention | | 2 | | | V |
| I$_{CCDR}$ [6] | Data Retention Current | V$_{CC}$ = 2V, $\overline{CE}$ ≥ V$_{CC}$ − 0.2V, V$_{IN}$ ≥ V$_{CC}$ − 0.2V or V$_{IN}$ ≤ 0.2V | | 1 | 7 | μA |
| t$_{CDR}$ [7] | Chip Deselect to Data Retention Time | | 0 | | | ns |
| t$_R$ [8] | Operation Recovery Time | | t$_{RC}$ | | | ns |

### Figure 3. Data Retention Waveform
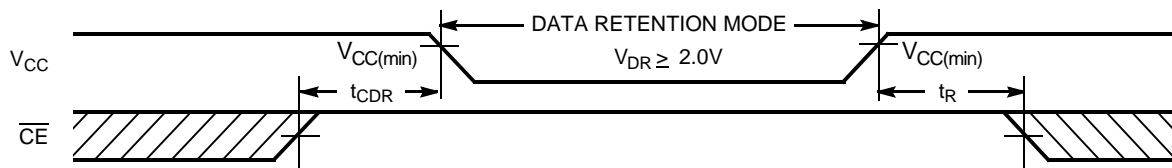


**Notes**
7. Tested initially and after any design or process changes that may affect these parameters.
8. Full device operation requires linear V$_{CC}$ ramp from V$_{DR}$ to V$_{CC(min)}$ ≥ 100 μs or stable at V$_{CC(min)}$ ≥ 100 μs.

[+] Feedback

## Switching Characteristics

Over the Operating Range [9, 10]

| Parameter | Description | 45 ns (Ind'l/Auto-A) | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| **Read Cycle** | | | | |
| $t_{RC}$ | Read Cycle Time | 45 | | ns |
| $t_{AA}$ | Address to Data Valid | | 45 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 10 | | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to Data Valid | | 45 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 22 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to LOW-Z[11] | 5 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High-Z[11, 12] | | 18 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to Low-Z[11] | 10 | | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to High-Z[11, 12] | | 18 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to Power Up | 0 | | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to Power Down | | 45 | ns |
| $t_{DBE}$ | $\overline{BLE}/\overline{BHE}$ LOW to Data Valid | | 22 | ns |
| $t_{LZBE}$ | $\overline{BLE}/\overline{BHE}$ LOW to Low-Z[11] | 5 | | ns |
| $t_{HZBE}$ | $\overline{BLE}/\overline{BHE}$ HIGH to HIGH-Z[11, 12] | | 18 | ns |
| **Write Cycle** [13] | | | | |
| $t_{WC}$ | Write Cycle Time | 45 | | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to Write End | 35 | | ns |
| $t_{AW}$ | Address Setup to Write End | 35 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | ns |
| $t_{SA}$ | Address Setup to Write Start | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 35 | | ns |
| $t_{BW}$ | $\overline{BLE}/\overline{BHE}$ LOW to Write End | 35 | | ns |
| $t_{SD}$ | Data Setup to Write End | 25 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High-Z[11, 12] | | 18 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low-Z[11] | 10 | | ns |

**Notes**
9. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of 1.5V, input pulse levels of 0 to 3V, and output loading of the specified $I_{OL}/I_{OH}$ as shown in AC Test Loads and Waveforms on page 4.
10. AC timing parameters are subject to byte enable signals ($\overline{BHE}$ or $\overline{BLE}$) not switching when chip is disabled. See application note AN13842 for further clarification.
11. At any temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZBE}$ is less than $t_{LZBE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any device.
12. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high-impedance state.
13. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$, $\overline{BLE}$ or both $= V_{IL}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

[+] Feedback

## Switching Waveforms

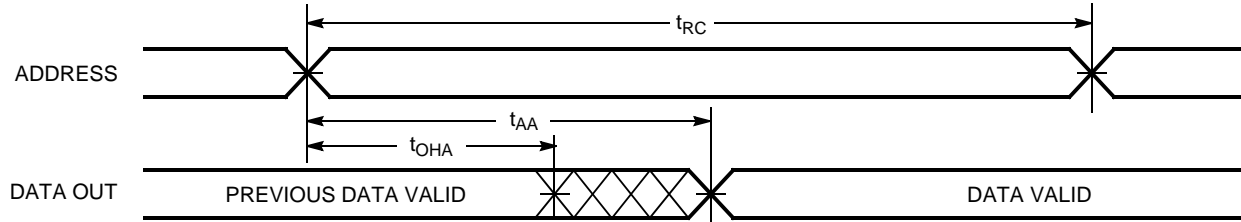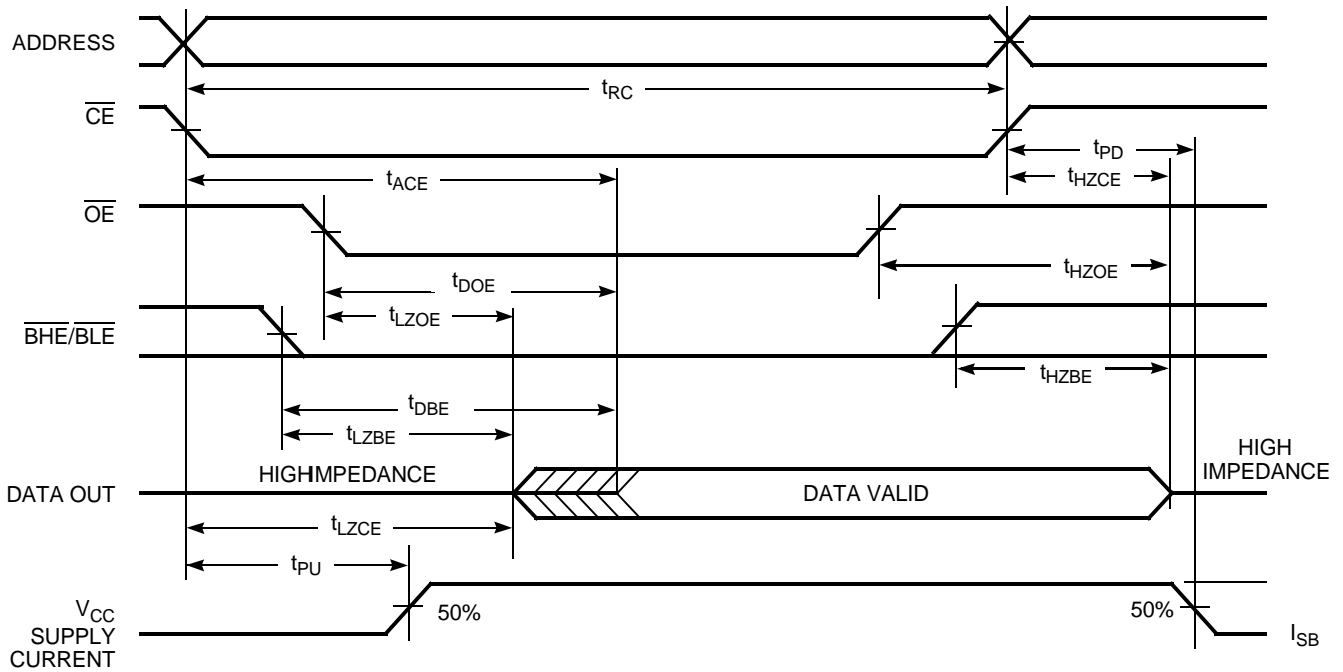**Figure 4.  Read Cycle No.1: Address Transition Controlled**. [14, 15]

ADDRESS

$t_{RC}$

$t_{AA}$

$t_{OHA}$

DATA OUT    PREVIOUS DATA VALID    DATA VALID

**Figure 5.  Read Cycle No. 2: $\overline{OE}$ Controlled** [15, 16]

ADDRESS

$\overline{CE}$

$t_{RC}$

$t_{PD}$

$t_{ACE}$

$t_{HZCE}$

$\overline{OE}$

$t_{DOE}$

$t_{HZOE}$

$t_{LZOE}$

$\overline{BHE}/\overline{BLE}$

$t_{HZBE}$

$t_{DBE}$

$t_{LZBE}$

HIGH IMPEDANCE

DATA OUT    HIGH IMPEDANCE    DATA VALID

$t_{LZCE}$

$t_{PU}$

$V_{CC}$ SUPPLY CURRENT    50%    50%    $I_{SB}$

**Notes**
14. <u>The</u> device is continuously selected. $\overline{OE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$, $\overline{BLE}$, or both = $V_{IL}$.
15. $\overline{WE}$ is HIGH for read cycle.
16. Address valid before or similar to $\overline{CE}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW.

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## Switching Waveforms (continued)

**Figure 6. Write Cycle No 1: $\overline{WE}$ Controlled** [13, 17, 18]
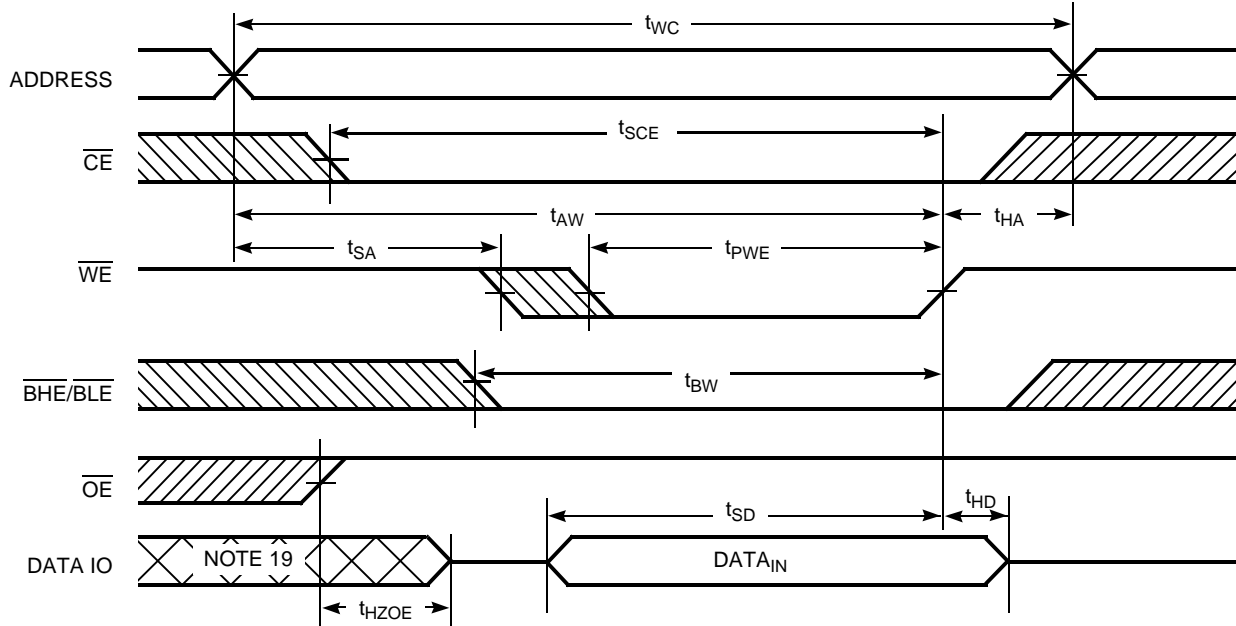


**Figure 7. Write Cycle 2: $\overline{CE}$ Controlled** [13, 17, 18]
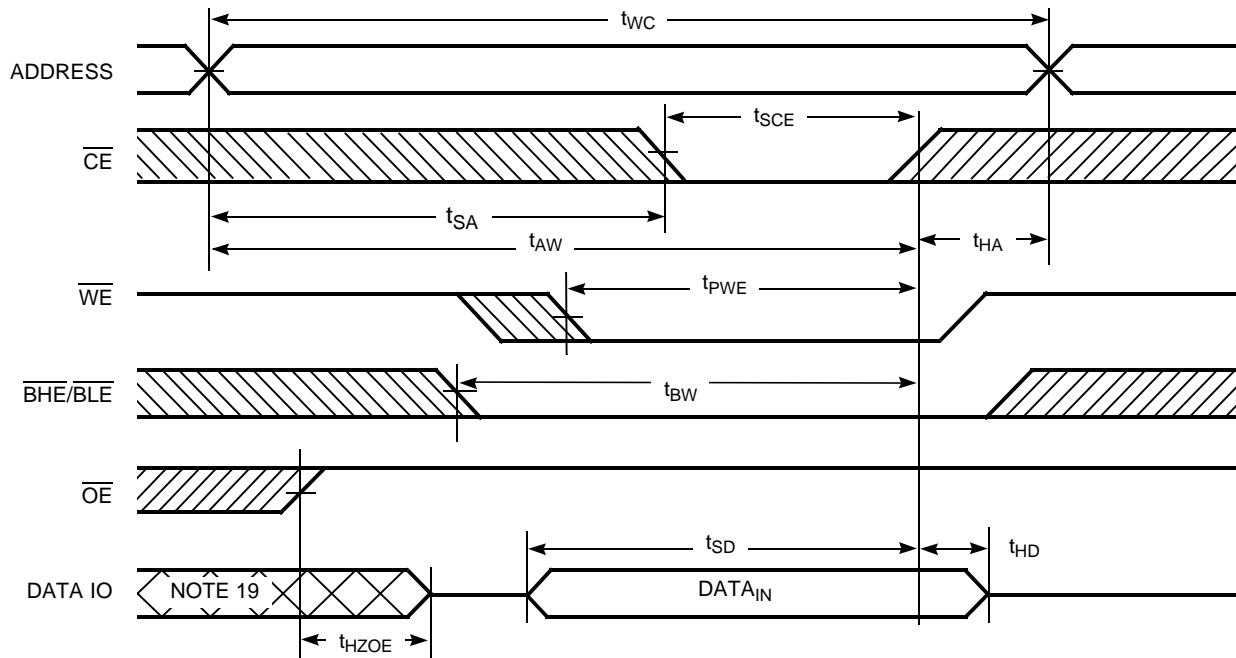


**Notes**
17. Data IO is high impedance if $\overline{OE} = V_{IH}$.
18. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
19. During this period, the IOs are in output state. Do not apply input signals.

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## Switching Waveforms (continued)

**Figure 8. Write Cycle 3: WE controlled, OE LOW** [18]
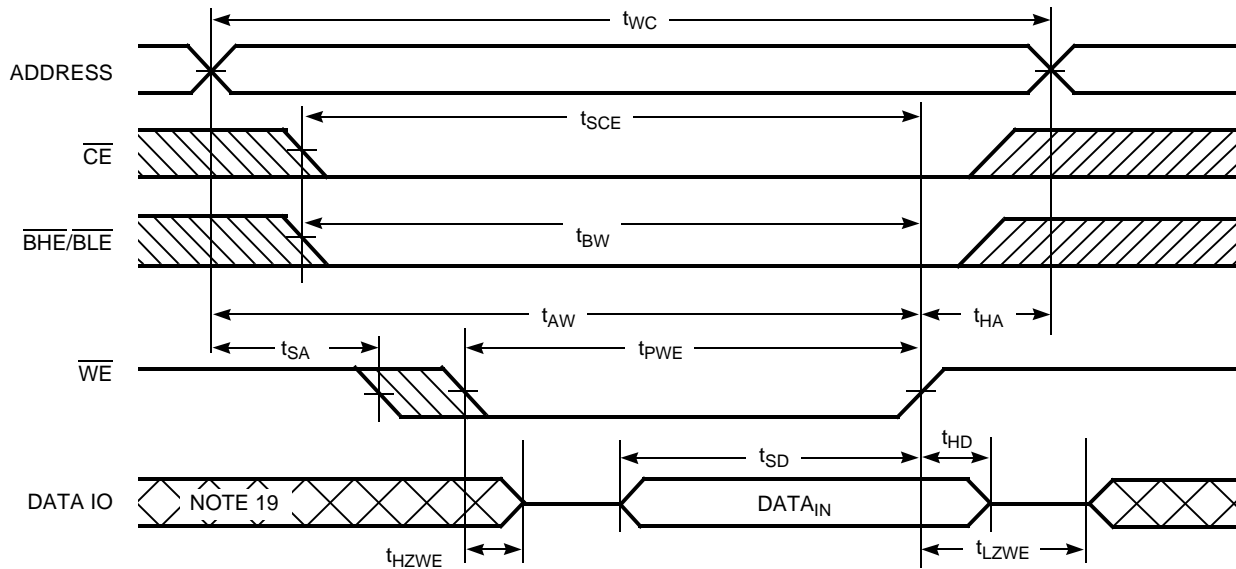


**Figure 9. Write Cycle 4: BHE/BLE Controlled, OE LOW** [18]

[+] Feedback
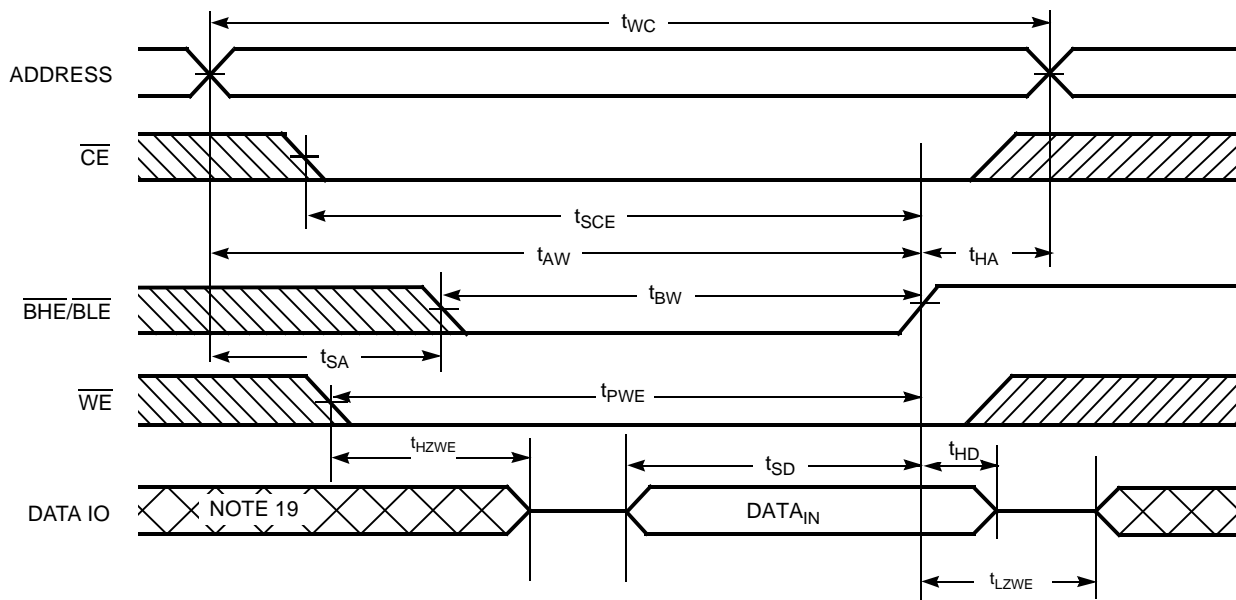
**Table 1. Truth Table**

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|---|---|---|
| H | X | X | X | X | High-Z | Deselect/Power down | Standby ($I_{SB}$) |
| L | X | X | H | H | High-Z | Output Disabled | Active ($I_{CC}$) |
| L | H | L | L | L | Data Out ($IO_0$–$IO_{15}$) | Read | Active ($I_{CC}$) |
| L | H | L | H | L | Data Out ($IO_0$–$IO_7$); $IO_8$–$IO_{15}$ in High-Z | Read | Active ($I_{CC}$) |
| L | H | L | L | H | Data Out ($IO_8$–$IO_{15}$); $IO_0$–$IO_7$ in High-Z | Read | Active ($I_{CC}$) |
| L | H | H | L | L | High-Z | Output Disabled | Active ($I_{CC}$) |
| L | H | H | H | L | High-Z | Output Disabled | Active ($I_{CC}$) |
| L | H | H | L | H | High-Z | Output Disabled | Active ($I_{CC}$) |
| L | L | X | L | L | Data In ($IO_0$–$IO_{15}$) | Write | Active ($I_{CC}$) |
| L | L | X | H | L | Data In ($IO_0$–$IO_7$); $IO_8$–$IO_{15}$ in High-Z | Write | Active ($I_{CC}$) |
| L | L | X | L | H | Data In ($IO_8$–$IO_{15}$); $IO_0$–$IO_7$ in High-Z | Write | Active ($I_{CC}$) |

## Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 45 | CY62146ELL-45ZSXI | 51-85087 | 44-pin Thin Small Outline Package II (Pb-free) | Industrial |
| | CY62146ELL-45ZSXA | 51-85087 | 44-pin Thin Small Outline Package II (Pb-free) | Automotive-A |

Contact your local Cypress sales representative for availability of these parts.

[+] Feedback

## Package Diagrams

**Figure 10. 44-Pin TSOP II, 51-85087**



51-85087-*A

[+] Feedback
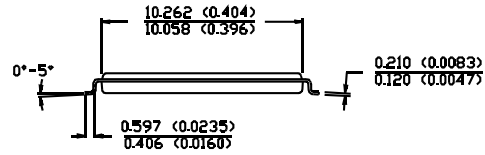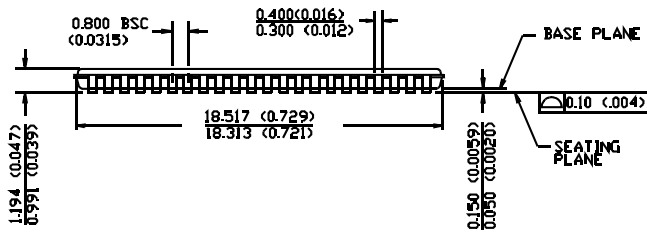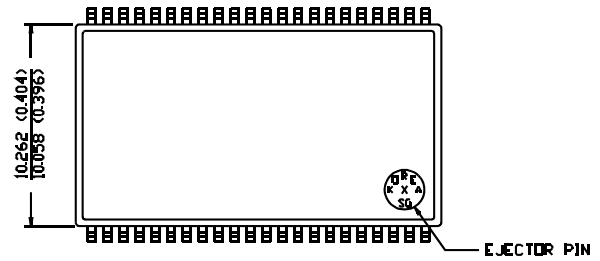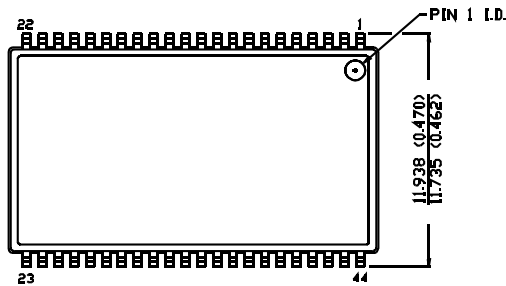
## Document History Page

| Document Title: CY62146E MoBL® 4-Mbit (256K x 16) Static RAM<br>Document Number: 001-07970 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 463213 | See ECN | NXR | New Data Sheet |
| *A | 684343 | See ECN | VKN | Added Preliminary Automotive-A Information<br>Updated Ordering Information Table |
| *B | 925501 | See ECN | VKN | Added footnote #8 related to $I_{SB2}$ and $I_{CCDR}$<br>Added footnote #13 related AC timing parameters |
| *C | 1045260 | See ECN | VKN | Converted Automotive-A specs from preliminary to final |
| *D | 2073548 | See ECN | VKN/AESA | Corrected typo in the Data Retention Waveform and removed its irrelevant footnote |

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