CYS25G0101DX-ATC Evaluation Board User's Guide

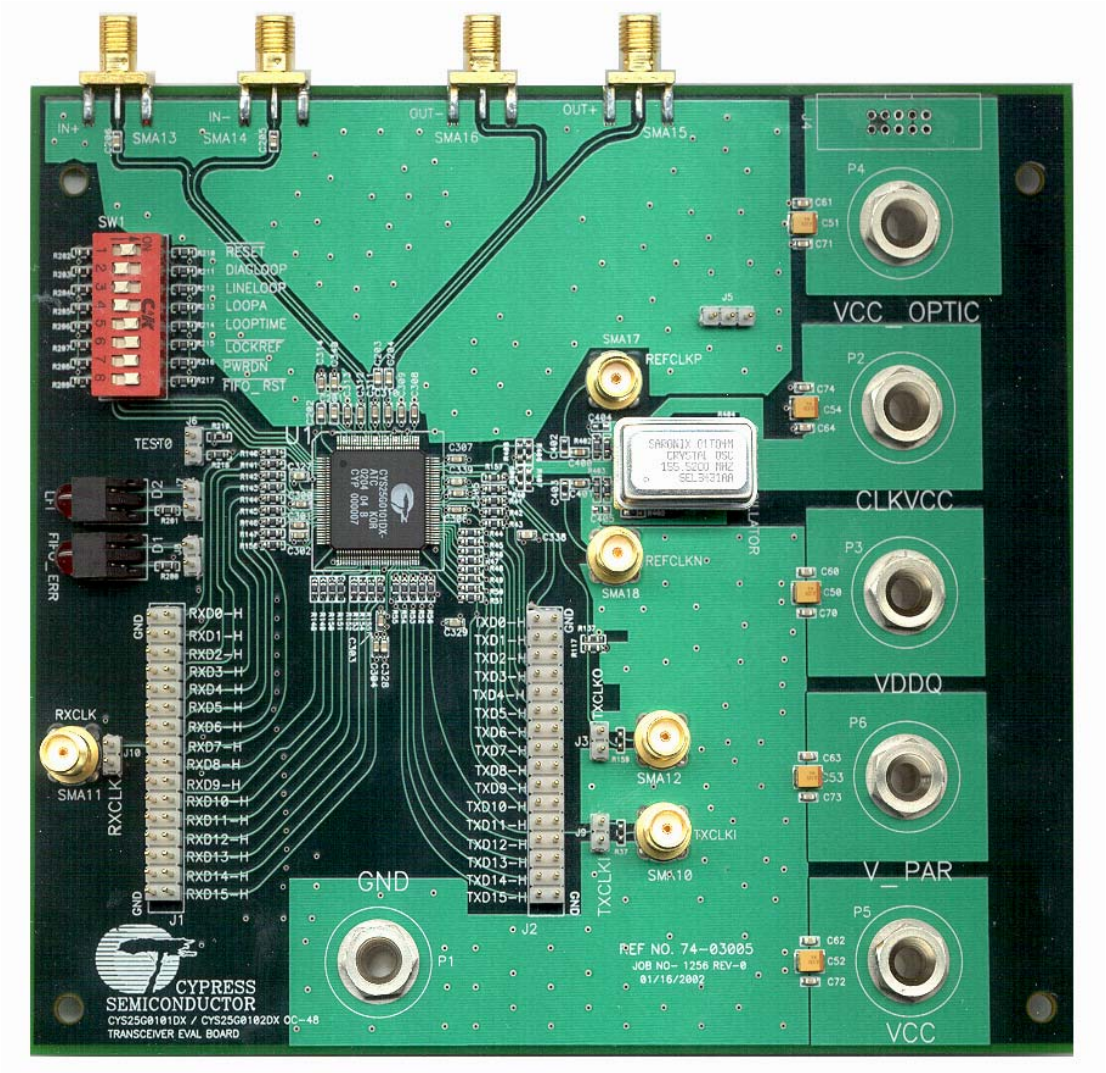

Table of Contents

List of Figures

List of Figures (continued)

List of Tables

1. Introduction

Cypress's CYS25G0101DX SONET OC-48 Transceiver is a communications building block for high-speed SONET data communications. It provides complete parallel-to-serial and serial-to-parallel conversions, clock generation, and clock and data recovery operations in a single chip, optimized for full SONET/SDH compliance. The CYS25G0101DX Evaluation Board is designed for evaluating as well as understanding the characteristics of the CYS25G0101DX SONET/SDH Transceiver. The CYS25G0101DX SONET/SDH Transceiver Evaluation Board provides the following advantages.

2. Features

- Flexible and easy to operate
- On-board Cypress 120-pin TQFP CYS25G0101DX SONET/SDH Transceiver
- Supports LVPECL and HSTL interfaces
- Dip switch for selecting different diagnostic modes
- Four diagnostic modes – Diagnostic Loopback mode, Line Loopback mode, Analog Line Loopback mode, and factory TEST0 (Parallel Line Loopback) mode
- LFI and FIFO_ERR LEDs
- Onboard oscillator for the REFCLK
- Supports external clock source for the REFCLK
- 16-bit RxD, 16-bit TxD bus, RXCLK, TXCLKI, TXCLKO interface
- SMA connectors for CML input and output buffers
- Separate Banana Jacks for all voltage sources for measuring current individually

3. Kit Contents

- CYS25G0101DX Evaluation Board
- Certificate of Compliance
- CYS25G0101DX Evaluation Kit CD
  - — Users Guide
  - — Application Notes
  - — Data Sheet

4. Functional Description

This board can be used to test the CYS25G0101DX in various modes, such as TEST0 (parallel line loopback mode), LINELOOP, LOOPA and LOOPTIME. The REFCLK of the CYS25G0101DX is connected to the onboard 155.52-MHz oscillator. The on-board REFCLK can be replaced by connecting the external reference clock source to J17 and J18. To use the external reference clock source, the C400 and C401 (0.01-μF cap) have to be removed and placed on C402 and C403 positions. Also, the P2, CLKVCC, has to be disconnected from the power supply (or power down). The CYS25G0101DX Evaluation Board provides an optional optical module interface for connecting to an optical module daughter card.

The block diagram of the CYS25G0101DX is shown in *Figure 1*. The detailed functional description can be found in the CYS25G0101DX data sheet. *Figure 2* shows the picture of the CYS25G0101DX Evaluation Board and the location of the jumpers. *Table 1* is the description of all jumpers and connectors. The bus connectors, J1 and J2, are used to connect to the 16-bit RxD and TxD buses for transferring and receiving the parallel data. *Table 2* and *Table 3* are the pin definitions of J1 and J2. A multi-function eight-position Dip switch provides the selection of the different diagnostic modes as well as the control functions. *Table 4* is the functional description of the Dip switch SW1. The TEST0 jumper, J6, when closed, is used to enable the factory TEST0 (Parallel Line Loop Back) mode. In the "Parallel Line Loop Back" mode, parallel output buffers are internally jumped to the parallel input buffers. There is no need to use external jumpers for the headers. J13, J14, J15, J16 and J4 are Differential CML input and output and power supply for the optional optical module daughter card. *Table 5* idescribes the optical module interface and *Table 6* idescribes the LED. *Figure 3* shows the jumper orientations of the CYS25G0101DX Evaluation Board.

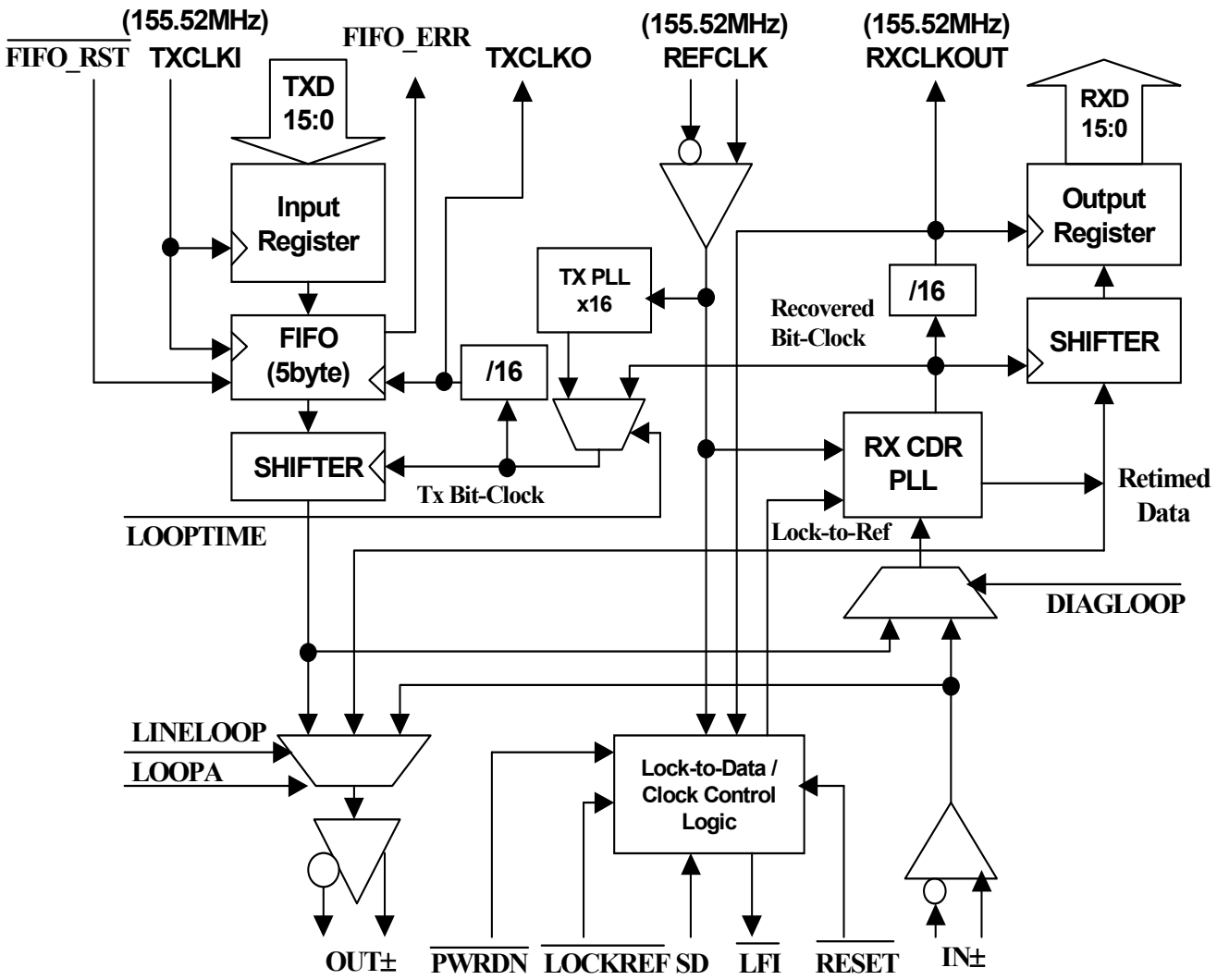

Figure 1. The Block Diagram of the CYS25G0101DX

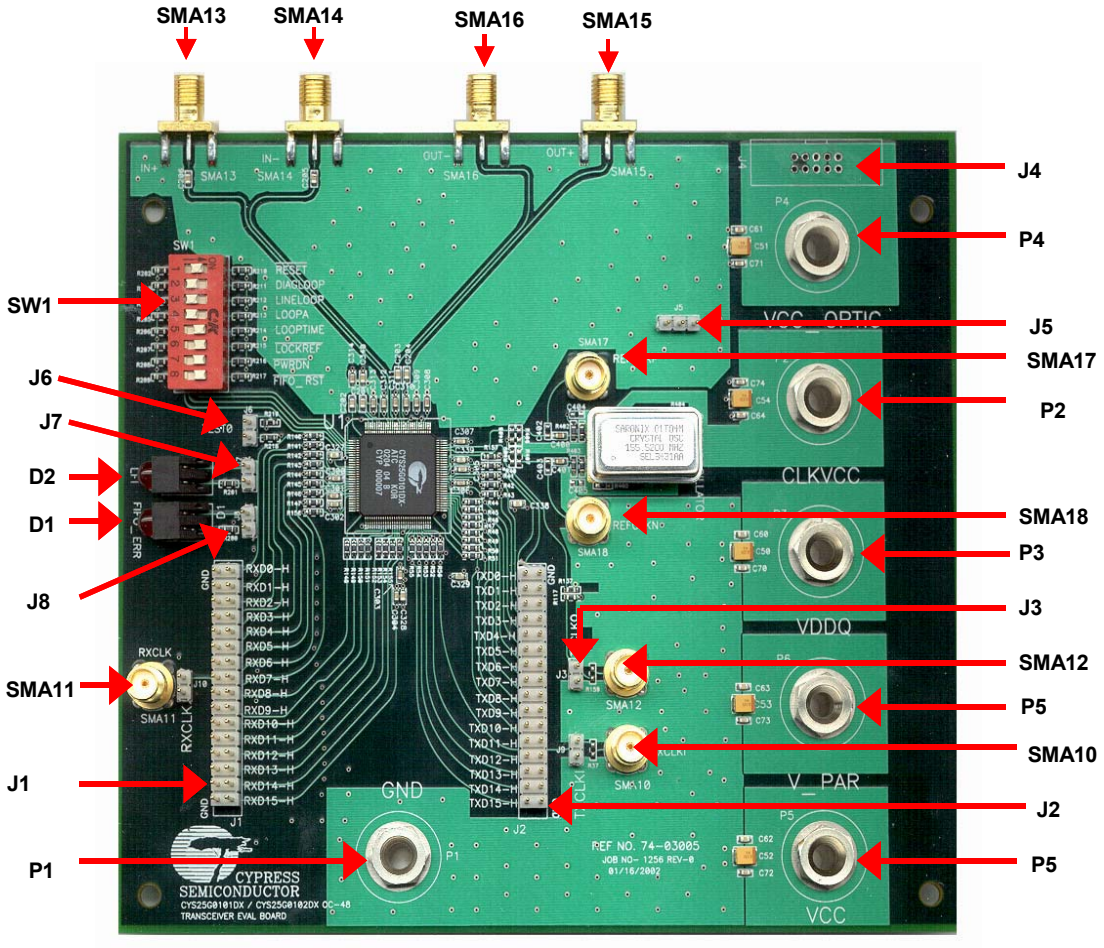

Figure 2. The CYS25G0101DX Evaluation Board

Table 1. Functional Description of the Connectors

Jumpers and Connectors	Name	Description
J1	RxD BUS	16-bit RxD Data Bus interface header (see *Table 2* for details). *Figure 3* shows the orientation of this header
J2	TxD BUS	16-bit TxD Data Bus interface header (see *Table 3* for details). *Figure 3* shows the orientation of this header
J3	TxCLKO_H	Header for CYS25G0101DX's TXCLKO (pin 79) and GND. *Figure 3* shows the orientation of this jumper
J4	OPTIC POWER	Power supply for external optical module (see *Table 5* for details)

Table 1. Functional Description of the Connectors (continued)

Jumpers and Connectors	Name	Description
J5	SD	This jumper is used to set the SD signal. When open (default), SD signal will be driven by the optical module. When 1-2 are shorted, SD is forced to HIGH. When 2-3 are shorted, SD is forced to LOW. *Figure 3* shows the orientation of this jumper
J6	TEST0	This jumper, when shorted, is to enable the Parallel Line Loopback mode.
J7	LFI	Test Tap for CYS25G0101DX's LFI (pin 1). *Figure 3* shows the orientation of this jumper
J8	FIFO_ERR	Test Tap for CYS25G0101DX's LIFO (pin 51). *Figure 3* shows the orientation of this jumper
SMA10	TXCLKI	Optional SMA connector for CYS25G0101DX's TXCLKI (pin 57). **R37 need to be populated, if this connector is used**
SMA11	RXCLK	Optional SMA connector for CYS25G0101DX's RXCLK (pin 24). **C118, R118, R138 and R158 need to be populated and C116, R116, and R136 need to be unpopulated, if this connector is used**
SMA12	TXCLKO	Optional SMA connector for CYS25G0101DX's TXCLKO (pin 79). **C119, R119, R139 and R159 need to be populated and C117, R117, and R137 need to be unpopulated, if this connector is used**
SMA13	IN+	SMA connector for CYS25G0101DX's IN+ (pin 109). This connector is also for the optional optical module interface
SMA14	IN-	SMA connector for CYS25G0101DX's IN– (pin 108). This connector is also for the optional optical module interface
SMA15	OUT-	SMA connector for CYS25G0101DX's OUT– (pin 104). This connector is also for the optional optical module interface
SMA16	OUT+	SMA connector for CYS25G0101DX's OUT+ (pin 103). This connector is also for the optional optical module interface
SMA17	REFCLKP	Optional SMA connector for CYS25G0101DX's REFCLK+ (pin 87). This connector is for using the external reference clock instead of using the "on-board" oscillator (155.52 MHz). **To use the external reference clock, C400 and C401 (0.01-μF cap) have to be removed and placed on C402 and C403 positions. Also, The CLKVCC, P2, has to be disconnected from the power supply**
SMA18	REFCLKN	Optional SMA connector for CYS25G0101DX's REFCLK+ (pin 87). This connector is for using the external reference clock instead of using the "on-board" oscillator (155.52 MHz). **To use the external reference clock, C400 and C401 (0.01-μF cap) have to be removed and placed on C402 and C403 positions. Also, The CLKVCC, P2, has to be disconnected from the power supply**
P1	GND	Power Ground. For external power supply
P2	CLKVCC	Power supply - +3.3V for the clock oscillator
P3	VDDQ	Power supply - +3.3V for LVPECL output. +1.5V for HSTL outputs
P4	VCC_OPTIC	Power supply - +3.3V for the optional optical module
P5	VCC	Power supply - +3.3V for digital and low-speed I/O function
P6	V_Par	Power supply - +3.3V for LVPECL output. +1.5V for HSTL outputs

Table 2. Pin Assignment of J1 Header and Description of J10 Header

Pin Number	Name	I/O Characteristics	Description
1	RXD15	HSTL output	Parallel receive data output RXD15. The outputs change following RXCLK↓
3	RXD14	HSTL output	Parallel receive data output RXD14. The outputs change following RXCLK↓

Table 2. Pin Assignment of J1 Header and Description of J10 Header (continued)

Pin Number	Name	I/O Characteristics	Description
5	RXD13	HSTL output	Parallel receive data output RXD13. The outputs change following RXCLK↓
7	RXD12	HSTL output	Parallel receive data output RXD12. The outputs change following RXCLK↓
9	RXD11	HSTL output	Parallel receive data output RXD11. The outputs change following RXCLK↓
11	RXD10	HSTL output	Parallel receive data output RXD10. The outputs change following RXCLK↓
13	RXD9	HSTL output	Parallel receive data output RXD9. The outputs change following RX-CLK↓
15	RXD8	HSTL output	Parallel receive data output RXD8. The outputs change following RX-CLK↓
17	RXD7	HSTL output	Parallel receive data output RXD7. The outputs change following RX-CLK↓
19	RXD6	HSTL output	Parallel receive data output RXD6. The outputs change following RX-CLK↓
21	RXD5	HSTL output	Parallel receive data output RXD5. The outputs change following RX-CLK↓
23	RXD4	HSTL output	Parallel receive data output RXD4. The outputs change following RX-CLK↓
25	RXD3	HSTL output	Parallel receive data output RXD3. The outputs change following RX-CLK↓
27	RXD2	HSTL output	Parallel receive data output RXD2. The outputs change following RX-CLK↓
29	RXD1	HSTL output	Parallel receive data output RXD1. The outputs change following RX-CLK↓
31	RXD0	HSTL output	Parallel receive data output RXD0. The outputs change following RX-CLK↓
2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32	GND	Ground	Ground
J10	RXCLK	HSTL output	Receive clock output. This clock is divided by 16 of the bit-rate clock extracted from the received serial stream

Table 3. Pin Assignment of J2 Header and Description of J9 Header

Pin Number	Name	I/O Characteristics	Description
1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31	GND	Ground	Ground
2	TXD15	HSTL output	Parallel transmit data input TXD15. The input data is sampled by TX-CLKI↑
4	TXD14	HSTL input	Parallel transmit data input TXD14. The input data is sampled by TX-CLKI↑
6	TXD13	HSTL input	Parallel transmit data input TXD13. The input data is sampled by TX-CLKI↑

Table 3. Pin Assignment of J2 Header and Description of J9 Header (continued)

Pin Number	Name	I/O Characteristics	Description
8	TXD12	HSTL input	Parallel transmit data input TXD12. The input data is sampled by TXCLKI↑
10	TXD11	HSTL input	Parallel transmit data input TXD10. The input data is sampled by TXCLKI↑
12	TXD10	HSTL input	Parallel transmit data input TXD9. The input data is sampled by TXCLKI↑
14	TXD9	HSTL input	Parallel transmit data input TXD8. The input data is sampled by TXCLKI↑
16	TXD8	HSTL input	Parallel transmit data input TXD8. The input data is sampled by TXCLKI↑
18	TXD7	HSTL input	Parallel transmit data input TXD7. The input data is sampled by TXCLKI↑
20	TXD6	HSTL input	Parallel transmit data input TXD6. The input data is sampled by TXCLKI↑
22	TXD5	HSTL input	Parallel transmit data 'input TXD5. The input data is sampled by TXCLKI↑
24	TXD4	HSTL input	Parallel transmit data input TXD4. The input data is sampled by TXCLKI↑
26	TXD3	HSTL input	Parallel transmit data input TXD3. The input data is sampled by TXCLKI↑
28	TXD2	HSTL input	Parallel transmit data input TXD2. The input data is sampled by TXCLKI↑
30	TXD1	HSTL input	Parallel transmit data input TXD1. The input data is sampled by TXCLKI↑
32	TXD0	HSTL input	Parallel transmit data input TXD0. The input data is sampled by TXCLKI↑
J9	TXCLKI	HSTL input	Parallel transmit data input clock

Table 4. Functional Description of DIP Switch 1 (SW1)

Position	Name	State		Description
1	RESET	ON*		Disable Reset - Normal operation
		OFF		Reset for all logic functions except the transmit FIFO
2	DIAGLOOP	ON		Transmit data (from TXD[15:0]) is routed through the receive clock and data recovery and presented at RXD[15:0] output
		OFF*		Received serial data (from IN±) is routed through the receive clock and data recovery and presented at RXD[15:0] output
3, 4	LINELOOP, LOOPA	ON	ON	Invalid setting
		ON	OFF	Received serial data is looped back from receive input (IN±) to transmit output (OUT±) **after being reclocked by the recovered clock**
		OFF	ON	Received serial data is looped back from receive input (IN±) to transmit output (OUT±), **but is not routed through the clock and data recovery PLL**
		OFF*	OFF*	Disable serial data loop back.

Table 4. Functional Description of DIP Switch 1 (SW1) (continued)

Position	Name	State	Description
5	LOOPTIME	ON	The transmission will be using the extracted receive bit-clock for the transmitted bit clock
		OFF*	The transmission will be using the REFCLK input (155.52 MHz), which is multiplied by 16, to generate the transmitted bit clock
6	LOCKREF	ON*	The receive PLL locks to serial data stream
		OFF	The receive PLL locks to the REFCLK
7	PWRDN	ON*	Disable Power Down - Normal Operation
		OFF	Enable Device Power Down mode. All the logic and drivers are disabled and placed into a standby condition where only minimal power is dissipated
8	FIFO_RST	ON*	Disable FIFO reset - Normal Operation
		OFF	Reset the transmit FIFO pointers. The in and out pointers of the transmit FIFO are reset to the maximum separation

Table 5. Functional Description of J4 Connector

Pin	Name	Description
1A, 1B, 3A, 3B	VCC_OPTIC	Power supply for optical module
2A, 2B, 4A, 4B	GND	Power ground
5A	NC	No Connection
5B	SD	SD signal from optical module

Table 6. Description of LED Indicators

LED	Name	LED Status	Description
D1	FIFO_ERR	ON	The transmit FIFO has either under or overflowed. The FIFO must be reset to clear the error (by switching the DIP switch SW1-8 to OFF and then ON. See *Table 4* for details)
		OFF	Indicates the FIFO has neither under or overflowed
D2	LFI	ON	Indicates no Line Fault. It will appear to be ON even when LFI is toggling. In such a case observe LFI using a scope on J7
		OFF	Indicates the selected receive data stream has been detected an invalid either LOW input on SD or by the receive VCO being operated outside its specified limits

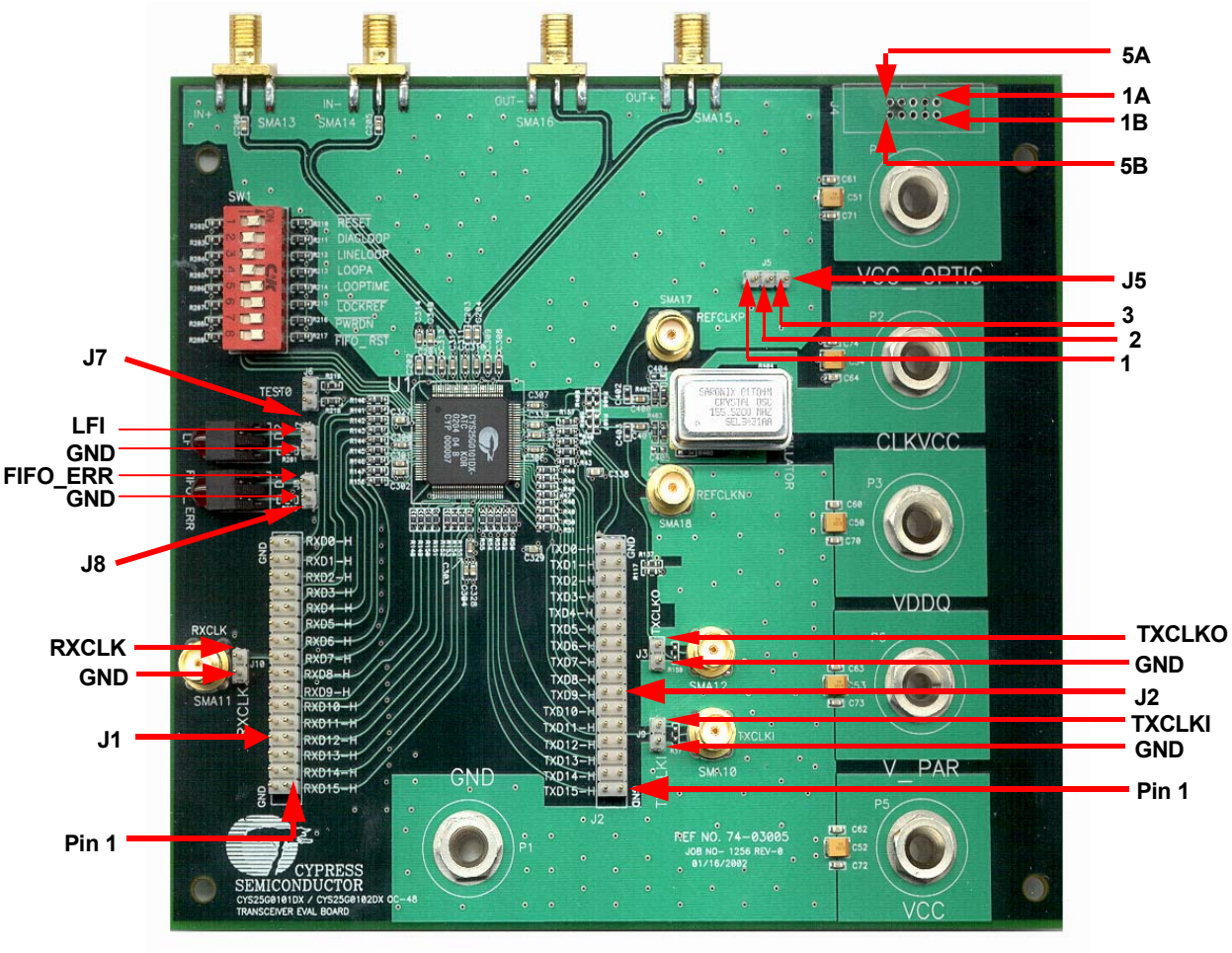

Figure 3. The Jumper Orientations of the CYS25G0101DX

5. Diagnostic Modes

The CYS25G0101DX Evaluation Board provides four different diagnostic modes—Diagnostic Loopback mode, Line Loopback mode, Analog Loopback mode and "Parallel Line Loopback" mode. *Figure 4* to *Figure 7* illustrate these diagnostic modes and *Figure 8* to *Figure 10* illustrate the testing equipment set-up for testing the characteristics of the CYS25G0101DX.

5.1 Diagnostic Loopback Mode

In the Diagnostic Loopback mode, parallel data will loop through the input buffer, serializer, CDR block, deserializer and the output buffer. *Figure 4* shows the data path (bold line) of the Diagnostic Loopback mode. To select the Diagnostic Loopback mode:

1. SW1-2 (DIAGLOOP) must be in ON position, SW1-3 (LINELOOP)
2. All other dip switches must be in their default positions as stated in *Table 4*
3. TEST0, jumper J6 must be opened
4. Apply the Testing Hookup illustrated in *Figure 8* to *Figure 10*

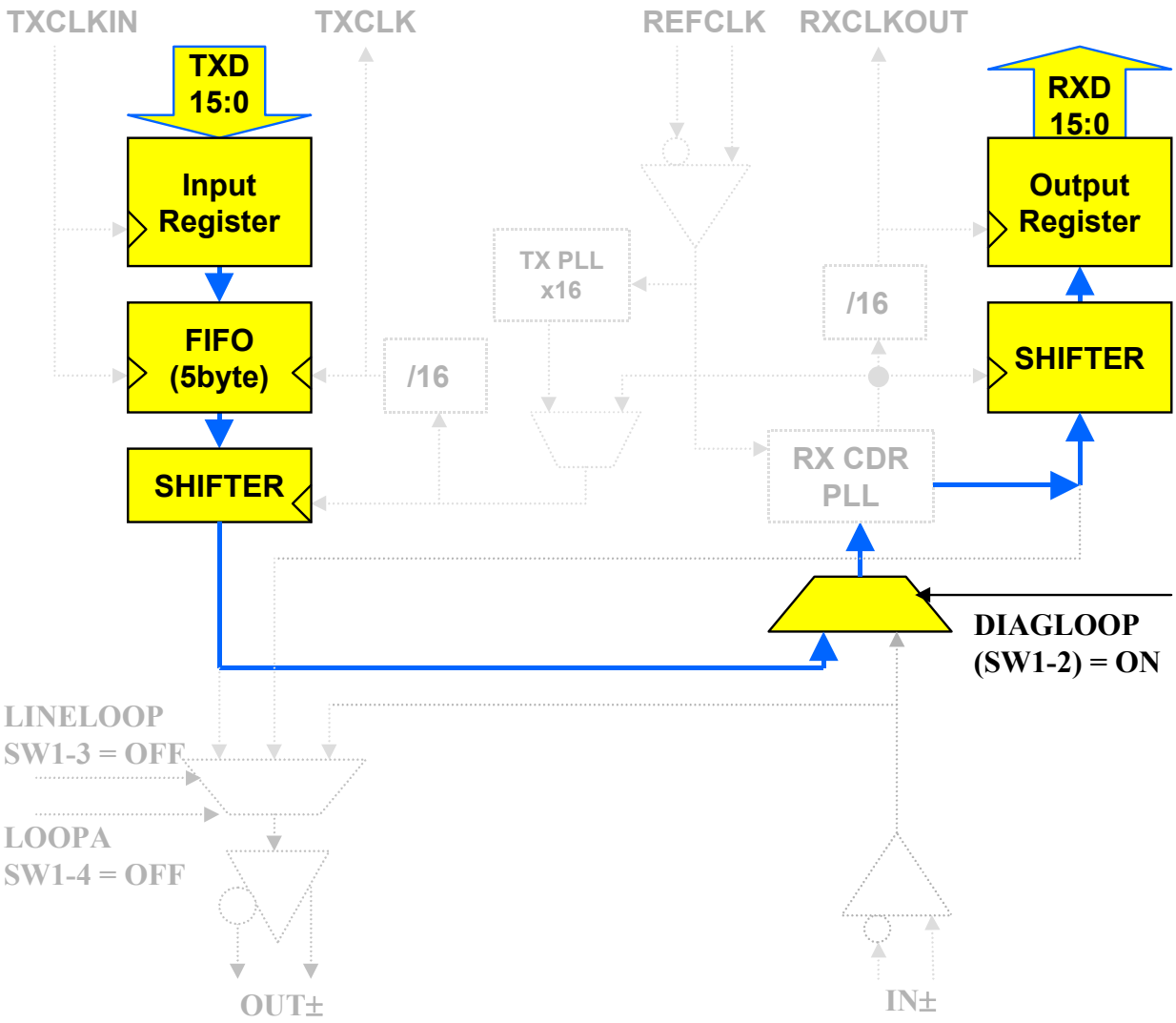

Figure 4. Diagnostic Loopback Mode Data Path

5.2 Line Loopback

In the Line Loopback mode, serial data (from IN±) will loop through the serial input buffer and CDR block to the serial output buffer (OUT±). *Figure 5* shows the data path (bold line) of the Line Loopback mode. To select the Line Loopback mode:

1. SW1-3 (LINELOOP) must be in ON position
2. All other dip switch settings must be in their default positions as stated in *Table 4*
3. TEST0, jumper J6 must be opened
4. Apply the Testing Hookup illustrated in *Figure 8* to *Figure 10*

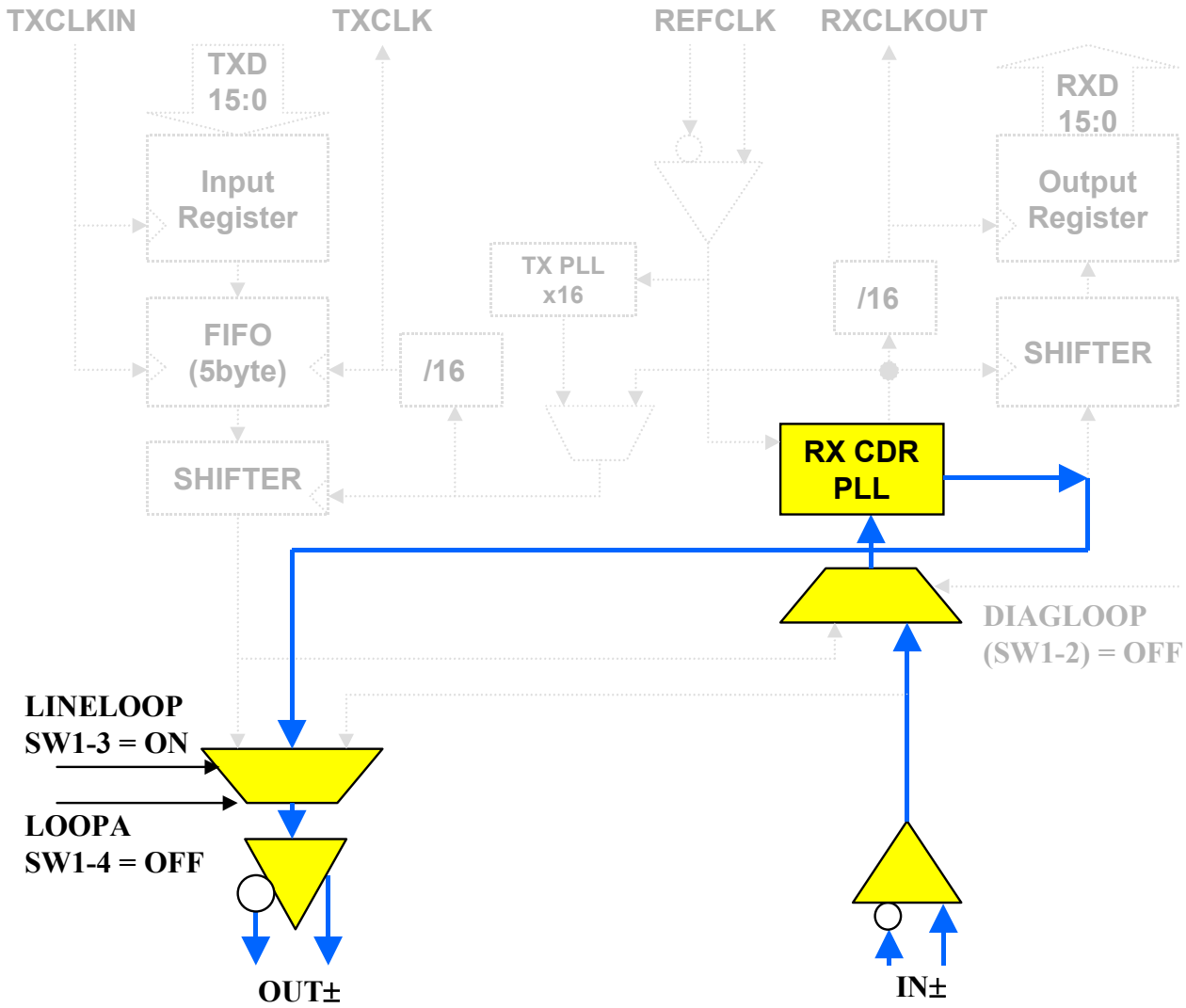

Figure 5. Line Loopback Mode Data Path

5.3 Analog Line Loopback

In the Analog Line Loopback mode, serial data (from IN±) will loop through directly from serial input buffer to the serial output buffer (OUT±). *Figure 6* shows the data path (bold line) of the Analog Line Loopback mode. To select the Analog Line Loopback mode:

1. SW1-4 (LOOPA) must be in ON position and SW1-3 (LINELOOP) must be in OFF position.
2. All other dip switches must be in their default positions as stated in *Table 4*
3. TEST0, jumper J6 must be opened
4. Apply the Testing Hookup illustrated in *Figure 8* to *Figure 10*

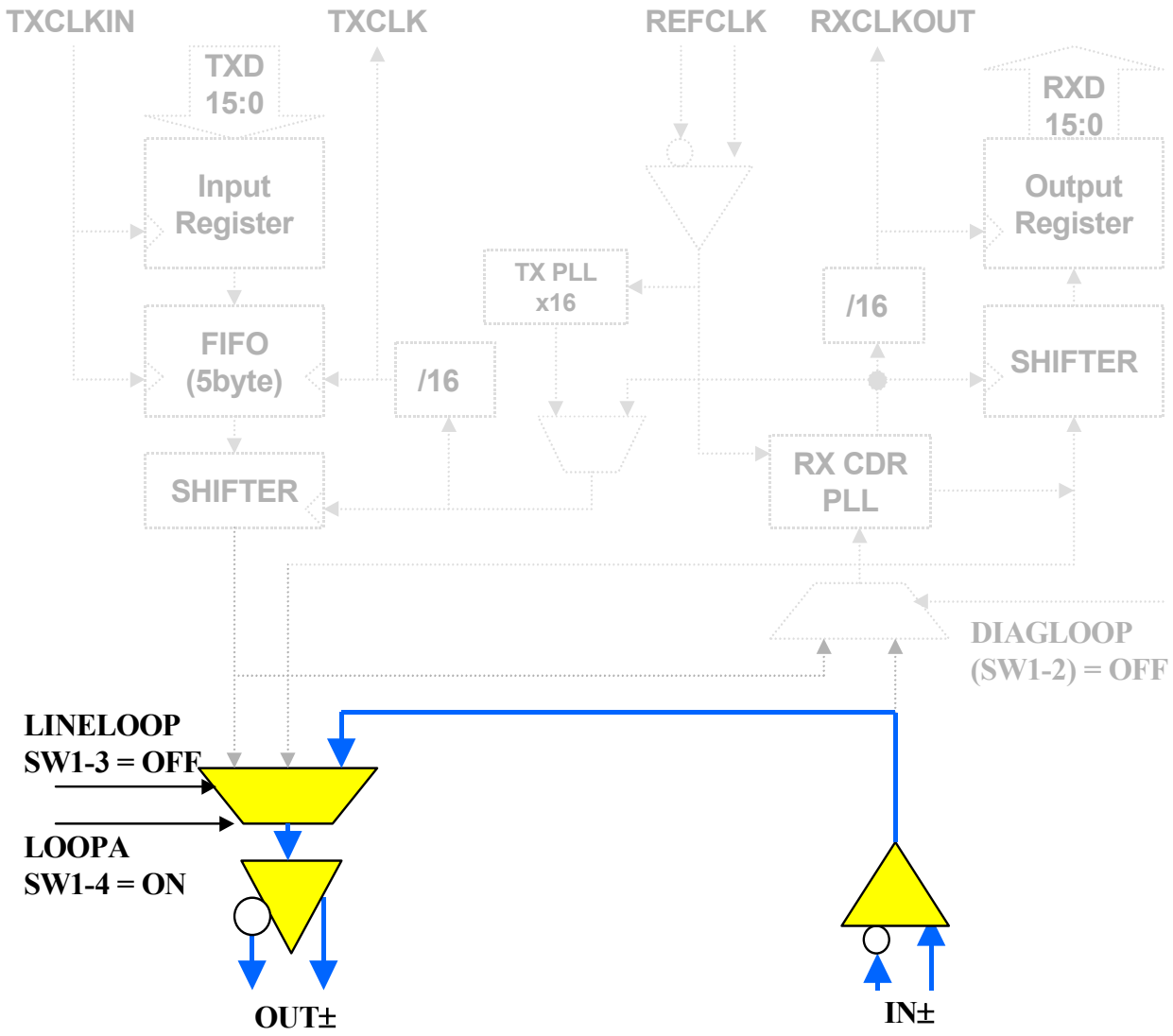

Figure 6. Analog Line Loopback Mode Data Path

5.4 "Parallel Line Loopback" (TEST0) Mode

In Parallel Line Loopback mode, the parallel output buffers are internally linked to the parallel input buffers. *Figure 7* shows the data path (bold line) of the Parallel Line Loopback mode. In this test mode, the internal RX CDR PLL and TX PLL can be tested by different configurations.

5.4.1 Test the Internal RX CDR PLL Only

1. TEST0, jumper J6 must be shorted
2. SW1-5 (LOOPTIME) must be in ON position
3. All other dip switches must be in their default positions (see *Table 4*)
4. Apply the Testing Hookup illustrated in *Figure 8* to *Figure 10* for the measurement

5.4.2 Test the Internal RX CDR PLL and TX PLL

1. TEST0, jumper J6 must be shorted
2. All dip switches must be in their default positions (see *Table 4*)
3. Disconnect CLKVCC (P2), remove the 155.52-MHz oscillator, place C400 on C402 and C401 on C403 positions (see *Table 1*, jumpers J17 and J18 for details)
4. Apply the Testing Hookup illustrated in *Figure 11* for the measurement

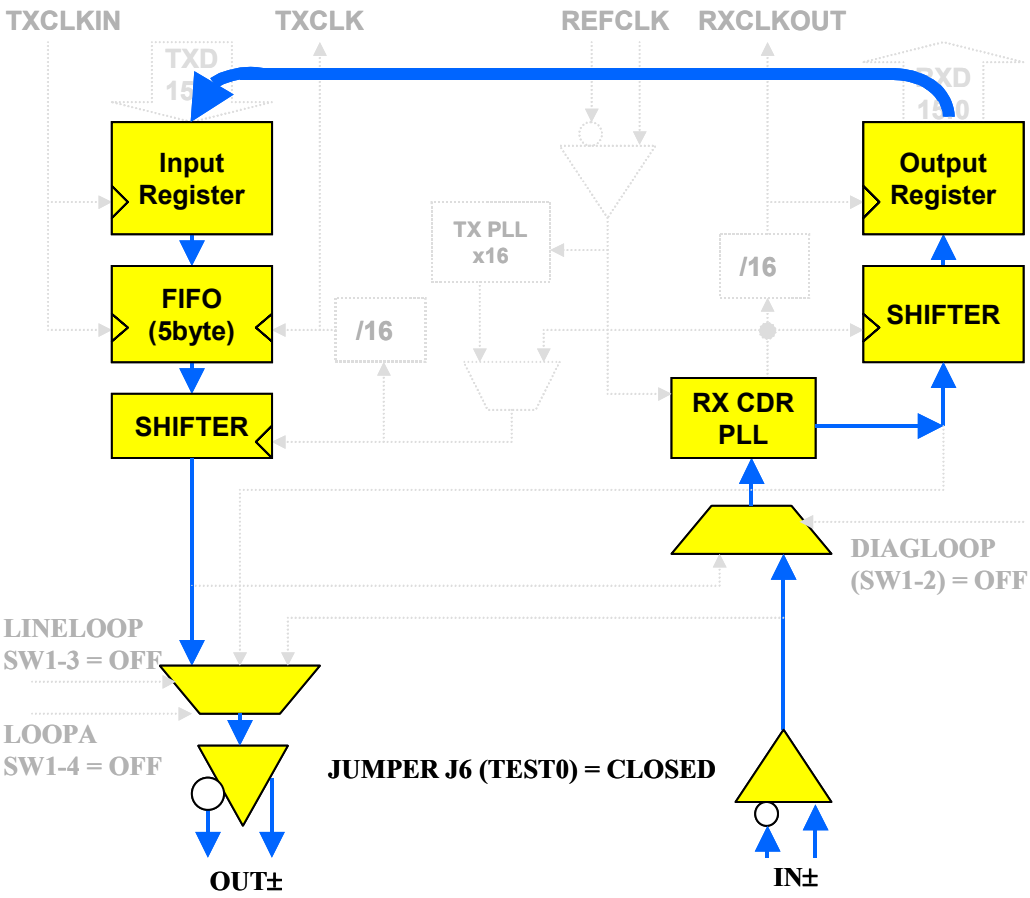

Figure 7. Parallel Loopback (TEST0) Mode Data Path

6. Testing Hookup

6.1 Set-up for BERT Test

Figure 8 illustrates the set-up for the BERT test. The equipment list:

1. Evaluation Board – Cypress CYS25G0101DX Evaluation Board
2. Pattern Generator – Tektronix D3186 Pattern Generator
3. Error Detector – Tektronix D3286 Error Detector
4. Power Supply – HP E3631A DC Power Supply

* All equipment in the list is for reference only

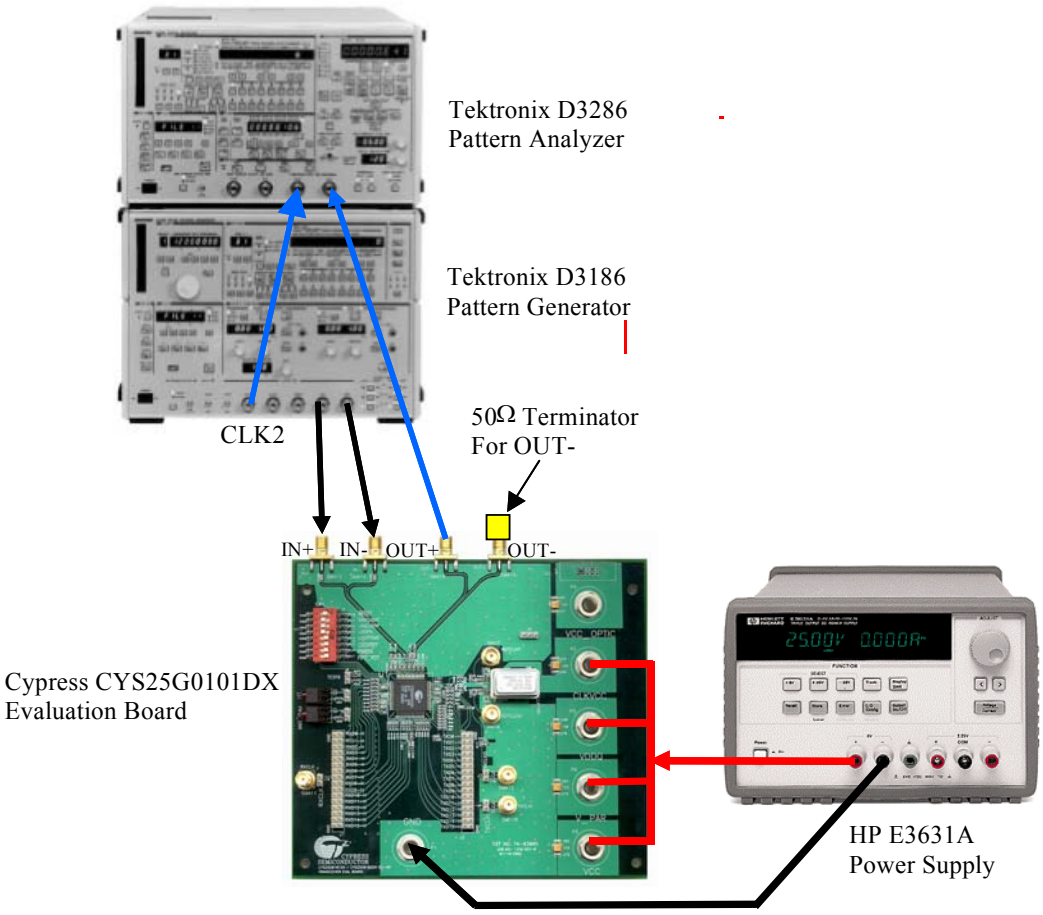

Figure 8. Equipment Set-up for BERT Test

6.2 Set-up for Eye Diagram Test

Figure 9 illustrates the set-up for testing the Eye Diagram. The equipment list:

1. Evaluation Board – Cypress CYS25G0101DX Evaluation Board
2. Pattern Generator – Tektronix D3186 Pattern Generator
3. Oscilloscope – Agilent Infiniium DCA 86100A with 83484A Dual-Channel 50GHz Module
4. Power Supply – HP E3631A DC Power Supply

* All equipment in the list is for reference only

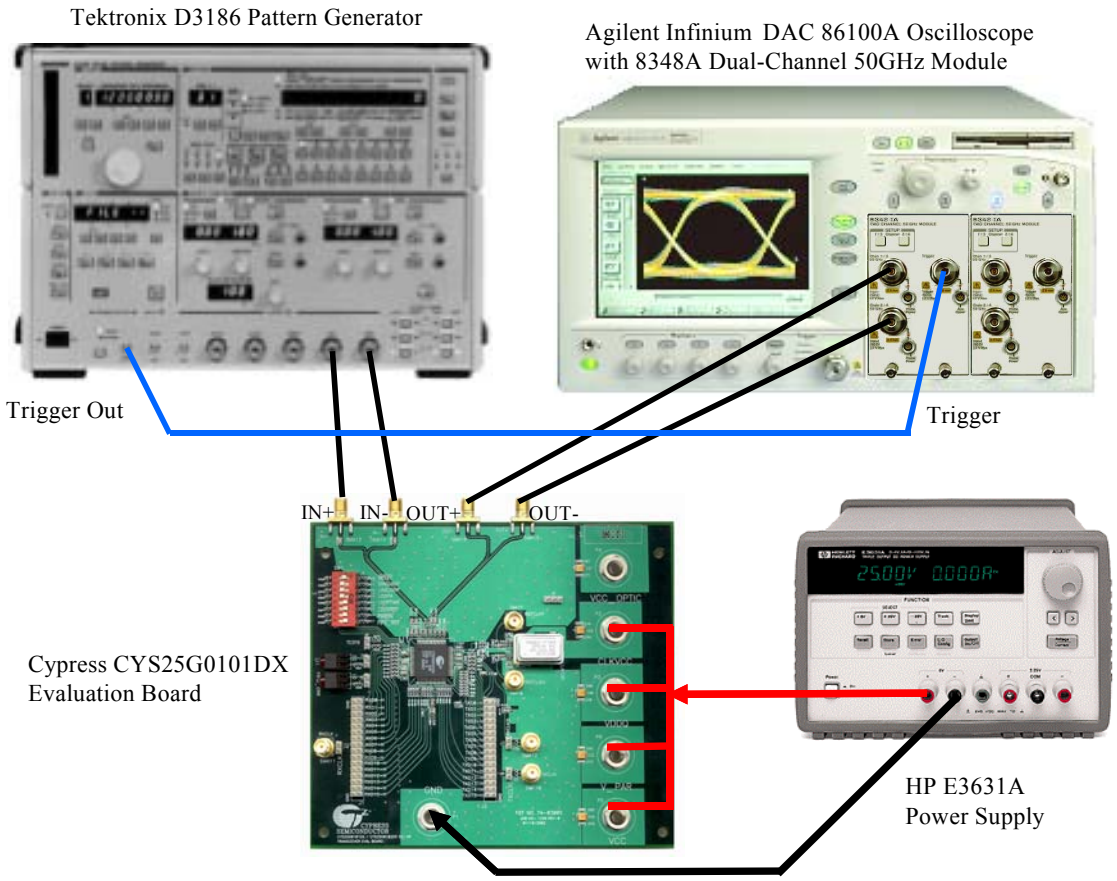

Figure 9. Equipment Set-up For Eye Diagram Test

6.3 SONET Jitter Transfer and Jitter Tolerance Test

Figure 10 illustrates the set-up for testing the jitter. The equipment list:

1. Evaluation Board – Cypress CYS25G0101DX Evaluation Board
2. SONET Tester – Agilent (HP) OmniBER 718 Communication Performance Analyzer
3. Optical Converters - Agilent (HP) 83446A Receiver and 83430A Transmitter
4. Power Supply – HP E3631A DC Power Supply

* All equipment in the list is for reference only

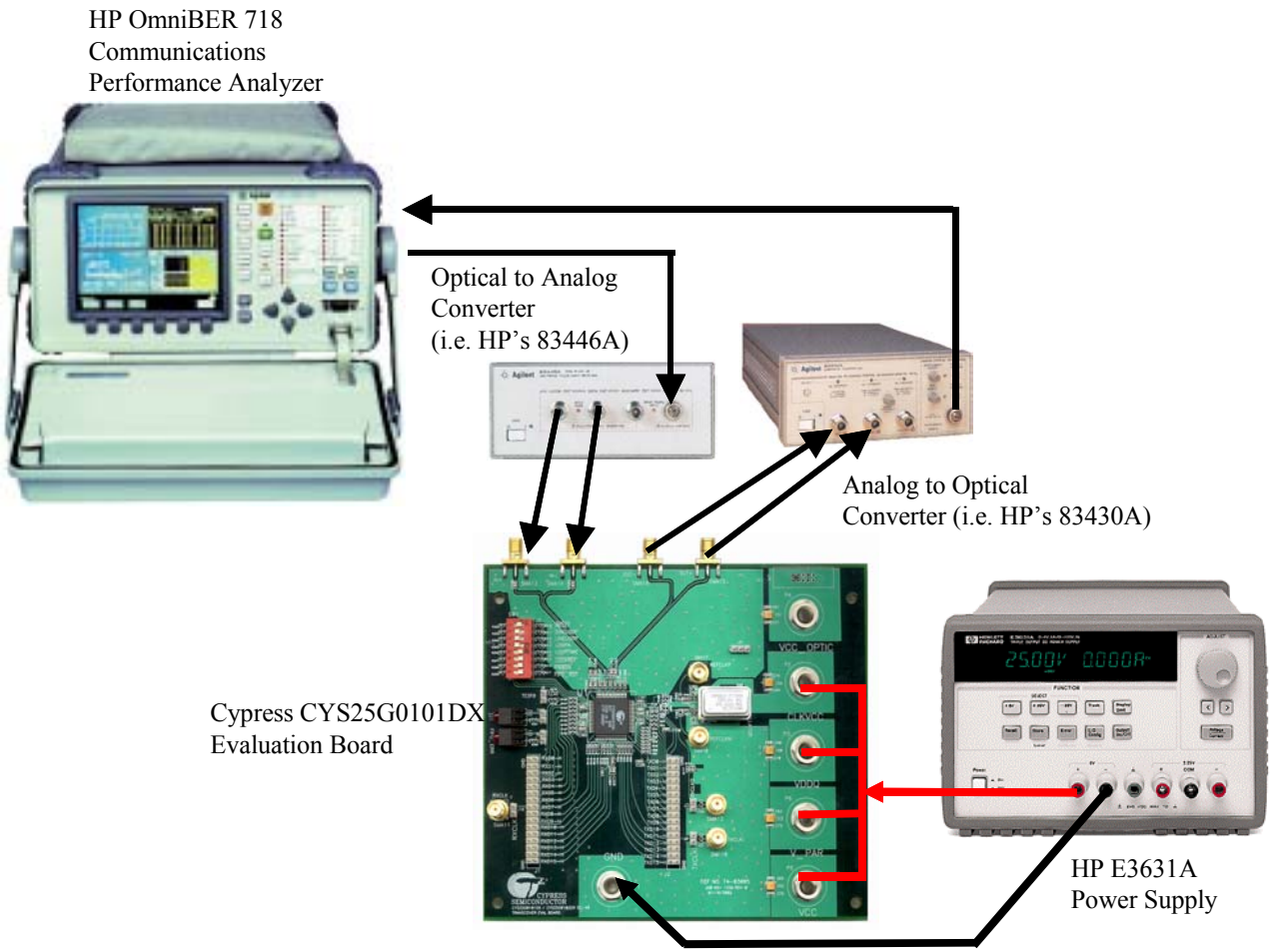

Figure 10. Equipment Set-up For Jitter Test

6.4 Set-up for Testing the TX PLL in Parallel Line Loopback Mode

Figure 11 illustrates the set-up for testing the TX PLL in Parallel Line Loopback Mode. The equipment list:

1. Evaluation Board – Cypress CYS25G0101DX Evaluation Board
2. Pattern Generator – Tektronix D3186 Pattern Generator
3. Error Detector – Tektronix D3286 Error Detector
4. Pulse Generator - HP 8133A Pulse Generator
5. Power Supply – HP E3631A DC Power Supply

* All equipment in the list is for reference only

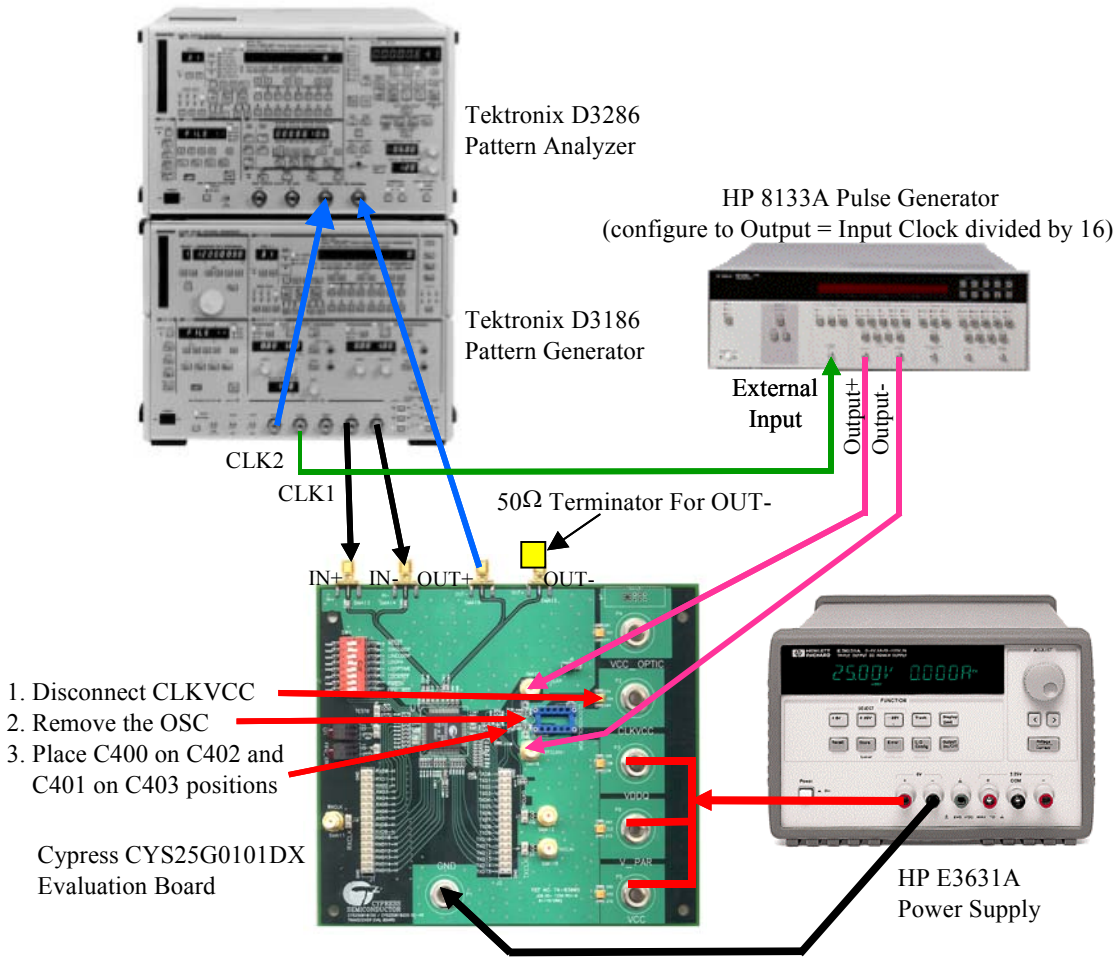

Figure 11. Equipment Set-up For Testing the TX PLL in Parallel Line Loopback Mode

7. Eye Diagram Testing Result

Figure 12 is the Eye Diagram measurement from CYS25G0101DX Evaluation Board by using the test set-up as in *Figure 9*. In this measurement, the evaluation board is configured to parallel loop back mode (*Figure 7*) and with no SONET filter at the oscilloscope.

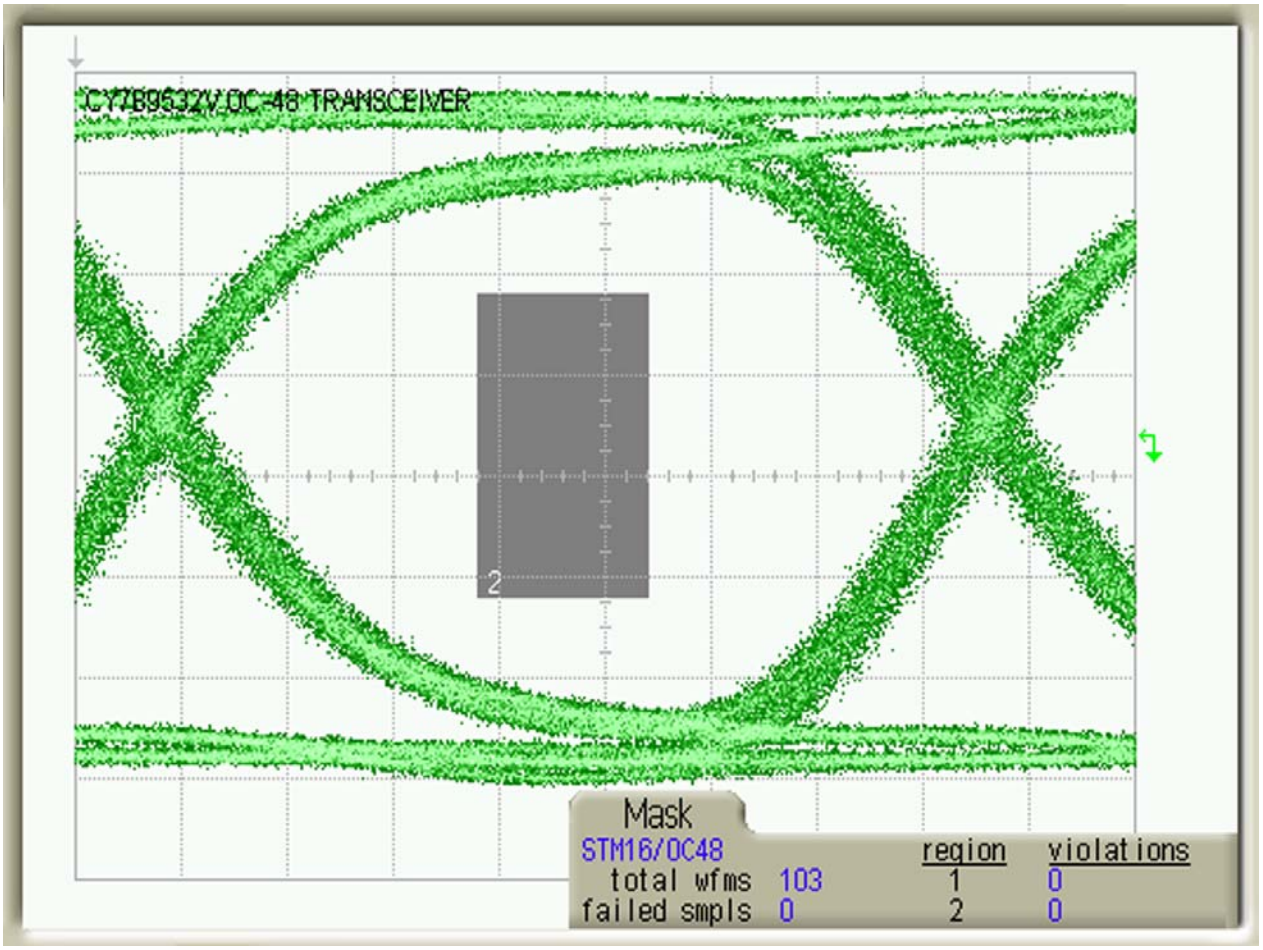

Figure 12. CYS25G0101DX Evaluation Board Eye Diagram

8. Jitter Transfer Testing Result

Figure 13 and *Figure 14* show the Jitter Transfer measurement by using the test set-up as in *Figure 10*. *Figure 13* is the measurement result of the GR-253 (Bellcore) standard and *Figure 14* is the measurement result of the G958 (ITU) standard. In this measurement, the CYS25G0101DX evaluation board is configured to parallel loopback mode (*Figure 7*).

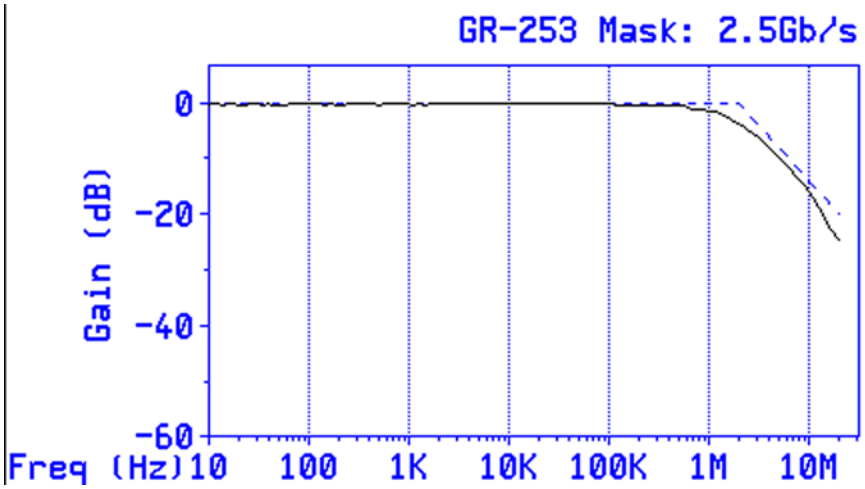

Figure 13. CYS25G0101DX Evaluation Board GR-253 Jitter Transfer Testing Result

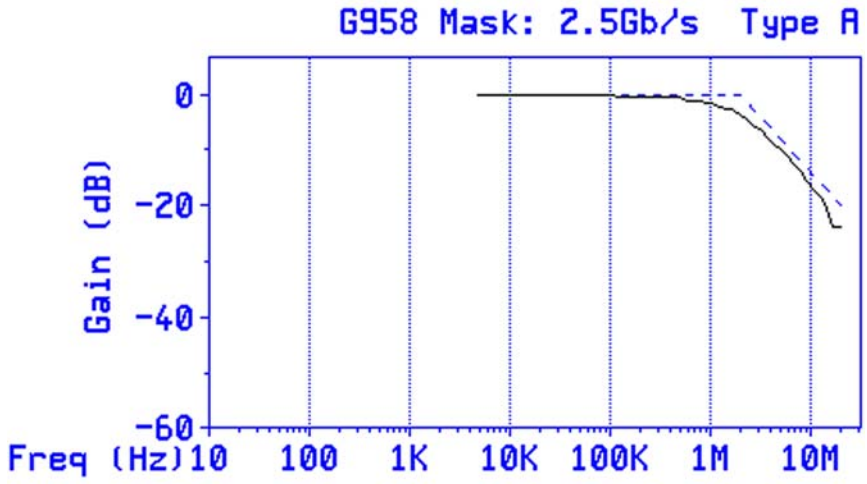

Figure 14. CYS25G0101DX Evaluation Board G958 Jitter Transfer Testing Result

9. Jitter Tolerance Testing Result

Figure 15 and *Figure 16* show the Jitter Tolerance measurement by using the test set-up as in *Figure 10*. *Figure 15* is the measurement result of the GR-253 (Bellcore) standard and *Figure 16* is the measurement result of the G825 (ITU) standard. In this measurement, the CYS25G0101DX evaluation board is configured to parallel loopback mode (*Figure 7*).

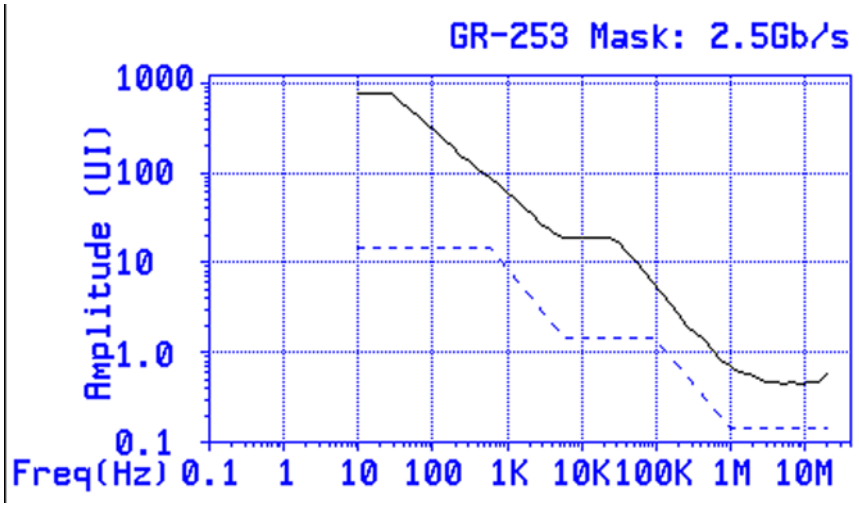

Figure 15. CYS25G0101DX Evaluation Board GR-253 JitterTolerance Testing Result

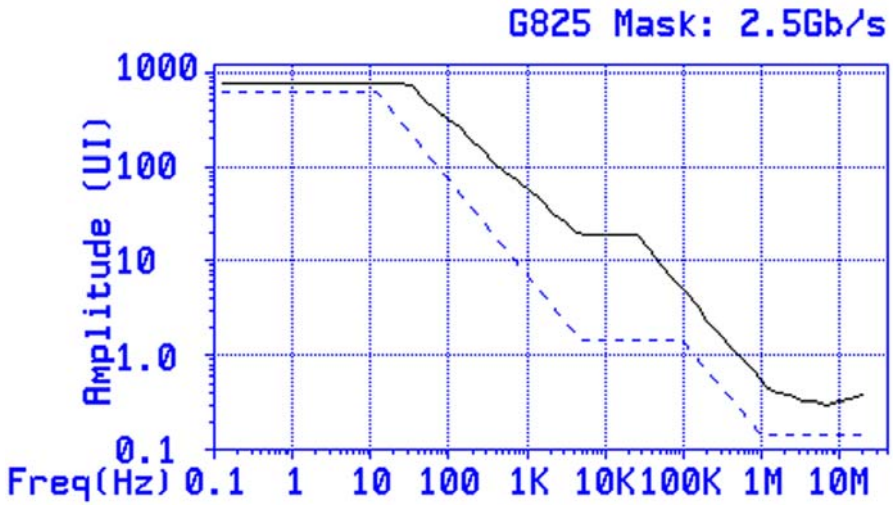

Figure 16. CYS25G0101DX Evaluation Board G825 Jitter Tolerance Testing Result

10. Schematic Diagram, PCB Layout and BOM (Bill of Material)

Figure 17 to *Figure 23* in *Appendix A* shows the schematic diagram of the CYS25G0101DX evaluation board. *Figure 17* is the top level diagram for the schematic diagrams for *Figure 18* to *Figure 23*. *Figure 24* to *Figure 32* in *Appendix B* show the PCB layout of each layer of the CYS25G0101DX evaluation board. The Bill of Material (BOM) of the evaluation board is listed in *Appendix C* (for LVPECL *Table 8* to *Table 11*) and *Appendix D* (for HSTL *Table 12* to *Table 15*) respectively.

Table 7. Operation Specification of CYS25G0101DX Evaluation Board

Description	Min.	Max.	Unit	Notes
Power Supply VCC	3.135	3.465	V	1
Current I_{VCC}	280	320	mA	2
Clock Power Supply CLKVCC	3.135	3.465	V	
Current I_{CLKVCC}	75	90	mA	3

Notes:

1. The operation voltage VCC for the device at the power supply nodes.
2. The operation current drawn by supply VCC at room temperature.
3. Assumes onboard clock option. If external clock (SMA option) is used the current drawn will depend on the termination resistors required for the external clock.

Appendix A: Schematic Diagrams of the CYS25G0101DX Evaluation Board

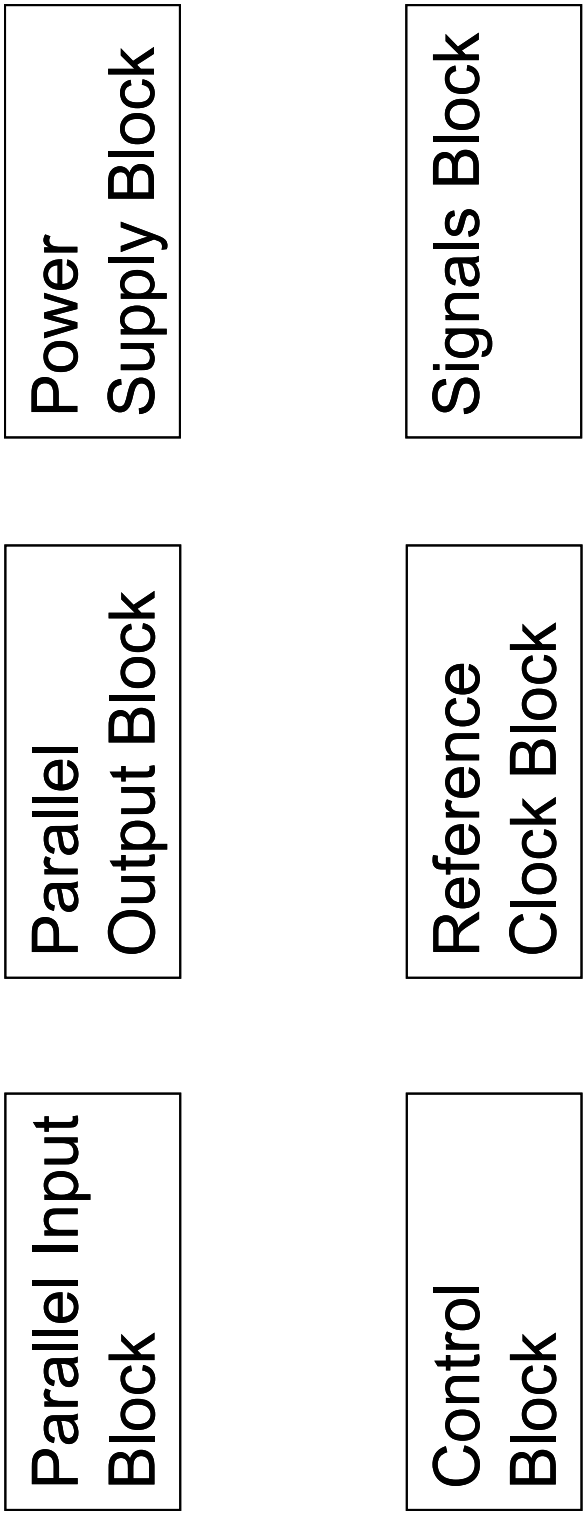

Figure 17. Top Level of CYS25G0101DX Evaluation Board Schematic Diagram

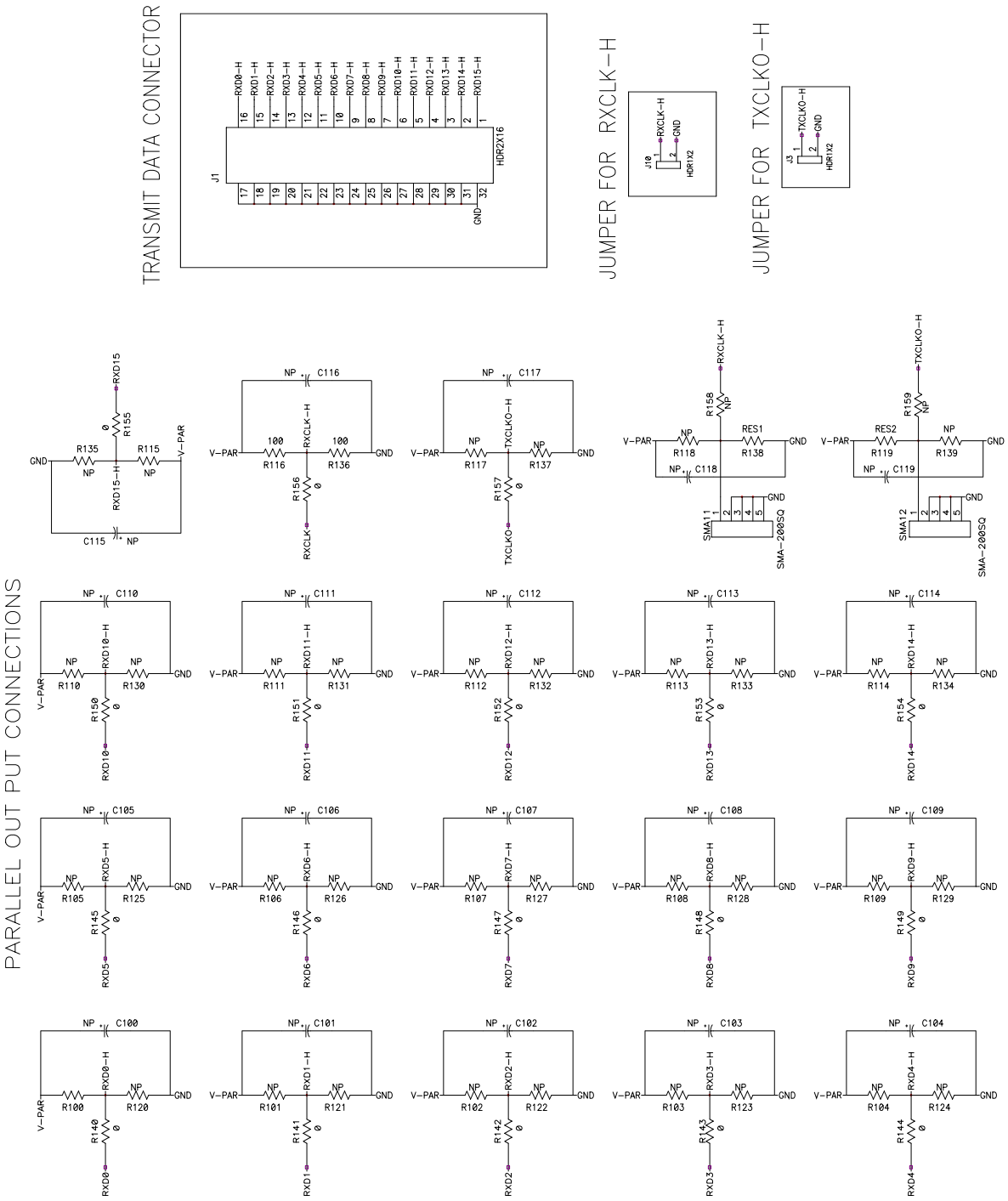

Figure 18. Parallel Output Block Schematic Diagram

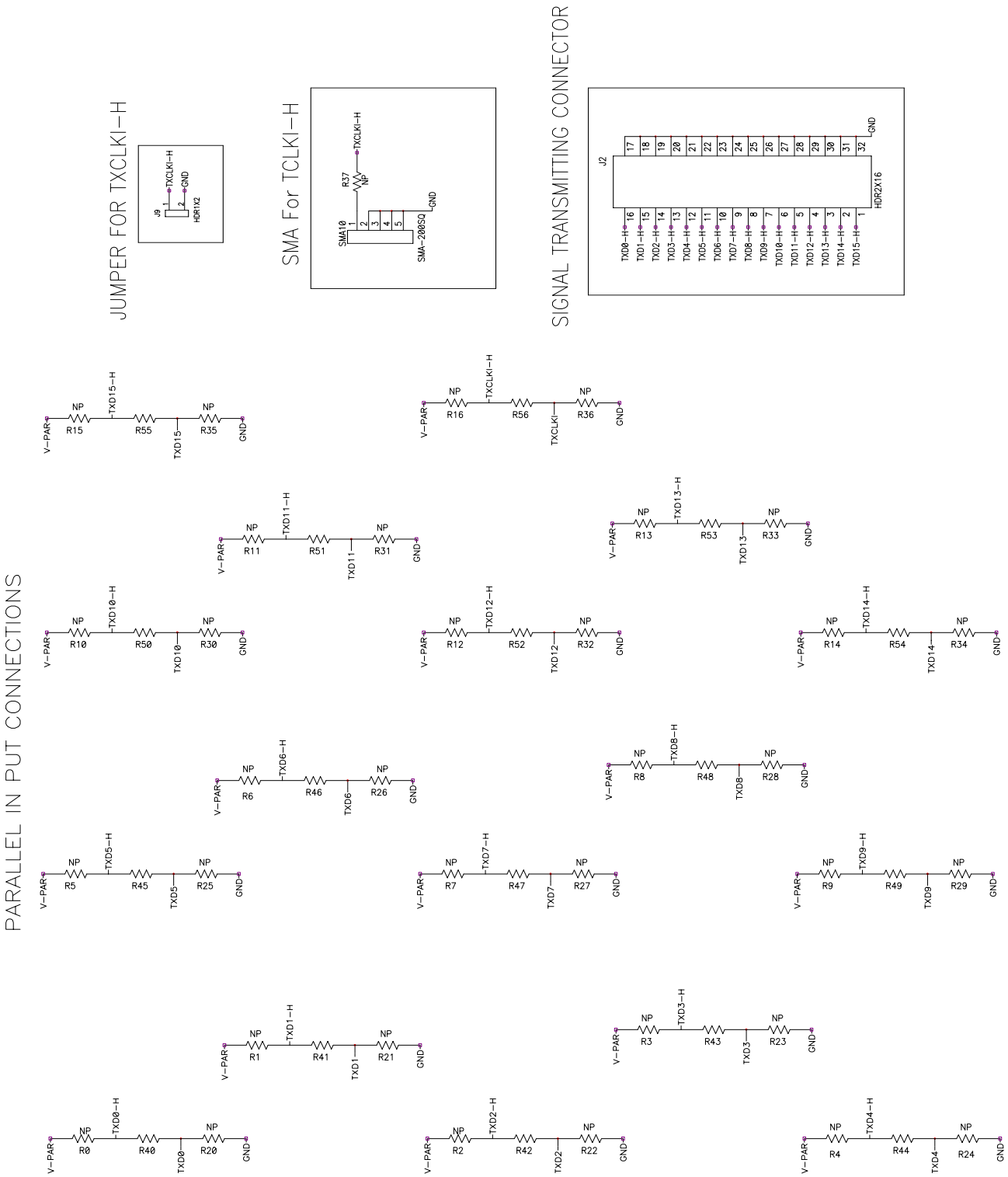

Figure 19. Parallel Input Block Schematic Diagram

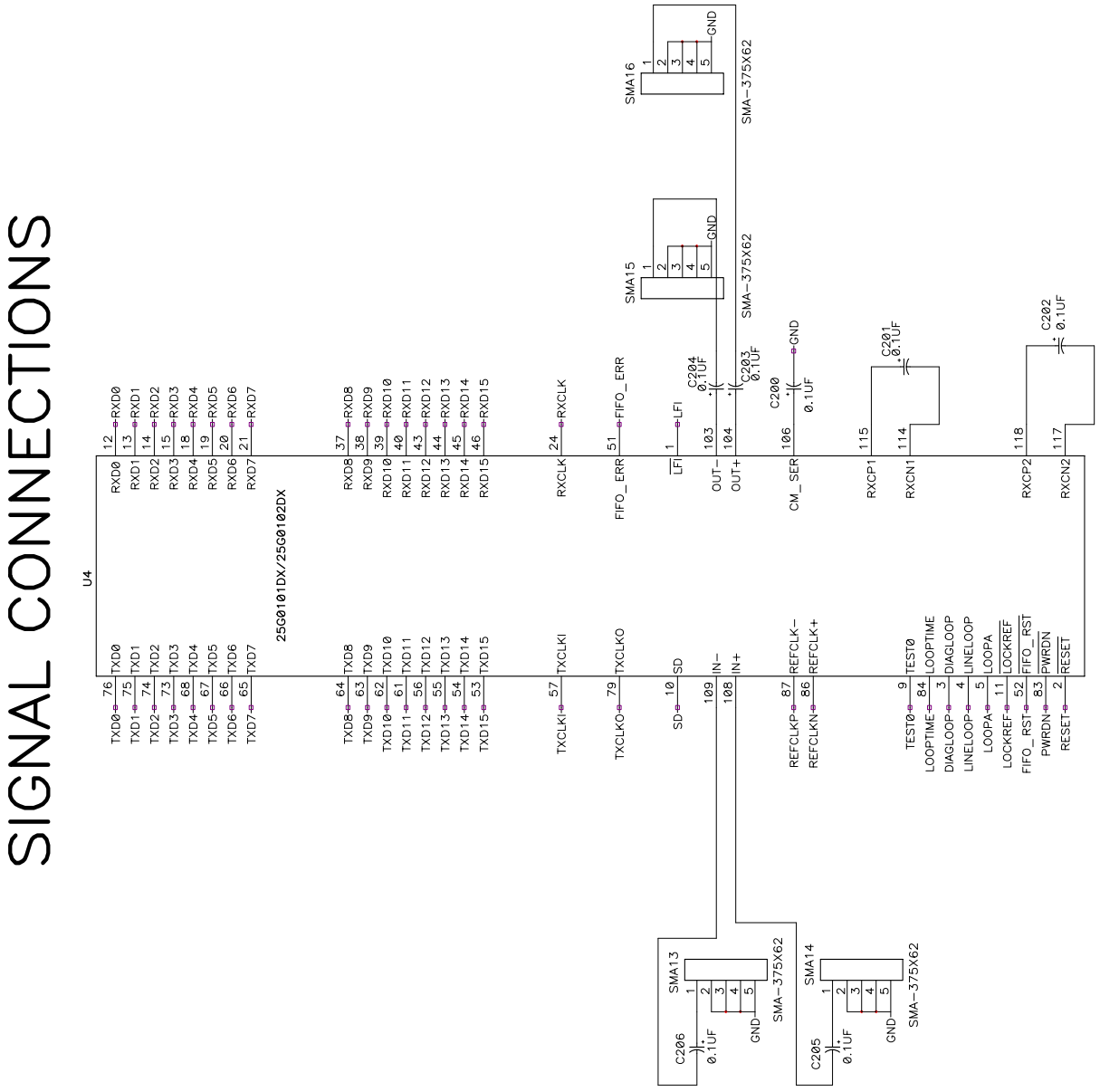

Figure 20. Signals Block Schematic Diagram

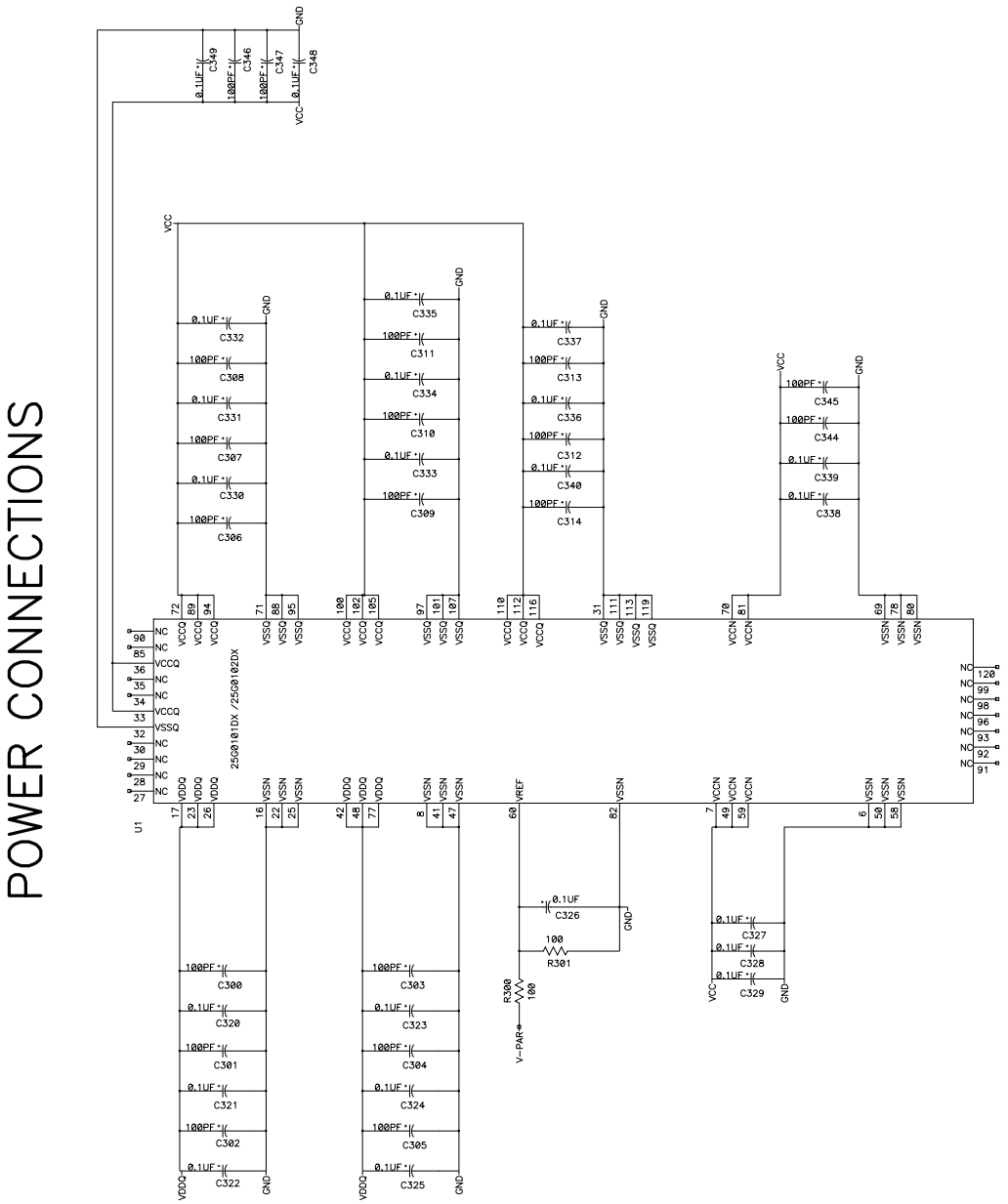

Figure 21. Power Supply Block Schematic Diagram

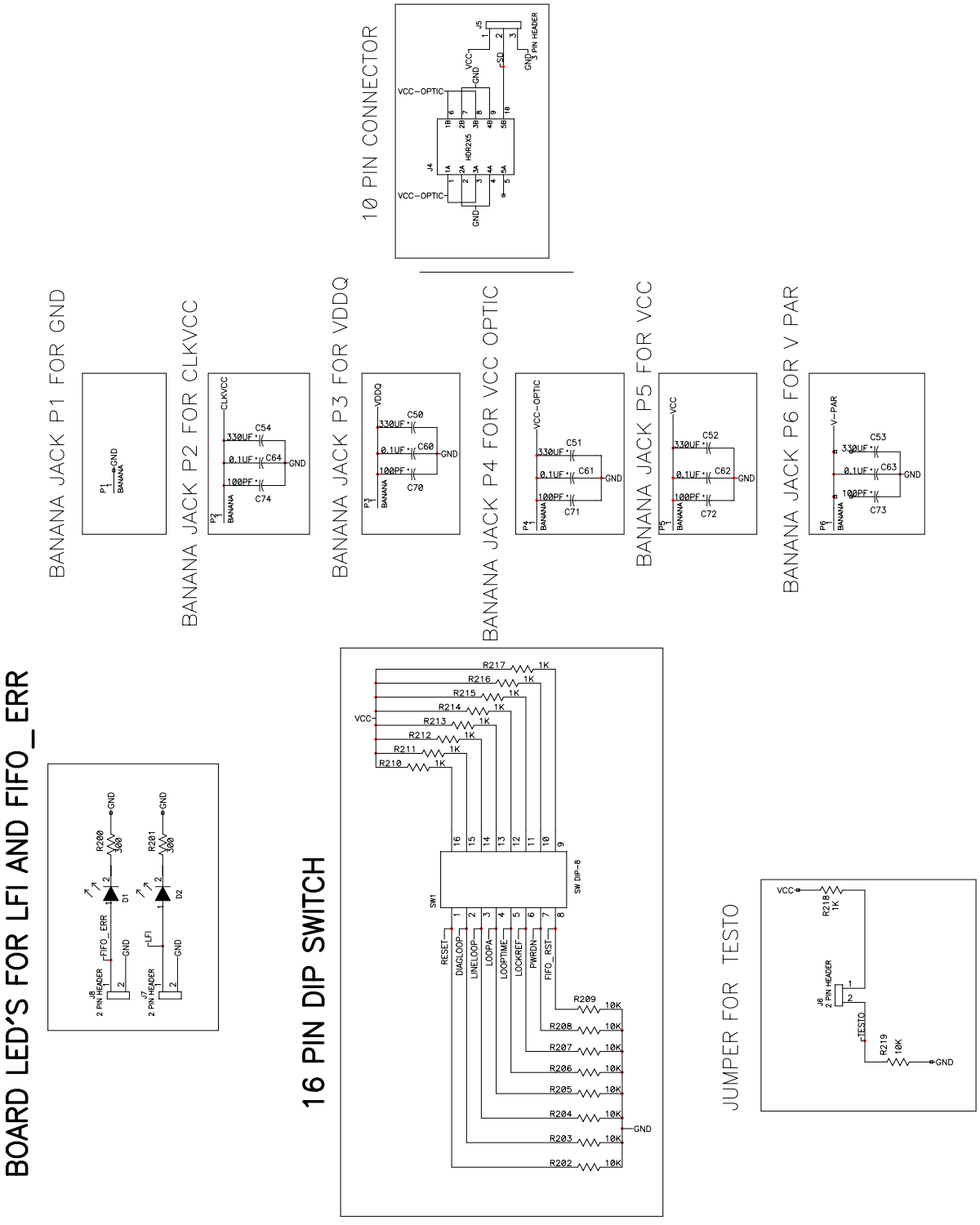

Figure 22. Control Block Schematic Diagram

CLOCK OSCILLATOR CIRCUIT

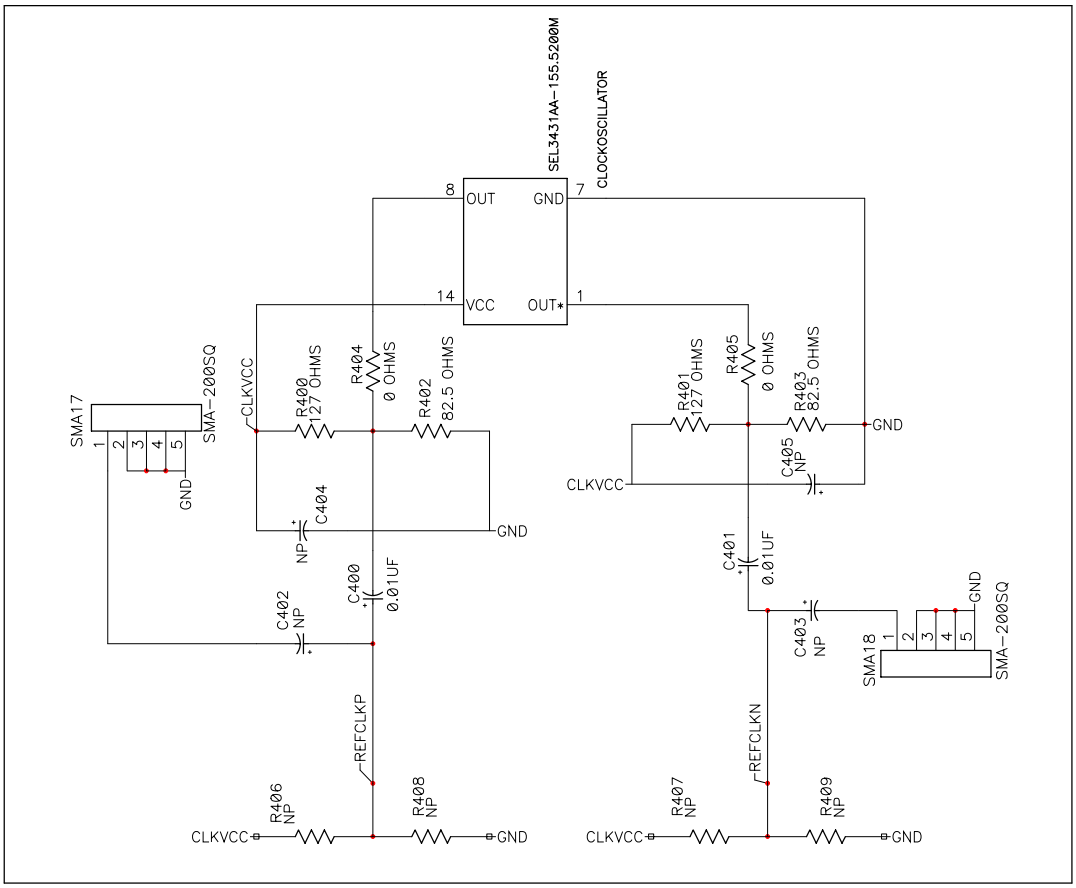

Figure 23. Reference Clock Block Schematic Diagram

Appendix B: PCB Layout Diagrams of the CYS25G0101DX Evaluation Board

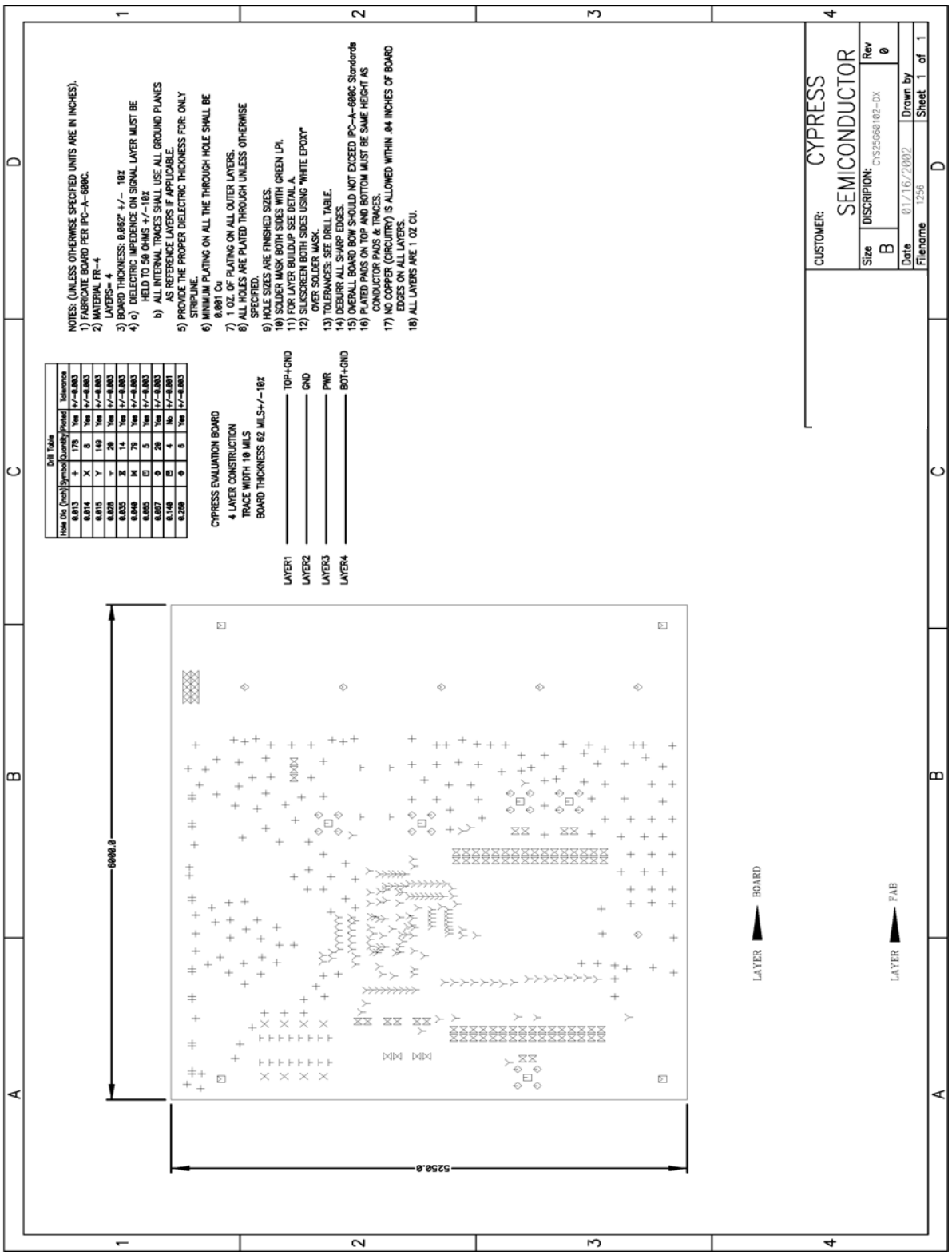

Figure 24. CYS25G0101DX Evaluation Board PCB Mechanical Drawing

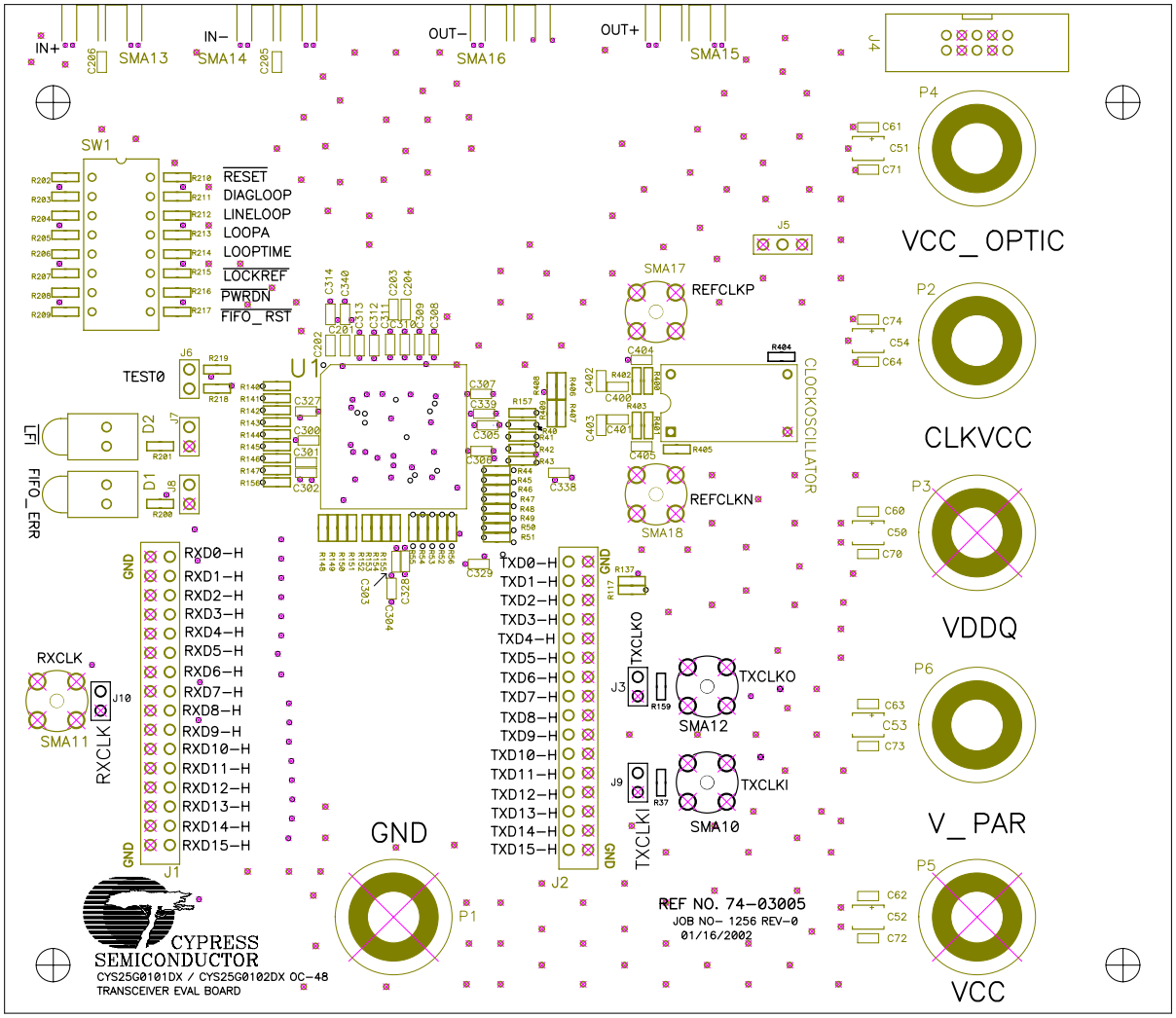

Figure 25. CYS25G0101DX Evaluation Board PCB Top Layer Silk Screen

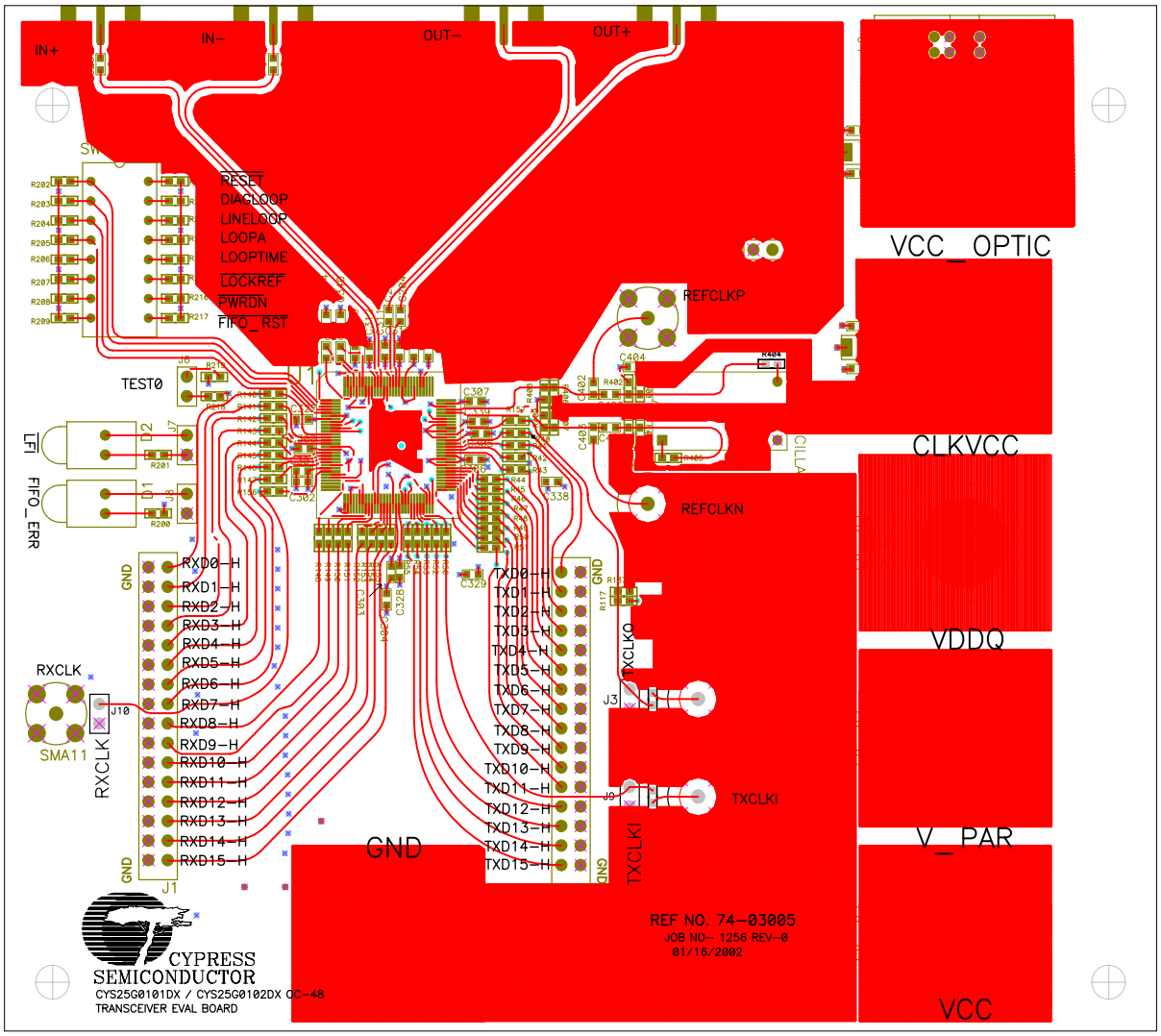

Figure 26. CYS25G0101DX Evaluation Board PCB Top Layer Layout

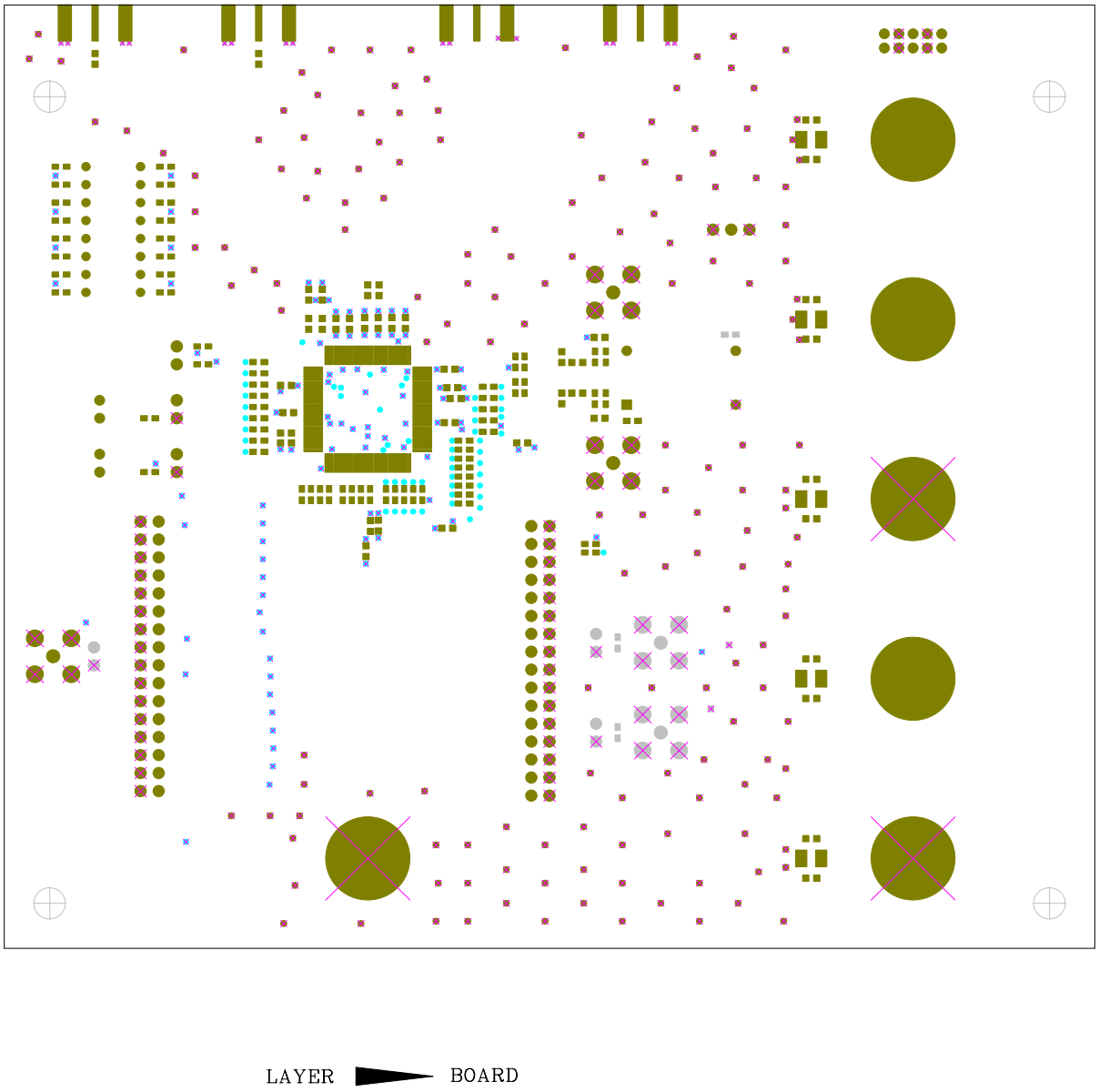

Figure 27. CYS25G0101DX Evaluation Board PCB Top Layer Solder Mask

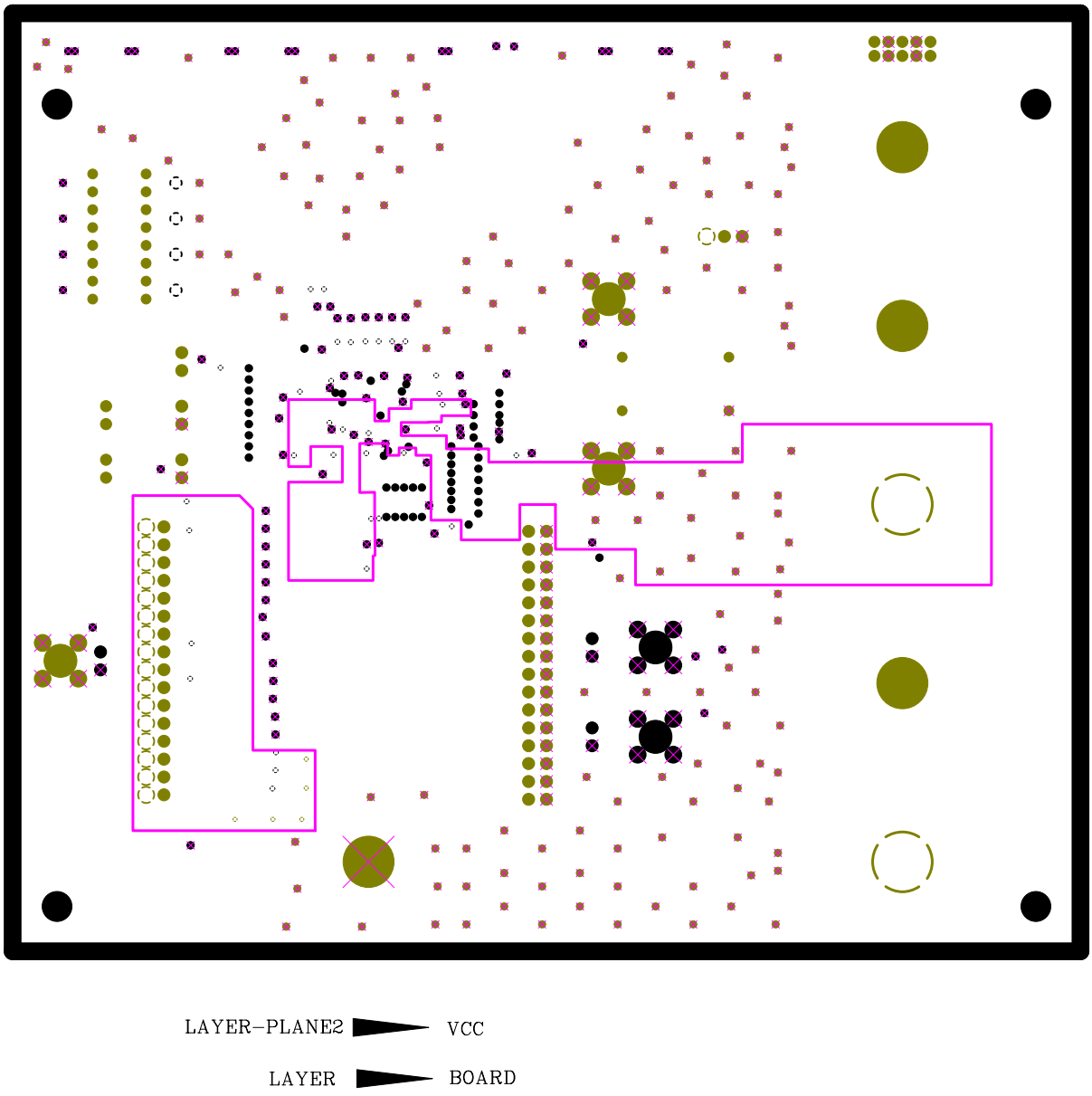

Figure 28. CYS25G0101DX Evaluation Board PCB Power Plane Layout

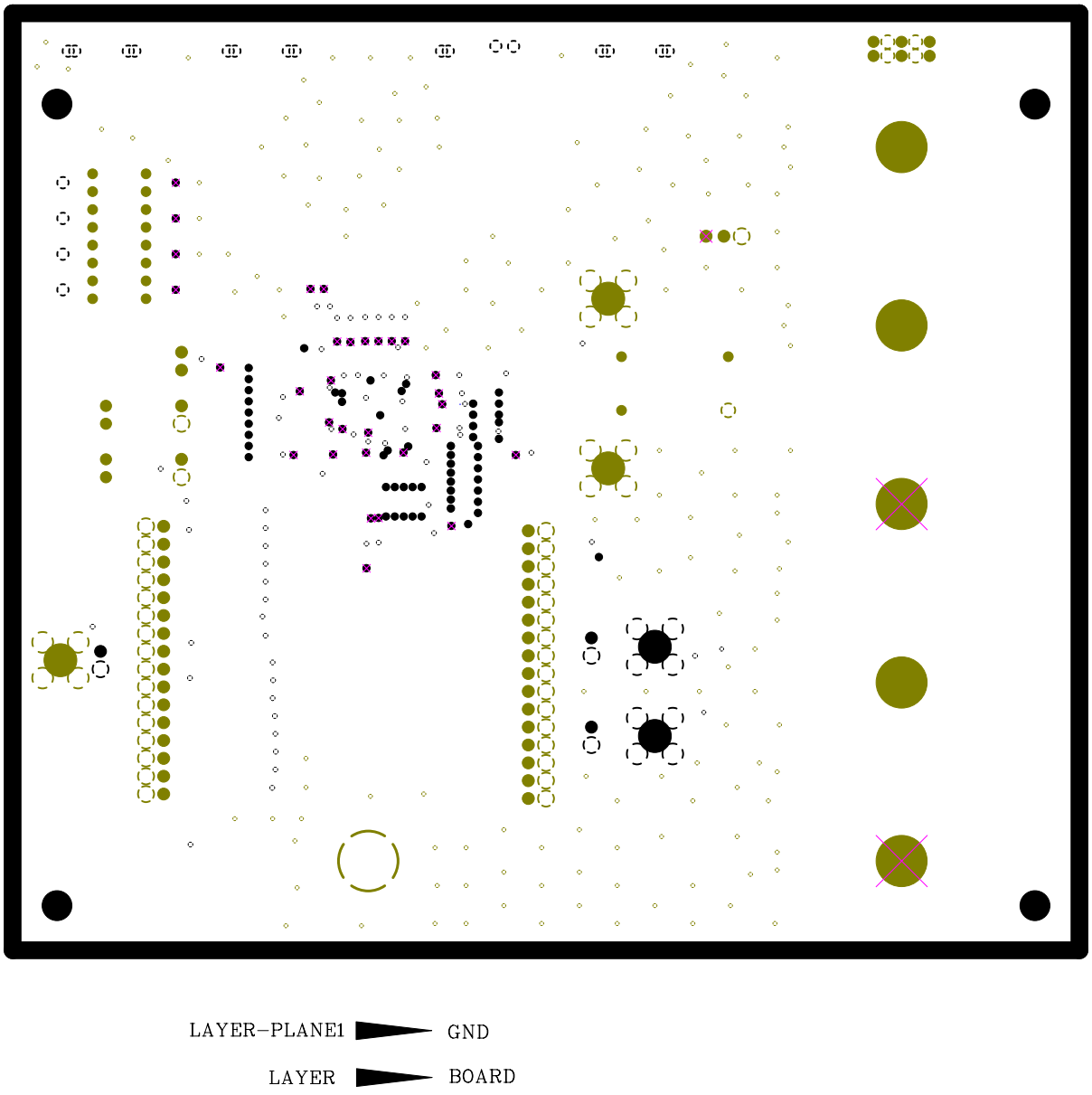

Figure 29. CYS25G0101DX Evaluation Board PCB Ground Plane Layout

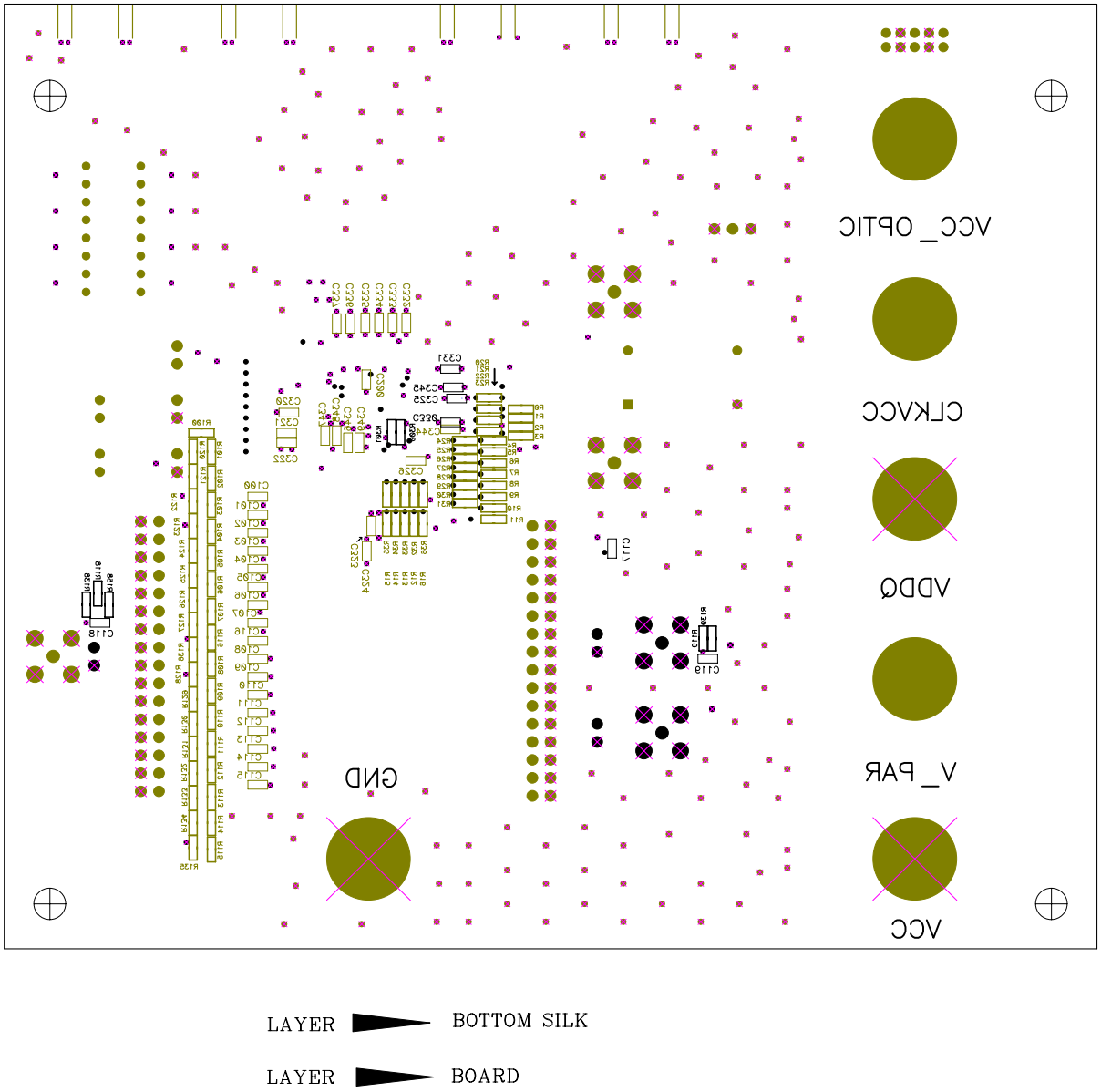

Figure 30. CYS25G0101DX Evaluation Board PCB Bottom Silk Screen

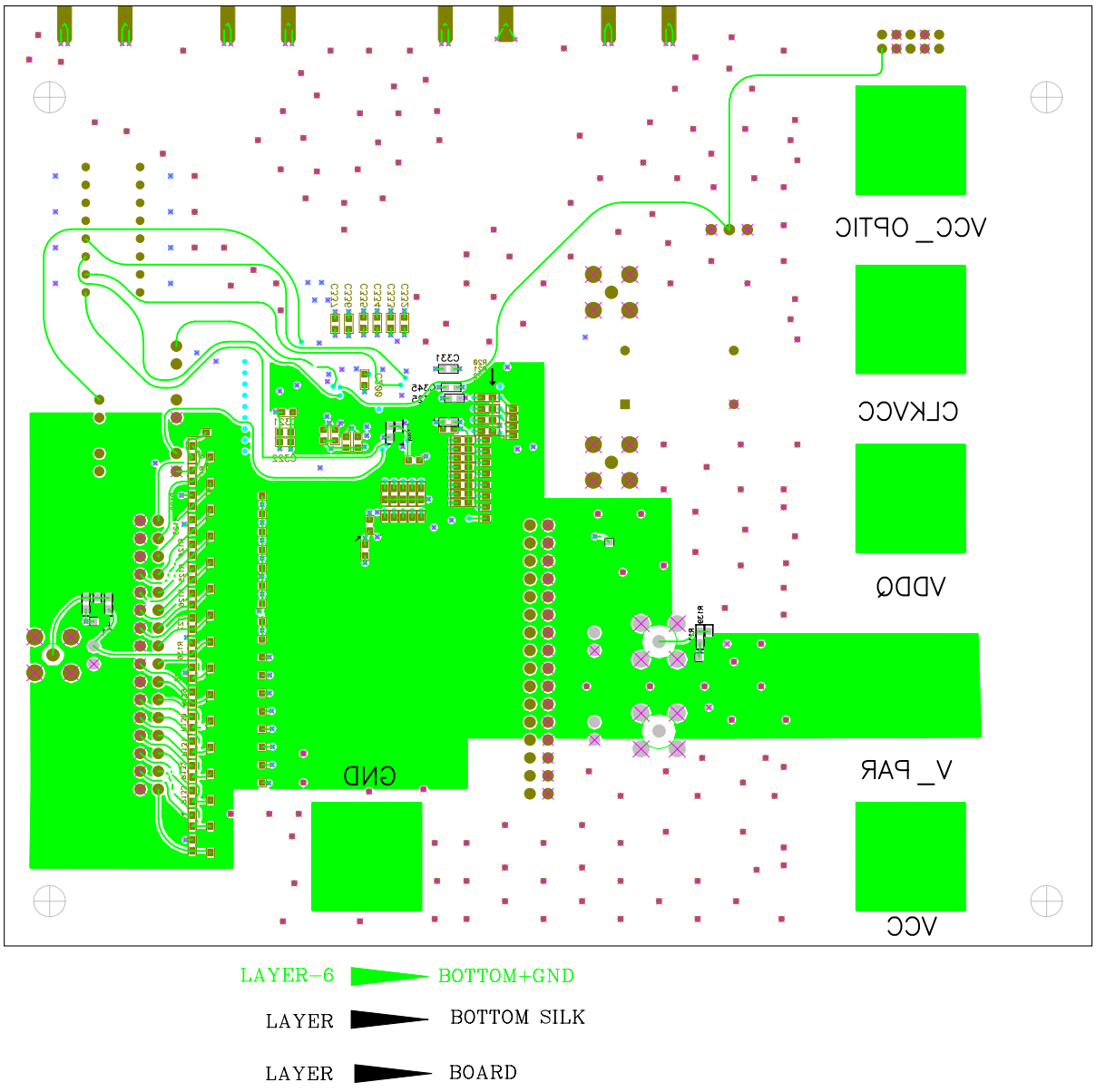

Figure 31. CYS25G0101DX Evaluation Board PCB Bottom Layer Layout

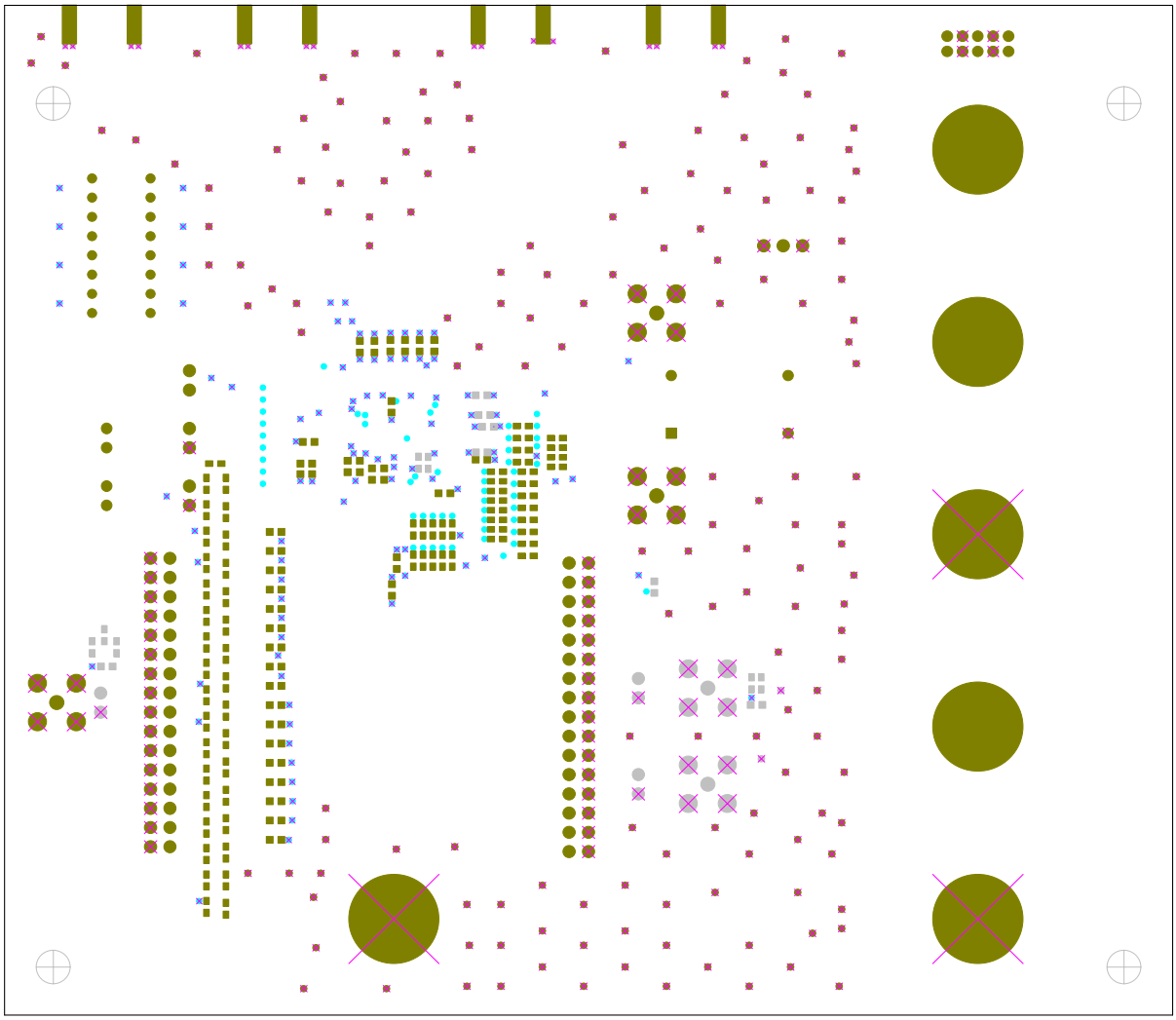

Figure 32. CYS25G0101DX Evaluation Board PCB Bottom Solder Mask

Appendix C: CYS25G0101DX Evaluation Board LVPECL BOM (Bill of Material)

Table 8. CYS25G0101DX Evaluation Board LVPECL BOM - Page 1 of 4

CYS25G0101DX Evaluation Board LVPECL BOM

Item #	Reference	Description	QTY	Manufacturer	Manufacturer P/N	Disti	Disti P/N #
1	C50, C51, C52, C53, C54	47uF 1411 case 'B' Tantalum Electrolytic Chip Capacitors	5		TMCMB0J476MTR		
2	C60, C61, C62, C63, C64, C200, C201, C202, C203, C204, C205, C206, C320, C321, C322, C323, C324, C325, C326, C327, C328, C329, C330, C331, C332, C333, C334, C335, C336, C337, C338, C339, C340	0.1uF 0603 Multilayer Ceramic Chip Capacitor	33		06032R104K250BA		
3	C70, C71, C72, C73, C74, C300, C301, C302, C303, C304, C305, C306, C307, C308, C309, C310, C311, C312, C313, C314, C344, C345	100PF 0603 Multilayer Ceramic Chip Capacitor	22		GMC10CG101J50NT		
4	C400, C401	0.01uF 0603 Multilayer Ceramic Chip Capacitor	2		06032R103K500BA		
5	C402, C403, C404, C405	NP 0603 Multilayer Ceramic Chip Capacitor	4		**DO NOT POPULATE**		
6	C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C110, C111, C112, C113, C114, C115, C116, C117, C118, C119	NP 0603 Multilayer Ceramic Chip Capacitor	20		**DO NOT POPULATE**		

Table 9. CYS25G0101DX Evaluation Board LVPECL BOM - Page 2 of 4

CYS25G0101DX Evaluation Board LVPECL BOM

Item #	Reference	Description	QTY	Manufacturer	Manufacturer P/N	Disti	Disti P/N #
7	R0, R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16	82ohm 0603 Resistor	17	Vishay	CRCW060382R0F CRCW060382R0F		
8	R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36	130ohm 0603 Resistor	17	Vishay	CRCW06031300F CRCW06031300F		
9	R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56	0 ohm 0603 Resistor	17	Vishay	CRCW060300N		
10	R100, R101, R102, R103, R104, R105, R106, R107, R108, R109, R110, R111, R112, R113, R114, R115, R116, R117	80.6ohm 0603 Resistor	18	Vishay	CRCW060380R6F		
11	R120, R121, R122, R123, R124, R125, R126, R127, R128, R129, R130, R131, R132, R133, R134, R135, R136, R137	121ohm 0603 Resistor	18	Vishay	CRCW06031210F		

Table 10. CYS25G0101DX Evaluation Board LVPECL BOM - Page 3 of 4

CYS25G0101DX Evaluation Board LVPECL BOM

Item #	Reference	Description	QTY	Manufacturer	Manufacturer P/N	Disti	Disti P/N #
12	R140, R141, R142, R143, R144, R145, R146, R147, R148, R149, R150, R151, R152, R153, R154, R155, R156, R157	137ohm 0603 Resistor	18	Vishay	CRCW0603137OF		
13	R37, R118, R119, R138, R139, R158, R159	NP 0603 Resistor	7		**DO NOT POPULATE**		
14	R200, R201	300 ohm 0603 Resistor	2	Vishay	CRCW0603300F		
15	R300	820ohm 0603 Resistor	1	Vishay	CRCW0603820F		
16	R301	1.3kohm 0603 Resistor	1	Vishay	CRCW06031301F		
17	R400, R401	127ohm 0603 Resistor	2	Vishay	CRCW06031270F		
18	R402, R403	82.5ohm 0603 Resistor	2	Vishay	CRCW060382R5F		
19	R404 R405	0ohm 0603 Resistor	2	Vishay	CRCW06030r		
20	R406, R407, R408, R409	NP 0603 Resistor	4		**DO NOT POPULATE**		
21	R202, R203, R204, R205, R206, R207, R208, R209, R219	10Kohm 0603 Resistor	9	Vishay	CRCW06031002F		
22	R210, R211, R212, R213, R214, R215, R216, R217, R218	1Kohm 0603 Resistor	9	Vishay	CRCW06031001F		
23	J3, J6, J7, J8, J9, J10	HDR1X2	6				

Table 11. CYS25G0101DX Evaluation Board LVPECL BOM - Page 4 of 4

CYS25G0101DX Evaluation Board LVPECL BOM

Item #	Reference	Description	QTY	Manufacturer	Manufacturer P/N	Disti	Disti P/N #
24	J4	HDR2X5 with Ejector Clips and Keying: SAMTEC EHT-105-01-S-D	1		EHT-105-01-S-D		
25	J5	HDR1X3	1				
26	P1, P2, P3, P4, P5, P6	BANANA	6	Johnson	108-0740-001		
27	U1	CYS25G0101DX: Cypress 120TQFP_14SQ SONET OC-48 Transceiver	1	Cypress	CYS25G0101DX-ATC		
28	J1, J2	HDR2X16	2				
29		155.5200MHz Clock Oscillator	1	SaRonixs	SEL3431AA-155.5200M		
30		4PIN_OSC_SKT DIP Osc	1			Digikey	A462-ND
31	J10, J11, J12, J17, J18	SMA	5	Johnson	142-0701-201	Digikey	J609-ND
32	J13, J14, J15, J16	SMA	4	Johnson	142-0701-801	Digikey	J502-ND
33	D1, D2	LED	2			Digikey	67-1225-ND
34	SW1	DIP Switch	1			Digikey	CKN3007-ND

Appendix D: CYS25G0101DX Evaluation Board HSTL BOM (Bill of Material)

Table 12. CYS25G0101DX Evaluation Board HSTL BOM - Page 1 of 4

CYS25G0101DX Evaluation Board HSTL BOM

Item #	Reference	Description	QTY	Manufacturer	Manufacturer P/N	Disti	Disti P/N #
1	C50, C51, C52, C53, C54	47uF 1411 case 'B' Tantalum Electrolytic Chip Capacitors	5		TMCMB0J476MTR		
2	C60, C61, C62, C63, C64, C200, C201, C202, C203, C204, C205, C206, C320, C321, C322, C323, C324, C325, C326, C327, C328, C329, C330, C331, C332, C333, C334, C335, C336, C337, C338, C339, C340	0.1uF 0603 Multilayer Ceramic Chip Capacitor	33		06032R104K250BA		
3	C70, C71, C72, C73, C74, C300, C301, C302, C303, C304, C305, C306, C307, C308, C309, C310, C311, C312, C313, C314, C344, C345	100PF 0603 Multilayer Ceramic Chip Capacitor	22		GMC10CG101J50NT		
4	C400, C401	0.01uF 0603 Multilayer Ceramic Chip Capacitor	2		06032R103K500BA		
5	C402, C403, C404, C405	NP 0603 Multilayer Ceramic Chip Capacitor	4		**DO NOT POPULATE**		

Table 13. CYS25G0101DX Evaluation Board HSTL BOM - Page 2 of 4

CYS25G0101DX Evaluation Board HSTL BOM

Item #	Reference	Description	QTY	Manufacturer	Manufacturer P/N	Disti	Disti P/N #
6	C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C110, C111, C112, C113, C114, C115, C116, C117, C118, C119	NP 0603 Multilayer Ceramic Chip Capacitor	20	DO NOT POPULATE			
7	R0, R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R100, R101, R102, R103, R104, R105, R106, R107, R108, R109, R110, R111, R112, R113, R114, R115, R116, R117, R120, R121, R122, R123, R124, R125, R126, R127, R128, R129, R130, R131, R132, R133, R134, R135, R136, R137	100 ohm 0603 Resistor	70	Vishay	CRCW06031000F		

Table 14. CYS25G0101DX Evaluation Board HSTL BOM - Page 3 of 4

CYS25G0101DX Evaluation Board HSTL BOM

Item #	Reference	Description	QTY	Manufacturer	Manufacturer P/N	Disti	Disti P/N #
8	R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R140, R141, R142, R143, R144, R145, R146, R147, R148, R149, R150, R151, R152, R153, R154, R155, R156, R157, R404, R405	0 ohm 0603 Resistor	37	Vishay	CRCW060300N		
9	R37, R118, R119, R138, R139, R158, R159	NP 0603 Resistor	7		**DO NOT POPULATE**		
10	R200, R201	300 ohm 0603 Resistor	2	Vishay	CRCW06033000F		
11	R300, R301, R210, R211, R212, R213, R214, R215, R216, R217, R218	1K ohm 0603 Resistor	11	Vishay	CRCW06031001F		
12	R400, R401	127ohm 0603 Resistor	2		CRCW06031270F		
13	R402, R403	82.5ohm 0603 Resistor	2	Vishay	CRCW060382R5F		
14	R406, R407, R408, R409	NP 0603 Resistor	4		**DO NOT POPULATE**		
15	R202, R203, R204, R205, R206, R207, R208, R209, R219	10Kohm 0603 Resistor	9	Vishay	CRCW06031002F		

Table 15. CYS25G0101DX Evaluation Board HSTL BOM - Page 4 of 4

CYS25G0101DX Evaluation Board HSTL BOM

Item #	Reference	Description	QTY	Manufacturer	Manufacturer P/N	Disti	Disti P/N #
16	J3, J6, J7, J8, J9, J10	HDR1X2	6				
17	J4	HDR2X5 with Ejector Clips and Keying: SAMTEC EHT-105-01-S-D	1		EHT-105-01-S-D		
18	J5	HDR1X3	1				
19	P1, P2, P3, P4, P5, P6	BANANA	6	Johnson	108-0740-001		
18	U1	CYS25G0101DX: Cypress 120TQFP_14SQ SONET OC-48 Transceiver	1	Cypress	CYS25G0101DX-ATC		
19	J1, J2	HDR2X16	2				
20		155.5200MHz Clock Oscillator	1	SaRonixs	SEL3431AA-155.5200M		
21		4PIN_OSC_SKT DIP Osc	1			Digikey	A462-ND
22	J10, J11, J12, J17, J18	SMA	5	Johnson	142-0701-201	Digikey	J609-ND
23	J13, J14, J15, J16	SMA	4	Johnson	142-0701-801	Digikey	J502-ND
24	D1, D2	LED	2			Digikey	67-1225-ND
25	SW1	DIP Switch	1			Digikey	CKN3007-ND