dCS 904

Analogue to Digital Converter

User Manual

Standard Software version 1.5x
P3D Software version 1.36

June 2000

Information contained in this manual is subject to change without notice, and whilst it is checked for accuracy, no liabilities can be accepted for errors.

[1] ***dCS*** Ltd is Data Conversion Systems Ltd. Company registered in the England no. 2072115

PRODUCT FEATURES

Formats

- DSD, and PCM from 192 kS/s down to 32 kS/s
- Data formats supported are: AES/EBU (XLR and BNC), Dual AES (XLR), Quad AES (XLR), AES data at TTL levels, and SDIF-2 (PCM and DSD), SDIF-3 (DSD), DSD packed into 4 AES links
- P3D option: DSD packed into 3 AES links

Syncing

- Operates in Master mode or can sync to Word Clock or AES reference, or signal, and sync to video option available

Functions

- Very high performance ADC, free from gain ranging
- High quality VCXO internal clocking in Master mode
- Multichannel Sync capability
- Noise shaping truncation (1^{st}, 3^{rd}, 9^{th} order)
- High speed or dual AES (88.2 kS/s, 96 kS/s)
- Dual or Quad AES (176.4 kS/s and 192 kS/s)
- Data mode – can take in digital data in both PCM and noise shape/truncate it, and in DSD can re-pack it

Test Generator

- High quality (160 dB) signal generator with mHz resolution. Can be noise shaped truncated

Ease of Use

- Remembers last settings
- Lockouts
- Software upgrade-able without opening the box
- Can be remote controlled from PC

CONTENTS

About this Manual

Note that there is a fuller **Contents** at the end of the manual (page 80), along with an index and lists of figures and tables.

References to other sections in the text have the **"Section Name"** page … in quotation marks and bolded.

IMPORTANT! *Important information is presented like this - ignoring this may cause you to damage the unit, or invalidate the warranty.*

The manual covers standard units and units with P3D option. P3D is a DSD data format, and these units have changed internal hardware to accommodate it. Information that is specific to P3D units is greyed.

The manual is designed to be helpful. If there are points you feel we could cover better, or that we have missed out - please tell us.

USING YOUR *dCS 904* FOR THE FIRST TIME

Product Overview

The ***dCS 904*** ADC (Analogue to Digital Converter) is a high performance converter designed for studio and live recording applications. It is designed to produce very high standard digital output (for example, 192 kS/s or DSD) that may be used directly or archived. If these formats are used, lower resolution formats (for example Red Book CD) may produced by subsequent downsampling. AES3, SPDIF, SDIF-2 PCM formats and several DSD formats are all supported. Multiple units may be slaved together for stable multi-channel operation.

The unit is mains powered and is housed in a 1U (1.75") high 19" rack mounting case. It may be controlled either from its front panel, or from a software based remote control running on a PC via a com port. The unit's last setting is automatically stored on power down, so that fixed installations may be set up at leisure, installed and then left alone. Unauthorised alterations to settings may be prevented by a "panel lock out" feature.

The unit is highly software based, and more functions and features are added from time to time. Software updates from ***dCS*** are free![2]

What's in the Box?

The contents of the box are at least:

dCS 904
User Manual
Quick Start Guide
Mains Lead
2 Spare Fuses
Remote cable
Remote software

Mains Voltages

The ***dCS 904*** is shipped with its mains voltage preset for operation in the destination country. The voltage is not intended to be changed by the user. If it needs to be changed, contact your dealer or ***dCS***.

IMPORTANT! *The **dCS 904** must be used with a mains earth!*

[2] free if we email them, and you download from a PC com port. Low cost if you ask us for EPROMs or other media - we charge for media and handling.

Installing Unit in a Rack

The unit is supplied with 19" rack mount ears fitted. If it is to be mounted in a 19" rack, the ears supplied may be used to locate it in the rack and stop the unit sliding forward – but they are not strong enough to support the unit.

IMPORTANT! *The ears should not be used as the only mechanical support. The unit should rest on a shelf, or be supported in some other way. The ears will just locate it in the rack, and stop it sliding forwards.*

If the unit is not to be rack mounted, the ears may be removed.

Getting Started

Here's what to do:

(If the unit does not behave the first time you power up – contact your dealer, or *dCS*.)

do this: Check the appropriate mains supply for your local mains is marked on the rear panel.

do this: If it is, using the lead supplied, connect the unit to the mains - connect no other leads at this stage - and switch on.

The seven segment display will briefly show:

- - - - 4

and then the sample rate, for example:

1 9 2

do this: Connect a signal source to the analogue inputs.

do this: Connect an output (eg from AES1) to your system or a DAC.

do this: Press the Sample Rate button (left hand end button) to get the sample rate you want. Press the Output Format button (right hand end) to get the format you want.

Set up like this, the *dCS 904* will operate in Master mode, and the system it is connected to will (have to) lock to it. You should have audio.

Use any of AES1, AES2, AES3, or AES4 as an output at 32 kS/s or 44.1 kS/s or 48 kS/s, or for double speed AES at 88.2 kS/s or 96 kS/s.

Use (AES1 + AES2) or (AES3 + AES4) for dual AES 88.2 kS/s or 96 kS/s or 176.4 kS/s or 192 kS/s.

Use all of (AES1 + AES2 + AES3 + AES4) for quad AES 176.4 kS/s or 192 kS/s. For DSD, see the DSD section.

Note that all the outputs are active simultaneously on the *dCS 904*. If the mode the unit is in needs them to be different, they will be – otherwise they will be the same, and may all be connected to external equipment simultaneously if required.

Now you will need to familiarise yourself with how the front panel controls and the menu system work.

do this: Read the short section on **"The Software – the Menu"** on page 18 so you know how the buttons and menu work.

You may also find it convenient to refer to the **Quick Start Guide** while you are getting to know the unit.

THE HARDWARE – CONTROLS AND CONNECTORS

Rear Panel

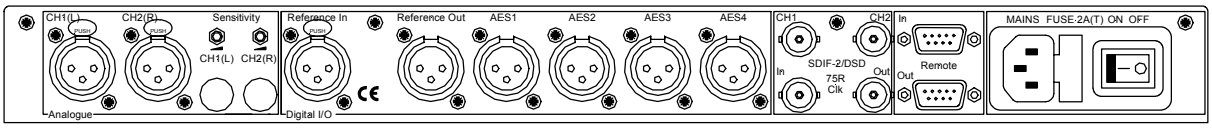


Figure 1– Rear Panel

All input and output connectors are mounted on the rear panel. Individual connectors are clearly identified by the panel legend. Viewed from the rear from left to right, the connectors are as follows:

Balanced Analogue Inputs **3 pin XLR female (2 off)**

Input Level Adjustment **(trimmers)**

Two multi-turn potentiometers set the full scale input levels. These are factory preset for full scale with input levels of +20dBu. If necessary, adjust with a suitable trim tool or a small screwdriver. Turn clockwise for increased gain. Take care to ensure the stereo inputs remain in balance. The trim range is ±6dB.

Reference In **3 pin XLR female**

Reference Out **3 pin XLR male**

Reference In is an AES/EBU reference input for synchronising the unit to a Master Clock. Reference Out is an unbuffered loop through, directly coupled to it, for use in a reference daisy chain. A terminating resistor may be turned on or off, using the menu (see **Ref In** command, page 23), if several units are to be daisy chained with the same word clock.

In addition, under the control of the **ADC/Data** button, the Reference In connector can be used as a data input. In this mode, it takes data from the input instead of from the internal ADC, and allows all the formatting and DSP functions (such as noise shaping and word length control) to be applied to input data. See page 14.

AES1, 2, 3 & 4 Digital Outputs **3 pin XLR male (4 off)**

Four AES/EBU outputs which may be used independently or in groups of two or four. They are used for the various PCM formats, including normal and double speed and two and four wire, and also for some DSD formats.

SDIF/DSD CH1, CH2 Data **BNC (2 off)**

These BNC connectors can be both outputs and inputs. In normal operation they are outputs for SDIF-2 encoded PCM, or for SDIF-2 and SDIF-3 encoded DSD. They are both TTL level signals for a 75 ohm line. They can be set to TTL level AES3 coded signals, using the menu (see the **BNC O** command, page 22).

In addition, they can be used for data input, for re-formatting DSD data, under the control of the **ADC/Data** button (see page 14)

SDIF/DSD Clk In **BNC**

SDIF/DSD Clk Out **BNC**

This pair take in and give out Word Clock, and can be set to Bit Clock for DSD. The functions are set by the menu. Clock In is terminated and Clock Out is regenerated internally, so these lines can be used for daisy chaining many units together, without loading problems. See **Figure 18** and **Figure 19** for the time alignment of these signals.

Remote In & Out **9 pin D type male (2 off)**

If the Windows™ Remote software is in use, connecting Remote In to a com port (RS-232 port) on a PC running the Remote Control program allows the unit to be controlled by the PC. Remote Out may be connected to another suitably equipped *dCS* unit, allowing several units to controlled by the same PC with one RS-232 daisy chain. In addition, the unit may be software upgraded without removing the lid by downloading new software via the Remote In port – see **Installing New Software** on page 71.

Connect up Remote ports using a 9-way screened cable, fitted with 9-way 'D'-type connectors at each end, wired pin 1 to pin 1, pin 2 to pin 2, etc. The same type of cable can be used unit to units as com port to first unit. Suitable cables are available from *dCS*.

Mains Supply **3 pin IEC (CEE22)**

Switched, fused and filtered IEC mains connector.

Additional Information

As well as connectors, the rear panel displays the following information about the unit, near the mains supply connector:

Mains Voltage The actual voltage setting supplied.
Model Number *dCS 904*
Manufacturers Name and Country of origin (*dCS* Ltd, UK)

Serial Number

The underside of the unit will have a label on that contains a number such as 904 4B1 6B2 2A1 3A2 12345. This is the serial number, but it also contains vital configuration information. We will need this number (all of it) to give you support over the phone, or to ship you software updates.

Front Panel

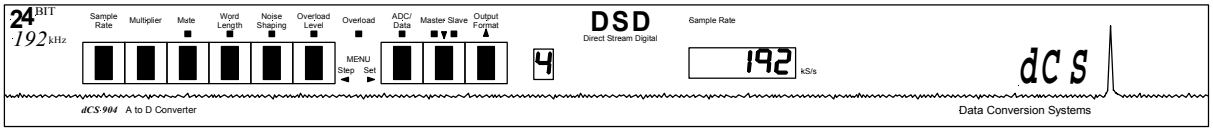


Figure 2 – Front Panel

The *dCS 904* uses a combination of front panel buttons for frequently changed functions and a step through menu for features you might set and forget.

Sample Rate

Multiplier

The 2 buttons on the left side of the front panel select the sample rate. Press the **Sample Rate** button repeatedly to cycle through the sample rates in the order:

192 ... 176.4 ... 96 ... 88.2 ... 48 ... 44.1 ... 32 ... 192 ... etc.

To step through more quickly, press the **Multiplier** button repeatedly to cycle through in one of the following sequences, depending on the starting sample rate:

48 ... 96 ... 192 ... 48 ... 96 ... 192 ... etc.
44.1 ... 88.2 ... 176.4 ... 44.1 ... 88.2 ... 176.4 ... etc.

To change sample rates quickly, use the two buttons together. For example, to change from 176.4 kS/s to 192 kS/s press **Sample Rate** once then **Multiplier** once. Do not press the buttons too fast as a delay is built in to the software. The sample rate selected is shown on the LED display in the centre of the panel.

Mute

The **Mute** button forces a mute, in addition to the automatic ones. The digital outputs are automatically muted at power up and when the sample rate is changed or the unit is locking to a reference source. A forced mute is indicated by the mute LED (above the mute switch) lighting up. In normal use, pressing the **Mute** button mutes the digital outputs and lights the mute LED. Pressing the Mute button again unmutes the ADC, as long as no automatic mute is being applied.

Word Length

Noise Shaping

Menu Back

The AES/EBU format accommodates data up to 24 bits. If a shorter word is needed and the extra bits are just ignored, the result is typical “digital” sound due to the abrupt chopping off of the low level signal information.

To avoid this, the *dCS 904* allows proper truncation of the data and uses Noise Shaping to maintain low level performance. See the section on “**Word Length Reduction**” on page 64 for some background on this. If you do use word length truncation, make sure that Noise Shaping is not set to OFF without realising it.

Pressing the **Word Length** button repeatedly cycles the word length through the sequence:

24, 23, 22, 21, 20, 19, 18, 17, 16, 24, etc.

The Word Length is briefly shown on the main display, and if a setting other than the maximum is set, the word length LED (above the button) lights.

Noise Shaping is a technique which improves the noise performance of the ADC in the audio band by moving the quantisation noise energy (introduced by reducing the word length) from one part of the spectrum to another. It keeps it out of the middle of the band, where the ear is most sensitive, and places it at the top end or ultrasonic region, where the ear is less sensitive or insensitive. See section **"Word Length Reduction"** on page 64 for more background.

Pressing the **Noise Shaping** button repeatedly cycles the unit through 5 noise Shaping characteristics. The characteristic is shown briefly on the main display.

Auto	Unit sets noise shaping automatically, depending on word length: 24 bits – no noise shaping 20 to 23 bits – 1st order noise shaping 16 to 19 bits – 3rd order noise shaping
Off	No noise shaping
1st	1st order noise shaping
3rd	3rd order noise shaping
9th	9th order noise shaping

The noise shaping LED (above the button) lights when the setting is other than Auto.

For Menu operation as the **Back** button, see the section **"The Software – the Menu"** on page 18.

Overload Level Menu Step

The **Overload Level** button is dual function – on its own (**blue** type on the front panel) it sets the level at which overloads are detected by the unit. With the other menu buttons (**white** type on the front panel) it is the menu **Step** button.

Overload detection is normally set to full scale. The detection level may be reduced in 0.1dB steps down to -3dB0 by pressing the **Overload Level** button repeatedly or holding it down. The set level is shown on the display for a few seconds. The overload level LED (above the button) lights when the setting is other than full scale (0.0dB0).

For Menu operation as the **Step** button, see the section "**The Software – the Menu"** on page 18.

Overload Indicator (Overload LED)

This overload LED lights for a few seconds when the set overload level is exceeded by a signal peak. The detection circuitry monitors both input and digital filtering circuitry for overload conditions. The analogue input sensitivity trims mounted on the rear panel should be set so that the overload indicator does not light on signal peaks.

The overload indication given by the ***dCS 904*** is comprehensive. The detection circuitry monitoring the digital filter does not simply check the final output word but all the data from which the output word is formed. If any of these overload (this may not be apparent from the output data), an overload is flagged.

The filter itself has sufficient numerical accuracy that if the input data is not overloaded, the filter computations cannot generate an overload - only a raw data overload can cause an error. The overload indication is thus much more accurate than any external meter based indication - for this reason it is stored in the AES/EBU validity bit for later reference.

ADC/Data **Menu Set**

The **ADC/Data** button is dual function – on its own (**blue** type on the front panel) it sets the input mode (analogue or digital). With the other menu buttons (**white** type on the front panel) it is the menu **Set** button.

As an input mode switch, it switches between the analogue inputs (ADC mode) or a digital input on the AES Reference input (Data mode).

Data mode routes the digital input through to the outputs, and makes noise shaping, word length reduction and some reformatting available to it. For normal operation, this is set to ADC (LED off). In Data mode, the ADC/Data LED lights and the data stream on the AES Reference Input is output on the AES1-4 outputs. If the Reference Input sample rate is 88.2 or 96kS/s and the Output Format is Dual AES, the input will be converted to Dual AES on AES1 & 2 and AES3 & 4.

Data mode also affects the SDIF connectors (BNCs) in any DSD mode. The data lines (two of the four connectors) become inputs, and DSD fed into these is packed and re-formatted into the output format selected. No DSP is carried out.

For Menu operation as the **Set** button, see the section "**The Software – the Menu"** on page 18.

Master/Slave **Menu Down**

The **Master/Slave** button is dual function – on its own (**blue** type on the front panel) it sets the clocking mode (master or slave). With the other menu buttons (**white** type on the front panel) it is the menu **Down** button.

In Master mode, the calibrated voltage controlled crystal oscillators (VCXOs) inside the unit generate an accurate sample rate. The LED labelled Master will be lit to indicate this. If a Master Clock is available, this may be connected to the Reference In connector (for AES/EBU reference) or the 75R In connector (for SDIF-2 Word Clock). To slave the unit to the Master Clock, press the **Master/Slave** button. The unit will attempt to lock to the Reference - this will take a few seconds. If lock is achieved, the Slave LED will light up brightly and the Master LED will turn off. To return to Master mode, press the **Master/Slave** button again.

If both AES Reference and Word Clock are connected, pressing the **Master/Slave** button cycles through the sequence:

Master ... AES Reference ... Word Clock ... Master ... etc.

If the active reference source is lost, the unit will select the next option in the sequence.

If the Auto-Slave option in the "Function Menu" is turned On the unit will automatically slave when a suitable reference is connected. If both AES Reference and Word Clock are connected, AES Reference takes priority. Word Clock may be selected by pressing the **Master/Slave** button – it moves down the priority list.

Once slaved, the unit can internally multiply the reference input sample rate by 2 or 4, if required, by pressing the **Multiplier** button. The Master Clock must be set to a suitable sample rate:

Master Clock Sample Rate (kS/s)	*dCS 904* Sample Rate (kS/s)
32	32
44.1	44.1 or 88.2 or 176.4
48	48 or 96 or 192
88.2	88.2 or 176.4
96	96 or 192

Table 1 Reference Clock and Sample Rates

For Menu operation as the Menu **Down** button, see the section "**The Software – the Menu"** on page 18.

Output Format Menu Up

The **Output Format** button is dual function – on its own (**blue** type on the front panel) it sets the output format (single, dual, quad AES, etc). With the other menu buttons (**white** type on the front panel) it is the **Up** button.

Pressing the **Output Format** button repeatedly causes the output format to cycle through the allowed options from the sequence:

Single AES ... Dual AES ... Quad AES ... Single AES ... etc.

If any format is not available at that sample rate, it is skipped from the sequence.

Mode Display

The single digit LED mode display to the right of the Format button shows the output format:

Display	Output Format
0	DSD mode, AES outputs turned off
1	Single AES
2	Dual AES
3	P3D mode
4	Quad AES or 4 wire DSD

Table 2 Output Data format indication, higher sample rates

When the Output Format is selected, the main display briefly shows the format code:

A1	for Single AES, Standard speed encoding
b1	for Single AES, Double speed encoding
b2	for Dual AES, Standard speed encoding
C2	for Dual AES, Double speed encoding
C4	for Quad AES, Standard speed encoding

If an invalid combination is selected (e.g. Single AES at 192kS/s), the invalid combination will flash (e.g. C1) then be replaced by the nearest available combination.

In Single AES mode, the same data stream is available on all four AES outputs. In Dual AES mode, two sets of identical data streams are available on AES1 & 2 and AES3 & 4 outputs. In Quad AES mode, the data stream uses all four AES outputs.

In DSD mode, data in the AES outputs can be turned off (leaving the unit just outputting an AES clock). This is controlled by the menu item **DSD 4** (or **AES O** for P3D optioned units). See page 20.

dCS equipment encodes messaging into the various data streams to enable receiving equipment to tell what is going on, and to decide which wire is which, in the unlikely event of user wiring errors. Not all equipment from other manufacturers does this, so:

IMPORTANT! *Take extra care when connecting Quad AES as it is very easy to connect the wires in the wrong order. If this is not detected, it may result in badly aliased mono signals being recorded. Numbering each connector is a sensible precaution.*

For Menu operation as the **Up** button, see the section "**The Software – the Menu"** on page 18.

Sample Rate Display

The main LED display generally shows the sample rate, in kS/s, or the mode (DSD). When other parameters are set, it briefly shows the new setting (word length, noise shaping, etc) then reverts to its normal display. In the case of an error condition, it will display an error message.

If the unit is being slaved, the display also indicates which input connector it is slaved to.

xxx	The sample rate, in kS/s (32, 44.1, 48, 88.2, 86, 176.4, or 192).
- xxx	Slaved to the BNC input (typically, word clock).
-- xxx	Slaved to AES Reference in.

There are also some temporary displays that show what the unit is doing during its locking phase:

d xxx	Temporary display during locking – the unit has detected the base reference sample rate and is attempting to lock to it.
. xxx	Temporary display during locking – the unit is lining up word clock out to word clock in.

Important error messages are given below – a full list is given in the section **Error Codes and Messages** on page 74.

BadFs	The clock source is not in pull in range, or is poorly formatted. The unit cannot lock to it.
Err.xy	An error has been detected. Please refer to **"Internal Device Error Codes"** on page 74 for more specific details on error codes.
Hot	The unit is overheating, probably due to inadequate ventilation. Please check positioning and cooling.
Ouch	The "Hot" warning has been ignored and the unit is getting so hot damage may follow.
(blank)	If the display is completely blank for any significant period, try switching off for 10 seconds then switching on again. If this does not solve the problem, contact your distributor or *dCS*.

The display is also used for **Menu** options.

THE SOFTWARE – THE MENU

Overview

The *dCS 904* has many other functions that either need to be accessed only occasionally, or are informative in nature. These functions can be accessed either by the Remote software, running on a PC and connected to the unit by an RS-232 link - or (in most cases) by the **Menu**. If a function is set by the menu or the Remote, the unit remembers it, and it will be set this way for ever (or until you set it to something different). You can customise your unit in this way. Information only items are displayed for a time, then the display reverts to normal.

Menu buttons are indicated by white text on the front panel. There are for:

Step	otherwise **Overload Level**
Set	otherwise **ADC/Data**
Down	otherwise **Master/Slave**
Up	otherwise **Output Format**
Back	otherwise **Noise Shaping**

Entering the Menu

The Menu is entered by holding down the **Step** and then pressing the **Set** button once. The display will show:

Func

You are now in the menu, and the menu buttons now have their alternate meanings.

Moving through the Menu

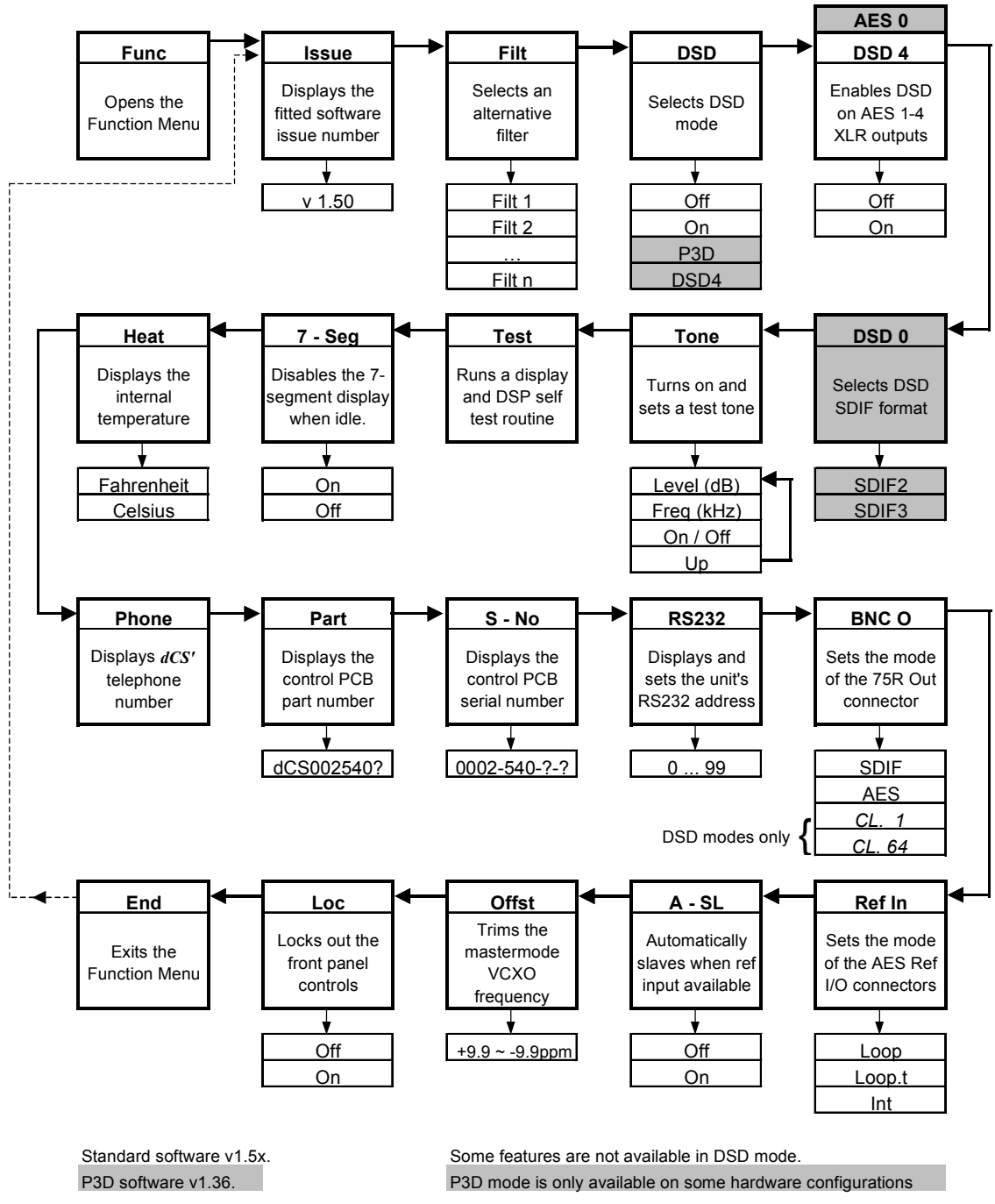
Press the **Step** button again to step through the Menu items listed below. When you reach the required item, press the **Set** button once to display the current setting, and press again to change its setting. This either toggles the previous state, or causes an information function to read out, or enters a lower level (as in the Tone generator, for example). If you have entered a lower level, pressing **Step** steps through its options. When you reach the one you want, press **Set** and then use the **Up** or **Down** buttons to increase or decrease a value (such as Level or Frequency on the Tone generator).

If no changes are made in 4 seconds, the unit exits the Menu. When one item has been set, press the **Step** button again if you wish to continue cycling through the Menu.

There is a knack in doing this easily – once it has been gained, it becomes very easy to use the functions it accesses.

The Menu Sequence

To access the Function Menu, hold down the **Menu Step** button and press the **Menu Set** button.
To step through the Menu items, press the **Menu Step** button repeatedly.
To step back, press the **Noise Shaping** button.
To select an item or one of its options, press the **Menu Set** button.
To exit the Function Menu, either select the **End** item or wait five seconds.



Standard software v1.5x.
P3D software v1.36.

Some features are not available in DSD mode.
P3D mode is only available on some hardware configurations

Figure 3 – Menu Sequence

Menu Items

Issue

Displays the software issue when **Set** is pressed.

Filt

Selects one of several anti-alias filter responses. The filters should be evaluated by ear. Filt1 gives the sharpest cut off, just below half the sampling frequency. This is the normal setting. Filt2, Filt3, Filt4 give progressively more relaxed responses, degrading the alias performance but sharpening the impulse response. This affects the stereo or multi-channel image. Different filters may be appropriate for different material.

DSD

Turns on DSD mode and in P3D units cycles through the DSD format options available (Off, On, P3D, DSD 4). When on, the unit displays "dSd". The mode takes about 15 seconds to load, during which time the menu cannot be used. This mode is so different from PCM that most of the PCM related front panel buttons are no longer appropriate. DSD is output on the BNC connectors, and the following other changes occur:

- XLR outputs are clock only unless DSD 4 (or AES O on P3D units) is on (see below).
- the BNC O options change to CL 1 (bit clock) or CL 64 (word clock)
- **ADC/Data** allows the SDIF connectors to be turned into inputs, so that DSD data can be fed in and formatted
- **Sample Rate**, **Multiplier**, **Mute**, **Word Length**, **Noise Shaping**, **Overload Level**, and **Output Format** buttons do not work
- the Tone Generator does not work

The **Master/Slave** button works and the Auto Slave function (see later in Menu Items) works. Filt works – there are 7 filter options in DSD mode. See the section on "**DSD**" starting on page 32 for more details – they trade-off in-band and out-of-band noise.

DSD 4 (or AES O for P3D units)

This function controls the use of the XLR connectors on DSD mode. There are two options, whose behaviour depends on whether the unit is a P3D unit or not.

Standard (non P3D) units:

Off	The XLRs carry AES clock only
On	The XLRs carry DSD data packed into 4 AES3 links for storage on 16 bit 8 channel 44.1 kS/s PCM machines (non P3D units)

P3D units:

Off	XLRs carry AES clock only

On	XLRs carry either DSD 4 format or P3D format, as set by he DSD menu item. In P3D format, where DSD to be packed into 3 AES3 links, the 4th XLR output carries a PCM encoded signal for metering purposes, to allow DSD to be recorded on existing 8 track 24 bit PCM recording machines, at a lower than normal level

This XLR control function is separate from DSD mode for safety reasons. Because DSD into a PCM device can cause full scale noise, with a very high high frequency content that can damage speakers, this feature has to be explicitly turned on.

If it is turned on, and DSD mode is turned on, the unit outputs DSD packed into AES3 data streams in the appropriate manner. Contact ***dCS*** for further details

If DSD is packed into AES3 links (DSD 4 or P3D), the ***dCS 904*** sets the Non Audio flag in the AES3 message, so that a DAC further downstream will mute if it cannot accept the format, but beware:

IMPORTANT! *if the Non Audio flag is stripped by the recorder, a DAC could accept DSD data as AES3 PCM and will output potentially damaging full scale noise.*

DSD O

This page selects the output format of the SDIF connectors – SDIF-2 or SDIF-3. SDIF-3 is only valid for DSD:

SDIF2	The BNCs output SDIF-2 formatted DSD in ADC mode
On	The BNCs output SDIF-3 (embedded clock) in ADC mode.

Definitions of these formats are available from the SONY Corporation.

Tone

This accesses a test generator, whose level and frequency can be adjusted. Pressing Set enters a submenu, which accesses the following functions:

Level	The output level, in dB0. It can be changed in 0.1dB steps using the **Up** and **Down** buttons.
Freq	The output frequency, in kHz. It can be changed below 1 kHz in 10 Hz steps, or above 1 kHz in 100 Hz steps by using the **Up** and **Down** buttons.
On/Off	Toggles whether the generator is on or off.
Up	Allows the menu to be re-entered to set other functions. Alternatively, if left, the menu will just time out keeping the last settings.

At power up, the generator is set to Off, 1 kHz and –18dB0 as a safety measure. When in use, if the generator is turned Off, the unit remembers the last frequency and level setting.

The generator frequency can be set to much finer (32 bit) resolution using the RS-232 control. See section **"RS-232 Remote Control Interface"** on page 53 for more details.

Test

Runs a display and DSP self test routine. When successfully completed, the unit displays Pass and returns to normal operation. Otherwise an error message Err.xy is displayed – please refer to **"Error Codes and Messages"** on page 74 for more specific information.

7-Seg

Disables the 7 segment LED display. When set to Off, the display turns off 4 seconds after the last button press. A dot in the lower right hand corner of the display remains lit to indicate that the display has been deliberately blanked. The display springs back into life (temporarily) if the menu is used subsequently. Error or warning messages are displayed regardless of this setting.

Heat

Displays the internal temperature of the unit, measured near the internal VCXOs. Press **Set** to toggle between Fahrenheit and Celsius. See section **"Operating Conditions"** on page 63

Phone

dCS telephone number scrolls across the display

Part

The control board part number (version) scrolls along the display.

S-No

The control board serial number scrolls along the display. You will need something to write this on, if you call us for help.

RS232

Displays - and allows access to – the unit's RS-232 identity code (an address between 0 and 99). This is used by the remote control software, to send specific messages to specific units. Use **Up** and **Down** to change this address if you are operating several units in a multichannel set up.

IMPORTANT! *Each unit in the daisy chain MUST be set to a different RS-232 address.*

BNC O

Sets the format of the 75 ohm BNC outputs, and changes depending on whether the unit is in PCM or DSD modes. In PCM mode, the options are

AES	Sends out AES3 coded data, but at TTL levels, at up to 96 kS/s on the Clk Out connector.
SDIF	Sends out SDIF-2 encoded data, with a word clock on the Clk Out connector.

In DSD mode, the options are changed to:

CL 1	Sends out DSD data along with a bit clock on the Clk Out connector.
CL64	Sends out DSD data along with a word clock on the Clk Out connector.

Ref In

Sets the mode of the AES Reference In/Out connectors. The options are:

Loop	Loops the input through to the output, with no termination resistor (termination is then about 1kohm, so several units can be daisy chained).
Loop.t	As above, but terminates the input. Use at the end of a daisy chain.
Int	The output (and input in parallel – beware!) is internally driven, with the same signal as AES 1.

A-SL

Turns Auto-slaving On or Off. When set to On, connecting an AES/EBU reference or a word clock in causes the unit to slave and lights the Slave LED. If both are present, the unit picks the highest priority one (AES/EBU) unless the **Master/Slave** button is used to move down the priority list. When set to Off, the unit does not react when a reference is connected.

Offst

Trims the appropriate VCXO frequency in master mode, by up to ±9.9ppm in 0.1ppm steps. Use the **Up** and **Down** buttons to change this setting, hold a button down to accelerate the change. The trim is remembered.

Loc

Panel Lock, normally Off. Set to On to prevent unauthorised changes using buttons. The menu has to be accessed to turn the lock off again.

End

Exits the menu.

TYPICAL APPLICATIONS

Using a dCS 904 to output DSD

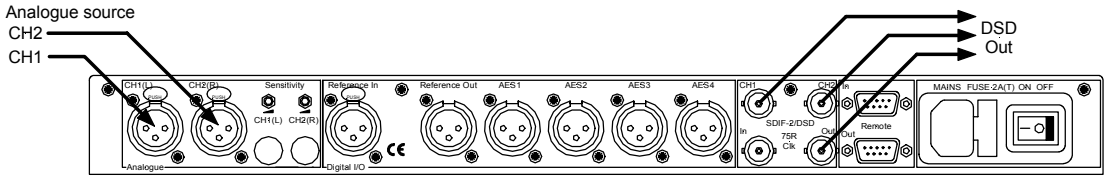


Figure 4 – DSD output configuration

do this: Set DSD in the menu to On.

do this: Most likely (check your other equipment) you will need word clock. Make sure BNC O is set to CL64.

do this: Select your filter.

P3D units only:

do this: Set DSD to P3D or DSD4 instead of On as required

Using a Master Clock to Sync a *dCS 904*

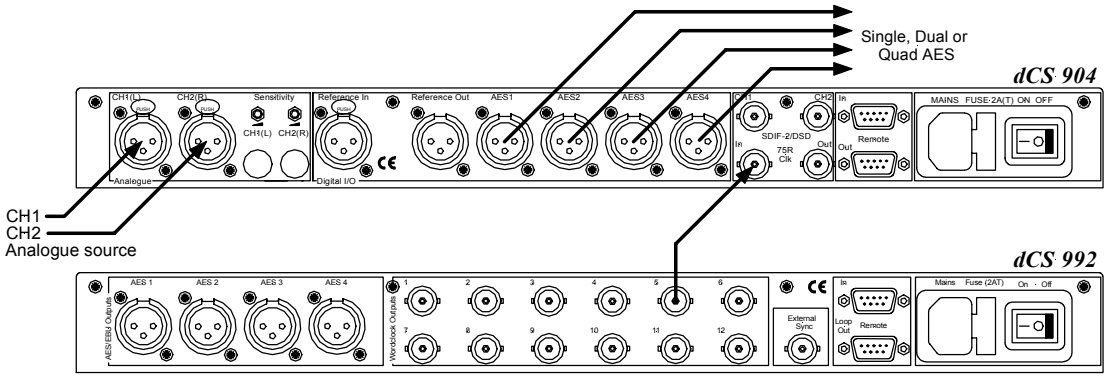


Figure 5 – Syncing a *dCS 904* to a Master Clock

do this: Make sure A-SL (Autoslave) is On and DSD is set to Off

Storing DSD on an 8 track 16/44.1 PCM Recorder

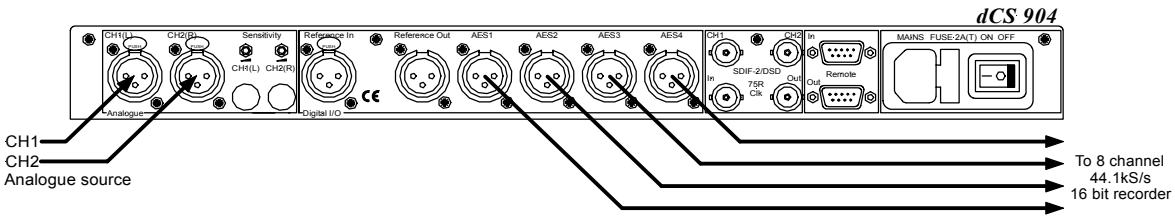


Figure 6 – Storing 2 channel DSD on an 8 track 16 bit 44.1 kS/s PCM recorder

do this: Set DSD to On and DSD 4 to On

P3D units only:

do this: Set DSD to DSD 4, set AES O to On.

Six Channel PCM Set Up

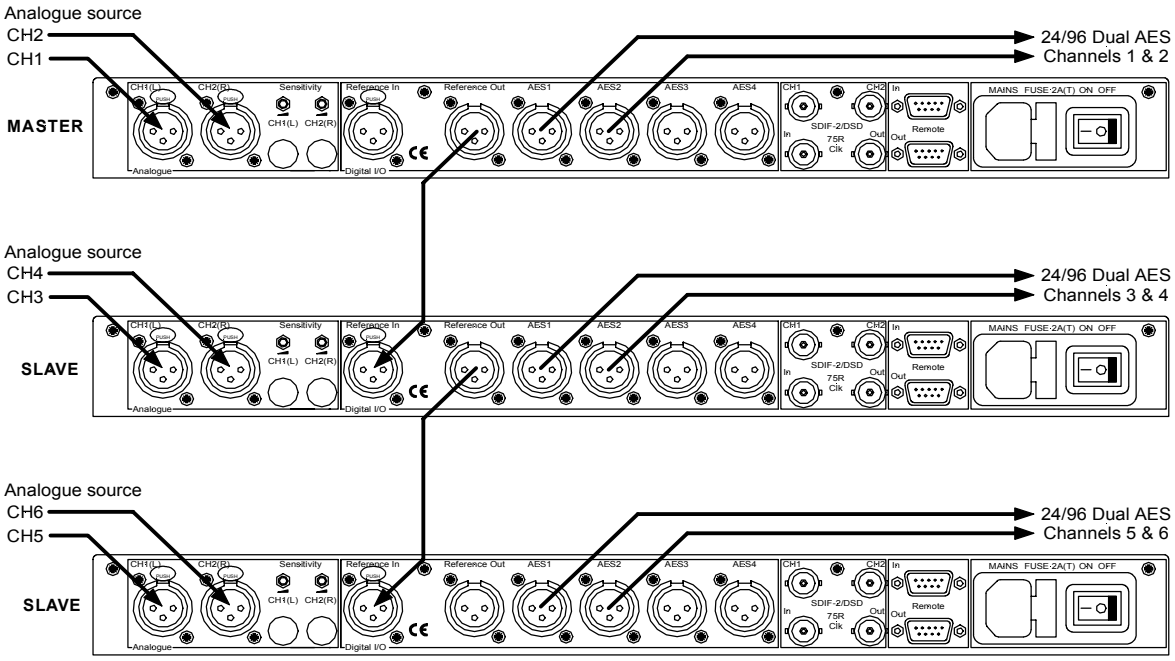


Figure 7 – Six channel set up without a Master Clock

The top *dCS 904* needs to have its Ref In option set to Int. The middle one should be set to Loop, and the bottom one should be set to Loop.t. The units self align quite accurately (see **"Sample Alignment"** on page 37 onwards). Alternatively, word clock may be used as the syncing method, with no special set ups.

Storing 6 channel DSD on a 24 track 16/44.1 PCM Recorder

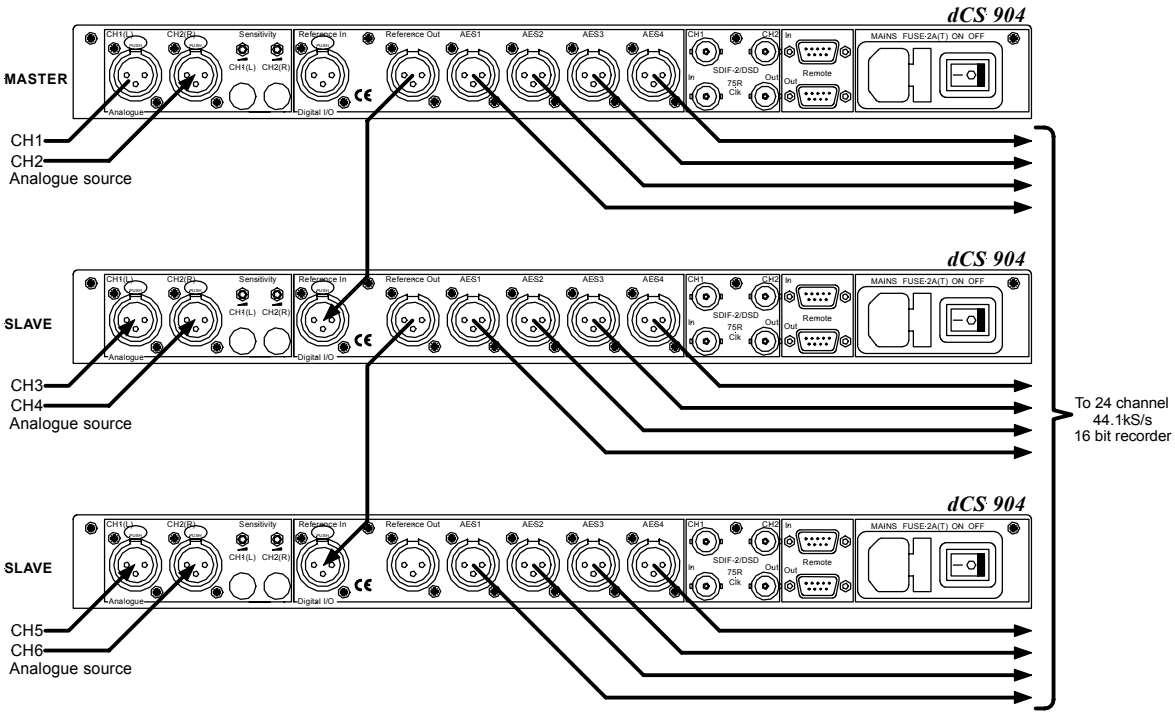


Figure 8 – Six channel DSD recording on a 24 track 16/44.1 kS/s recorder

Make sure DSD 4 is turned on, from the menu. The top ***dCS 904*** needs to have its Ref In option set to Int. The middle one should be set to Loop, and the bottom one should be set to Loop.t The units self align quite accurately (see **"Sample Alignment"** on page 37 onwards). Alternatively, word clock may be used as the syncing method, with no special set ups.

P3D option only:

do this: Set DSD to DSD 4, set AES O to On

Operating Several Units on One Remote Chain

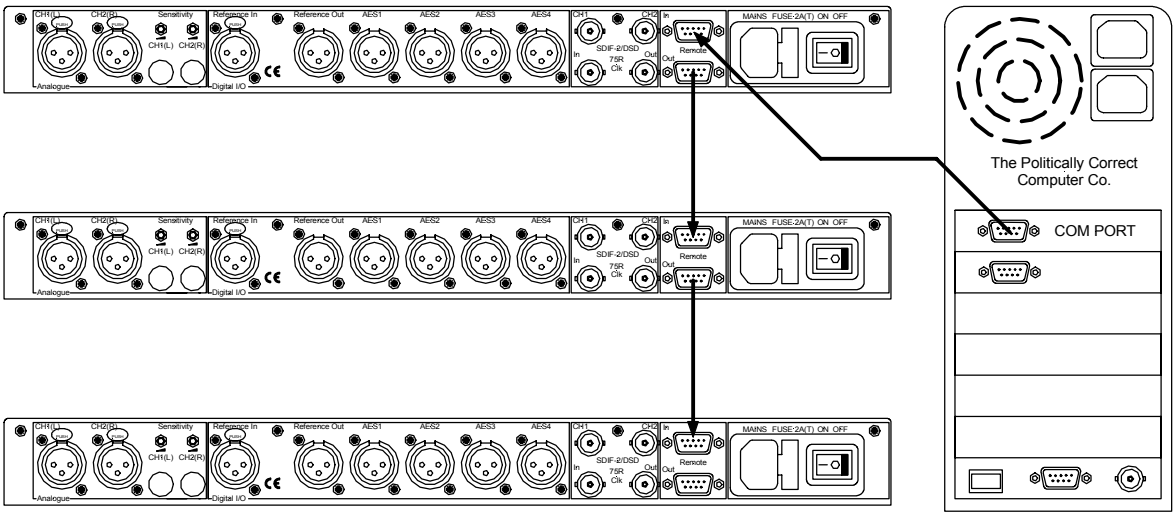


Figure 9 – Multi-unit Remote Daisy Chain

The PC can control several units (up to about 5) on each daisy chain. To make them individually addressable, each unit needs its RS-232 address to be different. They can then be identified, and grouped, in the remote window.

See **"Remote In & Out"** on page 11 for cable details.

8 Channel P3D DSD Set Up with Monitoring

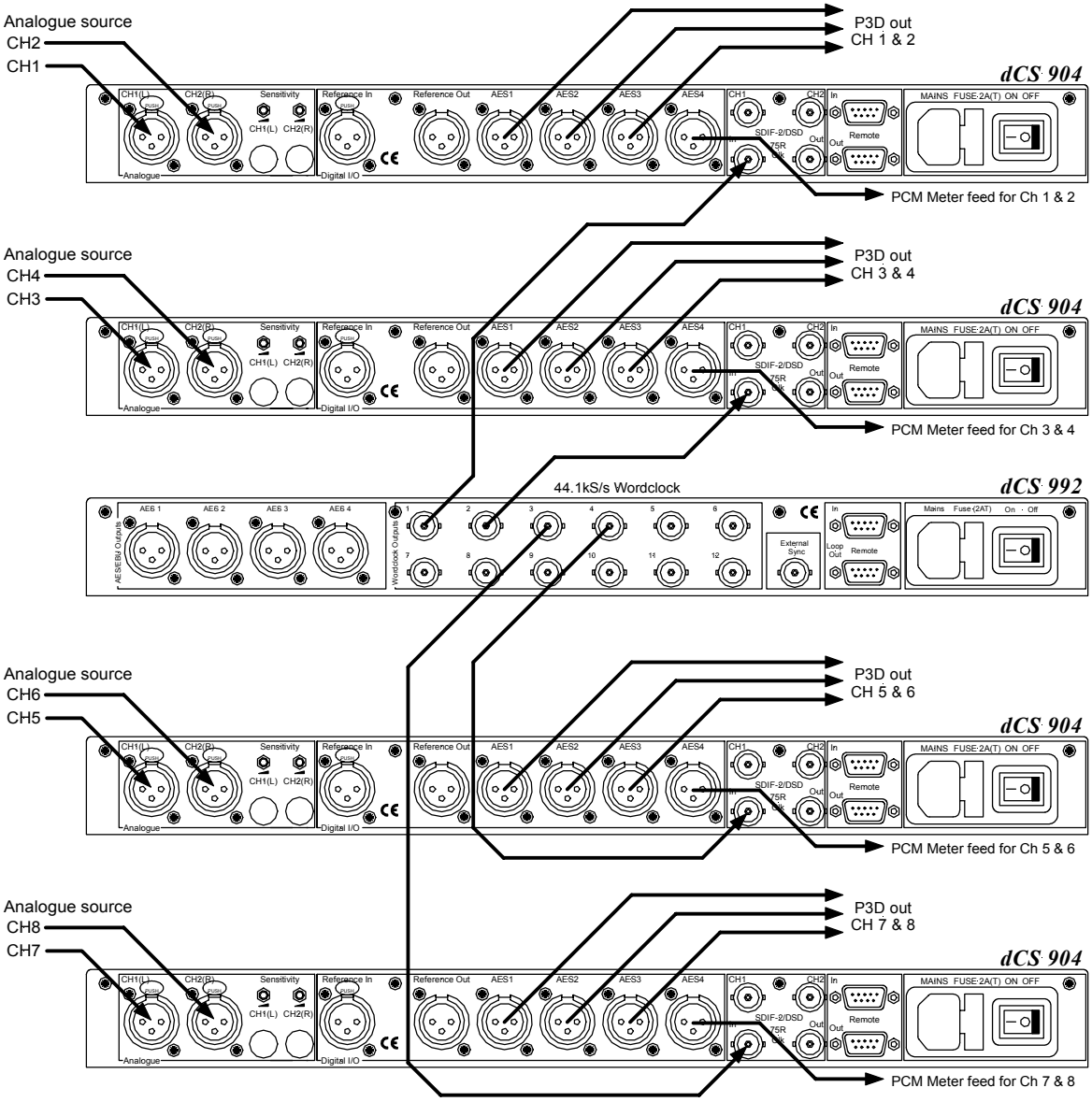


Figure 10 – 8 Channel P3D DSD Set Up

Four P3D capable ***dCS 904*** units and a Master Clock can be used as above to give 8 channel DSD with additional simultaneous AES3 PCM outputs to give level monitoring on PCM equipment.

dCS 904 TECHNICAL INFORMATION

Anti Alias Filtering

The ***dCS 904*** offers a choice of 4 anti-alias filters on most sample rates. These filters affect the ultrasonic part of the spectrum - 20 kHz upwards.

The unit is an ADC, with an output data rate set by the interface standard used. The bandwidth of the input stages and oversampling converter used is high, and so any signals that that are in the input signal, up to a MHz or so, will be aliased[3] back into the output signal if they are not removed by filtering. The demands on this anti-alias filter can be quite severe at the lower ("normal") sample rates - it must pass signals in the audio band (0-20 kHz) unimpaired, but it must prevent aliasing about Fs/2. This can result in a very sharp filter, and it is an unavoidable mathematical result that sharp filters have a poor, ringing, transient response. One effect of the ringing is to spread the energy in a transient over a significant period of time (it can be up to 1 ms). This seems to affect the stereo image that the ear would otherwise form.

One can trade off filter roll off, and energy smear - more relaxed roll off gives less energy smear, but it may allow some of the signals in the input to alias irrevocably into the output data. Once a signal has aliased, it cannot be corrected. However, as far as the ear is concerned, this may not matter. The ear can tell the frequency of a signal - up to a point. As the frequency rises, the accuracy with which the ear can tell what the frequency is decreases, and above a limit, all the ear can tell is that there is a signal, and it is above ... kHz. It can tell no more. So - it may be that some degree of aliasing is acceptable to the ear.

The filters that we have included give increasingly good energy smear performance, and consequently have increasingly relaxed roll off. **FiLT1** gives the sharpest roll off, with no aliasing, but the worst energy smear. Then as the number increases the smear decreases, but the aliasing increases. Try them, to see which you prefer.

You may find that for different material, different filters are appropriate - and you may find that for different stages in the recording and mastering process, different filters are appropriate.

The ***dCS 904*** uses linear phase FIR filters to avoid the limit cycle problems that come with many IIR filters. Linear phase gives filters a symmetrical transient response before and after a transient ("pre-ringing"). The passband may or may not have a ripple[4], depending on the filter being used. The stop band is typically below –110 dB and can be as low as –130 dB.

[3] See, for example "Principles of Digital Audio", 3rd Edition, by Ken C Pohlmann (McGraw-Hill Inc, 1995)
[4] Filters always have some ripple. For "zero ripple" filters this is in the μdB to pdB region.

Clocking

The sample clock quality significantly determines the output performance of an ADC.

The highest quality clocks that are available are crystals, so we use these. In Master mode, the ***dCS 904*** uses one of two on-board voltage controlled crystal oscillators (VCXOs) as clock sources – one for 48 kS/s related outputs and one for 44.1 kS/s related outputs. When an external clock is applied for Slave operation, the internal VCXO is synchronised to this by a phase locked loop (PLL). The PLL is of a special narrow bandwidth type, that provides a high degree of "clock cleaning" - but even so, signal quality may degrade if particularly poor slave clocks are used. A consequence of the narrow bandwidth is that it takes quite a long time for the PLL to lock to a new clock frequency – of the order of 2 seconds. The PLL uses DSP assistance to keep this time acceptable.

Internal clock

Accuracy when shipped	± 10 ppm
Long Term Stability	± 10 ppm/year at room temp.
Temperature Stability	± 15 ppm over operating temperature range

The VCXO frequency can be trimmed by using the Offst function in the menu (see page 23)– each VCXO is independently adjustable

Synchronising to source

Pull in range	± 300 ppm about nominal frequency
Lock in time	<2 seconds for most situations

The PLL is very robust, and will lock to very poor signals if necessary. Data is decoded using a much wider band (faster) PLL, so AES3 type low frequency jitter on the input clock can be handled, and will be cleaned.

If you need to synchronise several items of digital equipment, we recommend using a ***dCS 992*** Master Clock.

DSD

DSD Overview

DSD is a single bit very high sample rate (2.822 MS/s) format, where the single bit words are heavily noise shaped to push noise energy above audio. The frequency response is very high (well above 100 kHz) although at these ultrsonic frequencies noise is also present.

The *dCS 904* offers a number of different DSD modulators – as Filter options. All the modulators in have the same signal frequency response. They differ in the way they shape the out of band Q noise, and in how far they suppress the in band Q noise. Filters 1 to 5 suppress Q noise at least 120 dB below the nominal 0dB DSD signal, which is one of the marketing specs for SACD.

Filter	Comments	SQNR (20 kHz, dB)	Stability	Description
1	High SQNR, high stability	126.14	$1.7*10^{10}$	Two complex zeros
2	High SQNR	127.23	$8.2*10^{8}$	Two complex zeros
3	High SQNR, very high stability	124.66	$1.5*10^{11}$	Two complex zeros
4	Extremely high stability	122.07	$3.0*10^{12}$	Two complex zeros
5	Reduced 100k noise	122.27	$7.1*10^{10}$	Two complex zeros
6	Single complex zero	110.78	$3.7*10^{11}$	Single complex zero
7	Real zeros	101.5	$2.0*10^{10}$	Real zeros only

Table 3 – DSD Filter Summary

Signal to Q Noise and SACD Specs

Although 120dB SNR over the 0-20 kHz band is a good target, it does not match the ears response that well. The F weighted curve is currently accepted as a good model for the ear, and we can use this to weight the noise produced by the various filter choices. Such a weighting is shown in Figure 14 on page 35. DSD gives very good performance using such a weighting (better than 23 bit pcm)

The figure shows that filter 6 and 7 give more F weighted Q noise suppression in the audio band than filters 1 to 5. Filter 6 gives around 20 dB more suppression than filters 1 to 5 under all circumstances and filter 7 gives 20 dB more suppression below 10 kHz.

SACD[5] specifies ultrasonic noise in two bands. These are specs informative specs E2 and E3, and filter performance for a number of specs including these are given below. The measurements given have been made using a Fourier Transform based method.

[5] Super Audio CD System Specifications, Part 2, Audio Specifications, available from Philips System Standards and Licensing, Licensing Support, Building SFF-8, PO Box 80002, 5600 JB Eindhoven, The Netherlands

Filter	Comments	SQNR (20 kHz, dB)	SQNR (F weighted dB)	E2 spec (dB)	E3 spec (dB)
1	High SQNR, high stability	126.14	-136.56	-25.98	-28.96
2	High SQNR	127.23	-138.76	-25.85	-28.95
3	High SQNR, very high stability	124.66	-134.38	-27.32	-30.49
4	Extremely high stability	122.07	-129.91	-25.54	-29.53
5	Reduced 100k noise	122.27	-130.14	-27.13	-31.99
6	Single complex zero	110.78	-151.02	-25.19	-23.55
7	Real zeros	101.5	-132.41	-25.29	-27.04
	SACD Spec			-20.00	-28.00

Table 4 – DSD Filter Performance

DSD Full Scale

The SACD standard sets 0 dB0 for programme material 6 dB below the peak to peak level one might expect a full scale sinewave to occupy. This ensures that artefacts that begin to occur at the limits of the DSD frequency range stay well away from the audio band, and is shown in Figure 11, on page 34. The dCS 904 complies with this standard. If the unit is set up for full scale PCM, and then switched to a DSD format, the levels will be correctly set to meet SACD standards.

DSD Mute

A DSD mute is unlike a PCM mute (which is 00000….), because with only two levels, there is not a single value that sets the output in the middle of the range. In all DSD formats except P3D, the dCS 904 outputs 010101010101…. as a DSD mute. For P3D it outputs 01101001 as a P3D DSD mute.

DSD Overload Behaviour

DSD is more benign than PCM under overload conditions. In the overload region, the performance gradually and gracefully degrades. The size of this region depends on the modulator used, but in general, a modulator with a higher stability will allow a larger overload region (see **Table 3 – DSD Filter Summary**). The overload region may be several dB. In the *dCS 904*, the signal level is digitally clamped about 1.5 dB above SACD 0dB level.

dCS modulators recover from overload rapidly

DSD Electrical and Data Structures

Electrically, for the SDIF-2 and SDIF-3 outputs, TTL levels are used. There is no framing or block structure, and each channel uses one BNC connector. The clock (word or bit clock) uses the third connector. See Figure 33 on page 52.

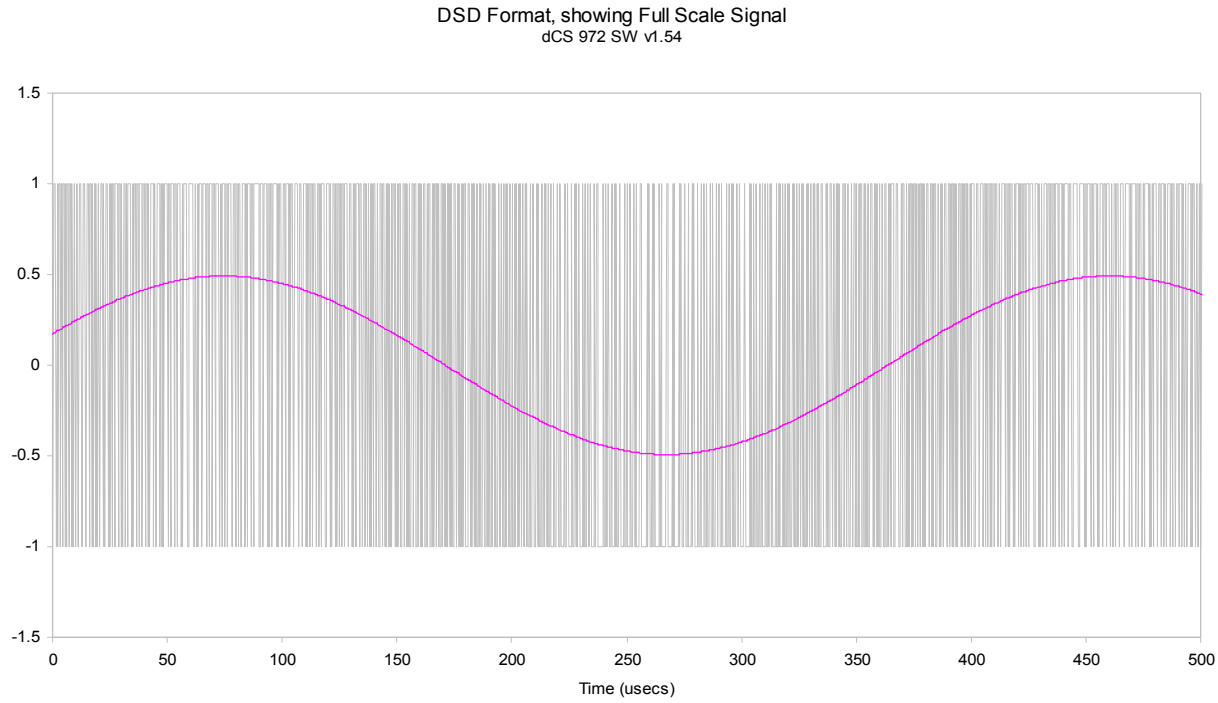


Figure 11 – DSD, showing DSD full scale

DSD has only two levels – printer artefacts make it look like more

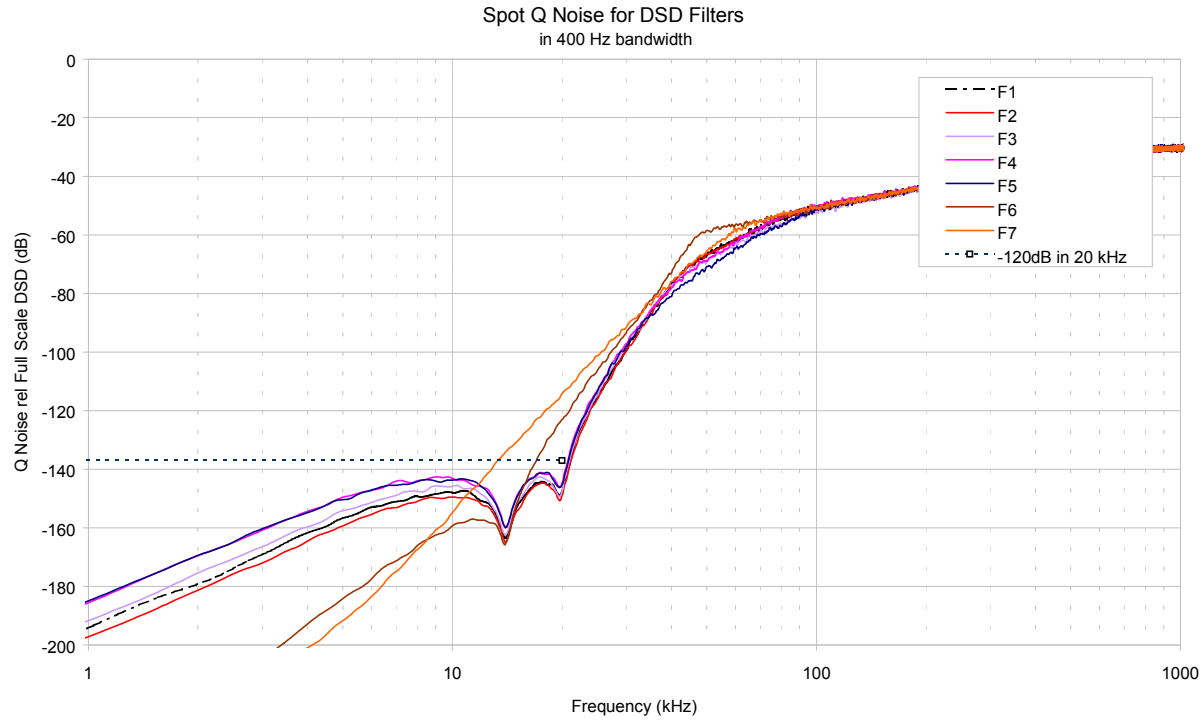


Figure 12 – DSD Output, Filter Responses (Spot Q Noise)

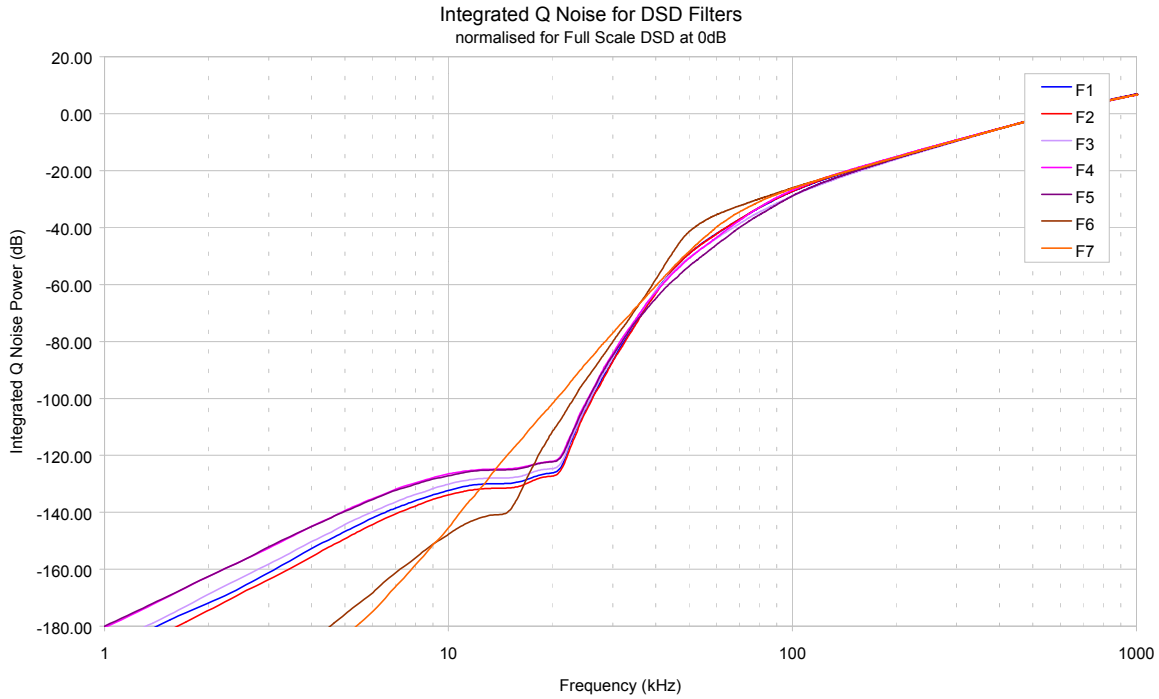


Figure 13 – DSD output, Filter responses (Integrated Q Noise)

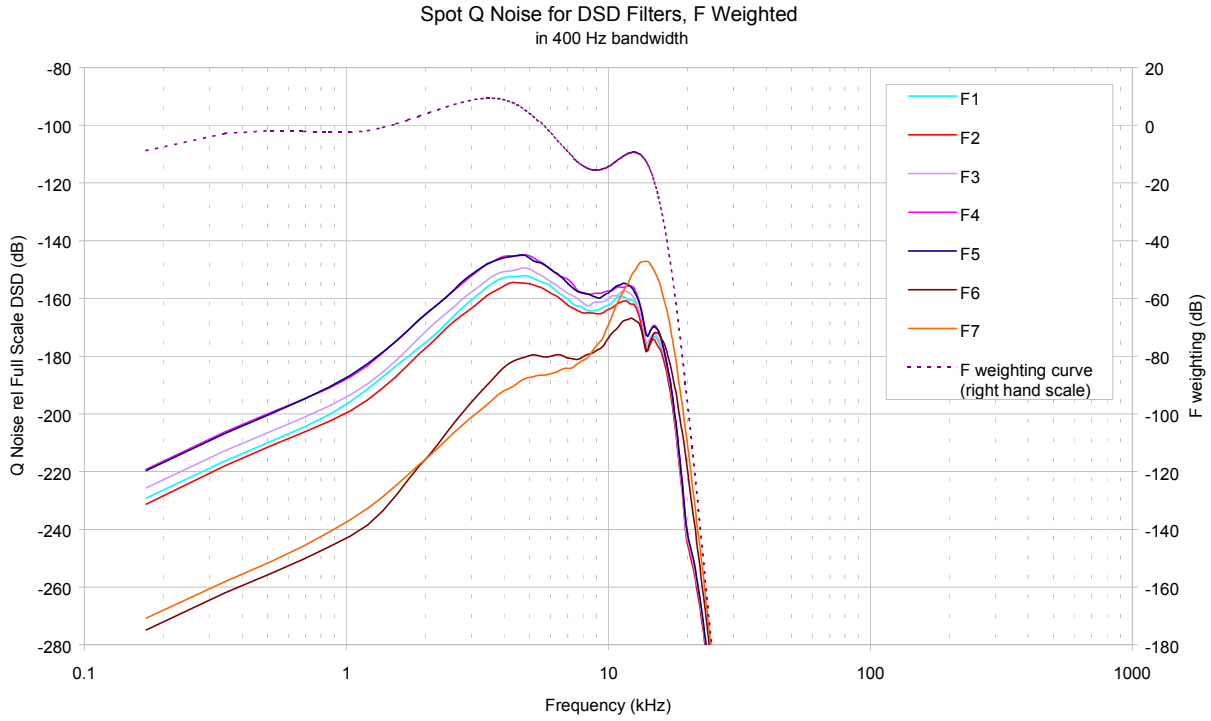


Figure 14 – DSD output, Filter responses (F weighted Spot Q Noise)

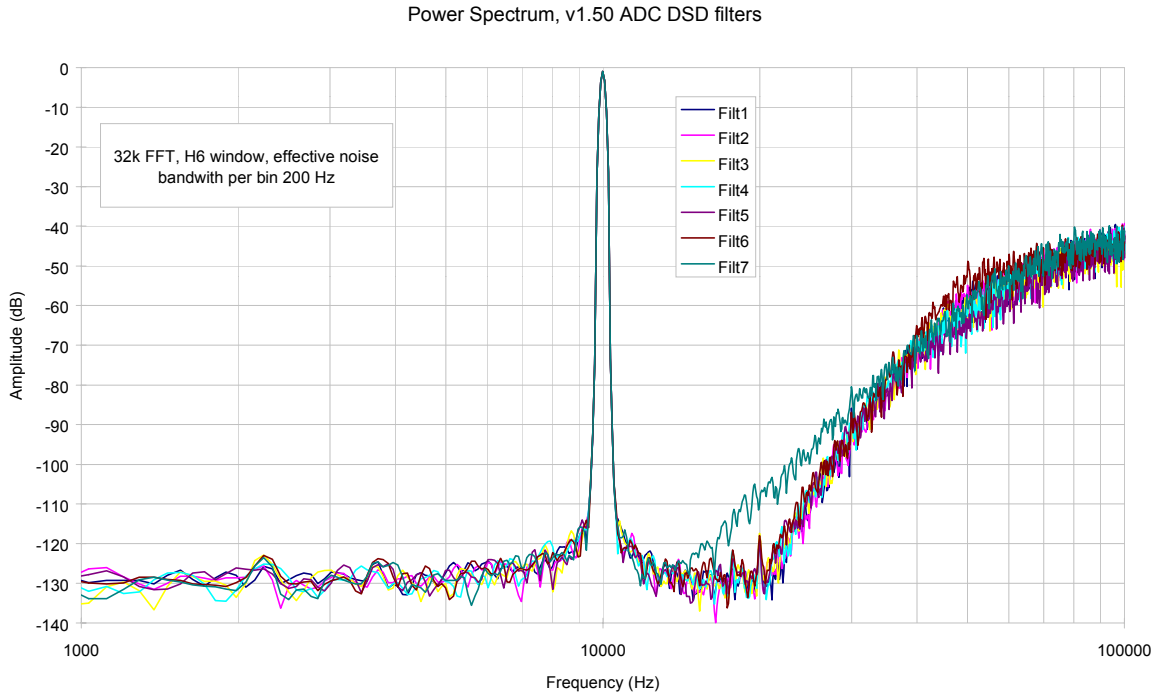


Figure 15 – DSD output, with analogue and Q spot noise

Sample Alignment

The ***dCS 904*** aligns samples such that word clock out aligns with AES3 samples out, the rising edge of word clock aligning with the start of the first illegal code in the X,Z subframe preamble and the falling edge aligning with the start of the Y subframe preamble. The scope shots below were taken in Master mode.

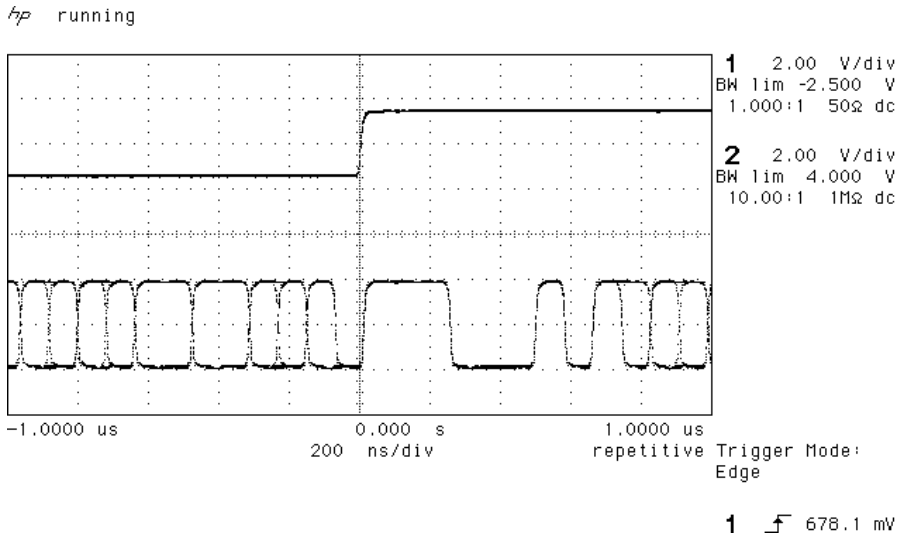


Figure 16 – Word Clock and AES3 outputs, 96 kS/s

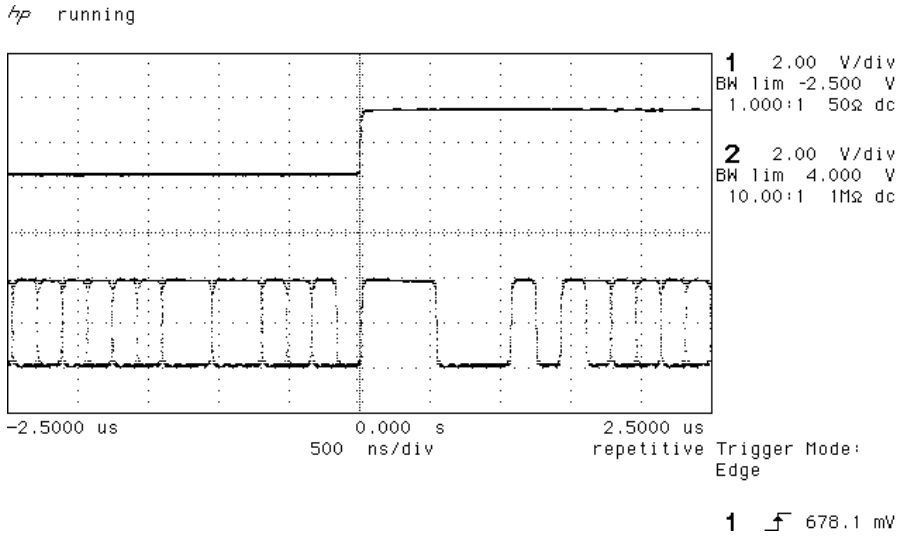


Figure 17 – Word Clock and AES3 outputs, 44.1 kS/s

When word clock in is used as a sync source, in and out are related as below. The lower waveform is the output, the upper one is the input. The misalignment is less than about 40 nsecs. The scope shots below were taken with the unit sync'd to Word clock in.

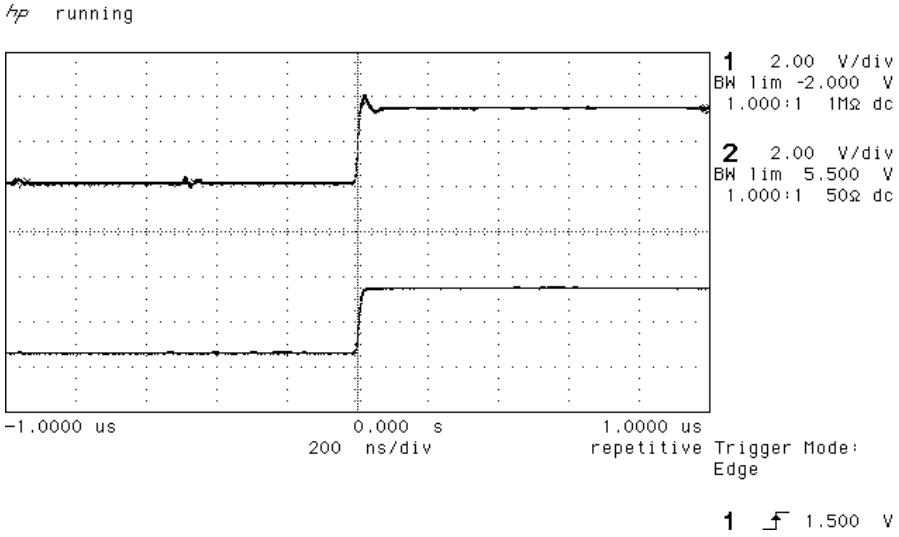


Figure 18 – Word Clock in to Word Clock out, 96 kS/s

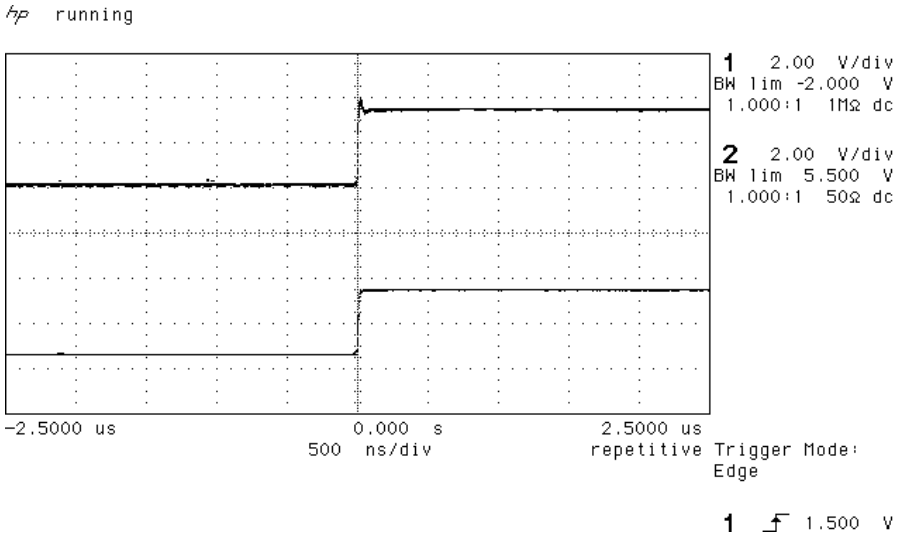


Figure 19 – Word Clock in to Word Clock out, 44.1 kS/s

AES3 in and out are related as below, where they are at the same sample rate, and the AES3 input is used as a sync source. The alignment is better than 40 nsecs. Input is at the top of the displays, output is at the bottom. Signals are at the sockets on the ***dCS 904***, and the unit was slaved to AES Ref In.

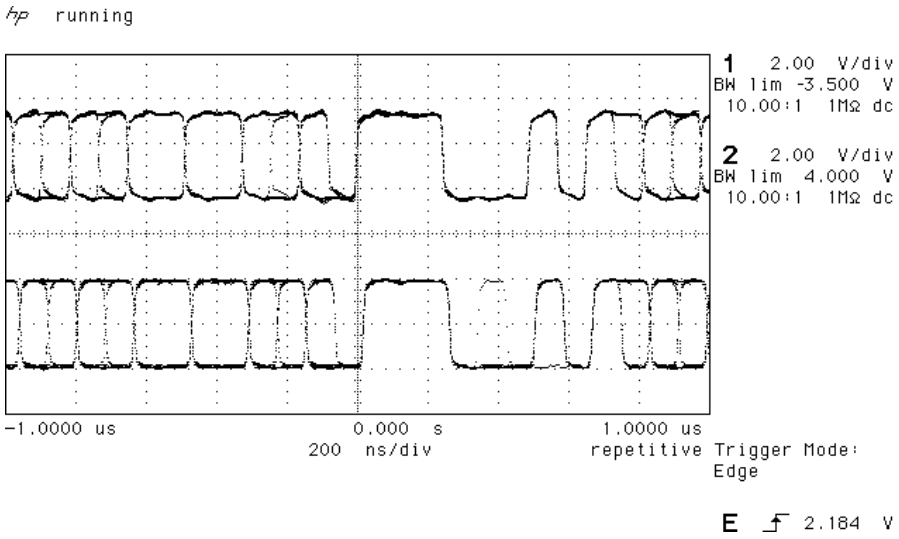


Figure 20 – AES3 in to AES3 out, 96 kS/s

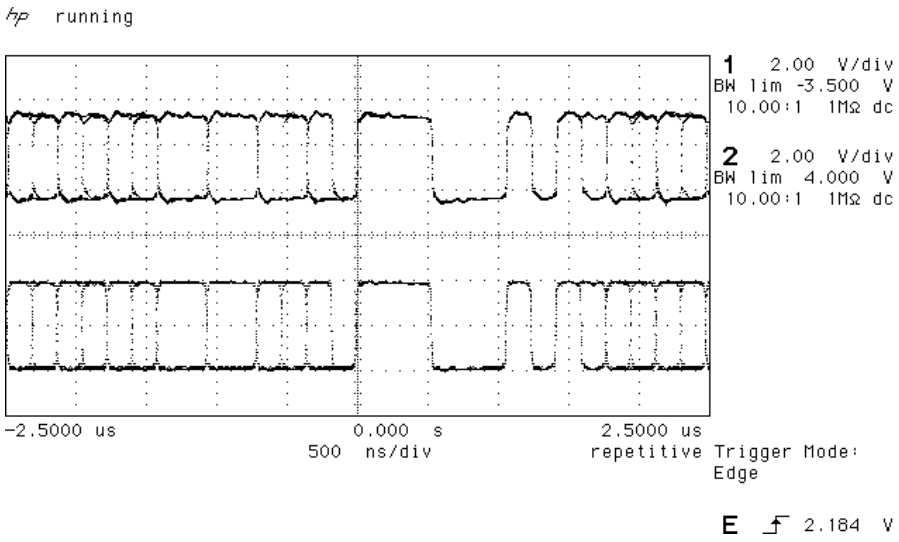


Figure 21 – AES3 in to AES3 out, 44.1 kS/s

AES3 data out is also related to the phase of word clock in. The scope shots below were taken with the unit sync'd to Word Clock.

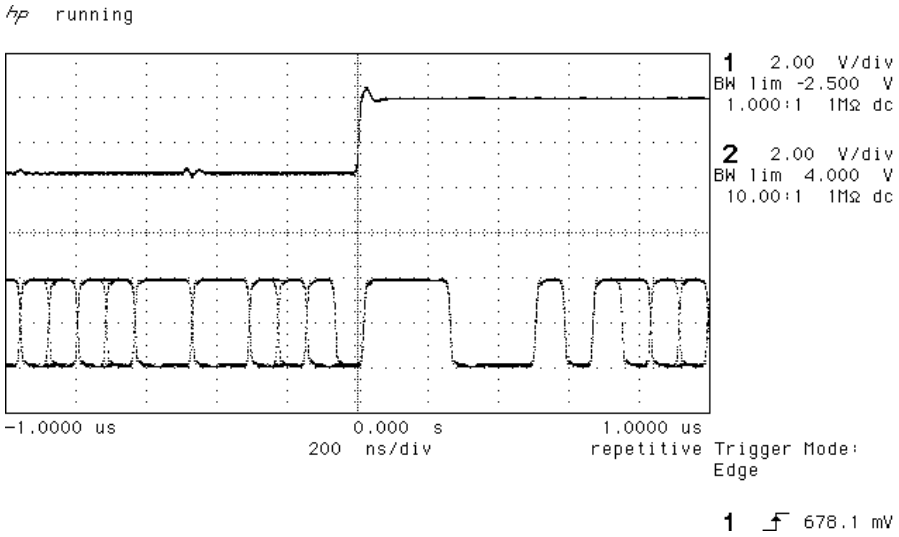


Figure 22 – Word Clock in to AES3 out, 96 kS/s

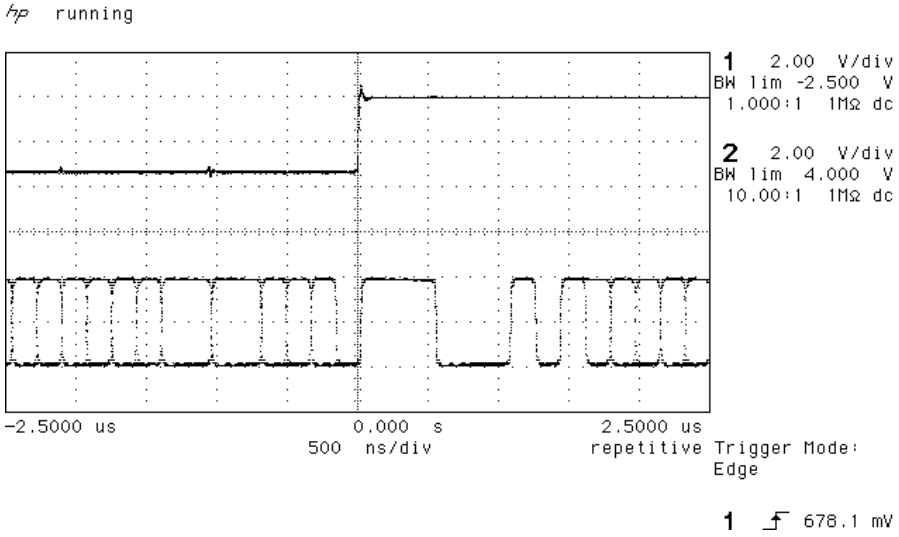


Figure 23 – Word Clock in to AES3 out, 44.1 kS/s

Noise Shaping

The ***dCS 904*** uses noise shaping[6] that is optimised to the F weighting curve[7]. It does not affect signal frequency or transient response, but shapes the frequency response of errors (Q noise, or truncation errors) so that they fall as much as possible in the less sensitive part of the spectrum. The architecture used also shapes dither, where this is added. For all the major sample rates (32 kS/s, 44.1 kS/s, 48 kS/s, 88.2 kS/s, 96 kS/s) the noise shapers have been individually optimised and the first 10 orders are offered. The 1st, 3rd, and 9th shapes for 44.1 kS/s agree well with Wannamaker's published results[8].

Noise Shaping adds more noise power, but because of the shaping it is perceived as lower noise. There is a compromise to be drawn – as more aggressive shaping is used, more noise is added, and less perceived improvement occurs. In practice, things stop improving much above the 9th order. The increased real noise power can cause (small) clicks in editing, if this is carried out after the shaping. For this reason, noise shaping should be used as late as possible in the mastering process – we recommend recording at the very highest possible sample rate and resolution, and only reducing either at the latest possible minute.

If, however, you have to reduce word length, the perceived noise gain (taking into account the ear's response) and the actual increase in noise (mainly out of band) in given in the table below.

Sample Rate (kS/s)	Perceived Gain, F weighted, 1st Order (dB)	Actual Increase in Noise, 1st Order (dB)	Perceived Gain, F weighted, 3rd Order (dB)	Actual Increase in Noise, 3rd Order (dB)	Perceived Gain, F weighted, 9th Order (dB)	Actual Increase in Noise, 9th Order (dB)
32	-3.3	1.9	-7.5	4.2	-8.1	6.1
44.1	-5.5	2.4	-10.5	6.9	-17.9	23.4
48	-6.2	2.5	-11.7	7.6	-21.0	23.8
88.2	-11.1	2.8	-23.8	11.3	-42.2	24.0
96	-11.8	2.9	-25.7	11.3	-45.3	22.5
176.4	-17.0	3.0	-40.6	12.6	-63.0	21.8
192	-17.7	3.0	-42.8	12.6	-65.9	21.8

Table 5 – Noise Shaper Gain by Order and Sample Rate

The 3rd order shaping tends to follow the E weighting curve, by chance. The 9th order is very aggressive, and can give very large gains at the higher sample rates. For example, 176.4 kS/s or 192 kS/s material truncated to 16 bits (so it can be stored on a DA-88 or ADAT) loses nothing in the audio band in terms of perceived noise, with either 3rd or 9th order shaping. For more information on this topic, either see section **"Word Length Reduction"** on page 64 or read the references below.

6 It actually uses an Error Shaping architecture, but the name is now being used for entirely other things and is less well known, so we call it, erroneously, Noise Shaping
7 "Minimally Audible Noise Shaping", S.P.Lipshitz and R.A.Wannamaker, J AES vol 39 no 11, p836-852
8 "Psychacoustically Optimal Noise Shaping", R.A.Wannamaker, J AES vol 40 no 7/8, p611-620

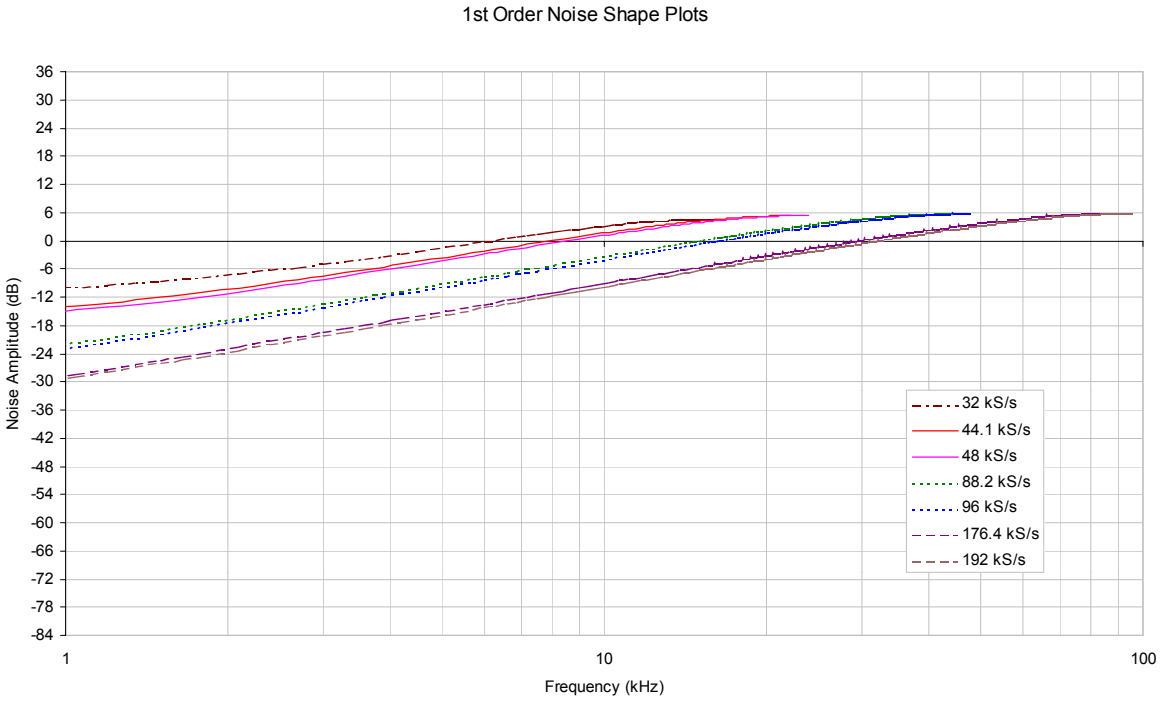


Figure 24 – 1st Order Noise Shapers implemented on ***dCS 904***

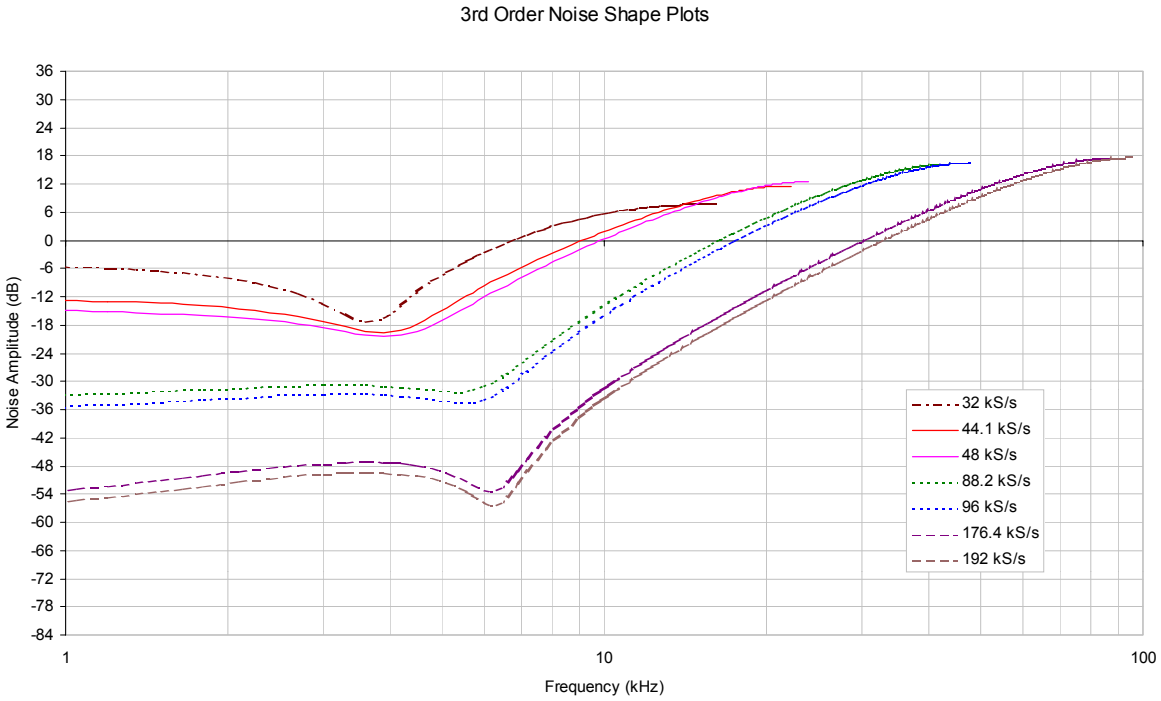


Figure 25 – 3rd Order Noise Shapers implemented on ***dCS 904***

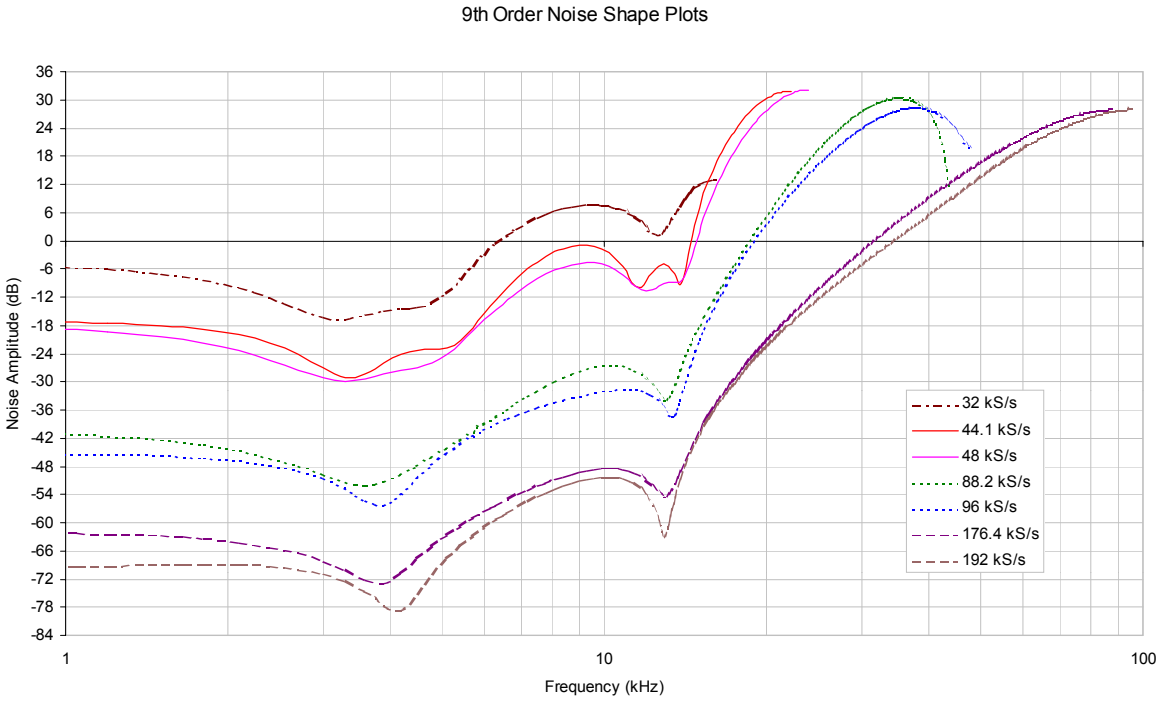


Figure 26 – 9th Order Noise Shapers implemented on *dCS 904*

The noise shaper plots above are all on the same vertical scales for easy comparison, and the vertical grid is approximately 1 bit per grid line. Note that for the audio band, 9th order noise shaping at 176.4 kS/s or 192 kS/s gives huge gains (8 bits or more).

This means that recording these formats on 8 channel 44.1 kS/s or 48 kS/s recording machines that store only 16 bits is quite practical, and there is, in practice, very little quality loss.

Digital Interface Specifications

AES/EBU (AES3)		Input	Output	
Type		*Balanced, differential*		
Impedance		110	110	Ω
Sensitivity (unloaded)		1 ~ 10	> 5	V pk-pk
Maximum Wordlength		24	24	bits
Damage level		> 20		V pk-pk
Connector		XLR3 female	XLR3 male	
Connections	Pin 1	Ground or shield		
	Pin 2	+Signal		
	Pin 3	-Signal		

Table 6 – AES/EBU i/o specifications

SDIF-2, SDIF-3 and DSD	Input	Output	
Type	*Single ended, ground referred*		
Impedance	100	25	Ω
Sensitivity (unloaded)	TTL	TTL	
Maximum Wordlength	24	24	bits
Damage level	> 10		V pk-pk
Time skew			
Wordclock in / out	< 50		ns
Connector	BNC x 1	BNC x 3	
Connections	CH1 (left)		
	CH2 (right)		
	Wordclock In & Out		

Table 7 – SDIF-2, SDIF-3 and DSD i/o specifications

Remote control interface	Input / Output
Type	RS-232
Level	RS-232
Baud Rates	1200, 2400, 4800
Data Format	See page 53
Connector	9 way D type male

Table 8 – Remote Control Interface Details

Analogue Input Specifications

Balanced Inputs			
Type		Balanced	
Format		AES14 : 1992	
Impedance	+	5	kΩ
	-	5	kΩ
CMRR	50 Hz	>100	dB, spec
	50 Hz	>120	dB, typ
	1 kHz	>108	dB, typ
	10 kHz	>80	dB, typ
	20 kHz	>74	dB, typ
Level for Full Scale (as shipped)		+20	dBu
Trim range		±6	dB
Connector type		XLR3 female	
Connections	Pin 1	Ground or shield	
	Pin 2	+Signal	
	Pin 3	-Signal	

Table 9 - Analogue XLR Interface Details

The analogue inputs are balanced (not floating) with a stable, high, common mode rejection ratio. Either input may be used on its own with the other floating if single ended operation is wanted.

Digital Data Formats Supported

The unit supports the following digital data i/o formats,

AES/EBU	(often referred to as AES3, PCM format)
Dual AES	(part of the AES3 spec, PCM format, for 88.2 kS/s, 96 kS/s)
Quad AES	(for 176.4 kS/s and 192 kS/s)
High Speed AES	(part of the AES3 spec, PCM format, for 88.2 kS/s, 96 kS/s)
Dual High Speed AES	(For 176.4 kS/s and 192 kS/s)
TTL AES	(AES3 on single ended TTL levels)
SDIF-2	(DSD or PCM)
High Speed SDIF-2	(for 88.2 kS/s and 96 kS/s)
SDIF-3	(DSD only)
DSD	(using the SDIF-2 or SDIF-3 connector format)

For all AES3 type formats, the incoming Channel Status and User messages are handled according to a priority system – they are either passed through, where this is sensible, or generated and inserted by the unit. See section **"AES3 (AES/EBU) Format"** on page 47 for more details.

The enhanced AES/EBU interface is fully implemented. Each channel has its own parity and data validity bit, as well as User and Channel Status messages. Cyclic Redundancy Counts (CRC's) are generated from the Channel Status message. The Dual AES interface allows a 96 or 88.2 kS/s 24 bit signal to be coded as two standard 48 or 44.1 kS/s 24 bit AES data streams, recorded as four channels on a recorder with standard capacity, replayed and decoded back into a single data stream / channel pair.

SDIF-2 used for PCM data has its message bits internally set to zero, with the exception of the block code, which is implemented. See section **"SDIF-2"** on page 50 for more details.

DSD has, at the time of writing, no messaging structure over SDIF-2 or SDIF-3. Messaging for P3D is allowed for, but not defined yet. Contact *dCS* for more details.

AES3 (AES/EBU) Format

Message Handling

The AES/EBU interface transmits a data structure that conforms to the ***dCS*** version of AES3-1992. This contains 28 bits of Manchester encoded data, and a 4 bit near-Manchester encoded preamble in a subframe, and subframes are further assembled in a block and frame structure. Each subframe contains:

- preambles, to allow the receiver to sync up
- up to 24 bits of audio data, transmitted lsb first
- V, a validity bit
- U, a user bit, for the "User Message"
- C, a Channel Status bit, for the "System Message"
- P, a parity bit

The default AES/EBU message attached to the output data by the unit before being changed by the user is as follows:

Professional:	On
Non-Audio:	Off
Mode:	Stereophonic
Source:	DCS1
Destination:	null

For more information on the way ***dCS*** implement the AES3 system message to handle higher sample rates, see the Appendix to this manual. For the formal definition of the AES3 interface, see footnote[9], from the AES.

How Far will it Go?

The AES/EBU format was designed to go reasonable distances, at 44.1 kS/s and 48 kS/s. Figure 27 and Figure 28 below show it over 16 m and 94 m using average cables. The waveform at 94 m can still be decoded, although it is quite degraded. Cable delay is about 5.6 nsecs/metre.

At 96 kS/s (twice the data rate the format was designed for) the allowed cable length is less. Figure 29 and Figure 30 below show this over 16 m and 94 m. At 16 m the waveforms are still very good, but at 94 m they are really quite unreliable.

We recommend restricting 96 kS/s cable runs to 20 m or less, and using good cable near this length.

[9] AES3-1992 (ANSI S4.40-1992) "AES Recommended practice for digital audio engineering – Serial transmission format for two-channel linearly represented digital audio data".

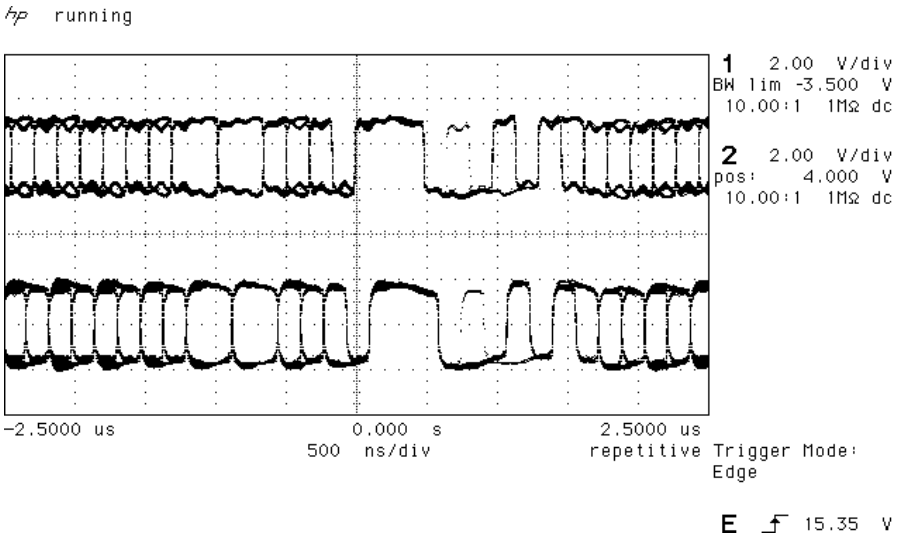


Figure 27 – AES3 format at 48 kS/s over 16 metres

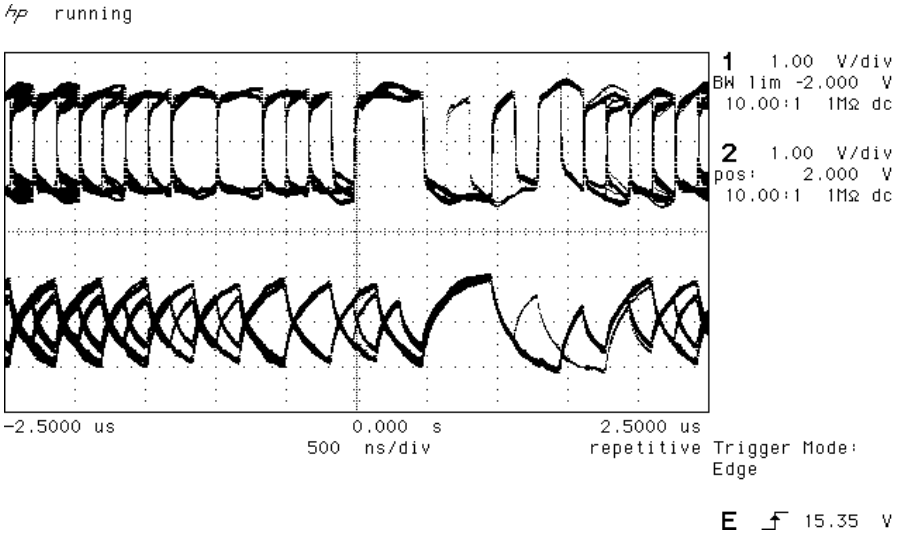


Figure 28 – AES3 format at 48 kS/s over 94 metres

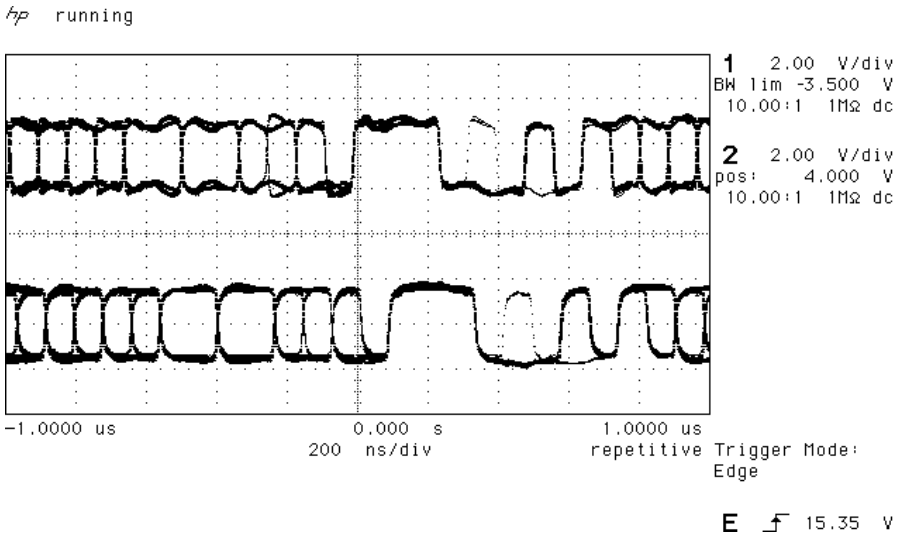


Figure 29 – AES3 format at 96 kS/s over 16 metres

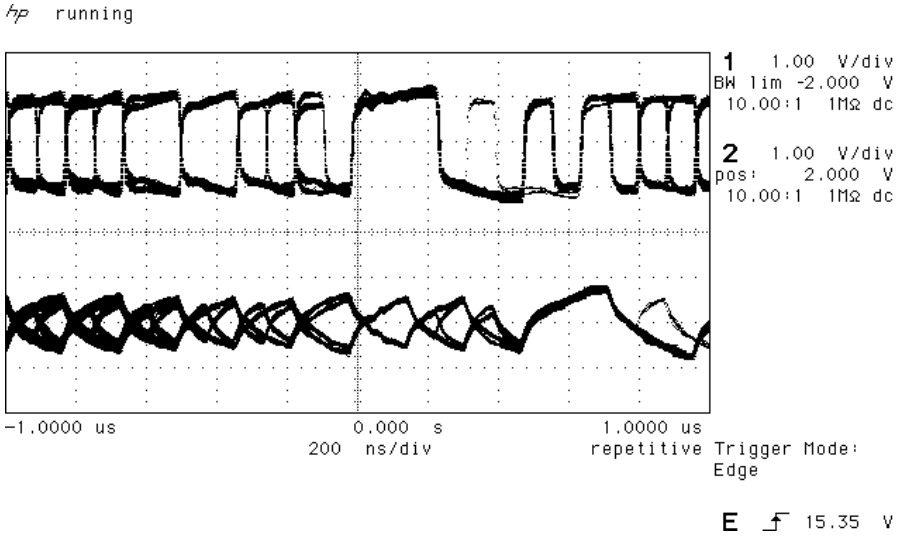


Figure 30 – AES3 format at 96 kS/s over 94 metres

SDIF-2

PCM Format

The SDIF-2 interface is a 4 wire NRZ interface - so the DC level on each signal line may not be constant. It contains 20 bits of audio data and has a block structure of 256 stereo samples, rather than the 192 of AES/EBU. There are 8 bits of message per channel per sample - with a further 3 bits being used for an "illegal code" based sync code. Of the 8 bits per sample, the 8 in the first sample are reserved for system messaging, and the rest are for User messages.

The 4 wires are:

Ground return
Left Channel
Right Channel
Word Clock

The sync codes can enable data recovery without the word clock, if necessary, but with the number of data formats in current operation, this method of locking is strongly discouraged. The waveforms below SDIF-2 waveforms (data and word clock) at 44.1 kS/s and 96 kS/s.

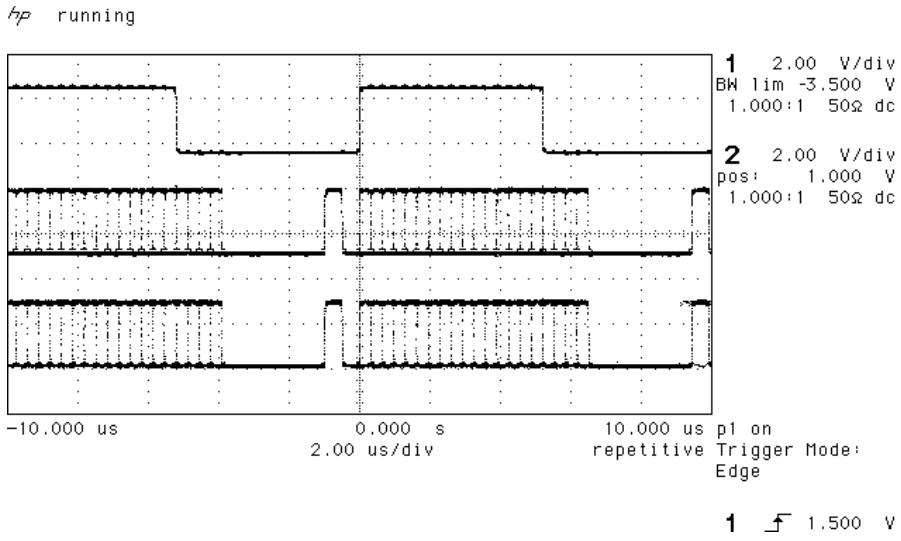


Figure 31 – SDIF-2 PCM format at 96 kS/s

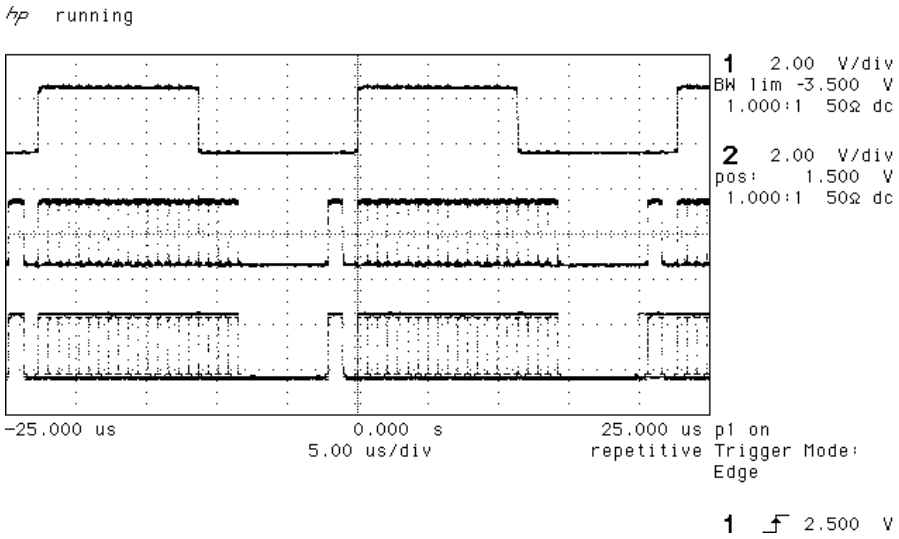


Figure 32 – SDIF-2 PCM format at 44.1 kS/s

SDIF-2 Messaging

The SDIF-2 message is given in the table following. The ***dCS 904*** implementation sets all bits of the User message to "0".

DESCRIPTION	Definition	Default Message
Undefined	0000 0xxx	0000 0xxx
Emphasis		
No emphasis	xxxx x00x	xxxx x00x
Emphasis (15µsec, 50µsec)	xxxx x01x	
Dubbing Prohibit		
Dubbing allowed	xxxx xxx0	xxxx xxx0
Dubbing inhibited	xxxx xxx1	
Block Code		
Start of block	xxxx xxxx 1...	as required
Not start of block	xxxx xxxx 0...	as required

Table 10 - SDIF-2 Message Table

DSD on SDIF-2

SDIF-2 can be used for DSD. The waveforms appear quite different to PCM format. However, they do produce transitions where the illegal code transitions were, and for this reason we advise against locking to the illegal transitions in SDIF-2.

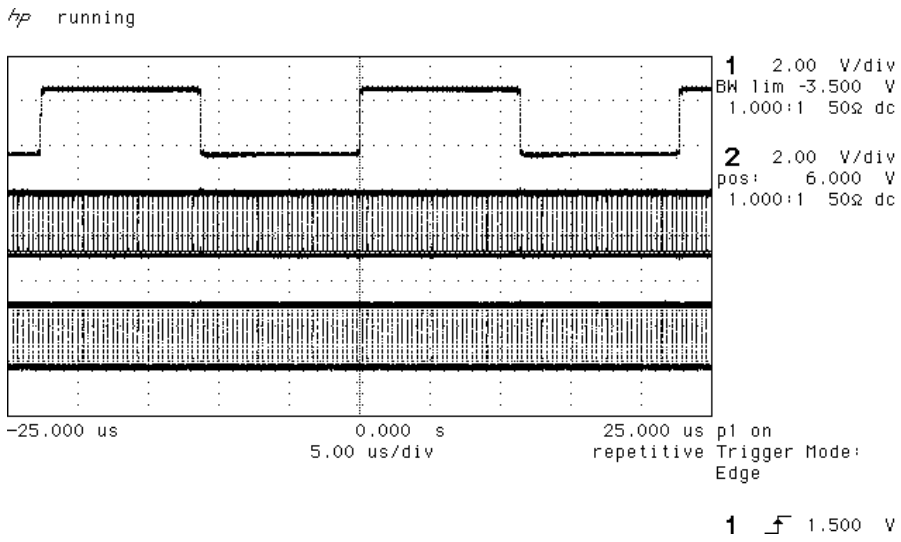


Figure 33 – DSD using SDIF-2 electrical format

DSD on SDIF-3

SDIF-3 embeds a clock in the SDIF-2 data stream, and so does not need word clock. It is used only for DSD – it is not used for PCM. Contact SONY for more details

RS-232 Remote Control Interface

Overall Description

dCS 9xx units can be controlled using a simple serial protocol, via the RS-232 ports, using the control format described below. All commands available from the front panel (and a few others, ***dCS*** use only) of a unit can be remotely controlled using this approach. Each unit must have a unique ID (in the range 0 to 99) which must be set up by hand using the menu system on the front panel. The units remember their ID when powered down, so this setting up only has to be done once.

Physical Interface

Units are all connected in a RS-232 daisy chain, up to a maximum of 11 units, with a serial cable (DB9 pin female straight cable) connected between the Serial Out and Serial In ports of the units. The same type of cable is used to connect the Serial In port of the first unit on the chain to the COM port of a PC.

By default all units are configured to operate at 1200 baud. Standard RS-232 signal levels are used. Bytes are transmitted with 1 start bit, 8 message bits, 1 stop bit and no parity.

Units can be switched to 1200, 2400, 4800 or 9600 baud. An RS-232 break will reset all units on the daisy chain to 1200 baud. A special command and ID is used to configure the units to other baud rates (see “Special Commands and Protocols” below). The following rates are recommended:

3 or less units	4800 baud
4 to 7 units	2400 baud
8 to 11 units	1200 baud

Operation of the daisy chain at higher than the recommended rates may result in incorrect behaviour of the system – either because the units misinterpret commands, or, more likely, because the controlling computer misinterprets their replies. Units will revert back to 1200 baud if they are switched off and on - they do not remember what they were last set to.

9600 baud is currently not fully tested over all temperatures. It can be used for single units operating in a benign environment.

Timing Accuracy and Warnings

The units use clock dividers derived from their crystals to produce the RS-232 signals. The frequency of operation is measured to be better than 2% for all baud rates with both crystals. Some of the commands, however, switch clock frequencies, and these may be controlled by phase locked loops with long time constants. While this is happening, correct RS-232 timing cannot be guaranteed, and the units should not be addressed – a period of 30 secs should be allowed after switching clock frequencies for timings to stabilise.

Units acknowledge and repeat back their actions on receipt of a command. The acknowledge should be waited for and checked before proceeding to the next command – see Acknowledge Message below

Transmit Message

The system employs the following protocol - all transactions are initiated by the PC. The PC is the transmitter and units on the daisy chain are receivers.

Byte 1 : ID of unit to process command
Byte 2 : Command (single byte)
Byte 3 : Length of parameter string
Byte 4 : List of parameters
.
.
Last byte : Checksum of parameter list

The minimum length of a transmit message is 4 bytes, maximum 64 bytes, limited by a buffer within the receiving unit. There are two cases for parameter length mismatch.

(a) Receiver expects n parameters, transmitter sends more.

This condition may arise when a later version remote tries to communicate with an earlier version of receiver. The receiver acts on first n parameters in list, ignores rest. The full parameter list is check summed.

(b) Receiver expects n parameters, transmitter sends less.

This condition may arise when a earlier version remote tries to communicate with an later version of receiver. The receiver acts on all parameters in list, and uses sensible defaults for the rest (ideally, no action except where this is silly). Do not truncate a command sequence expecting the receiver to do something sensible. The full parameter list is check summed.

The checksum is the sum of the bytes in the parameter list (bytes 4 to (last-1) byte) modulo 256. The receiving unit checks the checksum and will only act upon a command if the command is complete and the checksum is correct.

Acknowledge Message

The addressed receiving unit (ADC, DAC, DDC, Master Clock, etc) acknowledges within 50 msecs of the last transmitted byte in the transmit message. For some special cases (dCS use only, see “Special Commands and Protocols” below) commands do not acknowledge. If the checksum is incorrect the receiving unit will ignore the command, clear its buffer and will not acknowledge. Only valid command bytes will generate an acknowledge, other command bytes will be ignored, clearing the receiver buffer.

The acknowledge response starts with:

Byte 1 : 101010xx – indicates successful transmission to physical address, with xx indicating the time the unit may take to respond to the command

and then, with a command dependant part:

Byte 2 : ID of unit that processed command
Byte 3 : Command (single byte)
Byte 4 : Length of response string
Byte 5 : List of response bytes
.
.
Last byte : Checksum of response list

The checksum is the sum of the bytes in the parameter list (bytes 5 to (last-1) byte) modulo 256. The minimum length of an acknowledge message is 1 byte, maximum 64. If the checksum is incorrect the transmitter should re-issue the command.

For the first byte, the response times are:

xx
00 immediate (less than 50 msecs)
01 up to 3 seconds
10 up to 15 seconds
11 up to 25 seconds

The receiving unit will ignore any transactions on the RS-232 while it is busy. If the transmitter sends commands to a unit when the unit is busy the unit will not send an acknowledge back. The transmitter must be designed to time out after 50 msec and repeat the command if necessary. In a multi-unit environment, it would be sensible to organise the transmitter to access units with a "round robin" polling scheme – in this way several units can be instructed to perform commands simultaneously, the transmitter coming back to busy units periodically. It is also recommended that units are not accessed for the first ¾ of their "response" time – nothing untoward will happen, but the unit will be ignoring the RS-232 and will not respond, so the transmitter would just time out anyway.

Example :

To set unit 2 Emphasis to AUTO using the RS-232 control format:

transmit the string [2][34][1][0][0],
and the receiving unit will respond [169].

Special Commands and Protocols

BREAK

Continuous high on transmit line for more than 100 msec. Resets ALL units on daisy chain to 1200 baud.

GLOBAL ADDRESSES

Address F0 hex (240 decimal)

ALL units on daisy chain react to command. Nothing acknowledges. This should only be used for setting baud rates to 2400, 4800 or 9600 baud. Never change baud rate from a higher rate to a lower rate, as this could result in unexpected behaviour, always reset the daisy chain to 1200 baud and then issue the appropriate command. Never change the baud rate of a single unit in a multi-unit daisy chain as this could result in the chain locking up.

Address F1 hex (241 decimal), Command RS_ENABLE_DEBUG (19 decimal)

ALL units on daisy chain react to command. Nothing acknowledges. This enables dCS debugging commands. This may result in unstable behaviour of the unit.

Command Streams

Example – a system of 9 units with ID's set up as noted:

1 Master Clock (ID 1),
4 P3D compatible ADCs (ID 2, 3, 4 and 5),
4 P3D compatible DACs (ID 6, 7, 8 and 9).

RS232 operating at 1200 baud.

It is assumed that the transmitter operates on a round robin polling scheme and that each step completes before the next allowing for time outs. Except in the case of a time out a unit should not be accessed within the response time of its previous command. Within each step there is no need to wait for the command response time prior to moving on to the next unit – once an acknowledge has been received, the controller can safely assume that the unit is getting on with the command it has received, and can move on to the next unit. At the end of a step there is no need to wait before moving on to the next step.

Command strings are not given fully, the parameter string and the checksum are not explicitly given. A typical command is shown as:

[ID][Command Type], information about command

A typical response is:

[ACK Type][ID], information (when requested)

When changing the operating frequency of a unit the internal crystals are switched. It is recommended that after a crystal switch units are allowed to settle for a short time (< 1 second) to ensure optimum performance. In this case the units are being controlled by a Master Clock, so time should be allowed for this to switch and for the other units connected to it to also switch and begin to settle. It is recommended that there is no RS-232 activity for 3 seconds after the Master Clock frequency is switched to ensure all units have time to settle.

When operating in DSD mode units assume their reference clocks are operating at 44.1kHz. If a different frequency reference is used they will continuously monitor the reference clock frequency, preventing RS-232 accesses. It is therefore important to ensure the reference clock is set to 44.1kHz prior to entering DSD mode, and that DSD mode is left prior to changing the reference clock to another frequency.

Example: Switching to 96k PCM

The following example covers the system of nine units, in two complex format changes. Change the ADC and DAC operating mode to PCM prior to changing the Master Clock frequency. Change the DAC operating mode prior to the ADC. When changing the Master Clock frequency the system should be allowed to settle to the new frequency before any further RS-232 activity.

1) Command DACs 6, 7, 8 and 9 to change mode, the units may take up to 15 seconds to complete this command (if the previous mode had been DSD the FPGAs need to be re-loaded, which takes time). There is no need to wait prior to moving on to step 2.

   Transmit -> [6][DSD_MODE], to change mode to PCM of unit 6
   Responds -> [ACK 15 seconds][6], requested mode

Transmit -> [7][DSD_MODE], to change mode to PCM of unit 7
Responds -> [ACK 15 seconds][7], requested mode
Transmit -> [8][DSD_MODE], to change mode to PCM of unit 8
Responds -> [ACK 15 seconds][8], requested mode
Transmit -> [9][DSD_MODE], to change mode to PCM of unit 9
Responds -> [ACK 15 seconds][9], requested mode

2) Command ADCs 2, 3, 4 and 5 to change mode, the units may take up to 15 seconds to complete this command (if the previous mode had been DSD the FPGAs need to be re-loaded, which takes time). There is no need to wait prior to moving on to step 3

Transmit -> [2][DSD_MODE], to change mode to PCM of unit 2
Responds -> [ACK 15 seconds][2], requested mode
Transmit -> [3][DSD_MODE], to change mode to PCM of unit 3
Responds -> [ACK 15 seconds][3], requested mode
Transmit -> [4][DSD_MODE], to change mode to PCM of unit 4
Responds -> [ACK 15 seconds][4], requested mode
Transmit -> [5][DSD_MODE], to change mode to PCM of unit 5
Responds -> [ACK 15 seconds][5], requested mode

3) Check DACs for mode change. This command allows the Transmitter to check the mode of the DACs. If a unit has not changed the transmitter should go back to step 1 and repeat the command.

Transmit -> [6][REQUEST_DSD_MODE]
Response -> [ACK immediate][6], actual mode
Transmit -> [7][REQUEST_DSD_MODE]
Response -> [ACK immediate][7], actual mode
Transmit -> [8][REQUEST_DSD_MODE]
Response -> [ACK immediate][8], actual mode
Transmit -> [9][REQUEST_DSD_MODE]
Response -> [ACK immediate][9], actual mode

4) Check ADCs for mode change. This command allows the Transmitter to check the mode of the ADCs. If a unit has not changed the transmitter should go back to step 2 and repeat the command

Transmit -> [2][REQUEST_DSD_MODE]
Response -> [ACK immediate][2], actual mode
Transmit -> [3][REQUEST_DSD_MODE]
Response -> [ACK immediate][3], actual mode
Transmit -> [4][REQUEST_DSD_MODE]
Response -> [ACK immediate][4], actual mode
Transmit -> [5][REQUEST_DSD_MODE]
Response -> [ACK immediate][5], actual mode

5) Command Master Clock to change frequency. Allow the system time to settle after this command with no RS232 activity, three seconds should be sufficient.

Transmit -> [SEL_FS], change to 96k
Responds -> [ACK 3 seconds], requested frequency
Wait for 3 seconds

Check Master Clock has changed frequency. If it has not go back to step 5.

Transmit -> [1][REQUEST_FS], request actual frequency
Responds -> [ACK immediate][1], actual frequency

The system is now set up with the Master Clock configured for 96k operation and the ADCs and DACs locked in PCM mode to 96k.

Example: Switching to P3D

Change the Master Clock frequency to 44.1k prior to changing the ADC and DAC operating mode to DSD. Change the DAC operating mode prior to the ADC. When changing the Master Clock frequency the system should be allowed to settle to the new frequency before any further RS-232 activity.

6) Command Master Clock to change frequency. Allow the system time to settle after this command with no RS-232 activity, three seconds should be sufficient.

Transmit -> [1][SEL_FS], change to 44.1k
Responds -> [ACK 3 seconds][1], requested frequency
Wait for 3 seconds

7) Check Master Clock has changed frequency. If it has not go back to step 6.

Transmit -> [1][REQUEST_FS], request actual frequency
Responds -> [ACK immediate][1], actual frequency

8) Command DACs 6, 7, 8 and 9 to change mode, the units may take up to 15 seconds to complete this command (if the previous mode had been PCM the FPGAs need to be re-loaded, which takes time). There is also no need to wait prior to moving on to step 9.

Transmit -> [6][DSD_MODE], to change mode to P3D of unit 6
Responds -> [ACK 15 seconds][6], requested mode
Transmit -> [7][DSD_MODE], to change mode to P3D of unit 7
Responds -> [ACK 15 seconds][7], requested mode
Transmit -> [8][DSD_MODE], to change mode to P3D of unit 8
Responds -> [ACK 15 seconds][8], requested mode
Transmit -> [9][DSD_MODE], to change mode to P3D of unit 9
Responds -> [ACK 15 seconds][9], requested mode

9) Command ADCs 2, 3, 4 and 5 to change mode, the units may take up to 15 seconds to complete this command (if the previous mode had been DSD the FPGAs need to be re-loaded, which takes time). There is also no need to wait prior to moving on to step 10.

Transmit -> [2][DSD_MODE], to change mode to P3D of unit 2
Responds -> [ACK 15 seconds][2], requested mode
Transmit -> [3][DSD_MODE], to change mode to P3D of unit 3
Responds -> [ACK 15 seconds][3], requested mode
Transmit -> [4][DSD_MODE], to change mode to P3D of unit 4
Responds -> [ACK 15 seconds][4], requested mode
Transmit -> [5][DSD_MODE], to change mode to P3D of unit 5
Responds -> [ACK 15 seconds][5], requested mode

10) Check DACs for mode change. This command allows the Transmitter to check the mode of the DACs. If a unit has not changed the transmitter should go back to step 8 and repeat the command.

Transmit -> [6][REQUEST_DSD_MODE]
Response -> [ACK immediate][6], actual mode
Transmit -> [7][REQUEST_DSD_MODE]
Response -> [ACK immediate][7], actual mode
Transmit -> [8][REQUEST_DSD_MODE]
Response -> [ACK immediate][8], actual mode
Transmit -> [9][REQUEST_DSD_MODE]
Response -> [ACK immediate][9], actual mode

11) Check ADCs for mode change. This command allows the Transmitter to check the mode of the ADCs. If a unit has not changed the transmitter should go back to step 9 and repeat the command.

Transmit -> [2][REQUEST_DSD_MODE]
Response -> [ACK immediate][2], actual mode
Transmit -> [3][REQUEST_DSD_MODE]
Response -> [ACK immediate][3], actual mode
Transmit -> [4][REQUEST_DSD_MODE]
Response -> [ACK immediate][4], actual mode
Transmit -> [5][REQUEST_DSD_MODE]
Response -> [ACK immediate][5], actual mode

The system should now be set up with the Master Clock configured for 44.1k operation and the ADCs and DACs locked in P3D mode.

Command name	Command Byte	Number of Parameters in Command	Parameters	Parameters in Response	ADC	DAC	DDC	MClk
RS_AUTO_SLAVE	15	1	0 = do not automatically slave 1 = automatically slave to a reference input	0	X			X
RS_MASTERSLAVE	16	2	First parameter 1 = Master 0 = Slave. If slave, second parameter: 0 = AES 2 = SDIF	0	X		X	X
RS_ENABLE_DEBUG	19	3	Global Command	None	X	X	X	X
RS_SEL_FS	32	1	Select Output Fs	Echos message	X	X	X	
RS_FILTER	33	1	Select Filter, 0-3	0	X	X	X	
RS_EMPH	34	1	Select De-emphasis filter to use, 0 = Auto 1 = 50/15 2 = CCITT 3 = None	0	X	X	X	
RS_OUT_MODE	36	1	0 = Output SDIF wordclock on w/clk out, 1 = Output AES on w/clk out	0	X	X		X
RS_TRUNC	39	1	No. of output bits (16 - 24)	0	X		X	X
RS_SNS	40	1	Noise shaper, 0 = Auto 1 = Off 2 = 1st Order 3 = 3rd order 4 = 9nth order	0	X		X	X
RS_DDC	41	1	0 = Normal mode (e.g. D in A out for DAC, A in D out for ADC), 1 = D in D out	0	X	X		X
RS_OUT_RATE	42	1	0 = Low speed output (e.g. Dual 88.2/ Quad 192 1 = High speed option	0	X		X	X
RS_MUTE	43	1	0 = Unmute 1 = Mute	0	X	X	X	X
RS_AUTO	44	1	1 = Turn off automatic input selection (DAC)	0		X		
RS_7SEGS	47	1	1 = Turn off 7-segment display	0	X	X		X
RS_INP_FORMAT	48	1	Select Input format for DACs – 0 = Auto 1 = Single wire 2 = Dual Wire 4 = Quad	0		X	X	
RS_4WIRE	49	1	0 = Enable 4-wire DSD outputs 1 = Disable 4-wire DSD outputs	0	X			
RS_FLIP	50	1	0 = Normal 1 = Flip channels	0		X	X	
RS_ACUT	51	1	1 = Disable Auto Digital Muting	0		X		
RS_FINE_LOCK_MODE	52	1	1 = Use coarse lock 0 = use fine lock	0		X		
RS_WAVETYPE	63	1	0 = Signal Generator Off 1 = Signal Generator ON	0	X	X	X	X
RS_AMP	64	1	Generator Amplitude, format X	0	X	X	X	X
RS_FREQ	65	1	Generator Frequency. Specified as a 32 bit number. Expressed as a fraction of Sample Frequency	0	X	X	X	X

Command name	Command Byte	Number of Parameters in Command	Parameters	Parameters in Response	ADC	DAC	DDC	MClk
RS_REF_MODES	77	2	first parameter is terminator (AES) 0 = unterminated 1 = terminated second is reference mode 1 = ref out is internal 0 = pass through	0	X	X		X
RS_OVLD_LEV	87	1	Overload threshold, format X	0	X			
RS_VOL	111	1	Digital volume control, format X	0		X	X	
RS_PHASE	112	1	Phase: 0 = None inverted 1 = Both inverted 2 = left inverted 3 = right inverted	0		X	X	
RS_REF_MODE	114	1	Select reference input to clock from: 0 = AES1 1 = AES2 2 = SDIF-2 Clock (word clock) 3 = SPDIF1 or AES3 4 = SPDIF2 or AES4 5 = SPDIF3	0		X	X	
RS_DSD_MODE	119	1	0 = DSD Off 1 = DSD (SDIF) 2 = 4-wire DSD	Echos message	X	X	X	
RS_BAUD_RATE	141	1	Global command	None	X	X	X	X
REQUEST_DSD_MODE	142	0	response -> DSD mode	Yes				
REQUEST_FREQUENCY	143	0	response -> Frequency of unit	Yes				

Table 11 – RS-232 Command Set

Format X – the level set number is –0.1dB times the 16 bit (positive integer) used. So, for example, 260 would set –26dB below full scale for generator amplitude.

Power Consumption

The ***dCS 904*** has a linear power supply, and so power consumption changes as the mains voltage changes. The internal regulation is comparatively efficient for a linear supply, so these changes are kept to a minimum. Power consumption is independent of mains voltage selector switch setting.

Power Consumption with Mains Voltage (measured as AC power into mains socket):

Nominal mains	25 W
Mains -10%	22 W
Mains +10%	27 W

The actual intended supply voltage is shown on the rear panel. 50 Hz or 60 Hz operation is not important – the unit can use either. In general, users will not need to change the mains input configuration. If you do need this to be done, please see the section **"Having Your Options Changed"**, page 68 in this manual and contact your distributor or ***dCS***.

Size and Weight

The ***dCS 904*** dimensions correspond to a standard 2U 19" rack mount case. Four heavy duty feet, fitted to the base, extend the overall height to slightly greater than 2U.

Dimensions

Width	430 mm	see note (i)
Height, without feet	44 mm	(2U)
Height, with feet	52 mm	
Depth	390 mm	see note (ii)
Weight	6.8 kg	see note (iii)

note (i)	Removable 19" rack mount ears are supplied, taking total width to 483 mm (19").
note (ii)	Measured from front panel to rear panel connectors. Additional depth should be allowed to accommodate cable connectors.
note (iii)	The high quality case is necessarily heavy, consideration should be paid to appropriate support shelving when installing the units in a rack.

Operating Conditions

The ***dCS 904*** has no ventilation slots or fan cooling. It dissipates relatively low power, so that usually allowing natural convection provides enough cooling in most circumstances. It is sensible, however, to not install the unit near heat sources such as radiators, hot air ducts or in direct strong sunlight.

Operating conditions should be such that internal temperature does not exceed 70°C substantially, as read out from the internal temperature sensor (see the menu function **Heat** on page 22). This will tend to be met if the ambient temperature is below 50°C, although it will depend a bit on how the unit is positioned. Internal temperature should not fall below 0°C, and should be a non-condensing. The unit monitors its internal temperature, and displays one of two error messages as the temperature rises. At and above an internal temperature of 78°C, the unit displays Hot on its front panel, as a warning. Performance and reliability will be degraded if operated in this range for long periods. At and above 88°C the unit displays Ouch, and should be turned off. See section **System Messages and Error Codes** on page 75.

Figure 34 below shows the rise of internal temperature for the middle unit of three stacked as in a rack, with support plates between. Allowing 3 cms between units gives reasonable cooling.

If in doubt, the easy test is – the ***dCS 904*** is happy to work anywhere a human is.

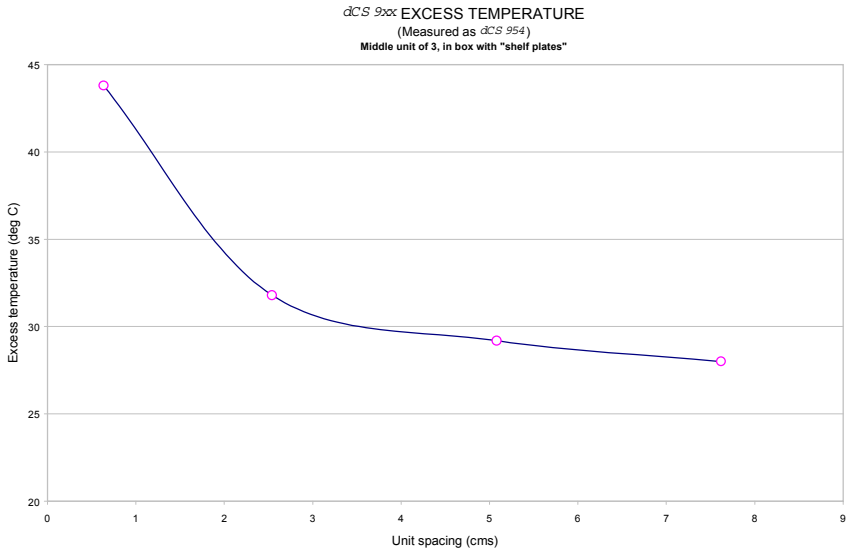


Figure 34 – Temperature rise above ambient for a unit in a stack of 3 with poor ventilation

GENERAL TECHNICAL INFORMATION

Word Length Reduction

Word length reduction (truncation) causes an error signal to be added to the wanted signal. The error signal is usually referred to as "Q noise" or Quantisation noise – the approximation is usually made that the errors are noise like. This is reasonably true for large signals, where the errors are very complex if they are not exactly noise like. Importantly, though, for smaller ones it is not so. As the wanted signal gets smaller, the complexity of the error signal decreases. The errors first of all pile into ever fewer lower order harmonics or intermods, and then, as the level of the signal sinks below the Q level, the majority of the error power piles into the signal fundamental. This causes its amplitude to become unpredictable – it may drop abruptly to zero and disappear, or it may cease to go down any more and just stay at a constant level. From the audio viewpoint, this sounds very unpleasant. As a signal tail decays away, the tonal quality changes, and then it decays into distorted mush and then either abruptly stops, or else keeps fuzzing away until a new signal starts. The level at which all this happens is the lsb of the output word – for CDs, it is at the 16 bit level, which equates to about -90 dB0. The level is high enough to be quite audible, and the effect must be tackled to make reasonable quality end product.

There is really only one way of tackling the problem – another signal has to be added to the wanted one to smooth the staircase transfer function that truncation causes. Mathematically, with two signals present, the transfer function that the wanted signal sees is the convolution of the PDF[10] of the second signal and the staircase function. The converse is also true – the transfer function the additional signal sees is the convolution of the PDF of the wanted signal and the staircase function. This aspect is not a problem with the dither types considered below, but it can be with some highly frequency shaped dithers.

The trick is to make the second signal as inaudible as possible. It is usually referred to as dither, and it is usually noise like, because then its statistics can be controlled, and the converse effect of the signal modulating the dither can be made insignificant, or zero. However, there are a number of ways that this dither signal can be generated and treated. The major options are:

- generate it from the signal or generate it independently and add it ("Dither"). It seems implausible that the dither signal can be generated from the signal, but it can, and this gives the lowest added noise power option. It is noise shaping on its own, but there are some circumstances where it needs help from additional dither.
- add inside or outside an error shaping loop
- frequency shape to match the ears response or not. One can use techniques that suppress error energy in the areas where the ear is sensitive, and put it in areas where the ear is not sensitive. Usually this shuffling around process costs something – we remove a little from the sensitive areas and add back rather more in the less sensitive parts, but that's life. We still gain some improvements.

The table below gives the actual noise levels for 16 bit truncated signals with no dither, various types of dither, noise shaping on its own, and noise shaping with dither. The 0 dB reference level is taken as the minimum noise we could

[10] PDF = Probability Distribution Function. References to Rectangular Dither or Triangular Dither refer the shape of the PDF of the dither.

possibly get away with – the amount that simple 16 bit truncation (16 bit Q noise) would give, if it were well behaved, which it is not.

xTruncation Type, with 44.1 kS/s data rate	Noise, unweighted, rel 16 bit Q noise[11]	Noise, F weighted, rel 16 bit Q noise	Comments
16 bit truncation	0 dB	0 dB	Unpleasant low level effects
16 bit truncation with Top Hat dither	3 dB	3 dB	Okay – can show noise modulation at low signal levels
16 bit truncation with Triangular dither	4.8 dB	4.8 dB	All noise modulation and unpleasant effects removed, but noise floor is high
16 bit truncation with Noise Shaped Triangular dither	4,8 dB	1.2 dB	All noise modulation and unpleasant effects removed. Not much perceived noise penalty
16 bit truncation with 3rd order noise shaping and no dither	6.9 dB	-10.5 dB	Okay with input noise floors down to –102 dB
16 bit truncation with 3rd order noise shaping and Noise Shaped Triangular dither	11.0 dB	-9.2 dB	Unconditionally free from truncation effects with all inputs
16 bit truncation with 9th order noise shaping and no dither	23.4 dB	-17.9 dB	Okay with input noise floors down to –120 dB
16 bit truncation with 9th order noise shaping and Noise Shaped Triangular dither	28.2 dB	-16.7 dB	Unconditionally free from truncation effects with all inputs

Table 12 – Dither and Noise Shaping Noise Powers

Straight forward dither always adds noise – it can only produce signals with a noise floor higher than Q noise on its own. However, the noise power added is a few dBs for simple types. Noise shaping adds rather more noise, but it can be made to add it in parts of the spectrum that the ear is less sensitive to, so the perceived noise (F weighted noise) is lower – up to three bits lower. It results in a signal that the ear hears as having a far **lower** noise floor than a 16 bit truncated signal, rather than the "not much worse" of dither alone, even though there is really more noise present[12].

[11] 16 bit Q noise is -98.1 dB relative to a full scale sine wave.
[12] DSD carries this further. The principle is the same, but with DSD, there is more noise than there is signal, even at full scale. It is just that it is in a part of the spectrum the ear cannot hear.

Noise shaping on its own is not perfect. It relies on a small amount of noise in the input signal to generate the frequency shaped correction signal, and if there is very low noise in the input signal, this mechanism can break down. With ADCs, however, this situation does not arise, because of the analogue noise in the ADC and the input signal.

There is another option not supported by the ***dCS 904*** – generate the dither independently of the signal and frequency shape it prior to addition, but do not add it in an error shaping loop. This seems to ***dCS*** to combine the worst of all worlds – the high noise floor in the 0-6 kHz area of straight dither, and the high total noise of noise shaping. However, some people use it.

What does it look like?

Figure 35 gives the spectra of 16 bit truncated 44.1 kS/s signals with a –90dB sine present, for two dither only signals (Top Hat, Noise Shaped Triangular), and with a 10th order noise shaped[13] signal, generated and processed by a ***dCS 972***. The equivalent simply truncated spectrum is shown in Figure 36, separately because it is so revolting. In it, we can see that at the signal level shown (-90 dB) error power from the quantising/truncation is beginning to pile into the fundamental, which is showing an amplitude error of +1.3 dB, as well as all the unwanted harmonics. This would show up on a conventional linearity plot, although the sign of the error could be either way.

We see that the noise shaping approach maintains low noise in the critical audio mid band.

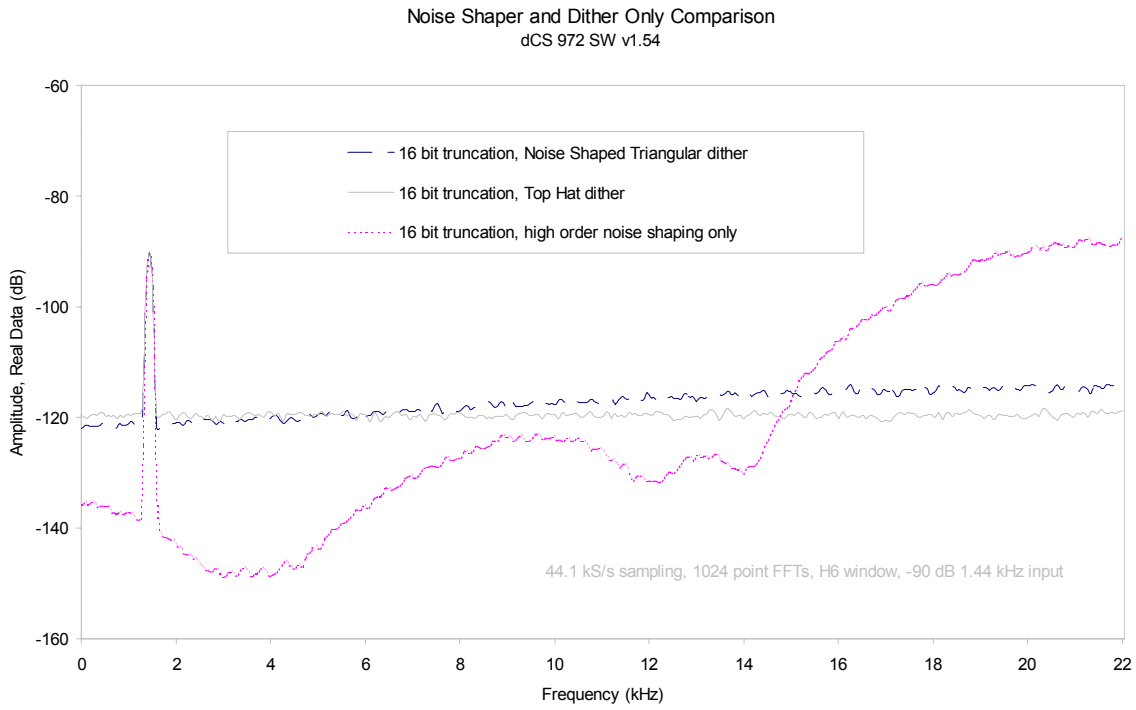


Figure 35 – Noise Shaping and Dither Spectra

[13] for comparison with the table, 10th and 9th order noise shaping are very similar.

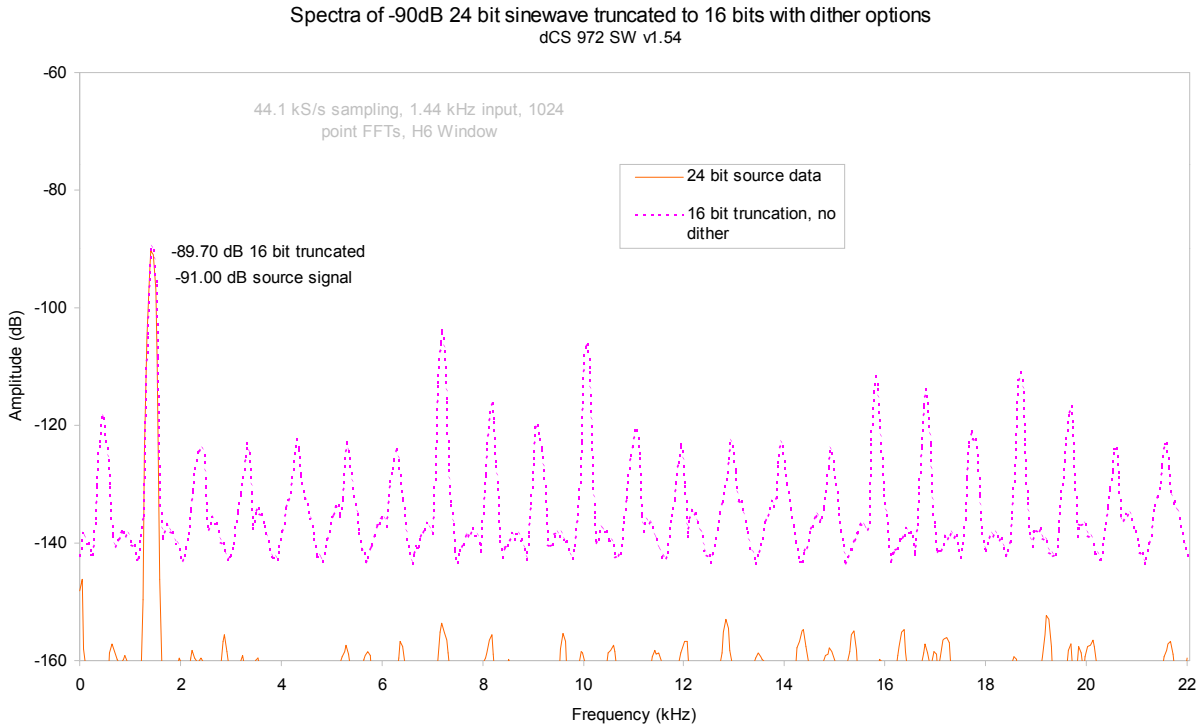


Figure 36 – Truncation Only Spectra

OPTIONS

Mains Voltage

We ship with the mains wired according to the destination. The voltage option should be specified when the unit is ordered, by specifying the country of use. It can be updated later by your dealer, if necessary.

Video Frequency VCXOs

We can fit additional video frequency VCXOs (enabling frequencies such as 44.056 kS/s and 47.952 kS/s). These are best fitted at ***dCS***, to allow full checking.

P3D, DSD Pro and Other Formats

We can fit larger FPGAs to allow P3D, DSD Pro and other formats. This has to be done at ***dCS***.

Ordering Options For A New Unit

To order any option, just tell us:

dCS 904 for use in <*country*>, with options ….

IMPORTANT! *Always specify the intended country of operation, otherwise we will assume that country of delivery is the same as country of operation.*

Having Your Options Changed

dCS support modifications, updates and option changes to supplied ***dCS 904*** units. If you are in any doubt, please contact your Distributor or ***dCS***. In general, these will be carried out at ***dCS***, because we have extensive test facilities and can verify the changes.

IMPORTANT! *Please do not attempt the changes yourself. The unit's performance and reliability may be impaired, and the warranty will be invalidated.*

MAINTENANCE AND SUPPORT

Hardware

Service & Maintenance

dCS audio products are designed not to need regular maintenance, and contain no user serviceable parts:

- there are no moving parts,
- there are no short life or wear-out parts used,
- the units have no holes through which liquids or
- contamination can normally enter,
- no dust deposits build up to degrade performance.

All parts are replaceable or upgradeable by ***dCS***, for a period of at least five years from the date you purchased your unit. If your unit is damaged in some way, please contact your Distributor or ***dCS***.

User Changeable Parts

There are no user serviceable parts inside the case. Routine maintenance is not necessary and repairs are generally carried out by ***dCS***, since this allows us to thoroughly verify the results before shipment.

There is a mains fuse in the mains socket, accessible from the outside of the unit. This may be changed by the user. The current consumption of the unit is very low (150 mA at 110 V) so it only blows if there is a fault - usually if the unit is set to its low voltage setting (100 - 120V) but has been plugged into a high voltage mains (220 - 240V). Usually no other damage is caused, but if the fuse blows repeatedly on replacement, some other damage will have been done and the unit must be returned to ***dCS*** for repair.

Fuse Type : 20 x 5mm 2 amp HRC fuse

If the fuse should fail, it is essential that it be replaced with one of the same type. Failure to do so could result in damage to the unit and may invalidate the guarantee. To gain access to the fuse, remove the IEC mains connector, use a small flat bladed screwdriver to pry up the tab on the fuse carrier and pull it out. Push the fuse out of the clip in the carrier and replace it with a new one. Push the carrier back into the unit so that it clicks home.

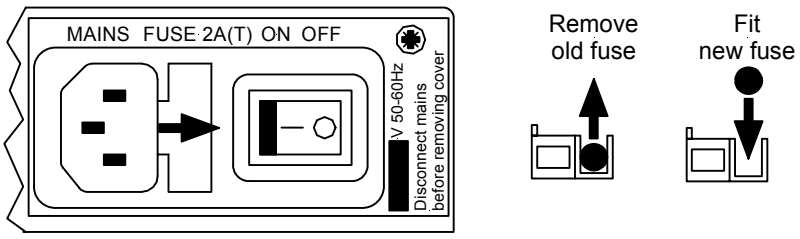


Figure 37 – Changing Mains Fuse

IMPORTANT! *Disconnect from the mains before changing the fuse.*

Software

Installing New Software

Updated operating software can be downloaded via the RS-232 link from a PC comm. port, using the Windows Remote software running on the PC, or can be copied from an EPROM installed internally.

Using the RS-232 download is hands free, but takes about 40 mins per unit. With special software (contact dCS) multiple units can be daisy chained together so that one PC can update them all serially (overnight).

To update the software by the RS-232 link, load the new software into a convenient directory on the PC, then run the Windows Remote programme with whatever units you want connected. The software will scan the RS-232 chain for units (this takes a while) to see what it thinks is connected, and then reports back. For each unit there is an **Info** button. Select the **Info** button for the unit you wish to update, and then select **Download Flash**. The programme will prompt you for the file to use, and then will start the download. If you want to programme many units automatically (say overnight) contact dCS for special software to enable this function.

IMPORTANT!

Do not turn the unit off until the download is complete. The unit has to erase its current programme before it can store the new one, so if the power is turned off, its internal programme store will have been erased but no new programme installed. Contact dCS if this happens inadvertently – the situation can be recovered if it does happen, but it involves taking the lid off the unit.

To find out if there are any software updates available for your equipment, call us, or email us, with your units serial number, or check our web site (www.dcsltd.co.uk). In general, software updates are free. Manuals for updated software can be downloaded from our web site, or just call us.

During An Update …

As soon as the download starts, the ADC will display **Prog**. The Windows programme will say **Erasing Flash** (10 secs), then **Flash Erased** (quick) then **Programming Flash**. At this stage a progress bar with a count down time is displayed, showing how much time is left (30 mins or so). After this has counted down, the PC says **Done** and the ADC reboots itself. Depending on the nature of the software update, it unit may then need to re-initialise its internals – if it does it will say **Hold** on its front panel. Do not do anything at this stage. Then, when that message disappears, it will be back to normal use.

Hardware Update or Calibration

You may wish to have your unit updated occasionally. ***dCS*** offer this service - we will install any modifications or hardware updates that have occurred since your unit was first shipped, and give the unit a full retest to current standards, including re-calibrating its VCXOs (which drift over time). The price will depend on the hardware changes necessary – so contact your dealer or us. In order to ensure speedy turn around please contact us prior to returning the unit.

Warranty

Your ***dCS 954*** is guaranteed for a period of 12 months against faulty workmanship or materials. Warranty repairs should only be carried out by ***dCS*** or an authorised distributor. This warranty will be invalidated if the unit is misused or tampered with in any way.

Safety and Electrical Safety

There are no user serviceable parts inside the ***dCS 904*** and so there is no need to remove the covers, apart from front panel software updates. If for some reason you do:

IMPORTANT! *Disconnect from the mains before removing any covers or changing the fuse.*

There are no substances hazardous to health inside the ***dCS 904***.

TROUBLESHOOTING

Error Codes and Messages

The error codes reported by ***dCS 904*** provide an effective means to diagnose the majority of problems that may be encountered in use - including problems with the overall system the unit operates in, internal device warnings and internal device failures. Please note that through damage or component failure, the unit self check may fail to operate. If this happens, please contact your distributor or ***dCS*** for assistance.

Internal Device Error Codes

Sometimes the unit may misbehave. If there is an internal reason, an internal device error code may be displayed as follows:

Err.xy an error xy (see table below) has been detected

where xy values have the following meanings:

Code	Description
01	E^2 memory (EEPROM) not present
02	Error initialising DSP
03	Error loading DSP
04	Error initialising DSP for coefficients
05	Error initialising DSP for coefficients
06	Error loading DSP coefficients
07	Error loading DSP coefficients
08	Error sending command
09	Error sending command
10	Error sending command
11	Error sending command
12	Error with LSB/MSB configuration
13	Error with LSB/MSB configuration
14	Error with LSB/MSB configuration
15	Error configuring FPGA
99	DSP error

Table 13 - Internal Error Codes

If you get any of these, please contact ***dCS***, with as much information as possible to help us re-create the problem. Some of these may have hardware problems as their cause, some may have software.

System Messages and Error Codes

Some other messages may be displayed that give indications of errors from other sources (outside the unit):

Display	Description
n.Aud	The data has been flagged by an AES3 message as non audio (perhaps a CD ROM). This message may also be displayed briefly when the sample rate is changed.
Hot	The unit is overheating, and performance may suffer.
Ouch	The unit is seriously overheating and should be turned off before damage occurs
Bad Fs	The sample rate coming in is not one the unit can lock to, or there is an input signal quality problem.

Table 14 - System Error Codes

Trouble Shooting Your System

If you experience difficulties when using your ***dCS 904***, the following suggestions may help to resolve the problem.

The unit fails to power up

- Ensure there is power available on the mains cable and the unit's mains switch is On.
- Check the rated supply voltage shown on the rear of the unit matches the local supply voltage.
- Check that the fuse has not blown - if so, correct any obvious cause then replace the fuse as described in the section "User Changeable Parts".
- Check that the mains cable is pushed fully home into the mains inlet in the rear of the unit.

The audio output is low or absent

- Check that all cables are connected correctly and not damaged. Damaged cables are a VERY common source of malfunctions!
- Check that the source and destination equipments are switched on and correctly set up.
- Check that an audio signal is present on one or both of the inputs.
- Ensure "Mute" is not enabled - LED off.

The level trimmers on the rear panel do not change the input level

- Ensure the trim tool or screwdriver you are using is narrow enough to reach the adjuster (about 2.5mm or 0.1" diameter) and long enough (at least 12mm or 0.5").
- The trimmer may be at the end of its travel - try turning it several times the other way. It is a 20-turn device.

The Left and Right channels are swapped

- Check that the audio input cables are not reversed.
- Check that the channels are not swapped elsewhere in the system.
- In Dual AES mode, ensure that the AES 1 (or AES 3) output is connected to the input on the destination equipment for the Left channel data (probably labelled AES 1, AES A or Left) and AES 2 (or AES 4) output is connected to the input on the destination equipment for the Right channel data (probably labelled AES 2, AES B or Right). See the manual of the destination equipment for information.

- In Quad AES mode, ensure that AES 1, 2, 3 & 4 outputs are correctly connected to the corresponding inputs on the destination equipment. See the manual of the destination equipment for information.

One output channel is low or absent

- Check that all cables are connected correctly and not damaged. Damaged cables are a VERY common source of malfunctions!
- Check that the balance is not offset elsewhere in the system.
- If the level trimmers on the rear panel have been adjusted, check that one has not been set much lower than the other.

Clicks or crackles occur on the outputs

- Check that all cables are connected correctly and not damaged.
- Check that the overload LED does not light.

The unit fails to slave to a Master Clock

- Press the **Master/Slave** button to select Slave mode. If a suitable reference is connected, the LED should light and the unit should lock after a few seconds.
- Check that the Reference In or 75R In cable is connected correctly and not damaged.
- Check that the Master Clock is switched on, set to the right sample rate and does not require re-calibration.
- Connect a different piece of digital equipment to test the locking capability of the unit. If the condition persists, contact your Distributor or ***dCS***.

The unit slaves to Word Clock but not AES/EBU

- This can be caused by erroneous system messages. Contact your dealer or ***dCS*** for advice.

The Overload indicator will not go out

- Remove any input and reference input. If the condition persists, contact your dealer or ***dCS*** - the unit may be faulty.

External meter does not show overload, *dCS 904* does.

- The ***dCS 904*** monitors a number of internal points and data word values in its calculation of overload. This may cause it to indicate an overload while the final external data word may not show it - for example with a very narrow but large spike, that the low pass decimation filter may broaden out sufficiently that the output data does not saturate. It is likely that if the ***dCS 904*** says it is in overload, it is. You can choose to ignore it!
- Some digital meters are quite insensitive to overloads. Such equipment may include a sensitivity setting, where an overload is only flagged when a number of consecutive digital words saturate - typically 1, 2, 4 or 8 consecutive samples. There is some justification for this - single saturation events are not always audible. The ***dCS 904*** flags their presence - it is up to the recording engineer to decide what to do about it.

dCS SUPPORT

I wish ....

If you wish your unit did something it does not, or that this manual told you something it does not, or that we made something we currently do not - tell us. If we can fix it with software, or a manual reprint, and we do so - we will update your unit free of charge. If we do decide to make the thing, we will discuss with you how you would like it to operate.

We value our customers, and we want to make products that do what you want.

If You Need More Help

The please contact *dCS*. Our office hours are 8:00 am to about 7:00 pm, Monday to Friday, UK time (UTC in summer, or UTC + 1hr in winter). Contact us by phone or fax on:

	Inside the UK	Outside the UK
Telephone	01799 531 999	+44 1799 531 999
Fax	01799 531 681	+44 1799 531 681

Table 15 – *dCS* Phone Numbers

You can write to us at:

dCS Ltd
Mull House
Great Chesterford Court
Great Chesterford
Saffron Walden CB10 1PF
UK

Our E-Mail address: more@dcsltd.co.uk

Our web site is: http://www.dcsltd.co.uk

Other Information

dCS produce technical notes from time to time, on issues related to ADCs. If you are interested in these, please do not hesitate to contact us, or check our web site.

INDEXES AND SOFTWARE VERSION NUMBERS

This manual is for standard software version 1.5x. and P3D unit software v1.36. v1.5x differs from v1.3x in having substantially improved DSD modulators, and in having a more friendly menu structure, with readback on current settings without having to change the settings.

Definitions of Units

dB0	Level in decibels, referred to a full scale sine wave in a sampled system. So, 0 dB0 is full scale.
dBu	Level in decibels, referred to a 0.775V rms sine wave, with no external loading (u = unloaded). The level of 0.775V is derived from the older dBm, for which the reference level is 1mW of signal power into a 600Ω termination from an output with 600Ω source impedance.
dBV	Level in decibels, referred to a 1.0V rms sine wave, with no external loading.
kS/s	Sample rate in kilo-samples per second. This replaces kHz which is technically incorrect when referring to sample rates.
ADC	Analogue to Digital converter, also known as an A/D
DAC	Digital to Analogue converter, also known as a D/A
DDC	DSP operations that change the data. Digital to Digital converter – used for format conversion and some

Full Contents

Tables

Figures

Keywords and Phrases