Insulated-Gate Transistors Simplify AC-Motor Speed Control

Application Note | September 1993 | AN-7511

An IGT's few input requirements and low On-state resistance simplify drive circuitry and increase power efficiency in motor-control applications. The voltage-controlled, MOSFET-like input and transfer characteristics of the insulated-gate transistor (IGT) (see EDN, September 29, 1983, pg 153 for IGT details) simplify power-control circuitry when compared with bipolar devices. Moreover, the IGT has an input capacitance mirroring that of a MOSFET that has only one-third the power-handling capability. These attributes allow you to design simple, low-power gate-drive circuits using isolated or level-shifting techniques. What's more, the drive circuit can control the IGT's switching times to suppress EMI, reduce oscillation and noise, and eliminate the need for snubber networks.

Use Optoisolation To Avoid Ground Loops

The gate-drive techniques described in the following sections illustrate the economy and flexibility the IGT brings to power control: economy, because you can drive the device's gate directly from a preceding collector, via a resistor network, for example; flexibility, because you can choose the drive circuit's impedance to yield a desired turn-off time, or you can use a switchable impedance that causes the IGT to act as a charge-controlled device requiring less than 10 nanocoulombs of drive charge for full turn-on.

Take Some Driving Lessons

Note the IGT's straightforward drive compatibility with CMOS, NMOS and open-collector TTL/HTL logic circuits in the common-emitter configuration Figure 1A. R_3 controls the turn-off time, and the sum of R_3 and the parallel combination of R_1 and R_2 sets the turn-on time. Drive-circuit requirements, however, are more complex in the common-collector configuration Figure 1B.

In this floating-gate-supply floating-control drive scheme, R_1 controls the gate supply's power loss, R_2 governs the turn-off time, and the sum of R_1 and R_2 sets the turn-on time. Figure 1C shows another common-collector configuration employing a bootstrapped gate supply. In this configuration, R_3 defines the turn-off time, while the sum of R_2 and R_3 controls the turn-on time. Note that the gate's very low leakage allows the use of low-consumption bootstrap supplies using very low-value capacitors. Figure 1 shows two of an IGT's strong points. In the common-emitter Figure 1A, TTL or MOS-logic circuits can drive the device directly. In the common-collector mode, you'll need level shifting, using either a second power supply Figure 1B or a bootstrapping scheme Figure 1C.

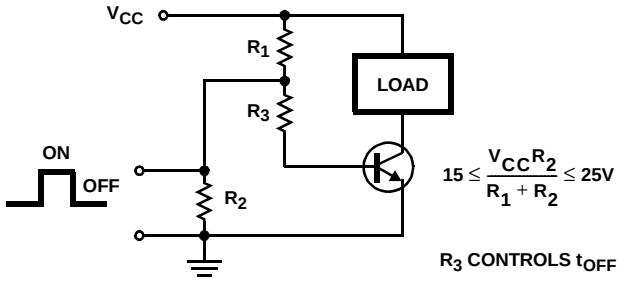

FIGURE 1A. SIMPLE DRIVING AND TRANSITION-TIME CONTROL

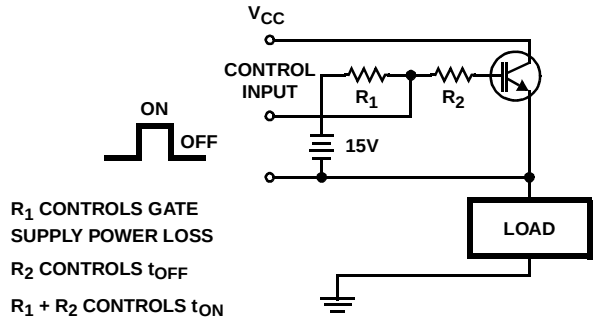

FIGURE 1B. A SECOND POWER SUPPLY

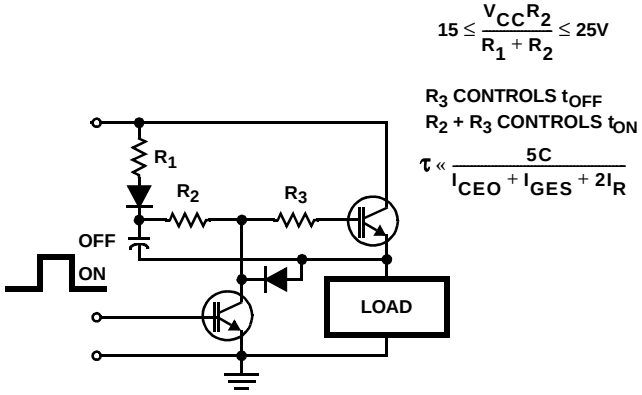

FIGURE 1C. BOOTSTRAPPING SCHEME

In the common-collector circuits, power-switch current flowing through the logic circuit's ground can create problems. Optoisolation can solve this problem (Figure 2A.) Because of the high common-mode dV/dt possible in this configuration, you should use an optoisolator with very low isolation capacitance; the H11AV specs 0.5pF maximum.

For optically isolated “relay-action” switching, it makes sense to replace the phototransistor optocoupler with an H11L1 Schmitt-trigger optocoupler (Figure 2B).) For applications requiring extremely high isolation, you can use an optical fiber to provide the signal to the gate-control photodetector. These circuit examples use a gate-discharge resistor to control the IGT’s turn-off time. To exploit fully the IGT’s safe operating area (SOA), this resistor allows time for the device’s minority carriers to recombine. Furthermore, the recombination occurs without any current crowding that could cause hot-spot formation or latch-up pnpn action. For very fast turn-off, you can use a minimal snubber network, which allows the safe use of lower value gate resistors and higher collector currents.

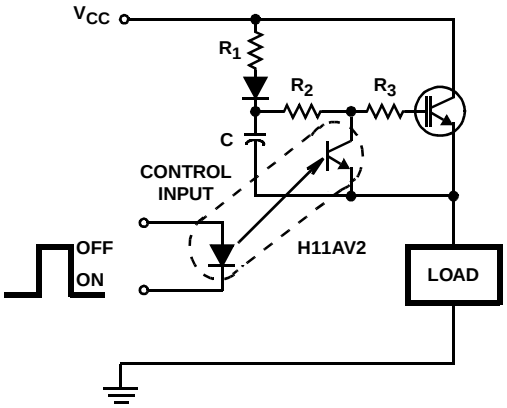

FIGURE 2A. AVOID GROUND-LOOP PROBLEMS BY USING AN OPTOISOLATOR. THE ISOLATOR IGNORES SYSTEM GROUND CURRENTS AND ALSO PROVIDES HIGH COMMON-MODE RANGE.

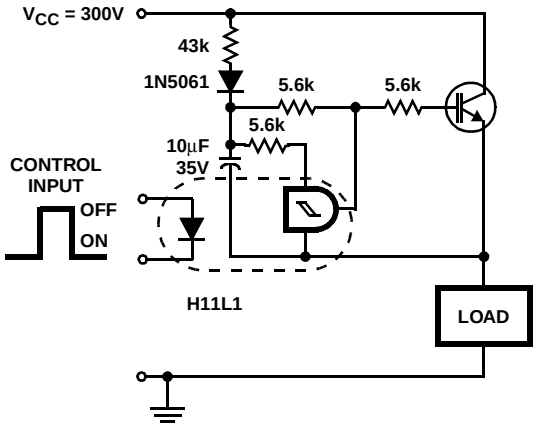

FIGURE 2B. A SCHMITT-TRIGGER OPTOISOLATOR YIELDS “SNAP-ACTION” TRIGGERING SIMILAR TO THAT OF A RELAY.

Pulse-Transformer Drive Is Cheap And Efficient

Photovoltaic couplers provide yet another means of driving the IGT. Typically, these devices contain an array of small silicon photovoltaic cells, illuminated by an infrared diode through a transparent dielectric. The photovoltaic coupler provides an isolated, controlled, remote dc supply without the need for oscillators, rectifiers or filters. What’s more, you can drive it directly from TTL levels, thanks to its 1.2V, 20mA input parameters.

Available photovoltaic couplers have an output-current capability of approximately 100μA. Combined with approximately 100kΩ equivalent shunt impedance and the IGT’s input capacitance, this current level yields very long switching times. These transition times (typically ranging to 1 msec) vary with the photovoltaic coupler’s drive current and the IGT’s Miller-effect equivalent capacitance.

Figure 3 illustrates a typical photovoltaic-coupler drive along with its transient response. In some applications, the photovoltaic element can charge a storage capacitor that’s subsequently switched with a phototransistor isolator. This isolator technique - similar to that used in bootstrap circuits provides rapid turn-on and turn-off while maintaining small size, good isolation and low cost.

In common-collector applications involving high-voltage, reactive-load switching, capacitive currents in the low-level logic circuits can flow through the isolation capacitance of the control element (eg, a pulse transformer, optoisolator, piezoelectric coupler or level-shift transistor). These currents can cause undesirable effects in the logic circuitry, especially in high-impedance, low-signal-level CMOS circuits.

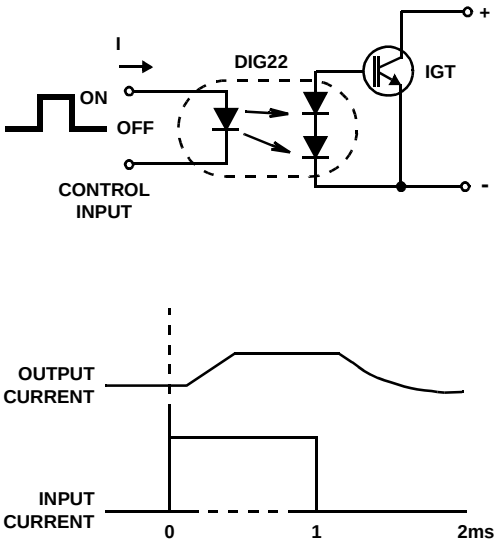

FIGURE 3. AS ANOTHER OPTICAL-DRIVE OPTION, A PHOTOVOLTAIC COUPLER PROVIDES AN ISOLATED, REMOTE DC SUPPIY TO THE IGT’S INPUT. ITS LOW 100μA OUTPUT, HOWEVER, YIELDS LONG IGT TURN-ON AND TURN-OFF TIMES.

The solution? Use fiber-optic components Figure 4 to eliminate the problems completely. As an added feature, this low-cost technique provides physical separation between the power and logic circuitry, thereby eliminating the effects of radiated EMI and high-flux magnetic fields typically found near power-switching circuits. You could use this method with a bootstrap-supply circuit, although the fiber-optic system’s reduced transmission efficiency could require a gain/speed trade-off. The added bipolar signal transistor minimizes the potential for compromise.

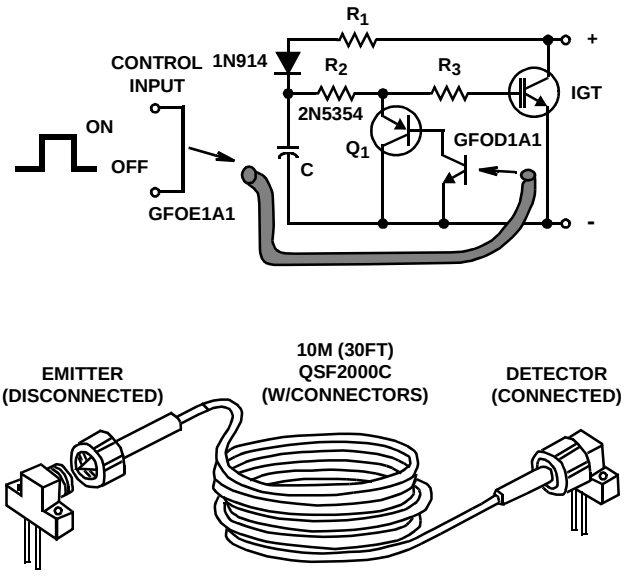

FIGURE 4. ELIMINATE EMI IN HIGH-FLUX OR NOISE ENVIRONMENTS BY USING FIBER-OPTIC COMPONENTS. THESE PARTS ALSO ALLEVIATE PROBLEMS ARISING FROM CAPACITIVE COUPLING IN ISOLATION ELEMENTS.

Piezos Pare Prices

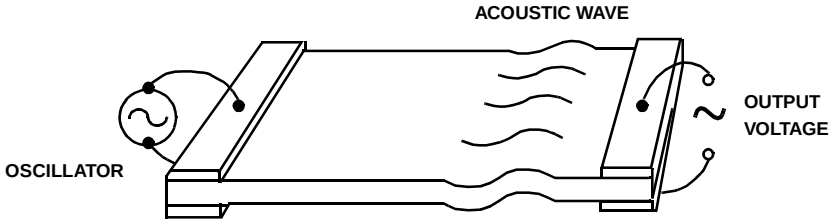

FIGURE 5A. YIELDING 4-kV ISOLATION, A PIEZOELECTRIC COUPLER PROVIDES TRANSFORMER-LIKE PERFORMANCE AND AN ISOLATED POWER SUPPLY.

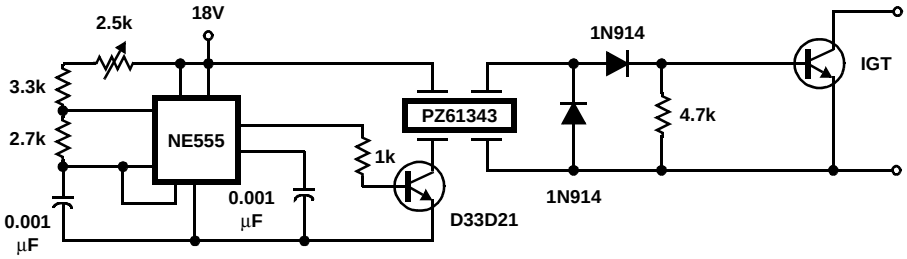

FIGURE 5B. THIS CIRCUIT PROVIDES THE DRIVE FOR THIS ARTICLE'S MOTOR-CONTROL CIRCUIT.

A piezoelectric coupler operationally similar to a pulse-train drive transformer, but potentially less costly in high volume is a small, efficient device with isolation capability ranging to 4kV. What's more, unlike optocouplers, they require no auxiliary power supply. The piezo element is a ceramic component in which electrical energy is converted to mechanical energy, transmitted as an acoustic wave, and then reconverted to electrical energy at the output terminals Figure 5A.

The piezo element's maximum coupling efficiency occurs at its resonant frequency, so the control oscillator must operate at that frequency. For example, the PZT61343 piezo coupler in Figure 5B's driver circuit requires a 108kHz, ±1%-accurate astable multivibrator to maximize mechanical oscillations in the ceramic material. This piezo element has a 1W max power handling capability and a 30mA p-p max secondary current rating. The 555 timer shown provides compatible waveforms while the RC network sets the frequency.

Isolate With Galvanic Impunity

Do you require tried and true isolation? Then use transformers; the IGT's low gate requirements simplify the design of independent, transformer-coupled gate-drive supplies. The supplies can directly drive the gate and its discharge resistor Figure 6, or they can simply replace the level-shifting supplies of Figure 2. It's good practice to use pulse transformers in drive circuitry, both for IGT's and MOSFETs, because these components are economical, rugged and highly reliable.

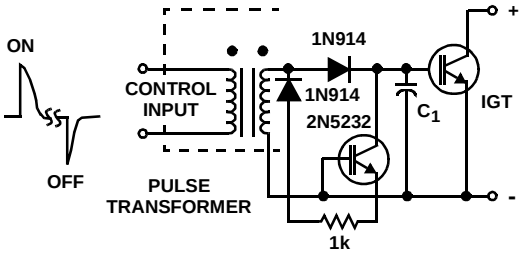

FIGURE 6A. PROVIDING HIGH ISOLATION AT LOW COST, PULSE TRANSFORMERS ARE IDEAL FOR DRIVING THE IGT. AT SUFFICIENTLY HIGH FREQUENCIES, C_1 CAN BE THE IGT'S GATE-EMITTERCAPACITANCE ALONE.

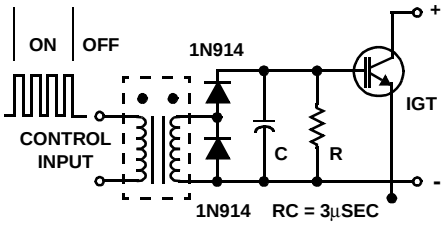

FIGURE 6B. A HIGH-FREQUENCY OSCILLATOR IN THE TRANSFORMER'S PRIMARY YIELDS UNLIMITED ON-TIME CAPABILITY.

In the pulse-on, pulse-off method Figure 6A, C_1 stores a positive pulse, holding the IGT on. At moderate frequencies (several hundred Hertz and above), the gate-emitter capacitance alone can store enough energy to keep the IGT on; lower frequencies require an additional external capacitor. Use of the common-base n-p-n bipolar transistor to discharge the capacitance minimizes circuit loading on the capacitor. This action extends continuous on-time capability without capacitor refreshing; it also controls the gate-discharge time via the 1kΩ emitter resistor.

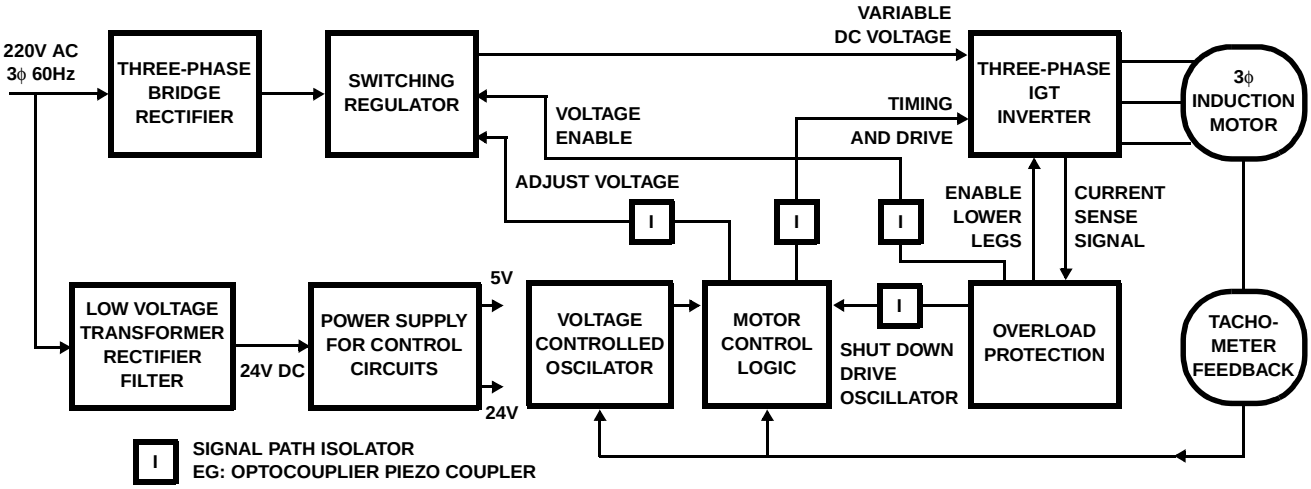

FIGURE 8. THIS 6-STEP 3-PHASE-MOTOR DRIVE USES THE IGT-DRIVE TECHNIQUES DESCRIBED IN THE TEXT. THE REGULATOR ADJUSTS THE OUTPUT DEVICES' INPUT LEVELS; THE VOLTAGE-CONTROLLED OSCILLATOR VARIES THE SWITCHING FREQUENCY AND ALSO PROVIDES THE CLOCK FOR THE 3-PHASE TIMING LOGIC. THE V/F RATIO STAYS CONSTANT TO MAINTAIN CONSTANT TORQUE REGARDLESS OF SPEED.

Piezoelectric Couplers Provide 4-kV Isolation

Using a high-frequency oscillator for pulse-train drive Figure 6B yields unlimited on-time capability. However, the scheme requires an oscillator that can be turned on and off by the control logic. A diode or zener clamp across the transformer's primary will limit leakage-inductance flyback effects. To optimize transformer efficiency, make the pulses' voltage x time products equal for both the On and the Off pulses. In situations where the line voltage generates the drive power, a simple relaxation oscillator using a programmable unijunction transistor can derive its power directly from the line to provide a pulse train to the IGT gate.

The circuit shown in Figure 7 accommodates applications involving lower frequencies (a few hundred Hertz and below). The high oscillator frequency (greater than 20kHz) helps keep the pulse transformer reasonably small. The voltage-doubler circuitry improves the turn-on time and also provides long on-time capability. Although this design uses only a 5V supply on the primary side of a standard trigger transformer, it provides 15V gate-to-emitter voltage.

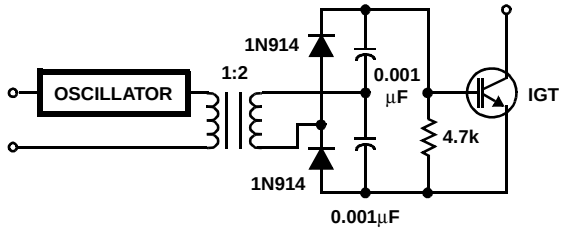

FIGURE 7. THIS DRIVING METHOD FOR LOW-FREQUENCY SWITCHING PROVIDES 15V TO THE IGT'S GATE

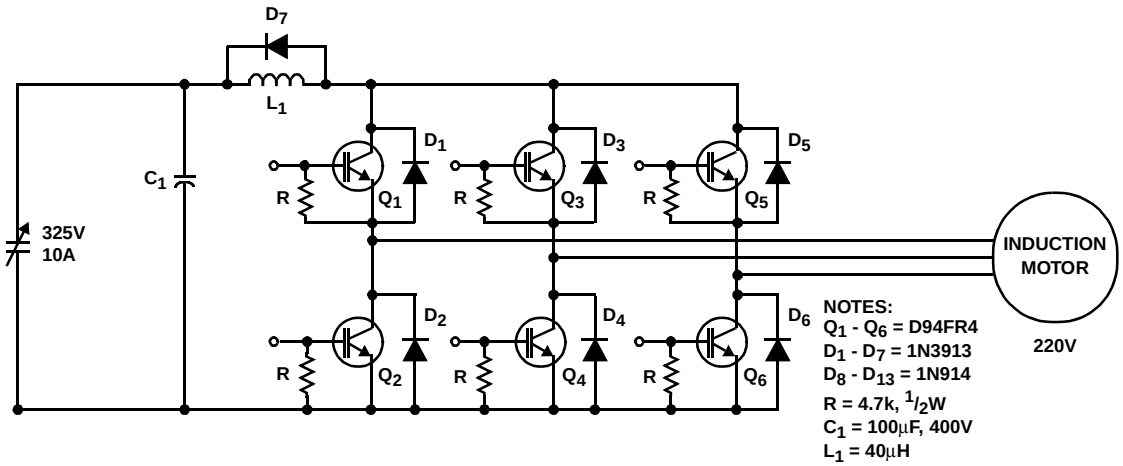

FIGURE 9A. THE POWER INVERTER'S DRIVE CIRCUIT USES SIX IGTS TO DRIVE A 2-HP MOTOR.

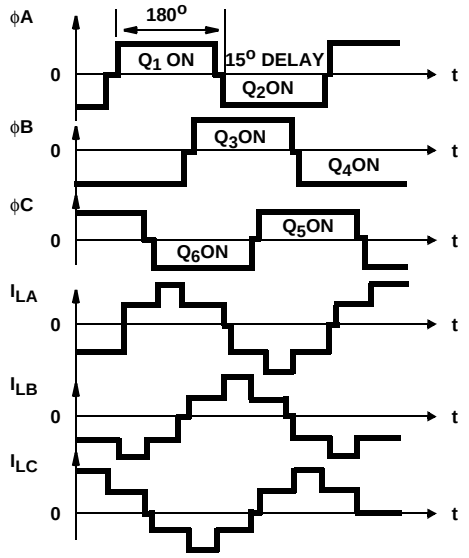

FIGURE 9B. THE TIMING DIAGRAM SHOWS THAT EACH IGT CONDUCTS FOR 165°× OF EVERY 360° CYCLE; THE DELAY IS NECESSARY TO AVOID CROSS CONDUCTION.

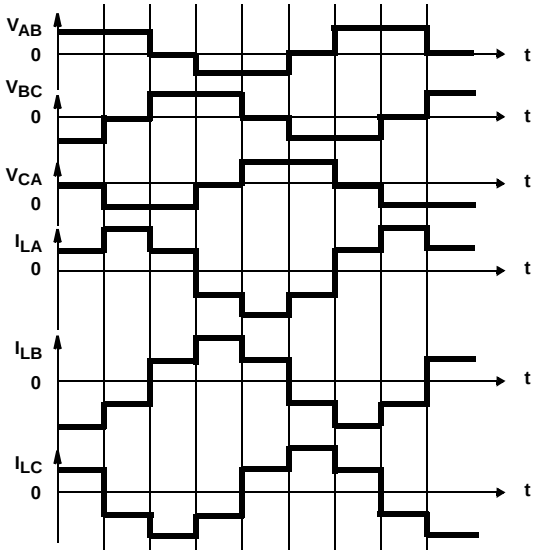

FIGURE 9C. THE THREE WINDINGS' VOLTAGES AND CURRENTS ARE SHOWN. NOTE THAT ALTHOUGH COSTLY SNUBBER NETWORKS ARE ELIMINATED, FREEWHEELING DIODES ARE NEEDED; THE IGTS HAVE NO INTRINSIC OUTPUT DIODE.

Polyphase motors, controlled by solid-state, adjustable-frequency ac drives, are used extensively in pumps, conveyors, mills, machine tools and robotics applications. The specific control method could be either 6-step or pulse-width modulation. This section describes a 6-step drive that uses some of the previously discussed drive techniques (see page 11, "Latch-Up: Hints, Kinks and Caveats").

Figure 8 defines the drive's block diagram. A 3-phase rectifier converts the 220V ac to dc; the switching regulator varies the output voltage to the IGT inverter. At the regulator's output, a large filter capacitor provides a stiff voltage supply to the inverter.

The motor used in this example has a low slip characteristic and is therefore very efficient. You can change the motor's speed by varying the inverter's frequency. As the frequency increases, however, the motor's air-gap flux diminishes, reducing developed-torque capability. You can maintain the flux at a constant level (as in a dc shunt motor) if you also vary the voltage so the V/F ratio remains constant.

Fiber-Optic Drive Eliminates Interference

In the example given, the switching regulator varies the IGT inverter's output by controlling its dc input; the voltage-controlled oscillator (VCO) adjusts the inverter's switching frequency, thereby varying the output frequency. The VCO also drives the 3-phase logic that provides properly timed pulsed outputs to the piezo couplers that directly drive the IGT.

Sensing the dc current in the negative rail and inhibiting the gate signal protect the IGT from overload and shoot-through (simultaneous conduction) conditions. If a fault continues to exist for an appreciable period, inhibiting the switching regulator causes the inverter to shut off. The inverter's power-output circuit is shown in Figure 9A; the corresponding timing diagrams show resistive-load current waveforms that indicate the 3-phase power Figure 9B and waveforms of the output line voltage and current Figure 9C.

In Figure 9's circuit, it appears that IGTs Q_1 through Q_6 will conduct for 180^o. However, in a practical situation, it's necessary to provide some time delay (typically 10^o to 15^o×) during the positive-to-negative transition periods in the phase current. This delay allows the complementary IGTs to turn off before their opposite members turn on, thus preventing cross conduction and eventual destruction of the IGTs.

Because of the time delay, the maximum conduction time is 165^o of every 360^o period. Because the IGTs don't have an integral diode, it's necessary to connect an antiparallel diode externally to allow the freewheeling current to flow. Inductor L_1 limits the di/dt during fault conditions; freewheeling diode D_7 clamps the IGT's collector supply to the dc bus.

The peak full-load line current specified by the motor manufacturer determines the maximum steady-state current that each transistor must switch. You must convert this RMS-specified current to peak values to specify the proper IGT. If the input voltage regulator had a fixed output voltage and a constant frequency, each IGT would be required to supply the starting locked-rotor current to the motor. This current could be as much as 15 times the full-load running current.

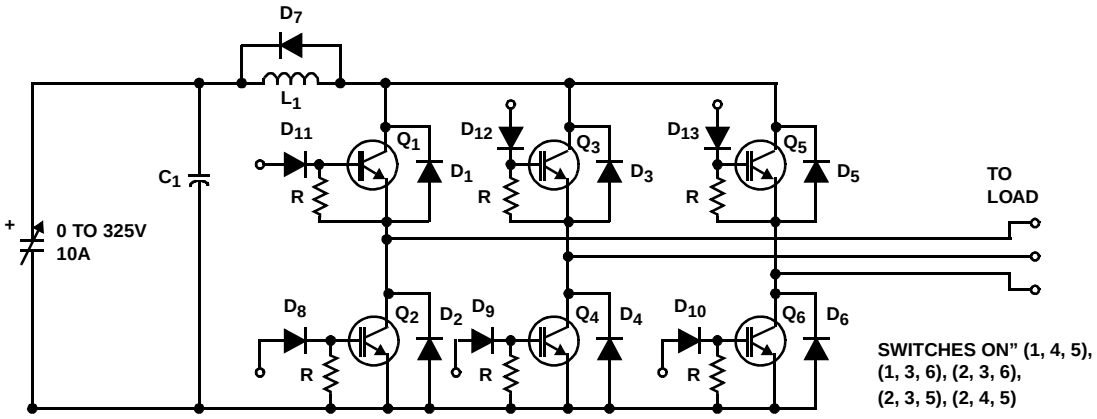

FIGURE 10A. COMPONENT SELECTION IS IMPORTANT. THE IGT SELECTED CIRCUIT HANDLES 10A, 500V AT 150°C. THE ANTIPARALLEL DIODES HAVE A SIMILAR CURRENT RATING.

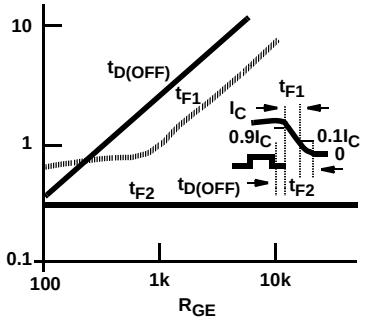

FIGURE 10B. SELECT R TO YIELD THE DESIRED TURN-OFF TIME. FINALLY, L1'S VALUE DETERMINES THE FAULT-CONDITION ACTION TIME.

It's impractical, however, to rate an inverter based on locked-rotor current. You can avoid this necessity by adjusting the switching regulator's output voltage and by providing a fixed output-current limit slightly higher than the maximum full-load current. This way, the current requirements during start-up will never exceed the current capability of an efficiently sized inverter.

For example, consider a 2-hp, 3-phase induction motor specifying V_L at 230V RMS and full-load current (I_{LFL}) at 6.2A RMS. For the peak current of 8.766A, you can select IGT type D94FR4. This device has a reverse-breakdown SOA (RBSOA) of 10A, 500V for a clamped inductive load at a junction temperature of 150^{o}C. A 400V IGT could also do the job, but the 500V choice gives an additional derating safety margin. You must set the current limit at 9A to limit the in-rush current during start-up. Note that thanks to the IGT's adequate RBSOA, you don't need turn-off snubbers.

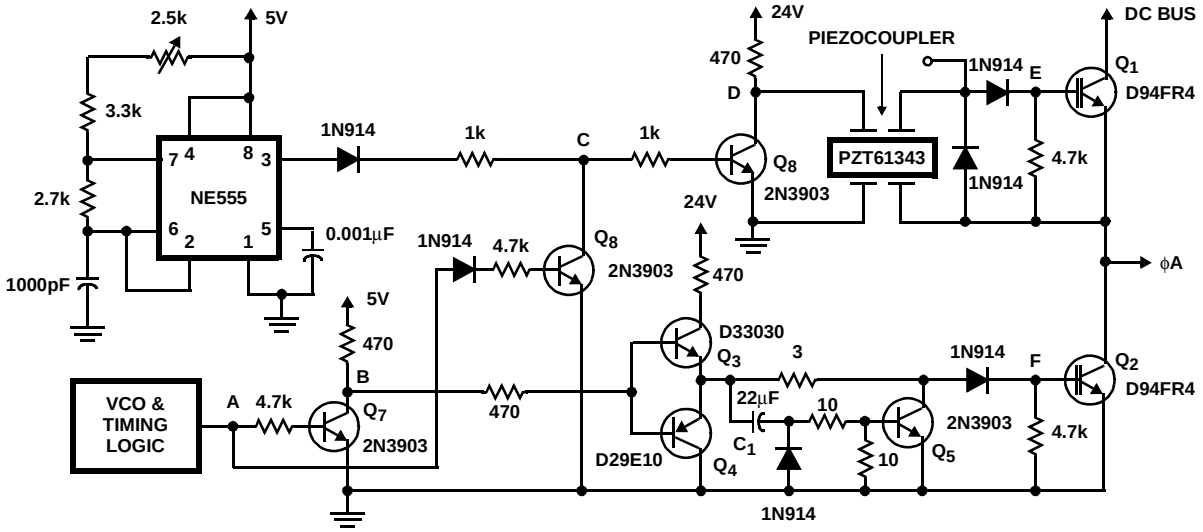

FIGURE 11A. PROVIDING PROPERLY TIMED DRIVE TO THE IGTS, THE CIRCUIT USES PIEZO COUPLING TO THE UPPER POWER DEVICE. THE 3-TRANSISTOR DELAY CIRCUIT PROVIDES THE NEEDED 15^{O} LAG TO THE LOWER IGT TO AVOID CROSS CONDUCTION.

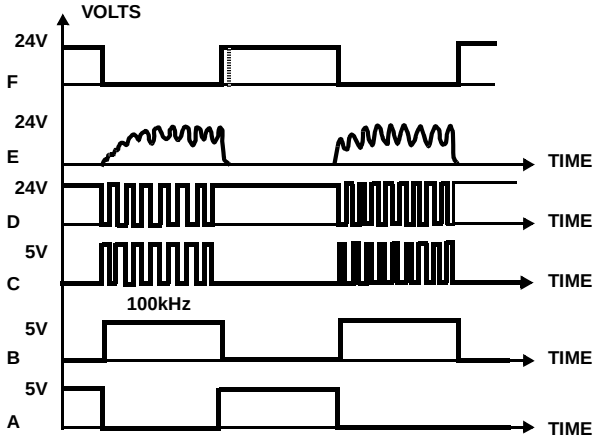

FIGURE 11B. THE TIMING DIAGRAM SHOWS THE 555'S 108-KHz DRIVE TO THE PIEZO DEVICE AND THE LATTER'S SLOW RESPONSE.

Use 6-Step Drive For Speed-Invariant Torque

Figure 10A shows the inverter circuit configured for this example. Diodes D_1 through D_6 carry the same peak current as the IGTs; consequently, they're rated to handle peak currents of at least 8.766A. However, they only conduct for a short time (15^o to 20^o of 180^o), so their average-current requirement is relatively small.

External circuitry can control the IGT's current fall time. Resistor R controls t_{F1} Figure 10B; there's no way to control t_{F2}, an inherent characteristic of the selected IGT. In this example, a 4.7-kΩ gate-to-emitter resistor provides the appropriate fall time. The choice of current-limiting inductor L_1 is based on the IGT's overload-current rating and the action time (the sum of the sensor's sensing and response time and the IGT's turn-off time) in fault conditions.

You could use a set of flip flops and a multivibrator to generate the necessary drive pulses and the corresponding 120^o× delay between the three phases in Figure 10's circuit. A voltage-controlled oscillator serves to change the inverter's output frequency. In this circuit, IGTs Q_1, Q_3 and Q_5 require isolated gate drive; the drive for Q_2, Q_4 and Q_6 can be referred to common. If you use optocouplers for isolation, you'll need three isolated or bootstrap power supplies (in addition to the 5V and 24V power supplies) to drive the IGTs. Another alternative is to use transformer coupling.

165^o Conduction Prevents Shoot-Through

Consider, however, using Figure 11A's novel, low-cost circuit. It uses a piezo coupler to drive the isolated IGT. As noted, the coupler needs a high-frequency square wave to induce mechanical oscillations in its primary side. The 555 oscillator provides the necessary 108-kHz waveform; its output is gated according to the required timing logic and then applied to the piezo coupler's primary. The coupler's rectified output drives the IGT's gate; the 4.7kW gate-to-emitter resistor provides a discharge path for C_{GE} during the IGT's turn-off. The circuit's logic-timing diagram is shown in Figure 11B.

The piezo coupler's slow response time Figure 12A contributes approximately 2^o to the 15^o to 20^o turn-on/turn-off delay needed to avoid shoot-through in the complementary pairs. The corresponding collector current is shown in Figure 12B. C_1 and its associated circuitry provide the remaining delay as follows:

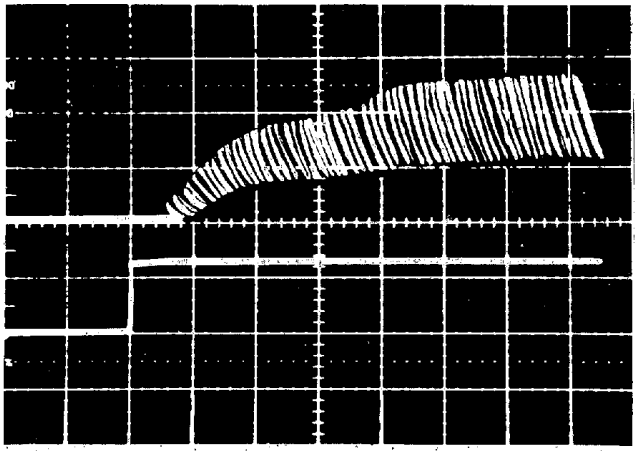

FIGURE 12A. THE PIEZO COUPLER'S SLOW RESPONSE IS NOT A DISADVANTAGE IN THIS ARTICLE'S CIRCUIT. IN FACT, IT CONTRIBUTES 2^o TO THE REQUIRED 15^o TURN-ON/TURN-OFF DELAY.

TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	200µSEC/DIV
B	5V/DIV	200µSEC/DIV

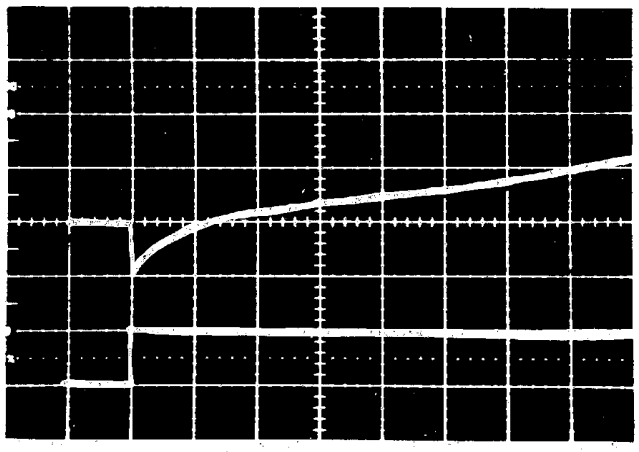

FIGURE 12B. THE DRIVEN IGT'S COLLECTOR CURRENT IS SHOWN

TRACE	VERTICAL	HORIZONTAL
A	3A/DIV	200µSEC/DIV
B	5V/DIV	200µSEC/DIV

When Q_3's base swings negative, C_1 - at this time discharged - turns on Q_5. Once C_1 is charged, Q_5 turns off, allowing a drive pulse to turn the IGT on. When Q_7's base goes to ground, Q_4 turns on and discharges C_1, initiating the IGT's turn-off. Figure 13 shows the motor current and corresponding line voltage under light-load Figure 12A and full-load Figure 12B conditions.

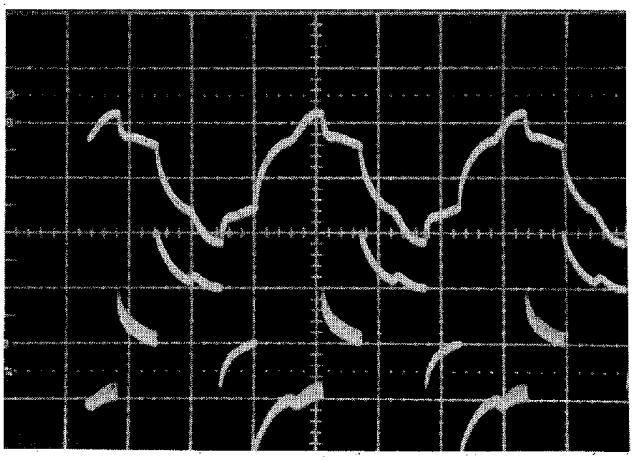

FIGURE 13A. MOTOR CURRENT AND VOLTAGE ARE SHOWN HERE, FOR LIGHT LOADS

TRACE	VERTICAL	HORIZONTAL
A	1A/DIV	1mSEC/DIV
B	50V/DIV	1mSEC/DIV

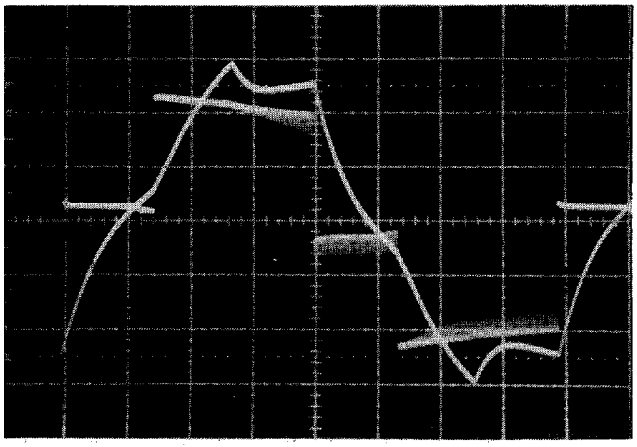

FIGURE 13B. MOTOR CURRENT AND VOLTAGE ARE SHOWN HERE, FOR HEAVY LOADS.

TRACE	VERTICAL	HORIZONTAL
A	3A/DIV	2mSEC/DIV
B	100V/DIV	2mSEC/DIV

To complete the design of the 6-step motor drive, it's necessary to consider protection circuitry for the output IGTs. The drive receives its power from a switching supply already containing provisions for protection from line over-voltage and under-voltage and transient effects. However, you still have to guard the power switches against unwanted effects on the output lines and the possibility of noise or other extraneous signals causing gate-drive timing errors.

The best protection circuit must match the characteristics of the power switch and the circuit's bias conditions. The IGT is very rugged during turn-on and conduction, but it requires time to dissipate minority carriers when turning off high currents and voltages. An analysis of the possible malfunction condition

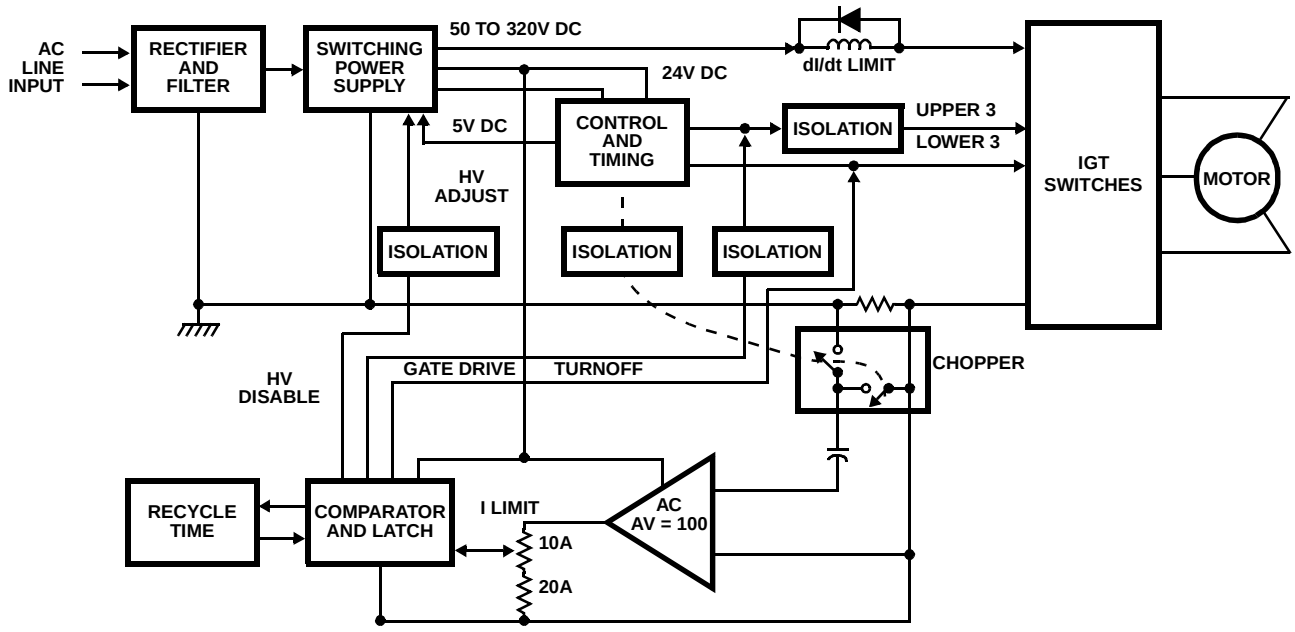

FIGURE 14. THE LOWEST COST SENSOR IMAGINABLE, A PIECE OF COPPER WIRE SERVES AS THE CURRENT MONITOR IN THIS SYSTEM. THE CHOPPED AND AMPLIFIED VOLTAGE DROP ACROSS THE WIRE TRIGGERS A GATE-DRIVE SHUT-OFF CIRCUIT UNDER FAULT CONDITIONS.

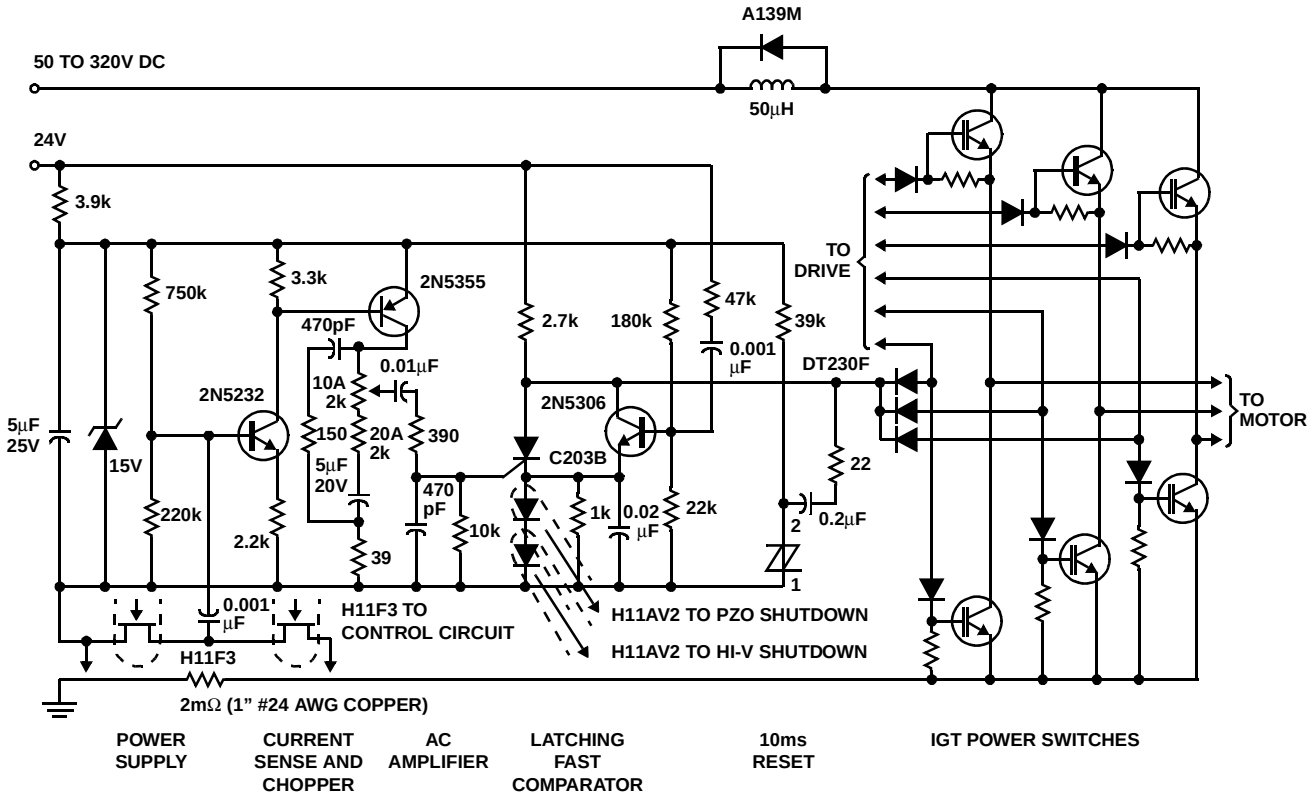

FIGURE 15A. THIS ALL-ENCOMPASSING PROTECTION SYSTEM PROVIDES THREE INDEPENDENT SHUTDOWN FUNCTONS - ONE EACH FOR THE UPPER AND LOWER IGTS AND THE HIGH-VOLTAGE SUPPLY.

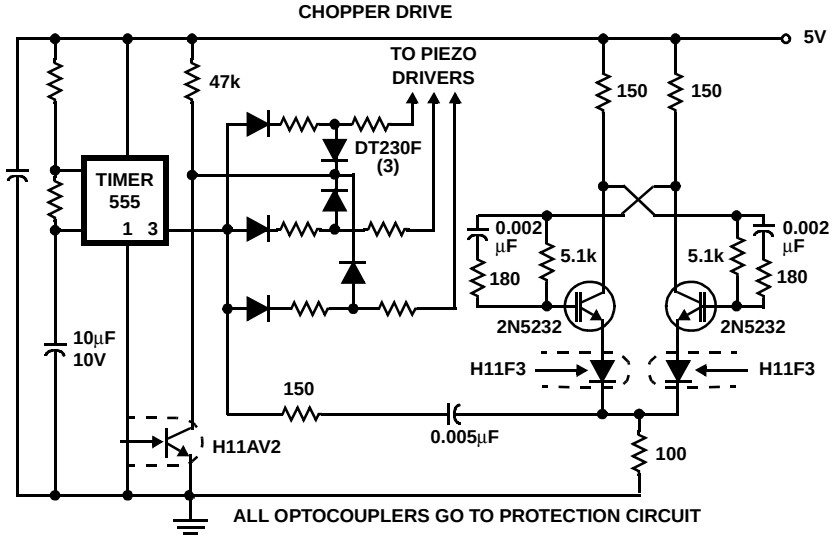

FIGURE 15B. THIS CIRCUIT PROVIDES CHOPPER DRIVE FOR THE COPPER-WIRE SENSOR IN FIGURE 15A.

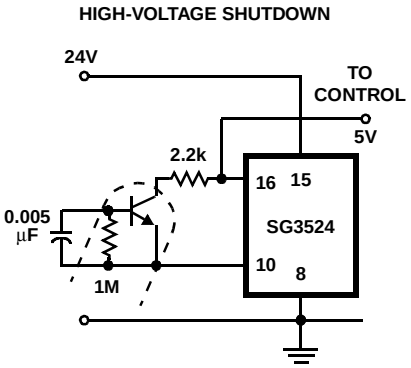

FIGURE 15C. SHOWS THE HIGH-VOLTAGE SHUTDOWN CIRCUIT.

Latch-Up: Hints, Kinks and Caveats

The IGT is a rugged device, requiring no snubber network when operating within its published safe-operating-area (SOA) ratings. Within the SOA, the gate emitter voltage controls the collector current. In fact, the IGT can conduct three to four times the published maximum current if it's in the ON state and the junction temperature is +150^{O}C maximum.

However, if the current exceeds the rated maximum, the IGT could lose gate control and latch up during turn-off attempts. The culprit is the parasitic SCR formed by the pnpn structure shown in Figure 16. In the equivalent circuit, Q_1 is a power MOSFET with a normal parasitic transistor (Q_2) whose base-emitter junction is shunted by the low-value resistance R_1.

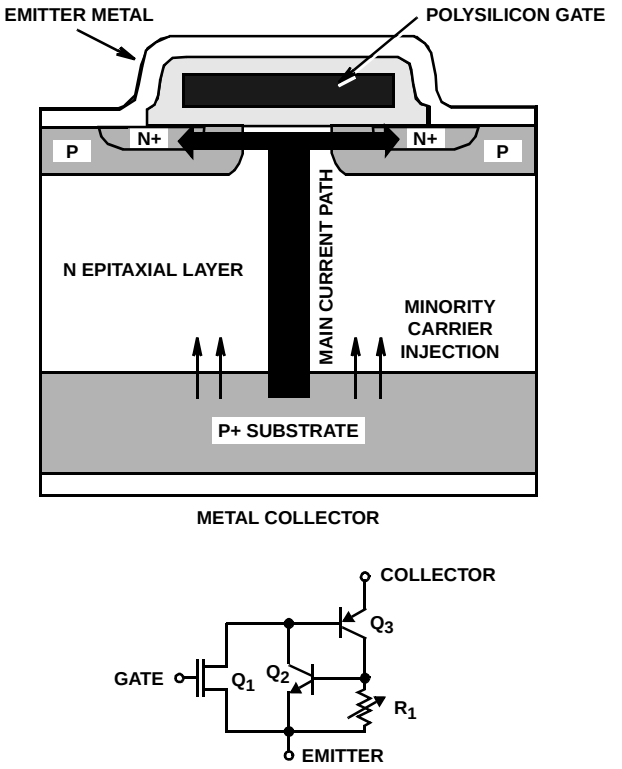

FIGURE 16. THE IGT'S PARASITIC SCR IS RESPONSIBLE FOR THE DEVICE'S LATCH-UP CHARACTERISTICS.

For large current overloads, the current flowing through R_1 can provoke SCR triggering. In the simplest terms, R_1 represents the equivalent of a distributed resistor network, whose magnitude is a function of Q_2's V_{CE}. During normal IGT operation, a positive gate voltage (greater than the threshold) applied between Q_1's gate and source turns the FET on. The FET then turns on Q_3 (a pnp transistor with very low gain), causing a small portion of the total collector current to flow through the R_1 network.

To turn the IGT off, you must reduce the gate-to-emitter voltage to zero. This turns Q_1 off, thus initiating the turn-off sequence within the device. Total fall time includes current-fall-time one (t_{F1}) and current-fall-time two (t_{F2}) components. The turn-off is a function of the gate-emitter resistance, Q_3's storage time and the value of V_{GE} prior to turn-off. Device characteristics fix both the delay time and the fall time.

Forward-Bias Latch-Up

Within the IGT's current and junction-temperature ratings, current does not flow through Q_2 under forward-biased conditions. When the current far exceeds its rated value, the current flow through R_1 increases and Q_3's V_{CE} also increases because of MOSFET channel saturation. Once Q_3's I_CR_1 drop exceeds Q_2's $V_{BE(ON)}$, Q_2 turns on and more current flow bypasses the FET.

The positive feedback thus established causes the device to latch in the forward-biased mode. The value of I_C at which the IGT latches on while in forward conduction is typically three to four times the device's maximum rated collector current. When the collector current drops below the value that provokes Q_2 turn-on, normal operation resumes if chip temperature is still within ratings.

If the gate-to-emitter resistance is too low, the Q_2-Q_3 parasitic SCR can cause the IGT to latch up during turn-off. During this period, R_{GE} determines the drain-source dV/dt of power MOSFET Q_1. A low R_1 causes a rapid rise in voltage - this increases Q_2's V_{CE}, increasing both R_1's value and Q_2's gain.

Because of storage time, Q_3's collector current continues to flow at a level that's higher than normal for the FET bias. During rapid turn-off, a portion of this current could flow in Q_2's base-emitter junction, causing Q_2 to conduct. This process results in device latch-up; current distribution will probably be less uniform than in the case of forward-bias latch-up.

Because the gains of Q_2 and Q_3 increase with temperature and V_{CE}, latching current - high at +25^{O}C - decreases as a function of increasing junction temperature for a given gate-to-emitter resistance.

How do you test an IGT's turn-off latching characteristic? Consider the circuit in Figure 17. Q_1's base-current pulse width is set approximately 2µsec greater than the IGT's gate-voltage pulse width. This way, the device under test (DUT) can be switched through Q_1 when reverse-bias latch-up occurs. This circuit allows you to test an IGT's latching current nondestructively.

The results? Clamped-inductive-load testing with and without snubbers reveals that snubbering increases current handling dramatically: With RGE = 1kΩ, a 0.02µF snubber capacitor increases current capability from 6A to 10A; with RGE = 5kΩ, a 0.09µF snubber practically doubles capacity (25A vs 13A).

Conclusions? You can double the IGT's latching current by increasing RGE from 1kΩ to 5kΩ, and double it again with a polarized snubber using CS < 0.1µF. The IGT is therefore useful in situations where the device must conduct currents of five to six times normal levels for short periods.

Finally, you can also use the latching behavior to your advantage under fault conditions. In other words, if the device latches up during turn-off under normal operation, you could arrange it so that a suitable snubber is switched electronically across the IGT.

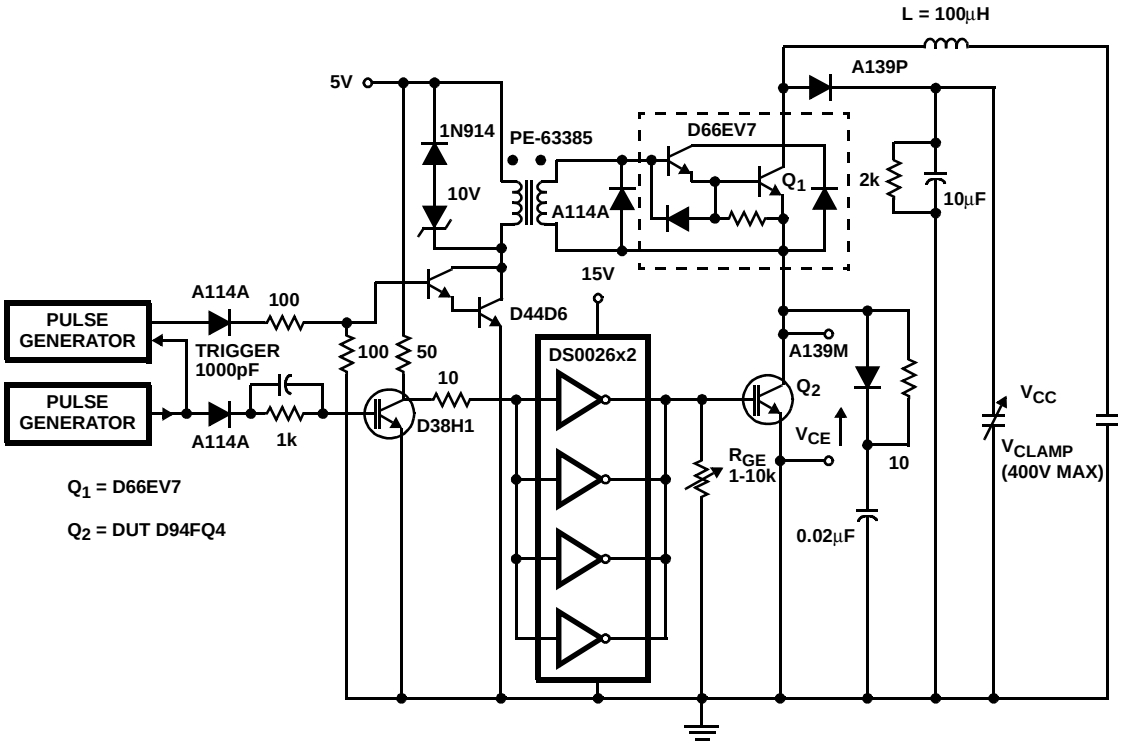

FIGURE 17. USE THIS LATCHING-CURRENT TESTER TO TEST IGTS NONDESTRUCTIVELY. Q_1'S BASE-DRIVE PULSE WIDTH IS GREATER THAN THAT OF THE IGT'S GATE DRIVE, SO THE IGT UNDER TEST IS SWITCHED THROUGH Q_1 WHEN REVERSE-BIAS LATCH-UP OCCURS.

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