

130nm node CMOS Process (CS90A)

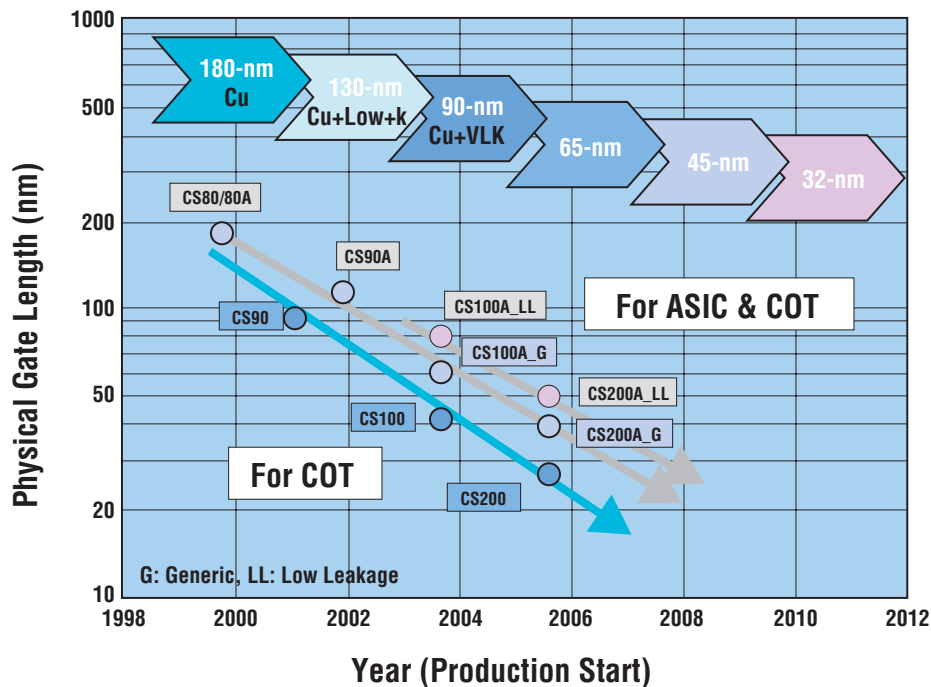
Features

Technology Code	CS90A			
Transistor	UHS	HS	ST	LL
Physical Gate Length (nm)	110	110	110	110
Gate Oxide Thickness (nm)	2.9	2.9	2.9	2.9
Supply Voltage (V)	1.2	1.2	1.2	1.2
NMOS Ids (μA/μm)	780	678	570	390
PMOS Ids (μA/μm)	-321	-276	-218	-150
NMOS Ioff (nA/μm)	36	4	0.18	0.005
PMOS Ioff (nA/μm)	-18	-3.1	-0.22	-0.015
Gate Leak Current (nA/μm)	0.01	0.01	0.01	0.01
Basic Gate Delay (ps)	14	17	28	45
Number of Available Poly Layer	1			
Number of Available Metal Layer	8Cu+1Al			
Via Filling	Cu Dual Damascene			
ILD Structure	Hybrid Low-k			
SRAM Cell Size (μm ²)	1.98			
Dual Gate Oxide Options	Available			
Mixed Signal Options	Available			
RF Elements	MIM cap., Poly Resistor, Inductor			
Fuse	RAM Redundancy			



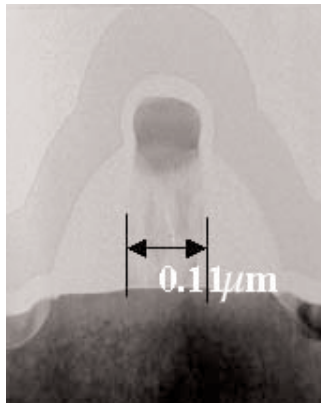
Mie plant

Technology Roadmap

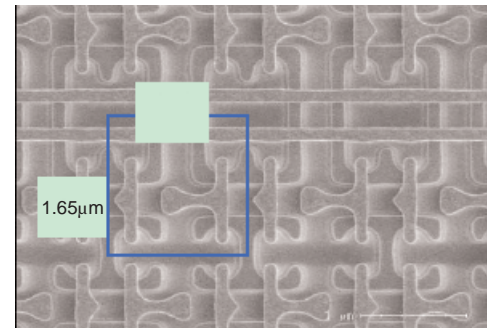


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Transistor

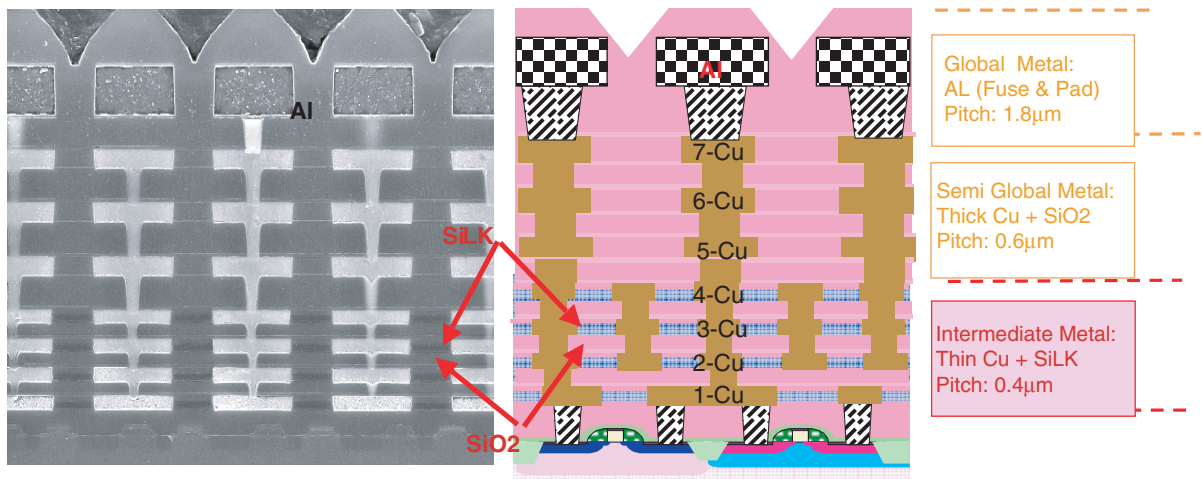


SRAM



Cell Size = $1.98\mu\text{m}^2$
 (1.2µm x 1.65µm)
 (2nd Generation SRAM)

Interconnect



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