HEWLETT hp PACKARD

SERVICE MANUAL

MODEL 3760A
DATA GENERATOR

SERIAL PREFIX: 1237-

This manual applied directly to HP Model 3760A Data Generator having serial prefix number 1237-.

OTHER SERIAL PREFIXES

For serial prefixes above 1237, a "Manual Changes" sheet is included with this manual.

Microfiche Part No. 03760-95025

These publications are also available in 6in x 4in microfiche form. Each sheet contains up to 60 pages, maximum, of text and illustrations.

03760-95000 Printed: NOVEMBER 1973

SPECIFICATIONS

Modes of Operation

PRBS NORMAL	Generates a repetitive $2^n - 1$ bit, maximal length, Pseudo Random Binary Sequence where n = 3 to 10 and 15.
PRBS ZERO ADD	Addition of a block of 1 to 99 zeros into PRBS NORMAL.
PRBS ERROR	Introduction of an error once per 2000 sequences by changing one bit to its logic complement.
1010	Generates a preset repetitive word, content 1010.
WORD NORMAL	Generates a continuous 3 to 10 bit word with selectable content.
WORD ZERO ADD	Addition of a block of 1 to 99 zeros into WORD NORMAL, occurring between words.

Clock Input

Rate	1.5 to 150MHz.
Impedance	50Ω ±5% dc coupled.
Trigger:	
Slope	+ve or -ve.
Manual	Level range -3 to +3V.
Auto	Input pulse mark: space ratio range 10:1 to 1:10.
Sensitivity	Better than 500mV.
Amplitude	±5V max.
Pulse width	3ns min.

Clock Output

Outputs	CLOCK or $\overline{\text{CLOCK}}$, from external or optional internal clock.
Impedance	Source impedance 50Ω ±5%.
Amplitude	Continuously variable in 5 ranges from 0.1 to 3.2V, symmetrical about offset level.
Rise/fall time	<1.2ns (10% to 90% level). <1.3ns for 75Ω
Overshoot	<10% of pulse amplitude.
DC Offset.	
Zero	<2% of pulse amplitude.
Variable	Continuous 0 to ±3V.

Options

001 75Ω CLOCK and DATA input/output impedances.

002 Internal variable frequency clock.
Rate: 1.5 to 150MHz
Jitter: <0.1% of period +0.1ns pk-pk

003 Options 001 and 002 combined

Data Output

Outputs	DATA and $\overline{\text{DATA}}$ simultaneously.
Format	RZ or NRZ.
Impedance	Source impedance 50Ω ±5%.
Amplitude	Continuously variable in 5 ranges from 0.1 to 3.2V, symmetrical about offset level.
Rise/fall time	<1.2ns (10% to 90% level). <1.3ns for 75Ω
Overshoot	<10% of pulse amplitude.
DC Offset:	
Zero	<2% of pulse amplitude.
Variable	Continuous 0 to ±3V.
Delay	Data (and Sync) delayed with respect to Clock continuously in 10 ranges from 0 – 100ns.

Sync Output

Rate	Once per PRBS or WORD cycle.
Duration:	
Normal	1 Clock period.
PRBS Error	1 Clock period.
Zero Add	Length of zero block plus 1 clock period.
Position:	
PRBS Normal	Front panel selectable.
Word Normal	Precedes word.
Zero Add	Precedes the zero block by 1 clock period.
PRBS Error	Precedes the error by 1 clock period.
Impedance	Source impedance 50Ω ±5%.
Amplitude	+1V.
Rise/Fall time	<2.5ns (10% to 90% level).

General

POWER: 90 to 125 or 200 to 250V 40 to 400Hz, consumption 90W	WEIGHT: 30lbs	DIMENSIONS: 16-3/4in wide 5-1/2in high 18-3/4in deep (425mm x 140mm x 467mm)

LIST OF CONTENTS

FRONT PANEL MODULE A1

SECTION VI
SERVICE (CONT.)

CLOCK MODULE A2

SECTION VI
SERVICE (CONT.)

DATA MODULE A3

SECTION VI
SERVICE (CONT.)

POWER SUPPLY MODULE A4

Figure 1-1 3760A Data Generator

SECTION I
GENERAL INFORMATION

INTRODUCTION

All the information necessary for the repair and maintenance of the *hp* 3760A Data Generator is given in this Service Manual under the following headings:

THEORY OF OPERATION	–	SECTION II
PERFORMANCE TESTS	–	SECTION III
ADJUSTMENT PROCEDURES	–	SECTION IV
TROUBLESHOOTING	–	SECTION V
SERVICE	–	SECTION VI

Operating Instructions for the 3760A Data Generator are given in the 3760A/61A Error Rate Measuring System Operating Manual. A copy of this publication is supplied with every Data Generator whether purchased as a separate instrument or as part of the System.

POWER CONNECTION

The 3760A has been designed to operate from 90 – 125V or 200 – 250V, 40 to 400Hz ac supply lines. The operating voltage is selected by a slide switch in the ac input module which is mounted on the rear panel. (The ac power cord must be removed before this switch can be operated). The appropriate fuse ratings are given in Table 1-1.

Table 1-1

Line Voltage	Slide Switch	Fuse Ratings
90 – 125V	115V	3.0A Timed
200 – 250V	230V	1.5A Timed

CAUTION

BEFORE CONNECTING THE INSTRUMENT TO THE POWER SUPPLY LINE, ENSURE THAT THE SLIDE SWITCH IS IN THE CORRECT POSITION AND THAT THE CORRECT FUSE HAS BEEN FITTED.

The power cable supplied with each instrument is varied according to the regulations of the country of destination. The colour codes normally used are given in Table 1-2.

Table 1-2

Supply	United States	Rest of World
LINE	BLACK	BROWN
NEUTRAL	WHITE	BLUE
GROUND	GREEN/YELLOW	GREEN/YELLOW

WARNING

THE METAL PARTS OF THIS INSTRUMENT ARE EARTHED VIA THE GREEN/YELLOW WIRE AND THE GROUND PIN IN THE POWER CABLE PLUG. IF THE INSTRUMENT IS OPERATED FROM A TWO WIRE SUPPLY, THE GREEN/YELLOW WIRE MUST BE EARTHED SEPARATELY.

IDENTIFICATION

The serial number of each instrument is stamped on a plate fitted to its rear panel and should be quoted in all correspondence with Hewlett-Packard, especially when ordering replacement parts. The serial number consists of a four digit serial prefix used to document changes, a reference letter denoting the country of origin (U = United Kingdom) and a five digit number unique to each instrument.

UPDATING

If the serial prefix of the instrument is not the same as that appearing on the title page of this manual then the manual will require updating. The relevant Manual Change Sheets are normally supplied with the instrument but additional copies can be obtained from any *hp* Sales and Service Office (see back page for list).

OPTIONS

Three options are available, all of which are fitted at the factory and are not available as retrofit kits. These are:

OPTION 001 – 75Ω CLOCK and DATA input/output impedances.

OPTION 002 – Internal variable frequency clock.

OPTION 003 – Options 001 and 002 combined.

Note that with Options 001 and 003, the impedance of the SYNC OUTPUT is still 50Ω.

AIR FILTER

The air intake and filter are located on the rear panel of the instrument. Inspect the air filter regularly and clean it before it becomes dirty enough to restrict air flow. To clean proceed as follows:

(i) Remove four screws holding filter in place.

(ii) Wash filter in warm water and detergent.

(iii) Allow filter to completely dry before refitting.

RECOMMENDED TEST EQUIPMENT

Table 1-3 provides list of recommended test equipment required for the Performance Tests and Adjustment Procedures given in Section III and IV respectively. Individual listings are given at the beginning of each section together with the minimum required specification for each instrument.

Table 1-3

Item	Model	Used in Sections
Test Oscillator	*hp* 651B	III
VHF Signal Generator	*hp* 608E	III and IV
Oscilloscope	*hp* 180A/1801A/1820A	III
Sampling Oscilloscope	*hp* 180A/1810A	III and IV
Electronic Counter	*hp* 5327A	III and IV
Digital Voltmeter	*hp* 3440A	III and IV
Pulse Generator	*hp* 8004A	III
Coaxial Attenuator	*hp* 8491A (Opt. 20)	III and IV

SECTION II
THEORY OF OPERATION

INTRODUCTION

This section contains a basic theory of operation which should be read before the Performance Tests, Adjustment and Troubleshooting Procedures given in subsequent sections are attempted. (Individual Service Sheets in Section VI give detailed circuit description of each assembly.)

The *hp* 3760A Data Generator is a high speed pseudo random binary sequence (PRBS) and binary word (WORD) generator. It consists physically of four modules in a mainframe, these modules are:

1. Front Panel Module, A1.
2. Clock Module, A2.
3. Data Module, A3.
4. Power Supply Module, A4.

If the front panel controls etc, are considered as part of their respective modules then the instrument can be considered electronically as three separate units (see Figure 2-1).

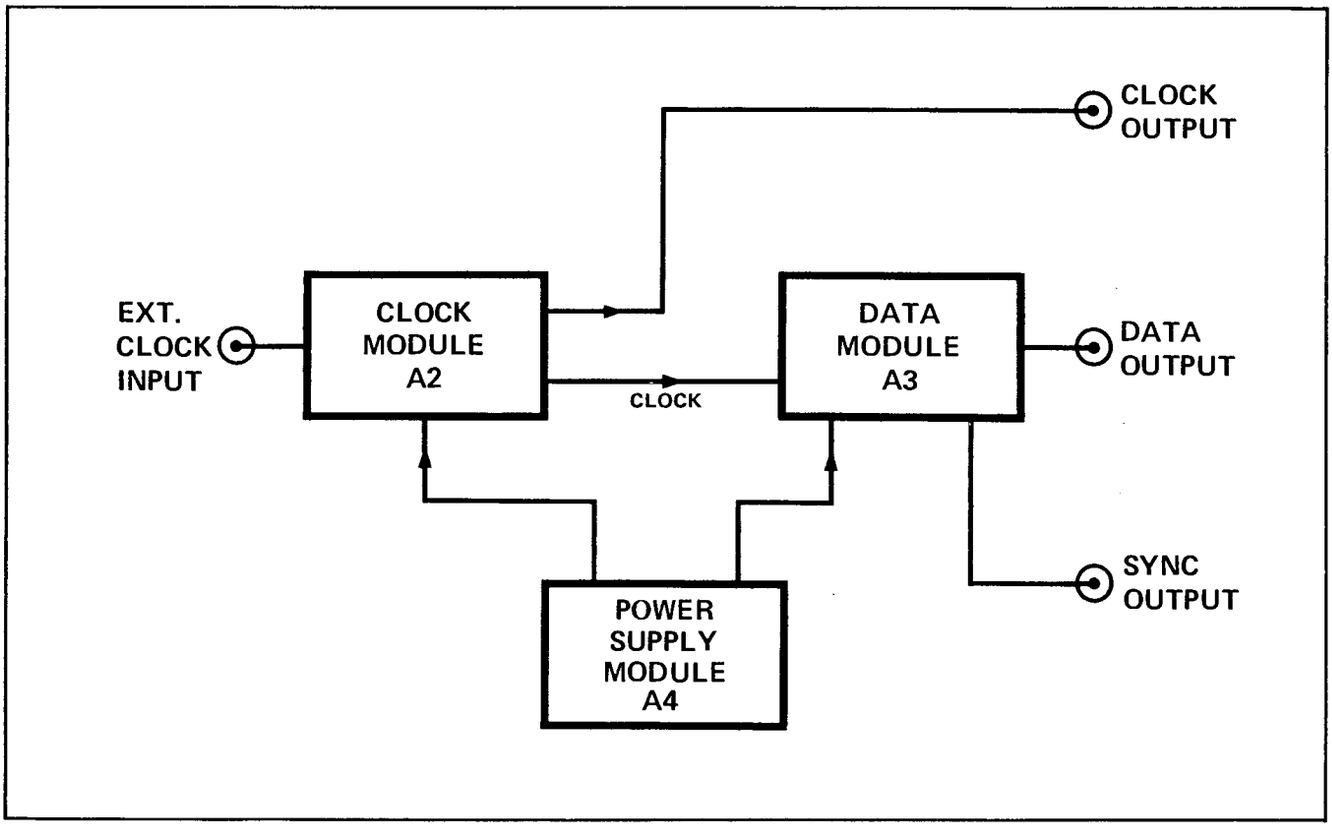


Figure 2-1 3760A Basic Block Diagram

SECTION III
PERFORMANCE TESTS

INTRODUCTION

This section contains a series of Performance Tests which can be used to verify that the 3760A Data Generator is operating within its published Specifications. Each test is self contained and is presented in two forms. The right hand page gives a step by step description of the test while the left hand page presents it in a graphical form. A list of reference settings to which the 3760A should be set at the beginning of each test is given on a "throw-clear" page to allow it to be consulted in conjunction with each Performance Test.

Although individual tests can be performed in any order, eg, as an aid to troubleshooting, for complete performance testing it is recommended that the sequence given in this section is followed.

Should the instrument fail to meet its specifications in any of the tests, one of the Adjustment Procedures given in Section IV may remedy the fault. If this fails or no adjustment is possible, a comprehensive guide to trouble-shooting is given in Section V.

OPTION 001/003

The following Performance Tests have been written for standard (50Ω) instruments. For Options 001 and 003 (75Ω), 50/75Ω matching pads etc. must be used where necessary and due allowance should be made for insertion losses.

LIST OF PERFORMANCE TESTS

Figure 3-1

CLOCK SECTION

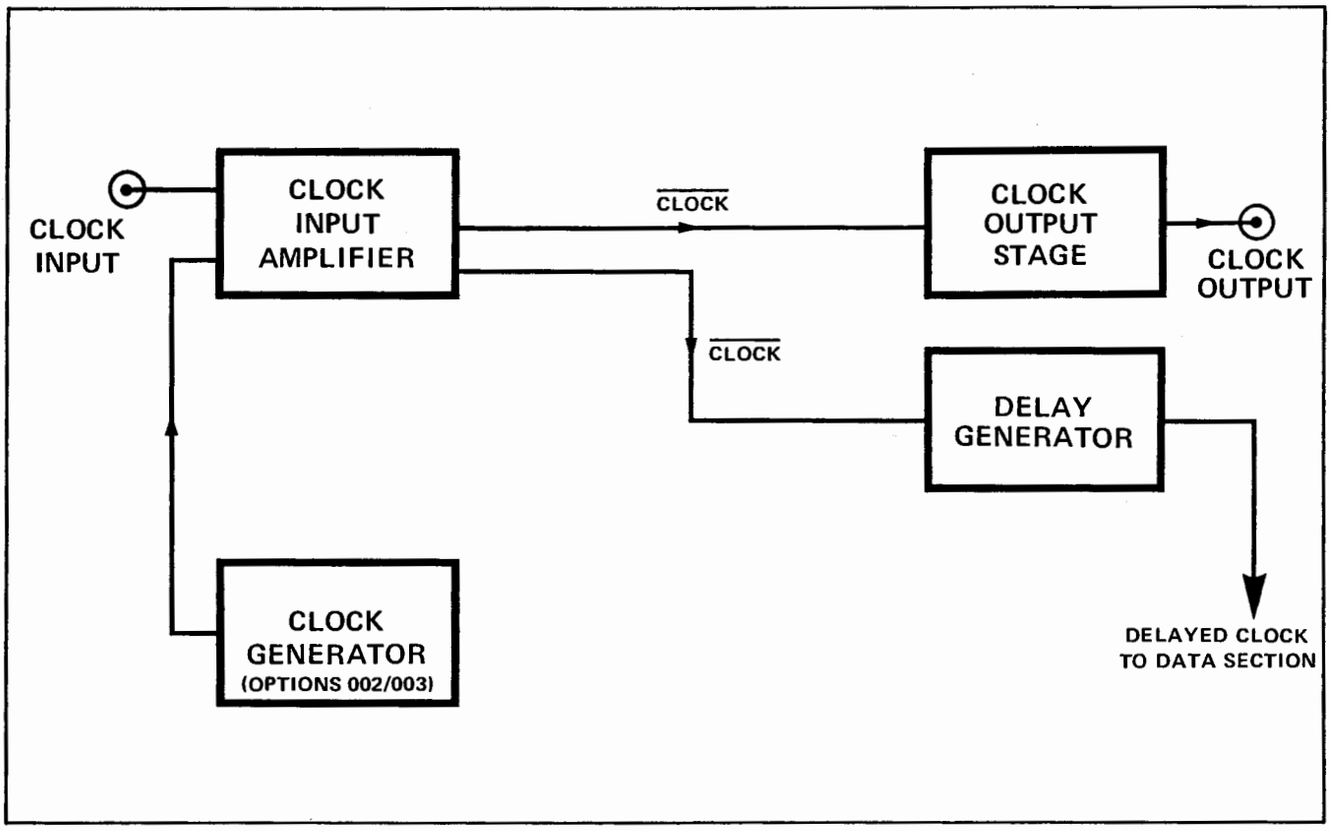


Figure 2-2 Clock Section

A simplified block diagram of the clock section is shown in Figure 2-2. The CLOCK INPUT is dc coupled and accepts waveforms of any shape in the frequency range 1.5 to 150MHz at amplitudes greater than 0.5V pk-pk (see Specifications for full details). MANUAL or AUTO triggering facilities are available and a front panel lamp indicates when correct triggering is achieved. A switch for manual clocking, located in the Clock Input Amplifier, is provided as an aid to servicing and will be referred to in later sections. The Clock Generator (Options 002 and 003 only) provides an internally generated variable frequency clock source in the range 1.5 to 150MHz.

The Delay Generator consists of a series of lumped LC delay lines which delay the clock signal to the Data Section. This allows the position of the output data stream to be varied with respect to the clock output. The undelayed clock signal drives the Clock Output Stage whose output, logically equal to CLOCK or $\overline{\text{CLOCK}}$, is variable between 0.1 and 3.2V pk-pk at dc offset levels between 0 and ±3V. The output amplitude and dc offset controls are non-interacting and since dc coupling is used throughout the Clock Output Stage, the offset level is unaffected by the duty cycle of the clock signal. The input and output impedances of the standard instrument are 50Ω but this is changed to 75Ω in Options 001 and 003.

DATA SECTION

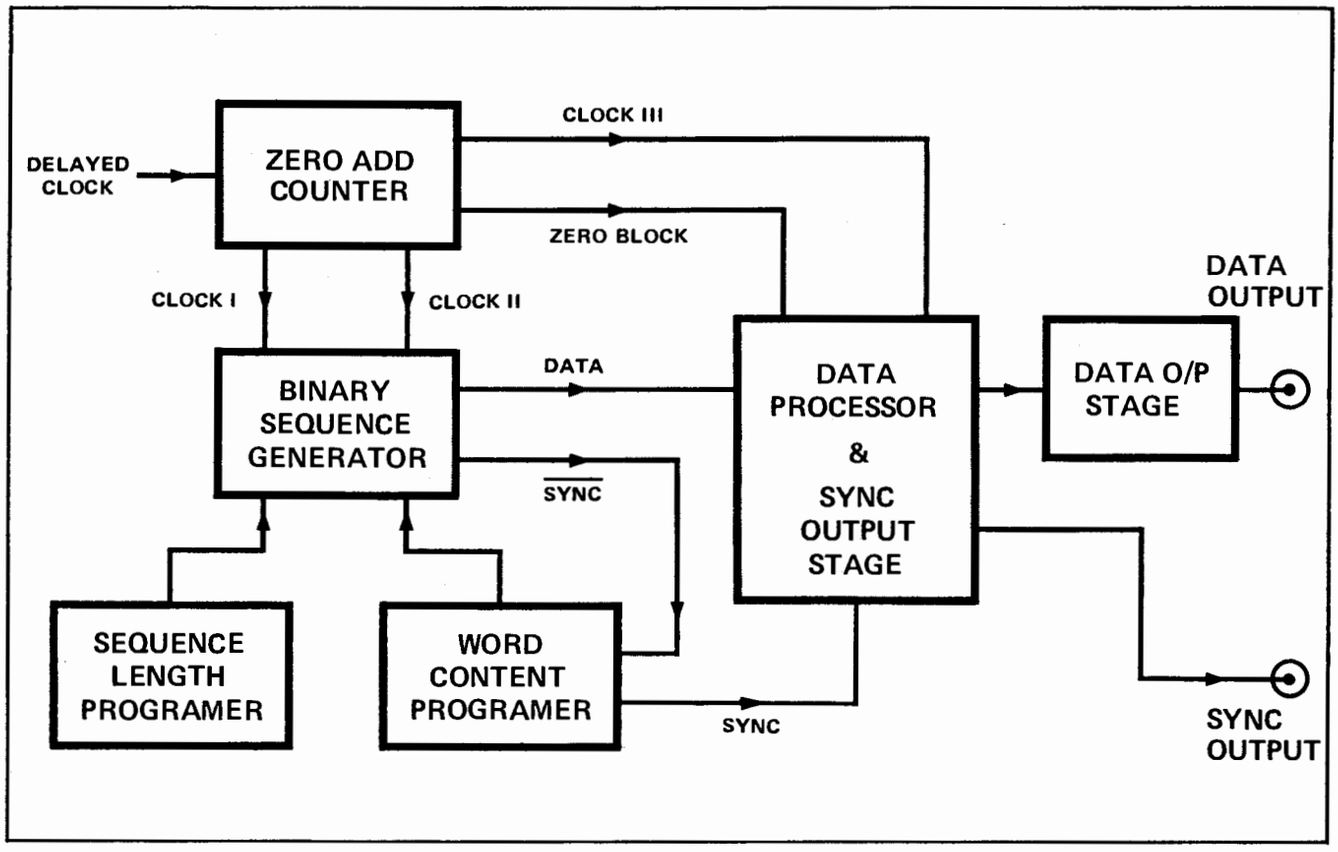


Figure 2-3 Data Section

Data Generation

The Binary Sequence Generator produces Pseudo Random Binary Sequences (PRBS) of length $2^n - 1$ where n = 3 to 10 or 15, and binary words (WORD) of length n, where n = 3 to 10. This generator is basically a 15 stage shift register with variable feedback taps controlled by the front panel DATA MODE and SEQUENCE LENGTH switches. Only one fixed PRBS for each sequence length can be generated but the content of the binary words is selectable from the front panel. A sync detection circuit produces one sync pulse per sequence at a point determined by the WORD CONTENT switches and can therefore be positioned anywhere in the sequence (see Service Sheet A32/33 for full details). Timing in the instrument has been adjusted so that in WORD the sync pulse occurs approximately coincident with the last bit of the sequence.

WORD content as defined by the front panel switches is programed into the Binary Sequence Generator by the Word Content Programer. In WORD, if the content or length is altered (deliberately or accidentally) the sync fails and this causes the word to be reloaded into the Binary Sequence Generator.

Zero Add

The bit density of the output data can be varied by introducing a block of zeros into the data stream once per sequence. The length of this block (0 to 99 bits) is controlled by the Zero Add Counter which, when triggered by the sync pulse inhibits the data stream in the Data Processor and holds the DATA OUTPUT at logic 0. The zero block is therefore inserted immediately after the sync pulse and to allow its position to be easily identified, the output sync pulse is "stretched" as shown in Figure 4. The Zero Add Counter also stops the Binary Sequence Generator by inhibiting its clock signals to prevent any of the sequence being lost during the zero block. Note, that in WORD the zero block is inserted between sequences.

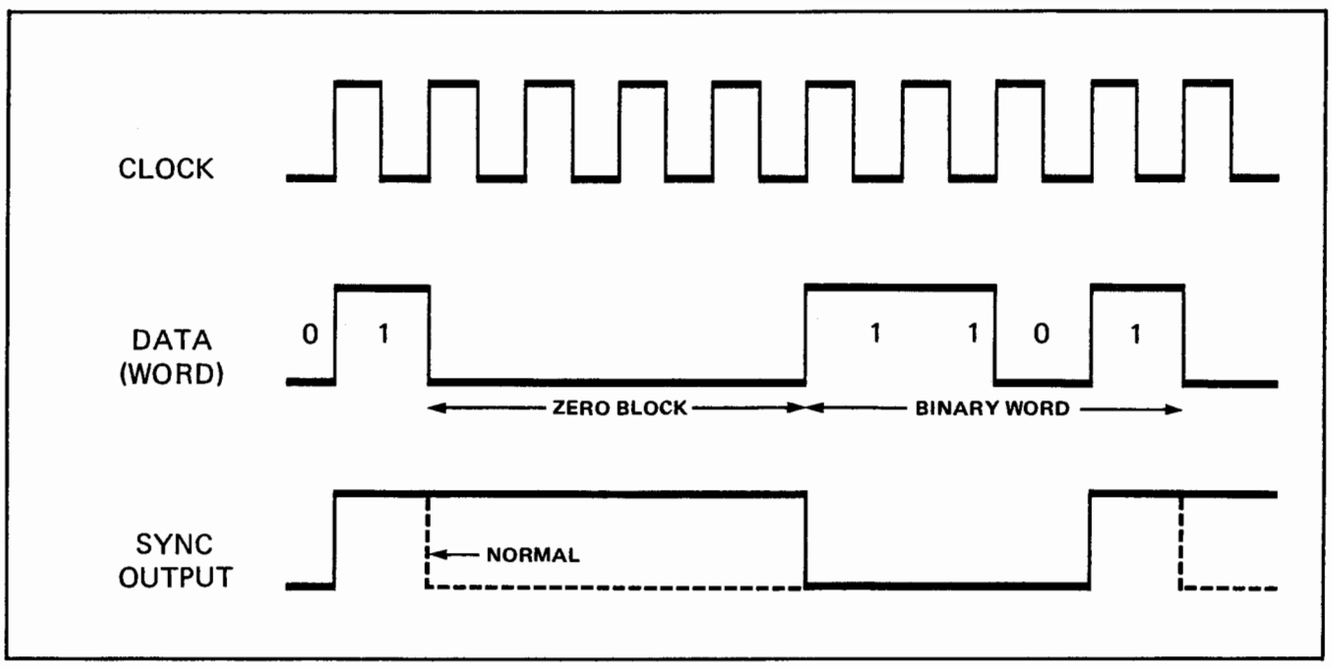


Figure 2-4 Zero Add

Data Processor

In addition to ZERO ADD, the Data Processor provides the following data modes:

(i) PRBS – ERROR ADD

(ii) 1010

(iii) NRZ/RZ

PRBS – ADD ERROR provides a useful self check facility when the 3760A is used in conjunction with the *hp* 3761A Error Detector by changing two consecutive bits in every 4000th sequence to their logic complement. These deliberate errors are timed by a sync pulse counter and occur immediately after the 4000th sync pulse. Their position in the sequence can therefore be predicted from the settings of the WORD switches (the position of the sync pulse is determined by these switched.

In the 1010 mode, the clock signals to the Binary Sequence Generators are Inhibited and the data output becomes the maximum change sequence 1010. The conversion of the output data format from Non Return to Zero (NRZ) to Return to Zero (RZ) is accomplished by combining the data and clock in such a way that the data output is only logic 1, when both the data and clock are 1. This is equivalent to performing the logic AND function and is shown graphically in Figure 5.

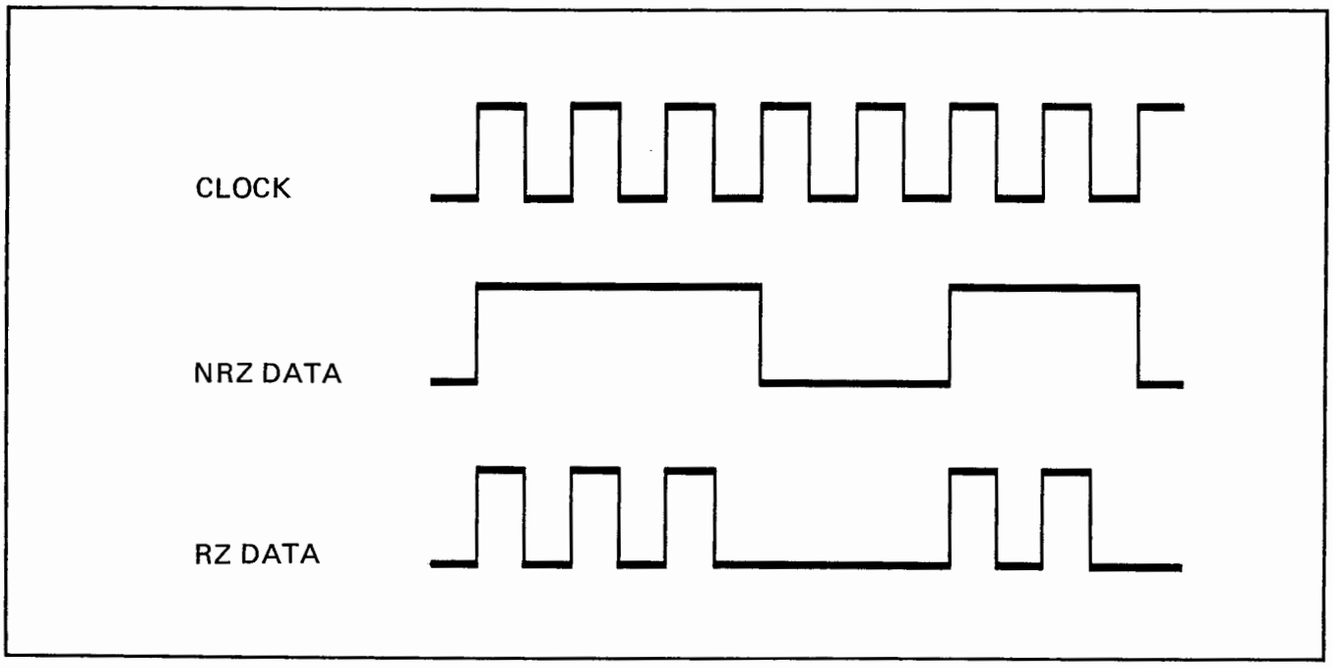


Figure 2-5 NRZ/RZ Conversion

Sync Output

The Sync Output Amplifier is housed in the same assembly as the Data Processor (A37) and delivers an output pulse amplitude of +1V into 50Ω (Standard and Options). With the internally mounted Sync Mode switch set to NORMAL, the output pulse width is one clock period (except in ZERO ADD) and in ÷2 the output becomes a square wave with the mark and space times equal to one sequence length. This latter setting is usually only used for servicing and the switch should always be returned to NORMAL.

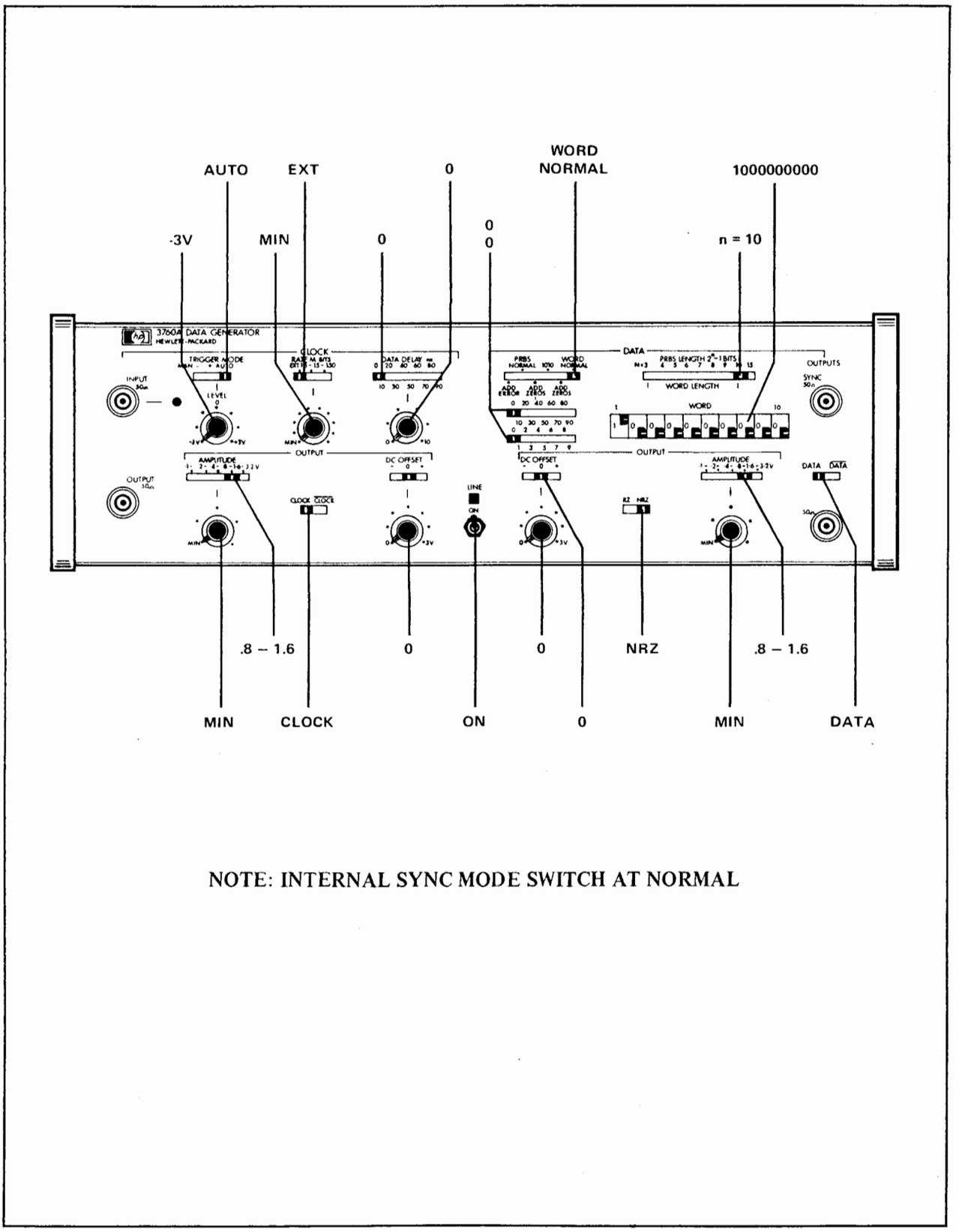
Data Output

The Data Output Stage is identical to the Clock Output Stage. In the standard instrument the output impedance is 50Ω but is changed to 75Ω in Options 001 and 003.

TEST EQUIPMENT

Item	Specification	Recommended
Test Oscillator	Frequency Range: 1.5 to 10MHz Output Level: 0 to 3V RMS	*hp* 651B
VHF Signal Generator	Frequency Range: 10 to 150MHz Output Level: 0 to 3V RMS	*hp* 608E
Oscilloscope	Bandwidth: 50MHz	*hp* 180A/1801A/1820A
Sampling Oscilloscope	Bandwidth: 1GHz Input Impedance: 50Ω External Trigger: 3ns pulse	*hp* 180A/1810A
Electronic Counter	Frequency Range: 0 to 150MHz External trigger and ratio measurement capability. 7 digit display	*hp* 5327A
Digital Voltmeter	Range: +5 to -5V dc Accuracy: ±0.01V	*hp* 3440A
Pulse Generator	Pulse Width: 10ns at Repetition Rate of 10MHz Amplitude 0.5V pk-pk	*hp* 8004A
Coaxial Attenuator	Range: DC – 12.4GHz Attenuation: -20dB	*hp* 8491A (Option 20)

Figure 3-2



NOTE: INTERNAL SYNC MODE SWITCH AT NORMAL

Figure 3-3

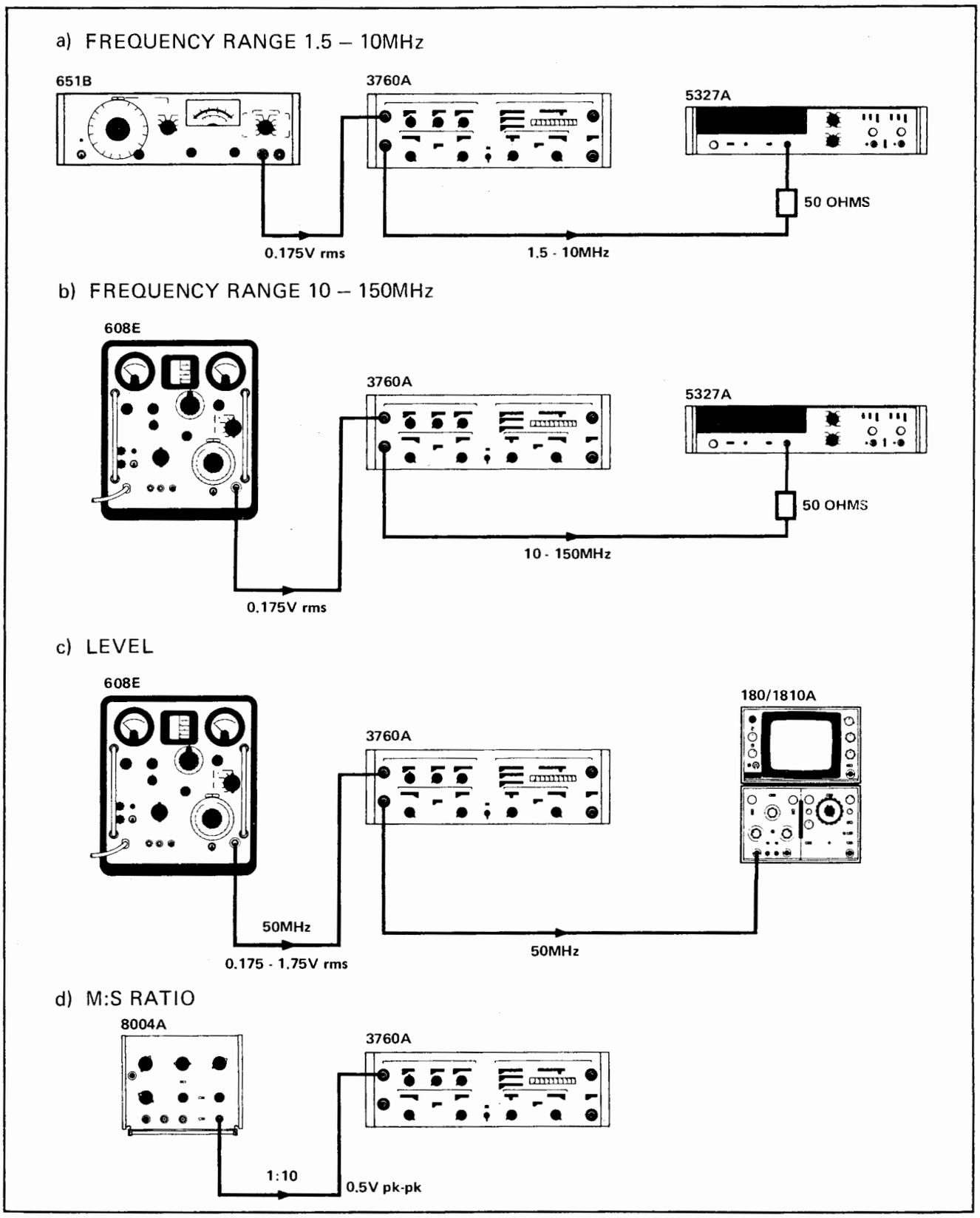


Figure 3-4 Clock Input – Auto Trigger

CLOCK INPUT – AUTO TRIGGER

SPECIFICATION:

Rate:	1.5 – 150MHz
Sensitivity:	Better than 500mV pk-pk
m:s Ratio:	1:10 to 10:1

PROCEDURE:

1. Set all controls to the Reference Settings as in Figure 3-3.
2. Connect the 651B Test Oscillator set to 1.5MHz at 0.175V rms (0.5V pk-pk), to the 3760A CLOCK INPUT.
3. Connect the 3760A CLOCK OUTPUT terminated in 50Ω to a 5327A Timer/Counter INPUT C (÷10).
4. Check that the 3760A Trigger Lamp is on and that the Counter displays the input frequency.
5. Slowly increase the Test Oscillator frequency up to 10MHz (maintaining its output amplitude at 0.175V rms) and check that the Counter display follows the input frequency. Check also that the Trigger Lamp remains on.
6. Replace the Test Oscillator with a 608E VHF Signal Generator set to 10MHz at 0.175V rms.
7. Repeat operation (5) over the frequency range 10 – 150MHz.
8. Replace the Counter with a 180/1810A Sampling Oscilloscope. Set the Signal Generator to 50MHz and check that the mark to space ratio of the displayed waveform is 1:1 over the input amplitude range 0.175 – 1.75V rms (0.5 – 5V pk-pk).
9. Replace the 608E with a 8004A Pulse Generator. Set the PULSE WIDTH to 10ns and adjust the REP RATE until the mark to space ratio of the output is 1:10. Set the amplitude of the output to 0.5V pk-pk (0.175V rms) and set the PULSE POLARITY to +.
10. Check that the Trigger Lamp is on.
11. Change the 8004A PULSE POLARITY to -. Check that the Trigger Lamp is on.

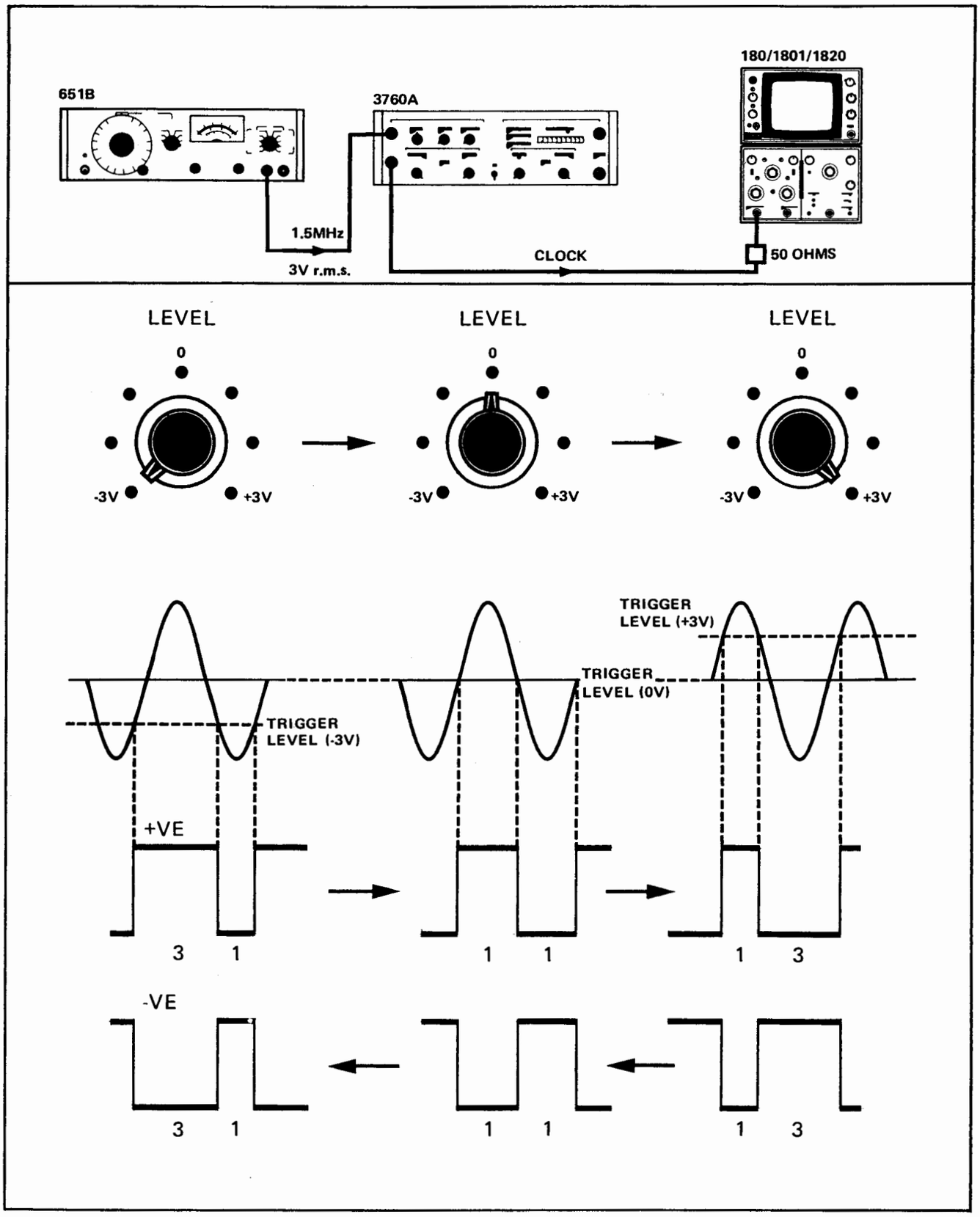


Figure 3-5 Clock Input – Manual Trigger

CLOCK INPUT – MANUAL TRIGGER

SPECIFICATION:

Sensitivity:	Better than 500mV pk-pk.
Trigger Level:	+3V to -3V.
Trigger Slope:	+ve or -ve.

PROCEDURE:

1. Set the 3760A TRIGGER MODE to MAN +, the TRIGGER LEVEL to -3V and all other controls to the Reference Settings as in Figure 3-3.

2. Connect a 651B Test Oscillator set to 1.5MHz at 3V rms (4.2V peak) to the 3760A CLOCK INPUT.

3. Connect a 180A/1801A/1820A Oscilloscope to the 3760A CLOCK OUTPUT.

4. Check that the Trigger Lamp is on and that the mark:space ratio of the displayed waveform is approximately 3:1.

5. Slowly turn the TRIGGER LEVEL control clockwise and check that the mark-space ratio decreases uniformily to a ratio of approximately 1:3 when the control is fully clockwise. The Trigger Lamp should remain on.

6. Change the 3760A TRIGGER MODE to MAN–.

7. Check that the mark:space ratio of the displayed waveform changes uniformily from 3:1 to 1:3 as the TRIGGER LEVEL is turned counterclockwise and that the Trigger Lamp remains on.

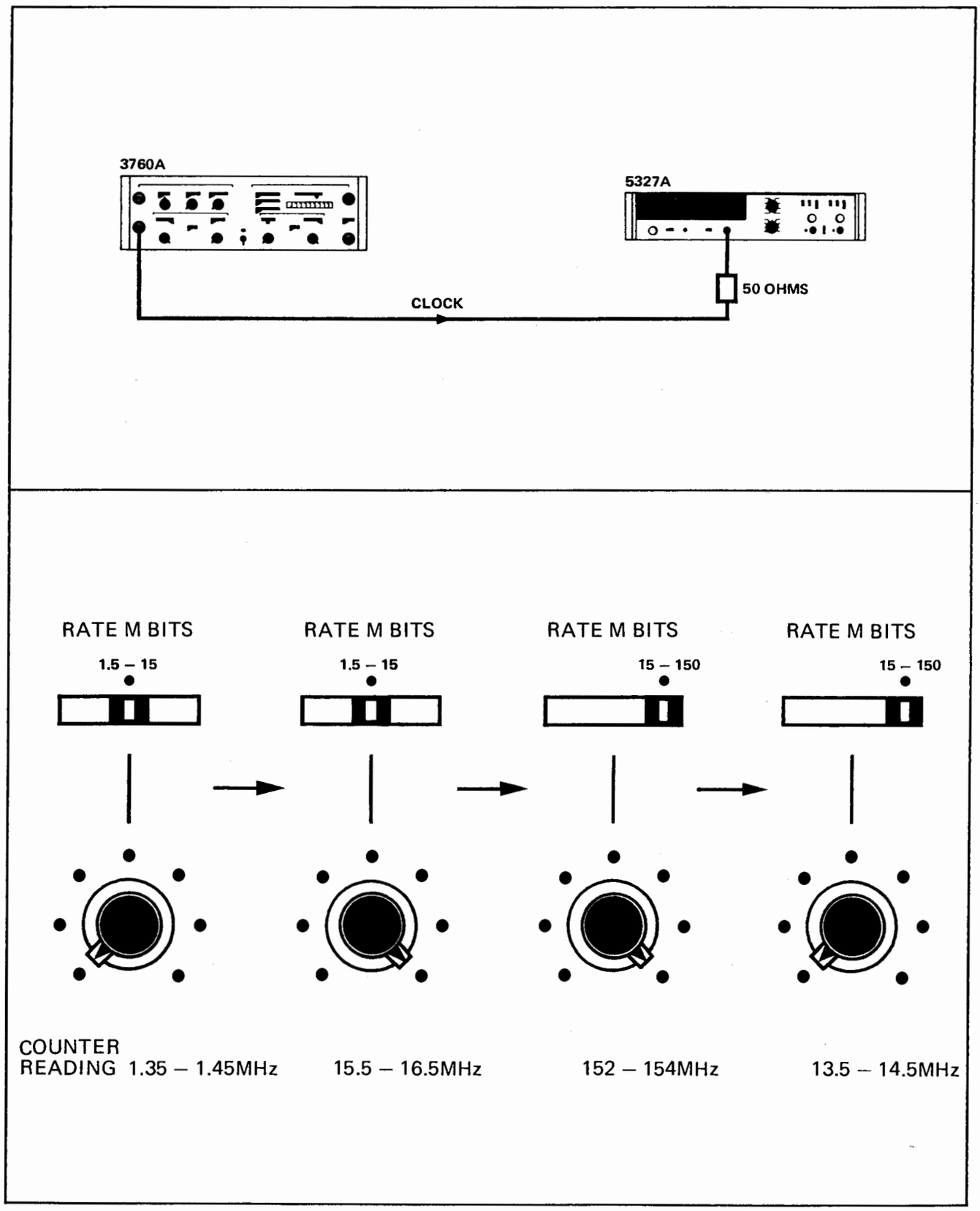


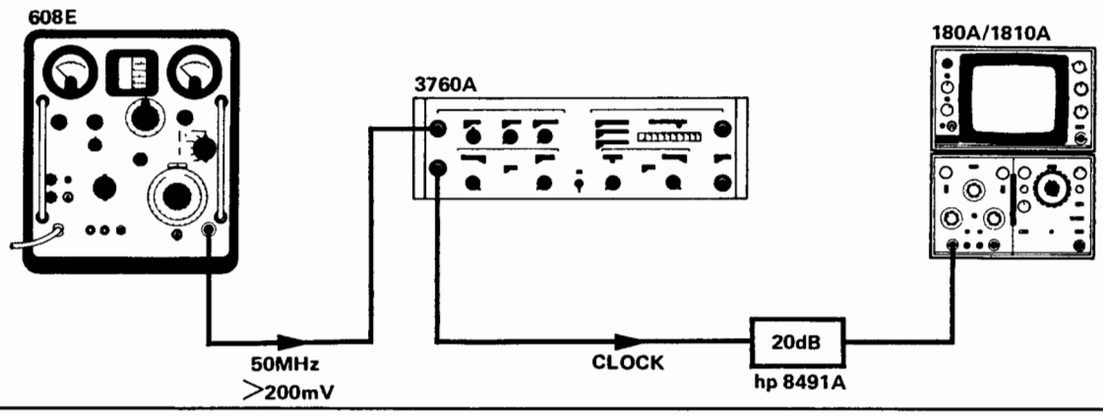
Figure 3-6 Clock Generator (Options 002/003)

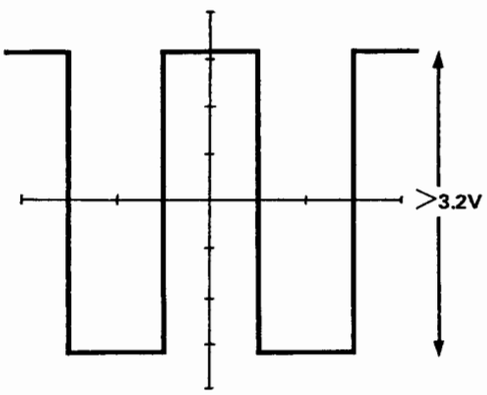
CLOCK GENERATOR (OPTIONS 002/003)

SPECIFICATION: Range: 1.5 to 150MHz in two decade ranges.

PROCEDURE:

1. Set the 3760A CLOCK RATE switch to 1.5 – 15MHz. All other controls to the Reference Settings as in Figure 3-3.
2. Connect the 3760A CLOCK OUTPUT terminated in 50Ω to a 5327A Timer/Counter, INPUT C, ÷10.
3. With the 3760A RATE vernier fully counterclockwise (minimum) the counter reading should be between 1.3 and 1.45MHz.
4. Turn the RATE vernier fully clockwise (maximum). The counter reading should now be between 15.5 and 16.5MHz.
5. Change the RATE switch to 15 – 150MHz. With the RATE vernier still fully clockwise the counter reading should be between 152 and 154MHz.
6. Turn the RATE vernier fully counterclockwise. The counter reading should now be between 13.5 and 14.5MHz.





AMPLITUDE RANGE	DISPLAY AMPLITUDE
1.6 – 3.2V	3.2V
0.8 – 1.6V	1.6V ±0.06V
0.4 – 0.8V	0.8V ±0.06V
0.2 – 0.4V	0.4V ±0.02V
0.1 – 0.2V	0.2V ±0.02V

Figure 3-8 Clock Output – Amplitude

CLOCK OUTPUT – AMPLITUDE

SPECIFICATION: Amplitude: Continuously variable in five ranges from 0.1 to 3.2V pk-pk.

PROCEDURE:

1. Set the 3760A CLOCK OUTPUT AMPLITUDE to 1.6 – 3.2V and the vernier fully clockwise. All other controls to the Reference Settings as in Figure 3-3.

2. Connect a 180A/1810A Sampling Oscilloscope via an 8491A (Option 20) 20dB Coaxial Attenuator to the 3760A CLOCK OUTPUT.

3. Connect a 608E VHF Signal Generator set to 50MHz at >200mV rms to the 3760A CLOCK INPUT.

4. The amplitude of the displayed waveform should be at least 3.2V pk-pk and the dc offset should be less than 0.06V.

5. Adjust the CLOCK OUTPUT AMPLITUDE vernier until the amplitude of the displayed waveform is exactly 3.2V pk-pk.

6. Switch through the CLOCK OUTPUT AMPLITUDE ranges and check the amplitude of the displayed waveform against the following table:

AMPLITUDE RANGE	DISPLAY AMPLITUDE
1.6 – 3.2V	3.2V
0.8 – 1.6V	1.6V ±0.06V
0.4 – 0.8V	0.8V ±0.06V
0.2 – 0.4V	0.4V ±0.02V
0.1 – 0.2V	0.2V ±0.02V

7. Set the CLOCK OUTPUT AMPLITUDE range to 1.6 – 3.2V and adjust the vernier until the amplitude of the displayed waveform is exactly 3.2V pk-pk. Set the CLOCK/$\overline{\text{CLOCK}}$ switch to $\overline{\text{CLOCK}}$.

8. The amplitude of the displayed waveform should still be 3.2V pk-pk.

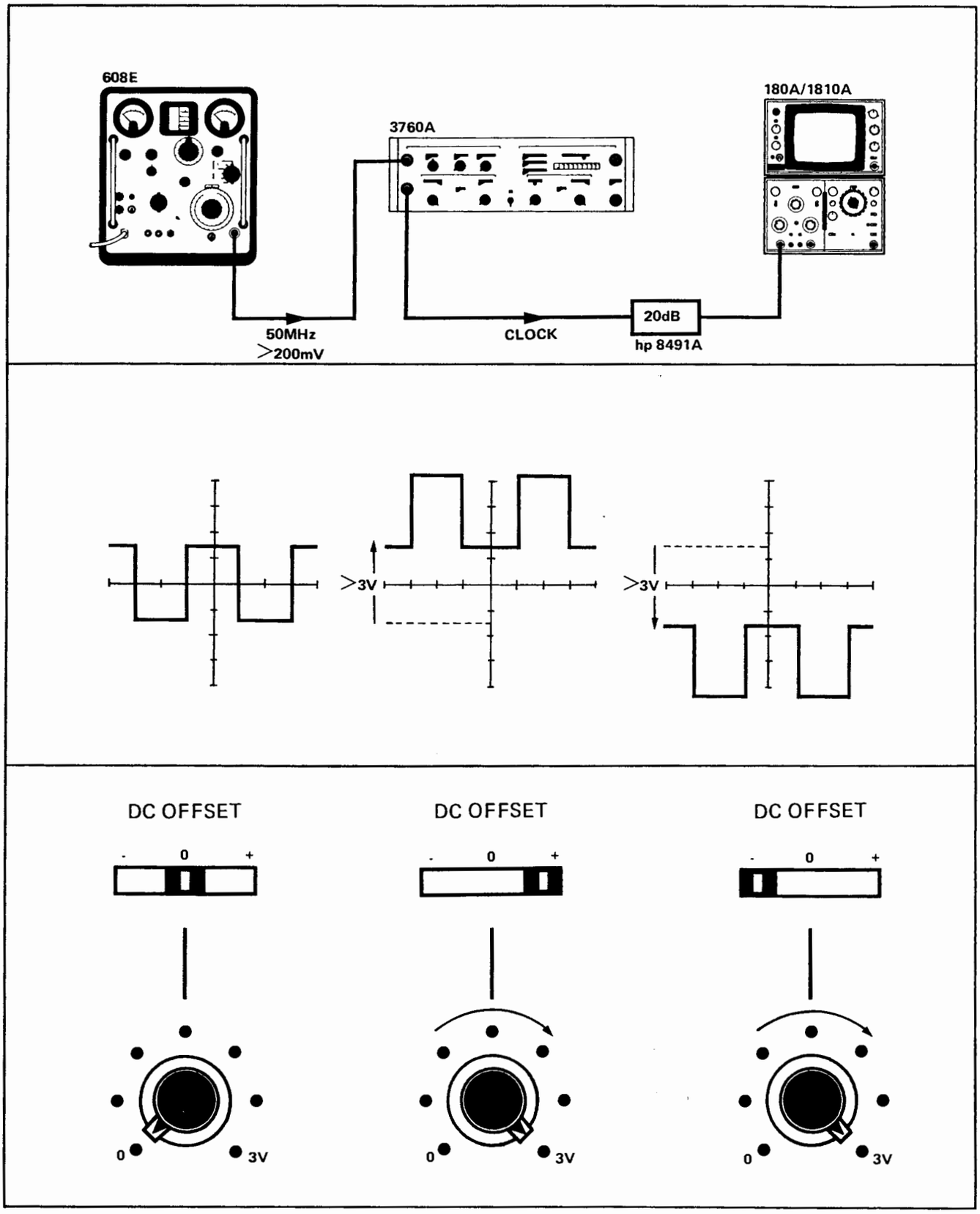


Figure 3-7 Clock Output – DC Offset

CLOCK OUTPUT – DC OFFSET

SPECIFICATION: Range: 0 to ±3V.

PROCEDURE:

1. Set the 3760A CLOCK OUTPUT AMPLITUDE range switch to 1.6 – 3.2V. All other controls to the Reference Settings as in Figure 3-3.
2. Connect a 608E VHF Signal Generator set to 50MHz at >200mV rms to the 3760A CLOCK INPUT.
3. Connect the 3760A CLOCK OUTPUT via an 8491A (OPTION 20) 20dB Coaxial Attenuator to the CHAN A input of a 180A/1810A Sampling Oscilloscope.
4. Adjust the 3760A CLOCK OUTPUT AMPLITUDE vernier for an output pulse amplitude of 3.0V and display this waveform on the oscilloscope.
5. Set the 3760A CLOCK DC OFFSET range switch to +.
6. Check that the dc offset of the displayed waveform increases from 0 to at least +3V as the CLOCK DC OFFSET vernier is rotated clockwise. Turn the vernier fully counterclockwise.
7. Set the 3760A CLOCK DC OFFSET range switch to -.
8. Check that the dc offset of the displayed waveform increases from 0 to at least -3V as the CLOCK DC OFFSET vernier is rotated clockwise.

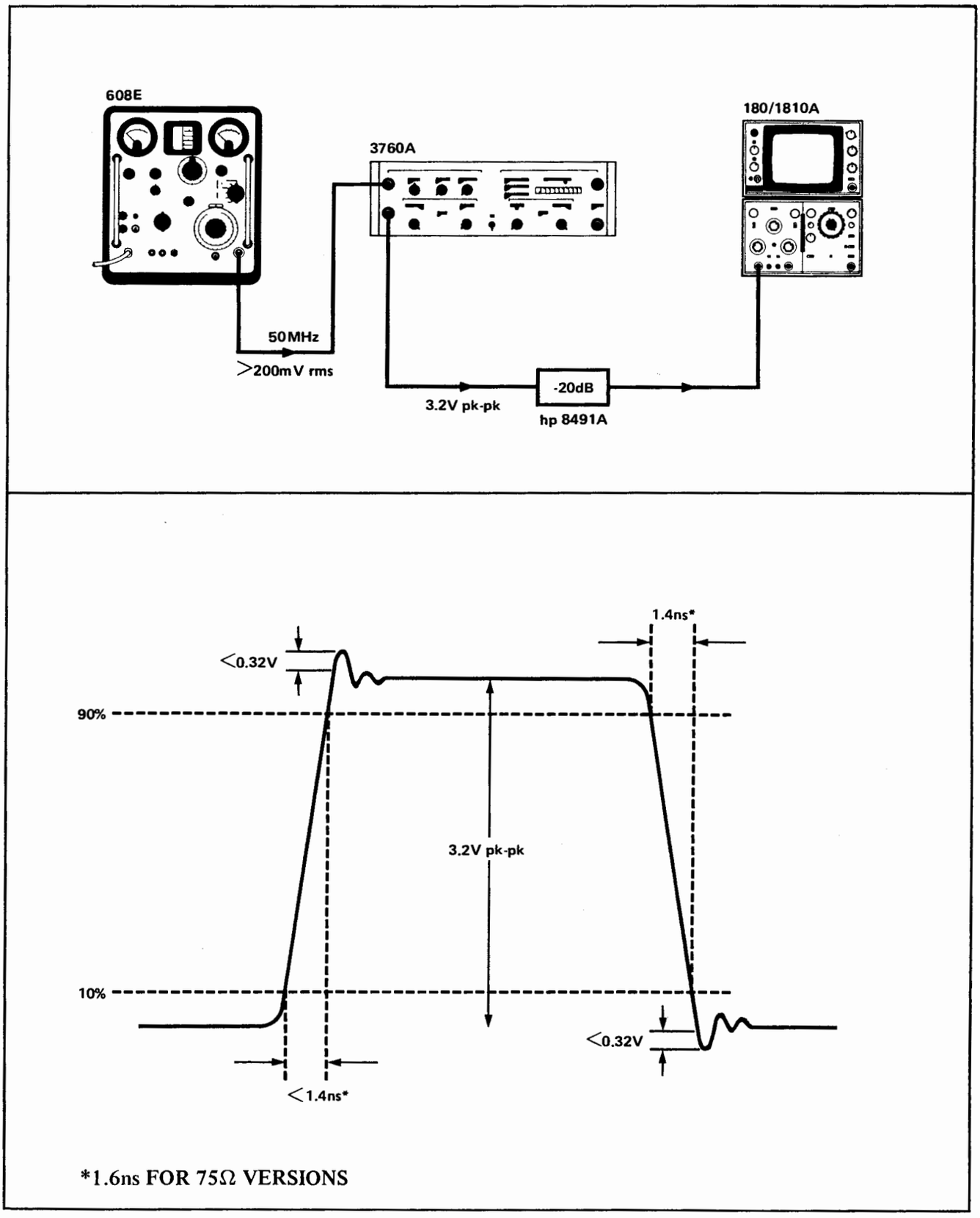


Figure 3-9 Clock Output – Pulse Shape

CLOCK OUTPUT – PULSE SHAPE & M:S RATIO

SPECIFICATION:

Rise/Fall Times: <1.4ns
<1.6ns for 75Ω versions
Overshoot: <10% of pulse amplitude

PROCEDURE:

1. Set the 3760A CLOCK OUTPUT AMPLITUDE range switch to 1.6 – 3.2V. All other controls to the Reference Settings as in Figure 3-3.

2. Connect a 608E VHF Signal Generator set to 50MHz at >200mV rms to the 3760A CLOCK INPUT.

3. Connect the 3760A CLOCK OUTPUT via an 8491A (Option 20) 20dB Coaxial Attenuator to the CHANNEL A input of a 180A/1810A Sampling Oscilloscope.

4. Adjust the 3760A CLOCK OUTPUT AMPLITUDE vernier for an output pulse amplitude of 3.2V pk-pk. The Rise/Fall time of the displayed waveform should be less than 1.4ns (1.6ns for 75Ω versions) (10% to 90% level) with an overshoot of less than 10% of the pulse amplitude ie, <0.32V.

5. Slowly reduce the amplitude of the CLOCK OUTPUT from 3.2 to 0.1V pk-pk and check that the overshoot is less than 10% of the output pulse amplitude over this range.

6. Set the signal generator output to 140MHz. The mark to space ratio of the CLOCK OUTPUT should be 1:1 ±10%.

7. Repeat operations (6) and (7) with the CLOCK/$\overline{\text{CLOCK}}$ switch set to $\overline{\text{CLOCK}}$.

OPTIONS 002/003 ONLY

8. Set the 3760A CLOCK RATE switch to 1.5 – 15MHz and the vernier fully clockwise.

9. The mark to space ratio of the displayed waveform should be 1:1 ±10%.

10. Change the 3760A RATE switch to 15 – 150MHz.

11. The mark to space ratio of the displayed waveform should be 1:1 ±10%.

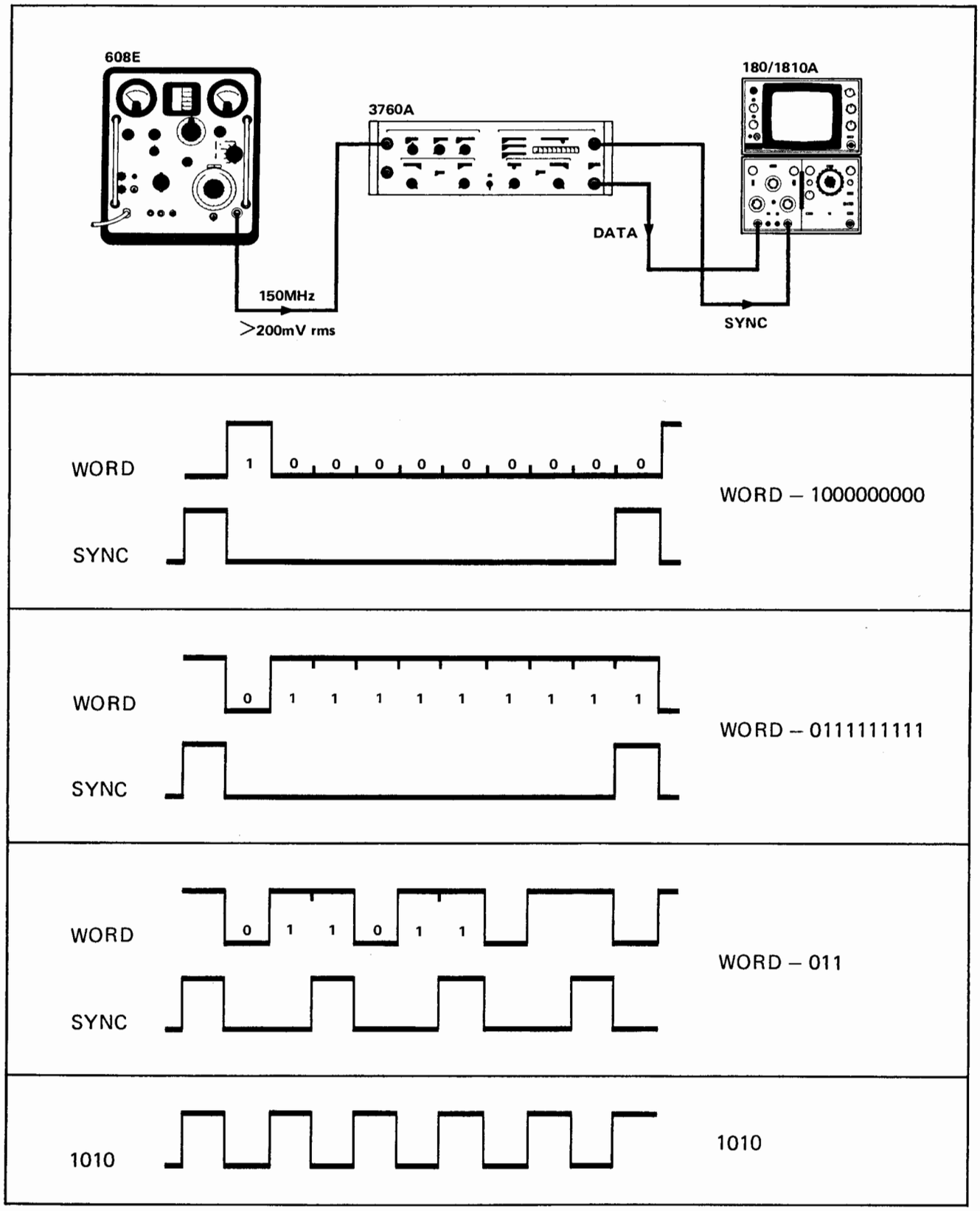


Figure 3-10 Word Normal and 1010

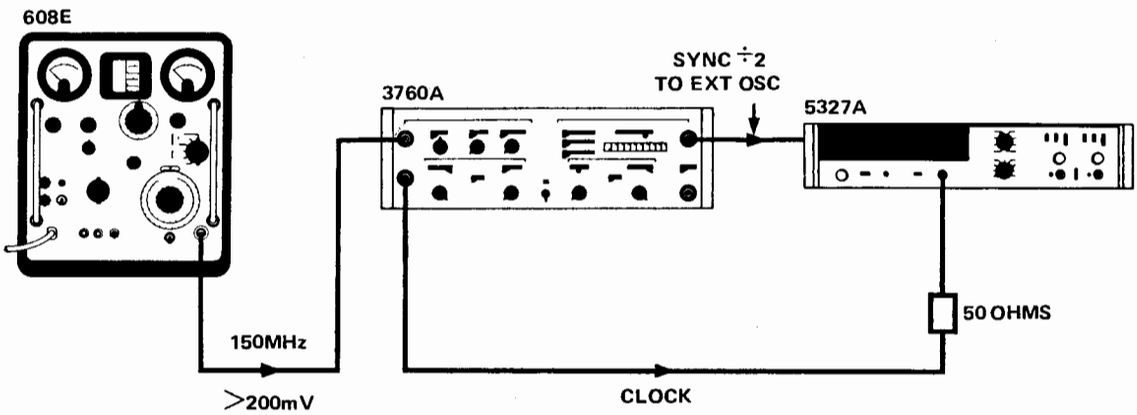
WORD NORMAL AND 1010

SPECIFICATION:

Word Normal:	Generation of a 3 to 10 bit word with selectable content.
1010:	Generation of the preset maximum change sequence, 1010.

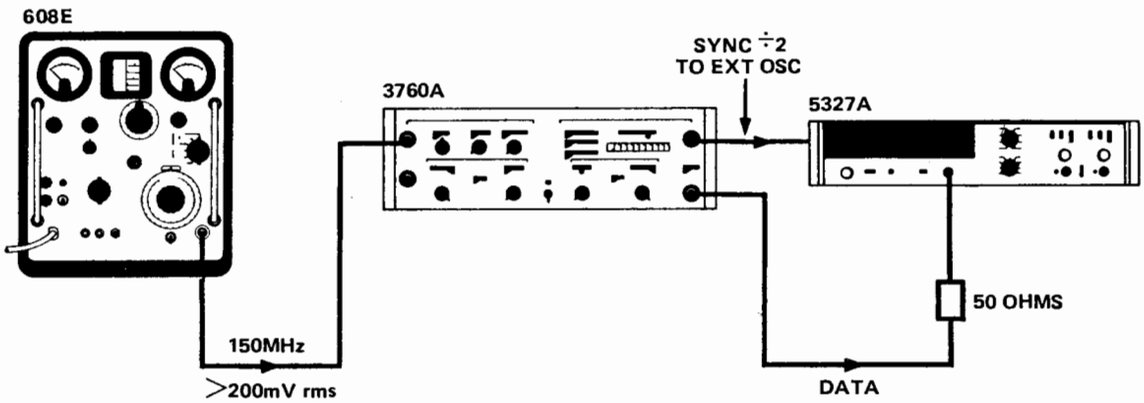
PROCEDURE:

1. Set the 3760A controls to the Reference Settings as in Figure 3-3.
2. Connect a 608E VHF Signal Generator set to 150MHz at >200mV rms to the 3760A CLOCK INPUT.
3. Connect the 3760A DATA OUTPUT to the CHANNEL A input of a 180/1810A Sampling Oscilloscope. Connect the 3760A SYNC OUTPUT to the oscilloscope CHANNEL B input and set the DISPLAY MODE switch to ALT-B TRIGGER.
4. Check that the ten bit word 1000000000 appears on the 3760A Word Content Display. Check also that this word is displayed on the oscilloscope.
5. Change the word content to 0111111111 and check that this word is displayed on the oscilloscope.
6. Reduce the WORD LENGTH in steps and check that the word is reduced by 1 until at n = 3, it is 011.
7. Set the DISPLAY MODE switch on the 180A/1810A Sampling Oscilloscope to A – A TRIG.
8. Change the 3760A MODE switch to 1010 and check that a repetitive 1010 . . . . sequence is displayed on the oscilloscope.



SEQUENCE LENGTH	COUNTER DISPLAY ±2
15	65,534
10	2,046
9	1,022
8	510
7	254
6	126
5	62
4	30
3	14

Figure 3-11 PRBS Normal



DATA MODE	WORD CONTENT	COUNTER READING
PRBS NORMAL	101	80000.00 ± .01
PRBS – ERROR ADD	101	80010.00 ± .01
PRBS – ERROR ADD	011	79990.00 ± .01

Figure 3-12 PRBS – Error Add

PRBS – ERROR ADD

SPECIFICATION: Introduction of an error by changing two consecutive bits in every 4000th sequence to their logic complement.

PROCEDURE:

1. Set the 3760A Data Mode to PRBS NORMAL, n = 3, the Data Format to RZ and the internal Sync Mode switch mounted on assembly A37 to ÷2. All other controls to the Reference Settings as in Figure 3-3.

2. Connect a 608E VHF Signal Generator set to 150MHz at >200mV rms to the 3760A CLOCK INPUT.

3. Connect the 3760A DATA OUTPUT terminated in 50Ω to INPUT C on a 5327A Timer/Counter. Connect the 3760A SYNC OUTPUT to the counter EXT OSCILLATOR input (rear panel). Set the counter controls as follows:

   INPUT C .. .. ÷10
   FUNCTION .. .. FREQ C
   MULTIPLIER .. .. 10^7
   OSC (rear panel) .. .. EXT

4. Set the WORD switches to 101.

5. The counter reading should be 80000.00 ±.01.

6. Change the Data Mode switch to PRBS – ERROR ADD and check that the counter reading is now 80010.00±.01.

7. Change the WORD switches to 011. The counter reading should now be 79990.00±.01.

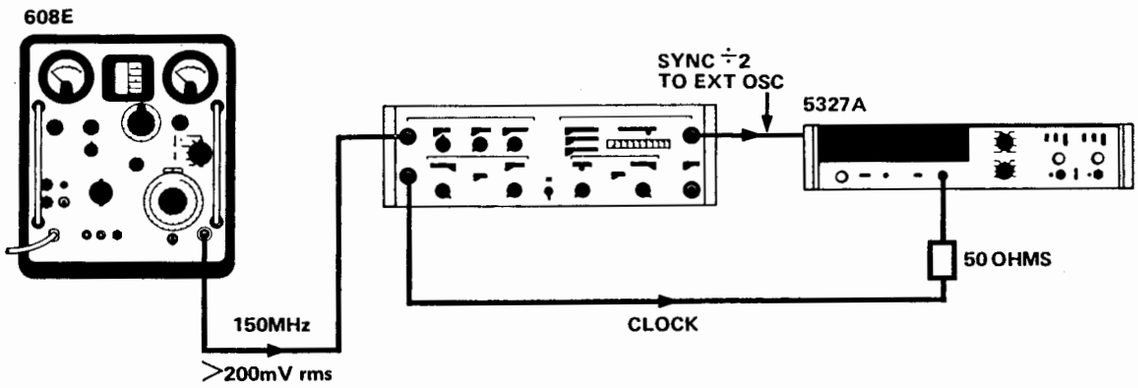


TABLE 1
WORD: n = 6

NUMBER OF ZEROS	COUNTER READING	NUMBER OF ZEROS	COUNTER READING
1	14	19	50
2	16	29	70
3	18	39	90
4	20	49	110
5	22	59	130
6	24	69	150
7	26	79	170
8	28	89	190
9	30	99	210

TABLE 2
PRBS: n = 5

NUMBER OF ZEROS	COUNTER READING	NUMBER OF ZEROS	COUNTER READING
1	64	19	100
2	66	29	120
3	68	39	140
4	70	49	160
5	72	59	180
6	74	69	200
7	76	79	220
8	78	89	240
9	80	99	260

Figure 3-13 Zero Add

ZERO ADD

SPECIFICATION:

Word Zero Add: Addition of a block of 1 to 99 zeros into WORD NORMAL, occurring between words.

PRBS Zero Add: Addition of a block of 1 to 99 zeros into PRBS NORMAL.

PROCEDURE:

1. Set the 3760A DATA MODE switch to WORD ZERO ADD and the WORD LENGTH switch to n = 6. All other controls to the Reference Settings as in Figure 3-3.

2. Connect a 608E VHF Signal Generator set to 150MHz at >200mV rms to the 3760A CLOCK INPUT.

3. Connect the 3760A CLOCK OUTPUT terminated in 50Ω to INPUT C on a 5327A Timer/Counter. Connect the 3760A SYNC OUTPUT to the counter EXT OSCILLATOR (rear panel). Set the counter controls as follows:

   INPUT C .. .. ÷10
   FUNCTION .. .. FREQ C
   MULTIPLIER .. .. 10^5
   OSC (rear panel) .. .. EXT

4. Set the 3760A Sync Mode switch mounted on A37 to ÷2.

5. Check that the counter reads twice the sequence length, ie, 12.

6. Add zeros in accordance with Table 1 and check the counter reading at each step.

7. Change the 3760A DATA MODE switch to PRBS – ADD ZEROS and the PRBS LENGTH to n = 5.

8. Check that the counter reads twice the sequence length, ie, 62.

9. Add zeros in accordance with Table 2 and check the counter reading at each step.

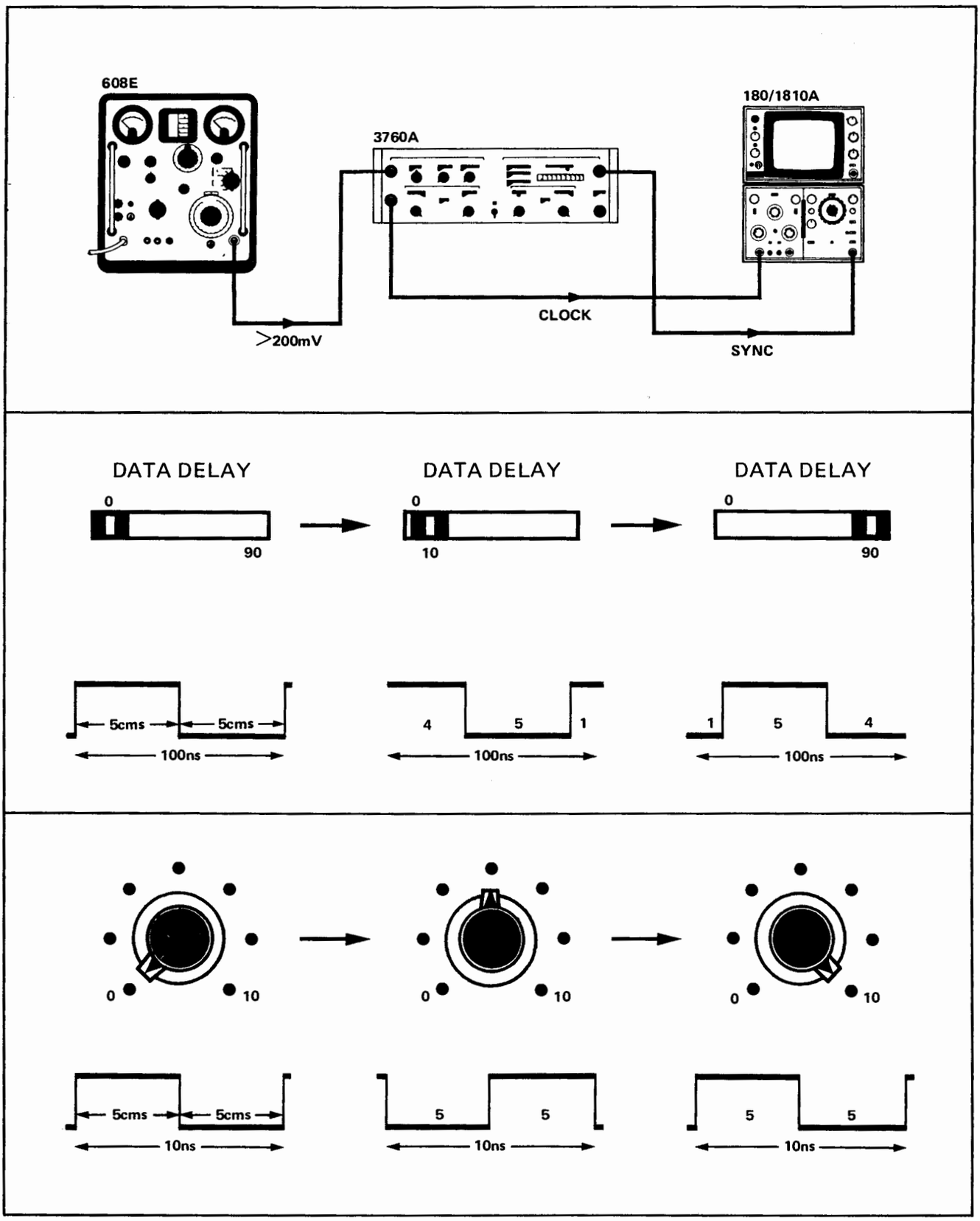


Figure 3-14 Data Delay

DATA DELAY

SPECIFICATION: Data Delay: 0 – 100nS in 10 ranges.

PROCEDURE:

1. Set the 3760A controls to the reference settings as in Figure 3-3.
2. Connect a 608E VHF Signal Generator set to 10MHz at >200mV rms to the 3760A CLOCK INPUT.
3. Connect the 3760A CLOCK OUTPUT to the CHAN A input of a 180/1810A Sampling Oscilloscope. Connect the 3760A SYNC OUTPUT to the oscilloscope TRIGGER input and switch trigger selector to EXT.
4. Adjust the oscilloscope controls to display exactly one clock period (100nS) over 10cms.
5. Switch the DATA DELAY range switch from 0 to 90nS in 10nS steps and check that the displayed waveform moves 1cm from right to left at each step.
6. Increase the Signal Generator frequency from 10 to 100MHz and again display exactly one clock period (10ns) over 10cms.
7. Check that the displayed waveform moves uniformily by 10cms from right to left as the DATA DELAY vernier is turned fully clockwise.

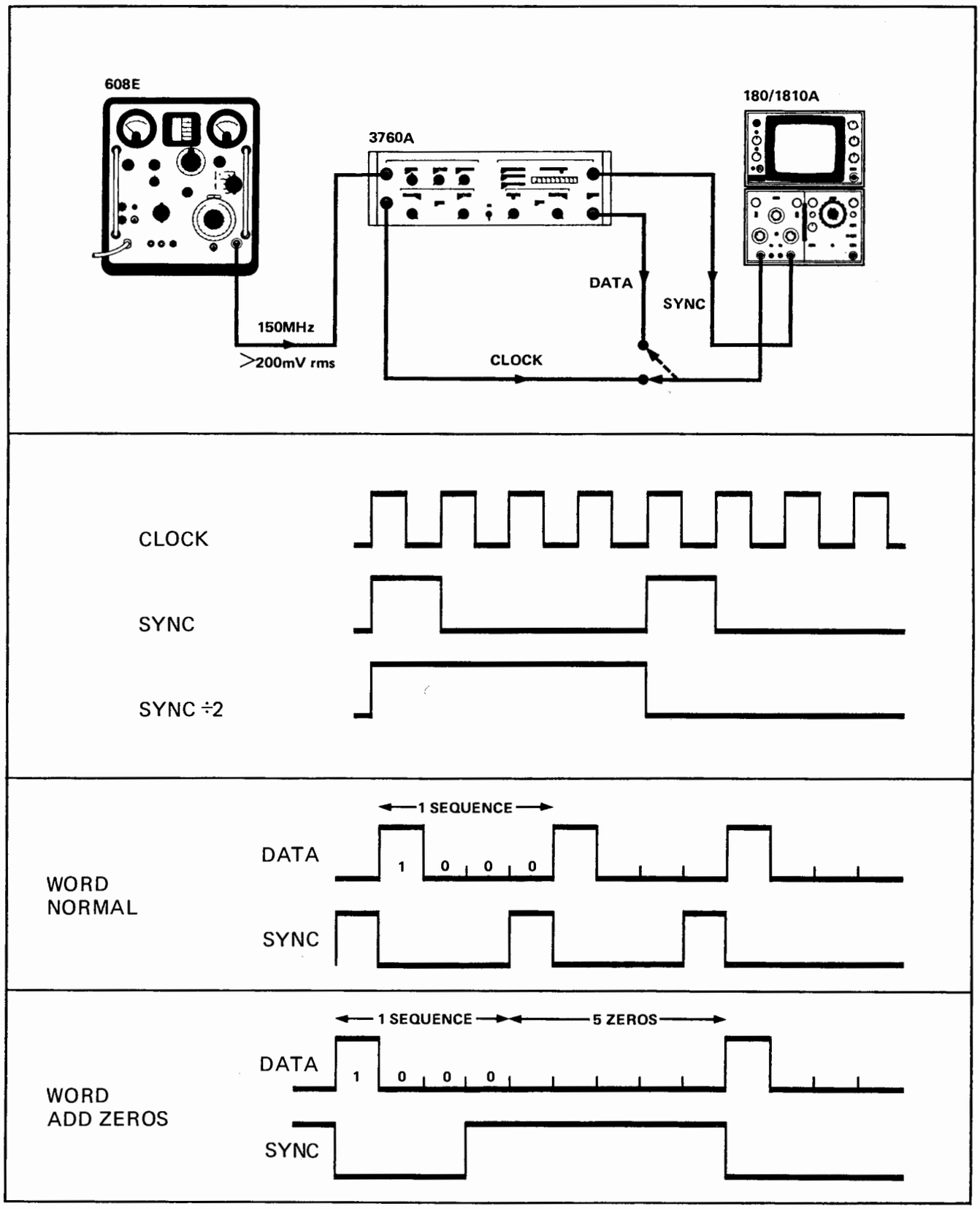


Figure 3-16 Sync Output

SYNC OUTPUT

SPECIFICATION:

Amplitude:	+1V nominal.
Rate:	Once per PRBS or Word cycle.
Duration:	One clock period plus the length of the zero block if added.
Position:	Front panel selectable on PRBS NORMAL. Precedes the Word, Zero Block and Error by 1 clock period in other modes.

PROCEDURE:

1. Set the 3760A WORD LENGTH to n = 4, the WORD switches to 1000 and all other controls to the Reference Settings as in Figure 3-3.

2. Connect a 608E VHF Signal Generator set to 150MHz at >200mV rms to the 3760A CLOCK INPUT.

3. Connect the 3760A CLOCK OUTPUT to the CHAN A input of a 180/1810A Sampling Oscilloscope. Connect the 3760A SYNC OUTPUT to CHAN B input and set the oscilloscope DISPLAY MODE switch to ALT – CHAN B.

4. Check that the amplitude of the Sync pulse displayed on the oscilloscope is approximately +1V.

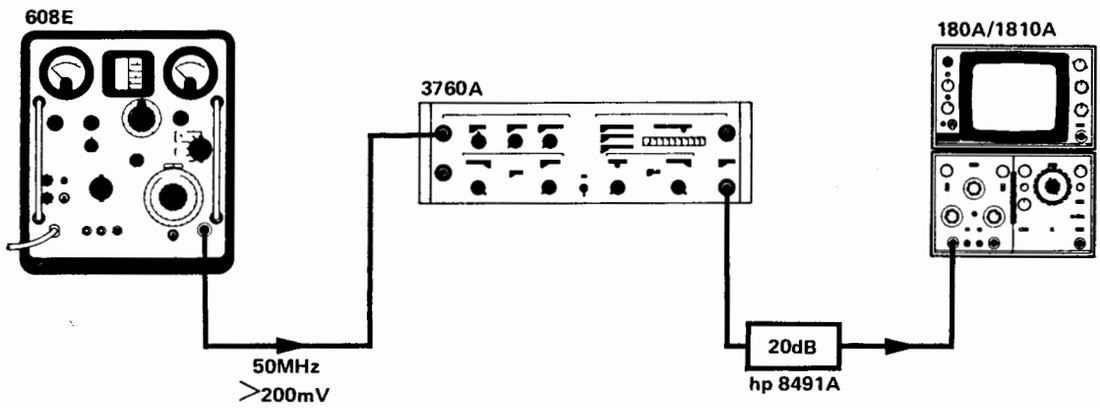
5. Check that the width of the sync pulse is one clock period.

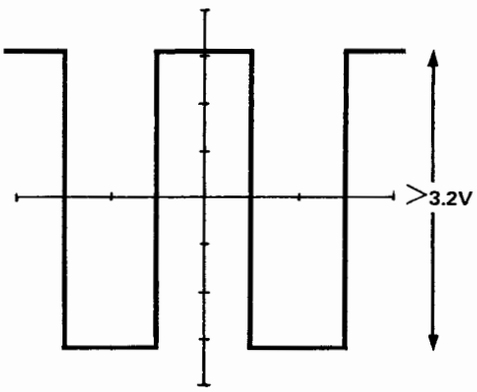
6. Change the Sync Mode switch mounted on A37 to ÷2 and check that the SYNC OUTPUT is now a square wave with a period equal to 2 sequence lengths, ie, 8 clock periods. Return the Sync Mode to NORMAL.

7. Change the 3760A DATA MODE to WORD – ADD ZEROS. Add 5 zeros and check that the sync pulse is now 9 clock periods long.

8. Disconnect the 3760A CLOCK OUTPUT and connect the DATA OUTPUT to the oscilloscope.

9. Check that the sync pulse precedes the word 1000 as shown in the diagram opposite.





AMPLITUDE RANGE	DISPLAY AMPLITUDE
1.6 – 3.2V	3.2V
0.8 – 1.6V	1.6V ±0.06V
0.4 – 0.8V	0.8V ±0.06V
0.2 – 0.4V	0.4V ±0.02V
0.1 – 0.2V	0.2V ±0.02V

Figure 3-18 Data Output – Amplitude

DATA OUTPUT – AMPLITUDE

SPECIFICATION: Amplitude: Continuously variable in five ranges from 0:1 to 3.2V pk-pk.

PROCEDURE:

1. Set the 3760A DATA OUTPUT AMPLITUDE to 1.6 – 3.2V and the vernier fully clockwise. All other controls to the Reference Settings as in Figure 3-3.

2. Connect a 180A/1810A Sampling Oscilloscope via an 8491A (Option 20) 20dB Coaxial Attenuator to the 3760A DATA OUTPUT.

3. Connect a 608E VHF Signal Generator set to 50MHz at >200mV rms to the 3760A DATA INPUT.

4. The amplitude of the displayed waveform should be at least 3.2V pk-pk and the dc offset should be less than 0.06V.

5. Adjust the DATA OUTPUT AMPLITUDE vernier until the amplitude of the displayed waveform is exactly 3.2V pk-pk.

6. Switch through the DATA OUTPUT AMPLITUDE ranges and check the amplitude of the displayed waveform against the following table:

AMPLITUDE RANGE	DISPLAY AMPLITUDE
1.6 – 3.2V	3.2V
0.8 – 1.6V	1.6V ±0.06V
0.4 – 0.8V	0.8V ±0.06V
0.2 – 0.4V	0.4V ±0.02V
0.1 – 0.2V	0.2V ±0.02V

7. Set the DATA OUTPUT AMPLITUDE range to 1.6 – 3.2V and adjust the vernier until the amplitude of the displayed waveform is exactly 3.2V pk-pk. Set the DATA/$\overline{\text{DATA}}$ switch to $\overline{\text{DATA}}$.

8. The amplitude of the displayed waveform should still be 3.2V pk-pk.

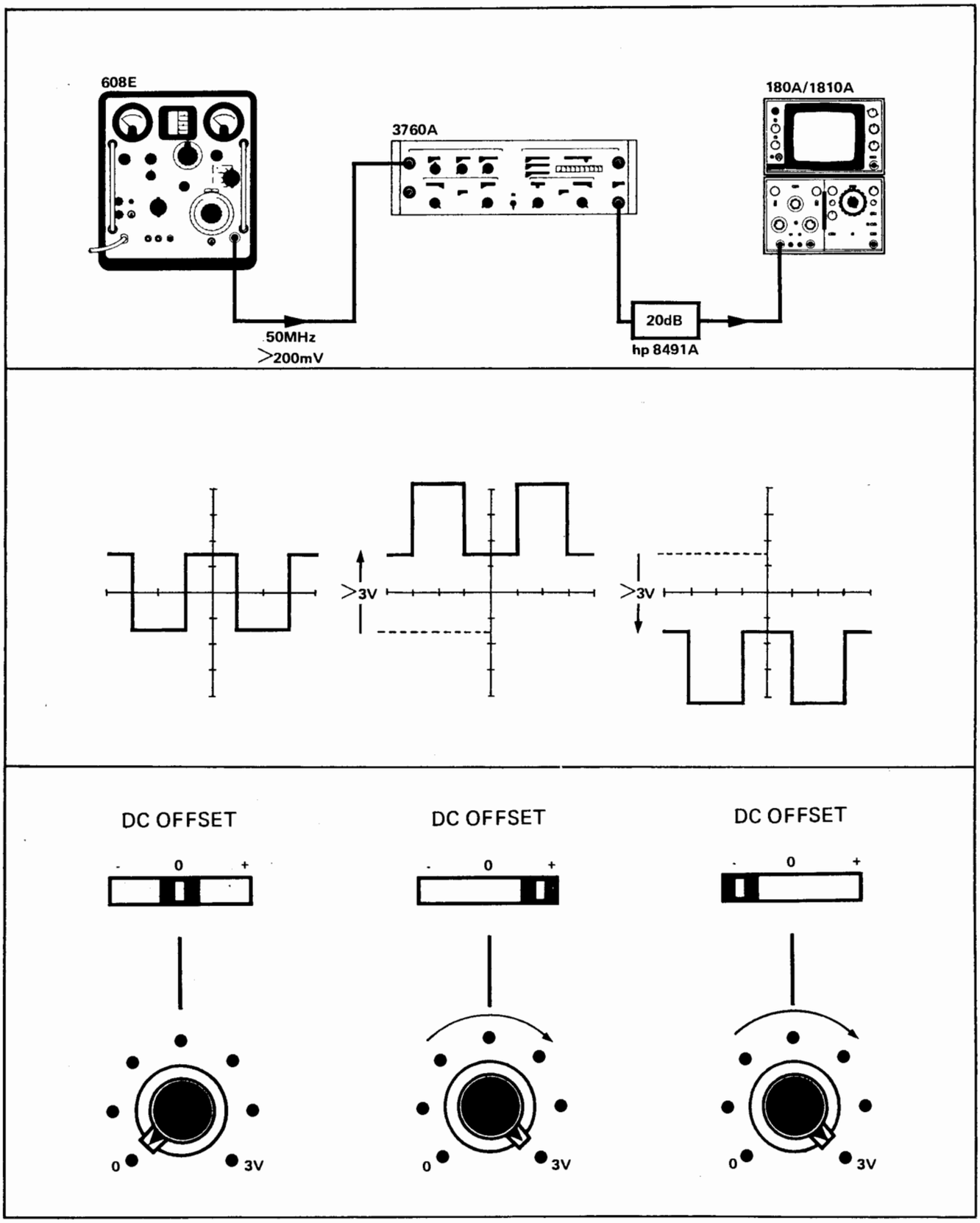


Figure 3-17 Data Output – DC Offset

DATA OUTPUT –
DC OFFSET

SPECIFICATION: Range: 0 to ±3V.

PROCEDURE:

1. Set the 3760A DATA OUTPUT AMPLITUDE range switch to 1.6 – 3.2V. All other controls to the Reference Settings as in Figure 3-3.
2. Connect a 608E VHF Signal Generator set to 50MHz at >200mV rms to the 3760A DATA INPUT.
3. Connect the 3760A DATA OUTPUT via an 8491A (OPTION 20) 20dB Coaxial Attenuator to the CHAN A input of a 180A/1810A Sampling Oscilloscope.
4. Adjust the 3760A DATA OUTPUT AMPLITUDE vernier for an output pulse amplitude of 3.0V and display this waveform on the oscilloscope.
5. Set the 3760A DATA DC OFFSET range switch to +.
6. Check that the dc offset of the displayed waveform increases from 0 to at least +3V as the DATA DC OFFSET vernier is rotated clockwise. Turn the vernier fully counterclockwise.
7. Set the 3760A DATA DC OFFSET range switch to -.
8. Check that the dc offset of the displayed waveform increases from 0 to at least -3V as the DATA DC OFFSET vernier is rotated clockwise.

PRBS NORMAL

SPECIFICATION:

PRBS NORMAL: Generation of a $2^n - 1$ maximal length, Pseudo Random Binary Sequence, where n = 3 to 10 and 15.

PROCEDURE:

1. Set the 3760A DATA MODE switch to PRBS NORMAL, the PRBS LENGTH switch to n = 15 and all other controls to the Reference Settings as in Figure 3-3.

2. Connect a 608E VHF Signal Generator set to 150MHz at >200mV rms, to the 3760A CLOCK INPUT.

3. Connect the 3760A CLOCK OUTPUT to a 5327A Timer/Counter, INPUT C. Connect the 3760A SYNC OUTPUT to the Counter EXT OSCILLATOR INPUT (rear panel). Set the Counter controls as follows:

   INPUT C .. .. ÷10
   FUNCTION .. .. FREQ C
   MULTIPLIER .. .. 10^3
   OSC (rear panel) .. .. EXT

4. Set the 3760A Sync Mode switch mounted on A37 to ÷2.

5. Change the PRBS LENGTH switch from n = 15 to n = 3 and check the counter reading against the following table at each step.

SEQUENCE LENGTH	COUNTER DISPLAY ±2
15	65,534
10	2,046
9	1,022
8	510
7	254
6	126
5	62
4	30
3	14

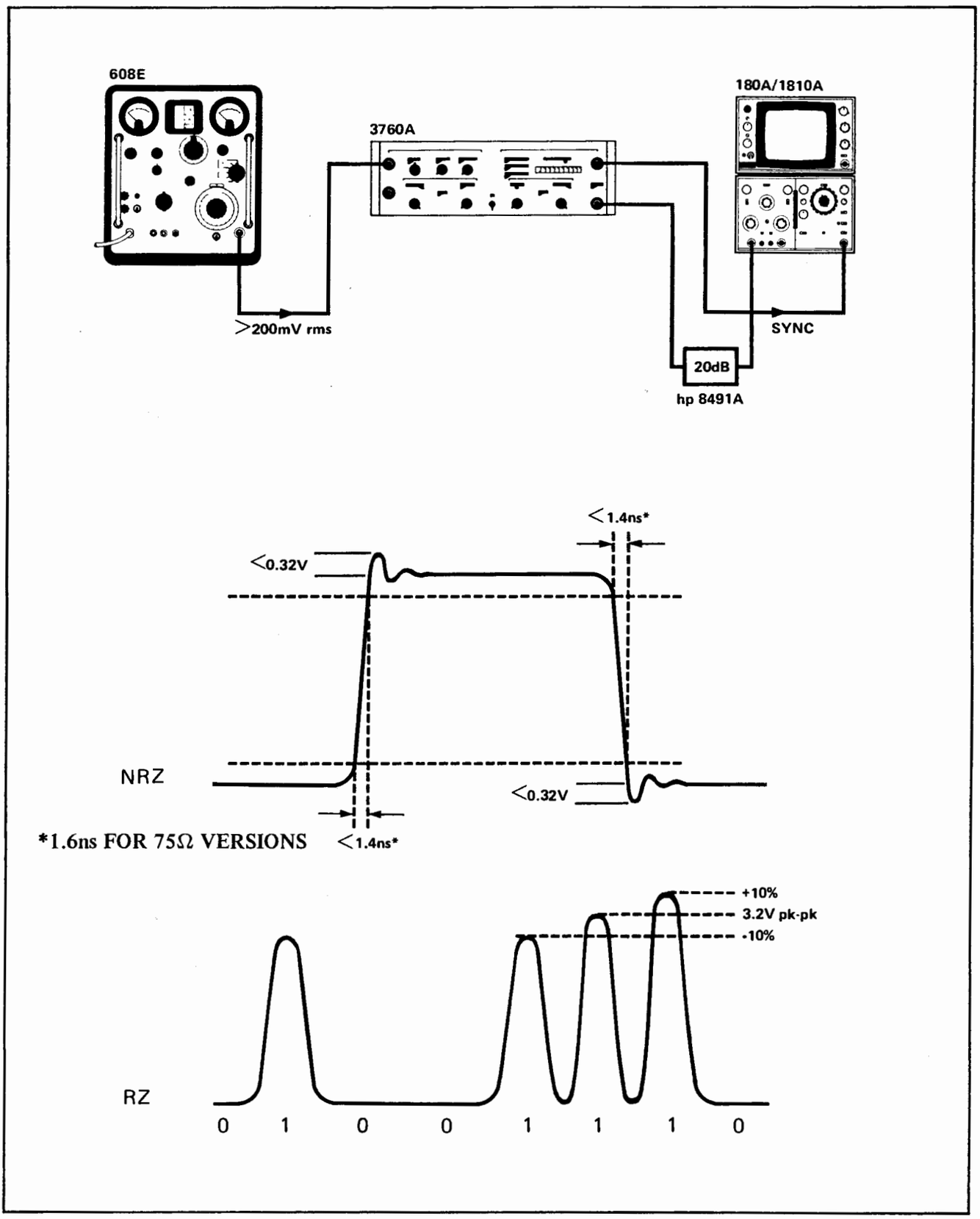


Figure 3-19 Data Output – Pulse Shape

DATA OUTPUT – PULSE SHAPE

SPECIFICATION:

Rise/Fall Time:	<1.4ns (10% to 90% level) <1.6ns in 75Ω versions
Overshoot:	<10% of pulse amplitude
Format:	NRZ RZ (up to 130Mb/s).

PROCEDURE

1. Set the 3760A DATA MODE switch to PRBS NORMAL, n = 3 and the DATA OUTPUT AMPLITUDE range switch to 1.6 – 3.2V. All other controls to the Reference Settings as in Figure 3-3.

2. Connect a 608E VHF Signal Generator set to 150MHz at >200mV rms to the 3760A CLOCK INPUT.

3. Connect the 3760A DATA OUTPUT via an 8491A (Option 20) 20dB Coaxial Attenuator to the Channel A input of a 180A/1810A Sampling Oscilloscope.
   Connect the 3760A SYNC OUTPUT to the 180A/1810A TRIGGER input and set the trigger selector to EXT.

4. Adjust the 3760A DATA OUTPUT AMPLITUDE vernier for an output pulse amplitude of 3.2V pk-pk. The Rise/Fall time of the displayed waveform should be less than 1.4ns/1.6ns for 75Ω versions) with an overshoot of less than 10% of the pulse amplitude ie, <0.32V.

5. Slowly reduce the amplitude of the DATA OUTPUT from 3.2V to 0.1V pk-pk and check that the overshoot is less than 10% of the output pulse amplitude over this range.

6. Reset the output pulse amplitude to exactly 3.2V pk-pk and change the data format from NRZ to RZ.

7. Reduce the Signal Generator output to 130MHz.

8. The data should now be displayed in the Return to Zero format and all pulses should be 3.2V ±0.32V pk-pk.

9. Note the width of the pulses.

10. Change the DATA/$\overline{\text{DATA}}$ switch to $\overline{\text{DATA}}$ and check that the pulse width is within 10% of that obtained in operation (9).

SECTION IV
ADJUSTMENT PROCEDURES

INTRODUCTION

The Adjustment Procedures described in this section are self contained and may be performed in any order, although for obvious reasons Power Supply adjustments should be made first. Each procedure is presented in two parts, the left hand page describes the procedure on a step by step basis while the right hand page presents it in graphical form. A list of Reference Settings to which the 3760A should be set at the beginning of each adjustment is given on Page 3-3.

LIST OF ADJUSTMENTS

Figure 4-1

TEST EQUIPMENT

Item	Minimum Specifications	Recommended
Digital Voltmeter	Range: +15 to -15V dc Accuracy: ±0.05%	*hp* 3440A
VHF Signal Generator	Frequency Range: 10 to 150MHz Output Level: 0 to 3V RMS	*hp* 608E
Test Oscillator	Frequency: 10MHz Output Level: ⩾200mV rms	*hp* 651B
Sampling Oscilloscope	Bandwidth: 1GHz Input Impedance: 50 ohms External Trigger: 3ns pulse	*hp* 180A/1810A
Electronic Counter	Frequency Range: 0 – 150MHz	*hp* 5327A

Figure 4-2

POWER SUPPLIES

SPECIFICATION: Nominal Voltage: ±0.02V

PROCEDURE:

1. Connect a 3440A Digital Voltmeter between the +15V test point on A42 and ground.
2. Adjust A42R12 for a reading of +15V ±0.02V.
3. Connect the Digital Voltmeter between the -15V test point on A42 and ground.
4. Adjust A42R2 for a reading of -15V ±0.02V.
5. Connect the Digital Voltmeter between A43TP1 and ground.
6. Adjust A43R9 for a reading of -5.2V ±0.02V.

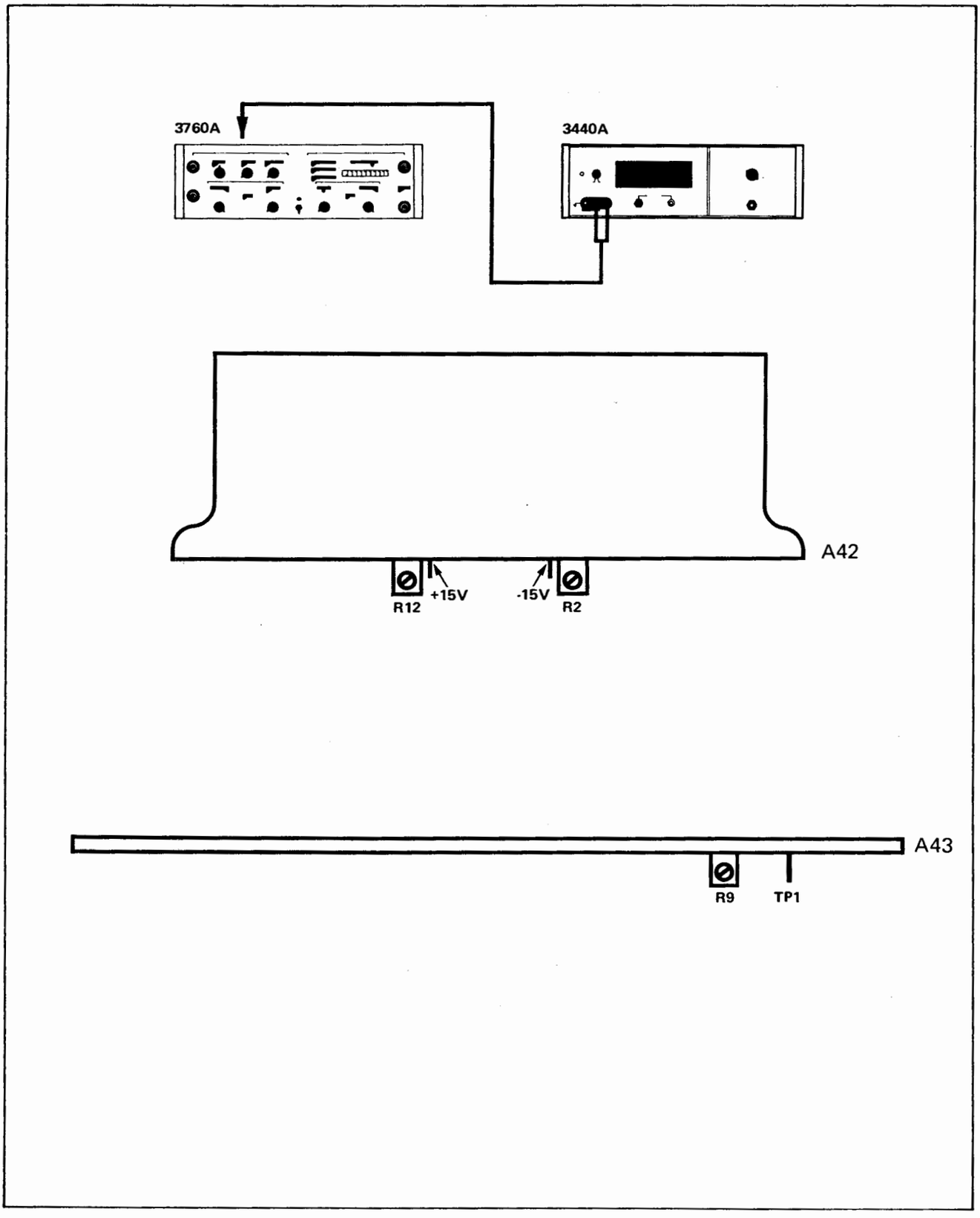


Figure 4-1 Power Supplies

CLOCK GENERATOR – FREQUENCY RANGE

SPECIFICATION: Frequency Range: 1.5 – 150MHz in two decade ranges

PROCEDURE:

1. Set the 3760A CLOCK RATE switch to 1.5 – 15, the CLOCK OUTPUT AMPLITUDE range switch to 1.6 – 3.2 and the vernier fully clockwise. All other controls to the Reference Settings as in Figure 3-3.
2. Connect a 5327A Electronic Counter terminated in 50Ω to the 3760A CLOCK OUTPUT.
3. Turn the 3760A RATE vernier fully counterclockwise.
4. Adjust A24R19 for a counter reading of 1.37MHz.
5. Turn the 3760A RATE vernier fully clockwise.
6. Adjust A24R17 for a counter reading of 16MHz.
7. Change the 3760A RATE switch to 15 – 150 and turn the vernier fully counterclockwise.
8. Adjust A24R18 for a counter reading of 14MHz.
9. Turn the vernier fully clockwise.
10. Adjust A24R16 for a counter reading of 153MHz.

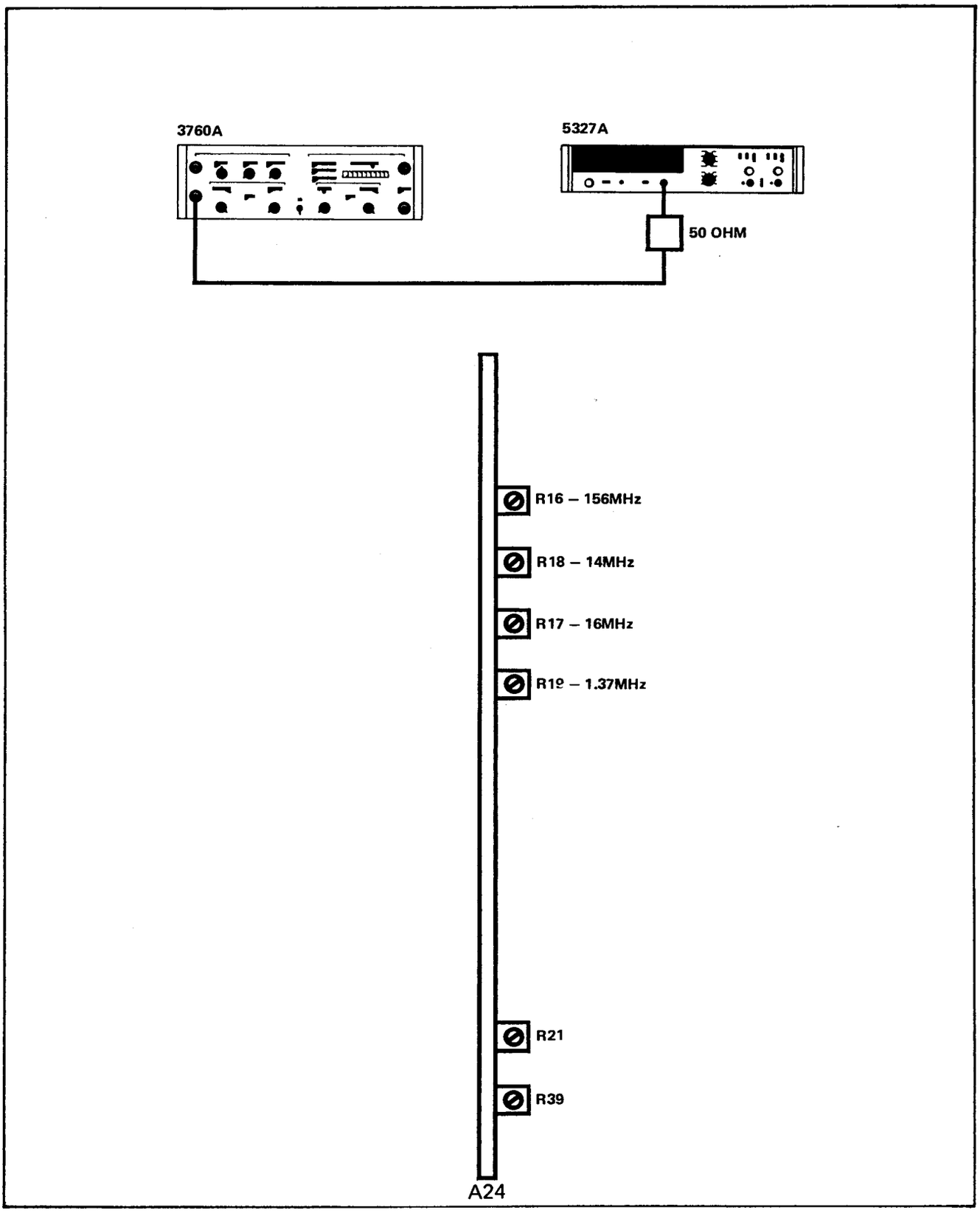


Figure 4-2 Clock Generator:Frequency Range

CLOCK OUTPUT – M:S RATIO

SPECIFICATION: Mark:Space ratio 1:1 ±10%

PROCEDURE:

1. Set the 3760A TRIGGER MODE to AUTO, the CLOCK OUTPUT AMPLITUDE range switch to 1.6 – 3.2V and the vernier fully clockwise. All other controls to the Reference Settings as in Figure 3-3.
2. Connect a 608E VHF Signal Generator set to 150MHz at 200mV rms to the 3760A CLOCK INPUT.
3. Connect a 180A/1810A Sampling Oscilloscope via an *hp* 8491A Coaxial Attenuator (Option 20) to the 3760A CLOCK OUTPUT.
4. Switch between CLOCK and $\overline{\text{CLOCK}}$ and adjust A29R3 for equal width CLOCK and $\overline{\text{CLOCK}}$ pulses.
5. With the output set to CLOCK, adjust A25R1 until the displayed waveform has a mark:space ratio of 1:1 ±10%.
6. Repeat operation (4) if necessary.

OPTIONS 002/004 ONLY

7. Change the 3760A CLOCK RATE switch to 1.5 – 15 and turn the vernier fully clockwise.
8. Adjust A24R21 until the displayed waveform has a mark:space ratio of 1:1 ±10%.
9. Change the 3760A CLOCK RATE switch to 15 – 150 (vernier fully clockwise).
10. Adjust A24R39 until the displayed waveform has a mark:space ratio of 1:1 ±10%.

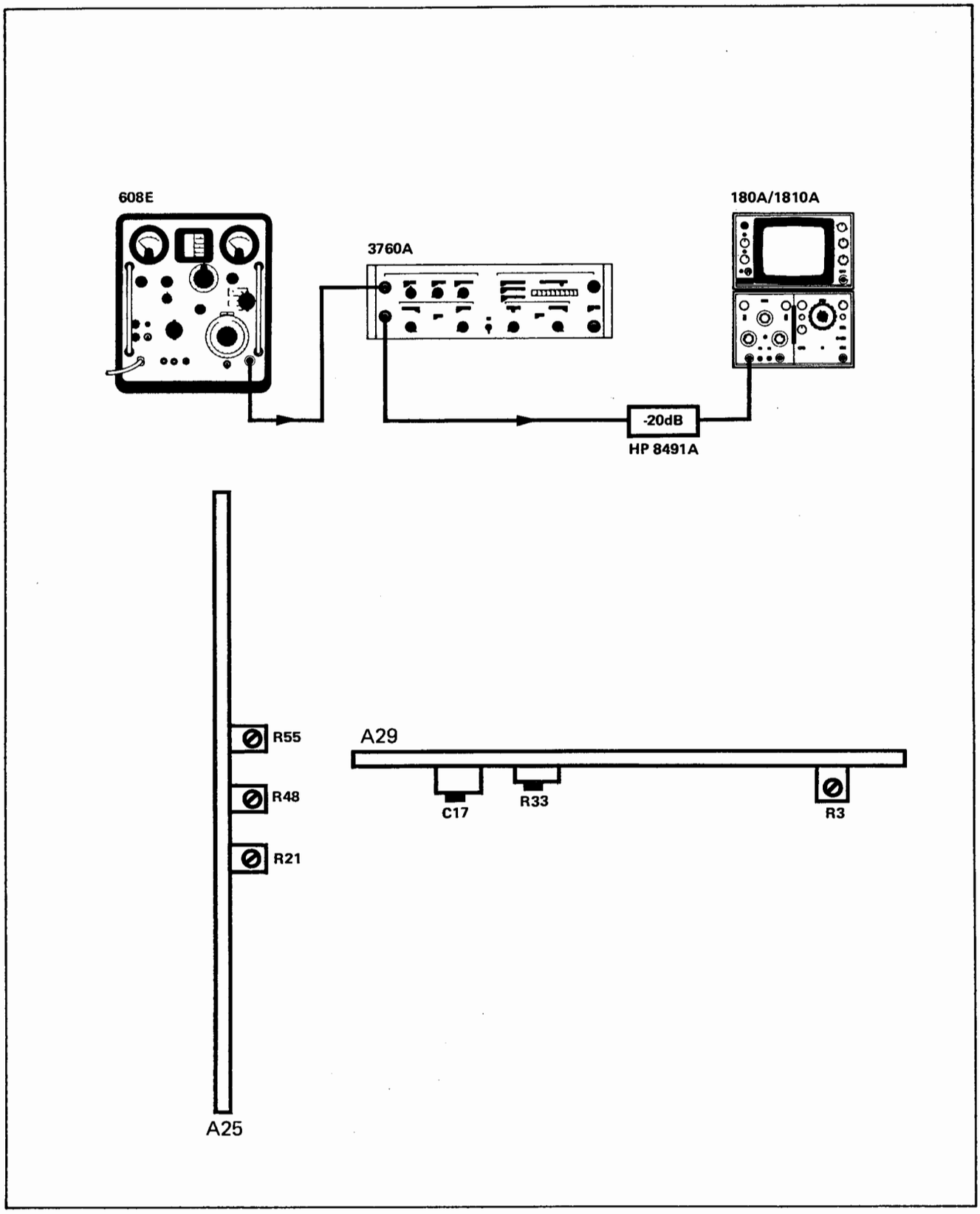


Figure 4-3 Clock Output – M:S Ratio

CLOCK OUTPUT – AMPLITUDE & PULSE SHAPE

SPECIFICATION:

Amplitude:	0.1 – 3.2V pk-pk
Rise/fall time:	<1.4ns (10% to 90% level) <1.6ns for 75Ω versions
Overshoot:	<10% of pulse amplitude

PROCEDURE:

1. Set the 3760A TRIGGER MODE to AUTO, the CLOCK OUTPUT AMPLITUDE to 1.6 – 3.2V and the vernier fully clockwise. All other controls to the Reference Settings as in Figure 3-3.

2. Connect a 608E VHF Signal Generator set to 50MHz at >200mV rms to the 3760A CLOCK INPUT.

3. Connect the 3760A CLOCK OUTPUT via an 8491A (Option 20) 20dB Coaxial Attenuator to the channel A input of a 180A/1810A Sampling Oscilloscope.

4. Adjust A28R7 and A28R10 until the amplitude of the displayed waveform is between 3.3V pk and 3.6V pk balanced about 0V.

5. Adjust A29R3 and A29C17 for minimum rise and fall times on the displayed waveform. Readjust A29R3 and A29C17 if necessary to reduce the overshoot to <0.32V but maintain a rise/fall time of <1.4ns (1.6ns for 75Ω versions).

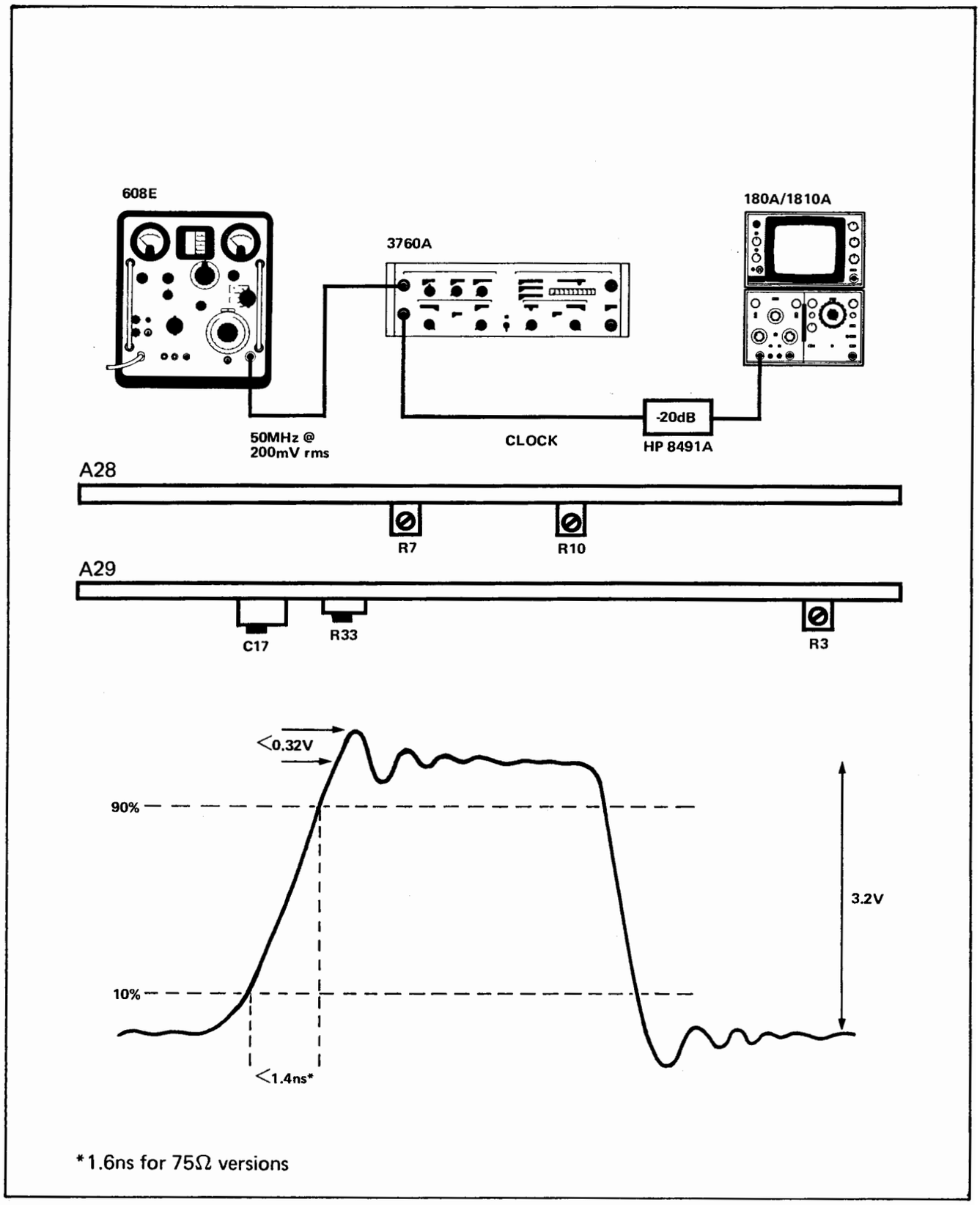


Figure 4-4 Clock Output – Amplitude & Pulse Shape

DATA DELAY

SPECIFICATION: Vernier Range: 10ns

PROCEDURE.

1. Set the 3760A controls to the Reference Settings as in Figure 3-3.
2. Connect a 608E VHF Signal Generator set to exactly 100MHz at >200mV rms to the 3760A CLOCK INPUT.
3. Connect the 3760A CLOCK OUTPUT to the CHAN A input of a 180A/1810A Sampling Oscilloscope.
   Connect the 3760A SYNC OUTPUT to the oscilloscope TRIGGER input and switch the trigger selector to EXT.
4. Set the DATA DELAY vernier fully clockwise and adjust the oscilloscope controls to display exactly one clock period (10ns) over 10cms.
5. Check that the displayed waveform moves uniformily by at least 10cms as the DATA DELAY vernier is turned fully counterclockwise. Adjust A27R12 if necessary.

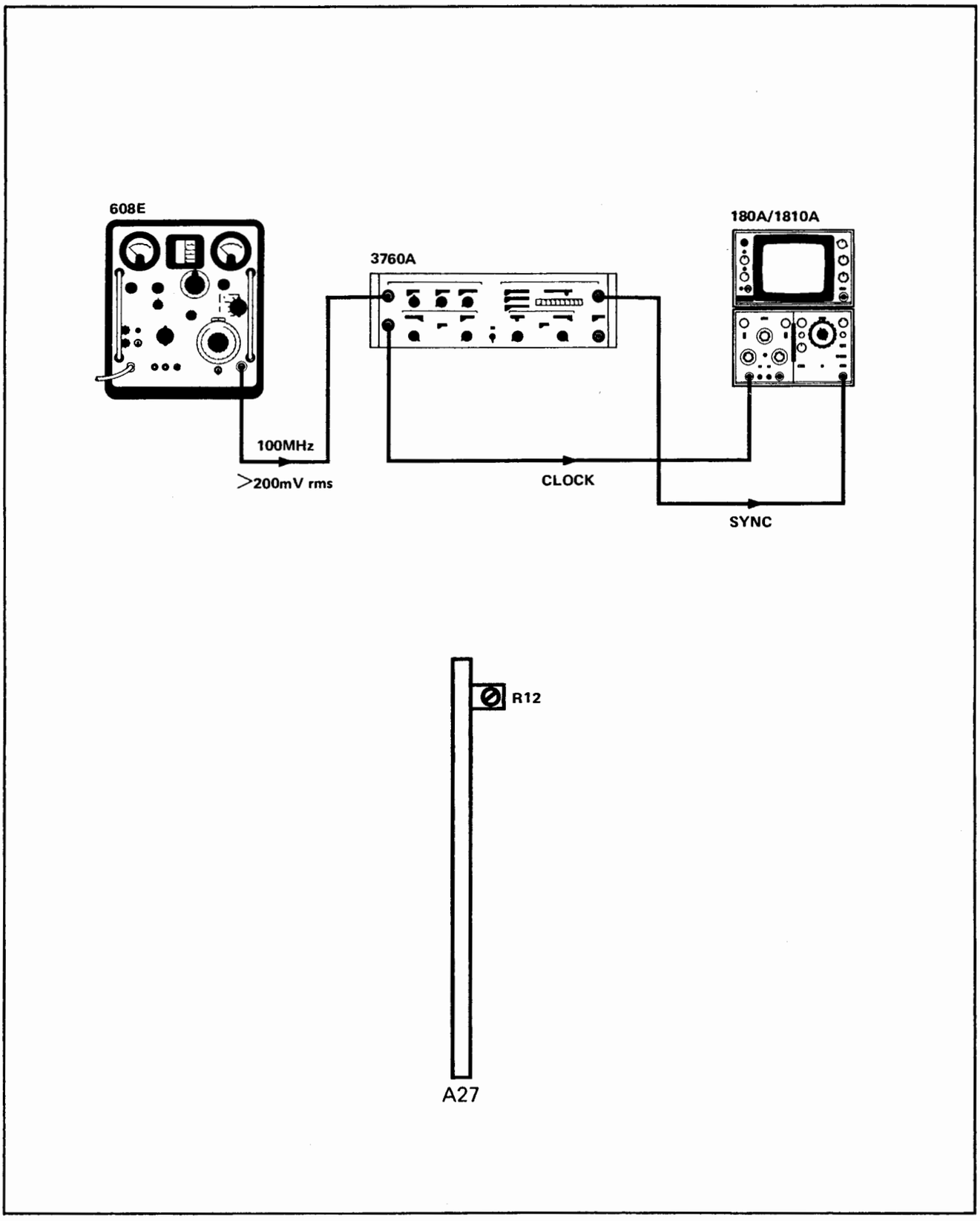


Figure 4-5 Data Delay

NRZ-RZ CONVERSION

SPECIFICATION: Conversion of the data format from Non Return to Zero (NRZ) to Return to Zero (RZ) up to 130Mb/s.

1. Set the 3760A data mode to 1010 and select RZ format. All other controls to the Reference Settings as in Figure 3-3.
2. Connect a 608E VHF Signal Generator set to 130MHz at >200mV rms to the 3760A CLOCK INPUT.
3. Connect the 3760A CLOCK OUTPUT to the CHAN B input of a 180A/1810A Sampling Oscilloscope.
4. Connect the 3760A DATA OUTPUT to the CHAN A input of the Sampling Oscilloscope.
5. Adjust A25R55 until the mark of the data stream is the same width as the mark of the clock signal.

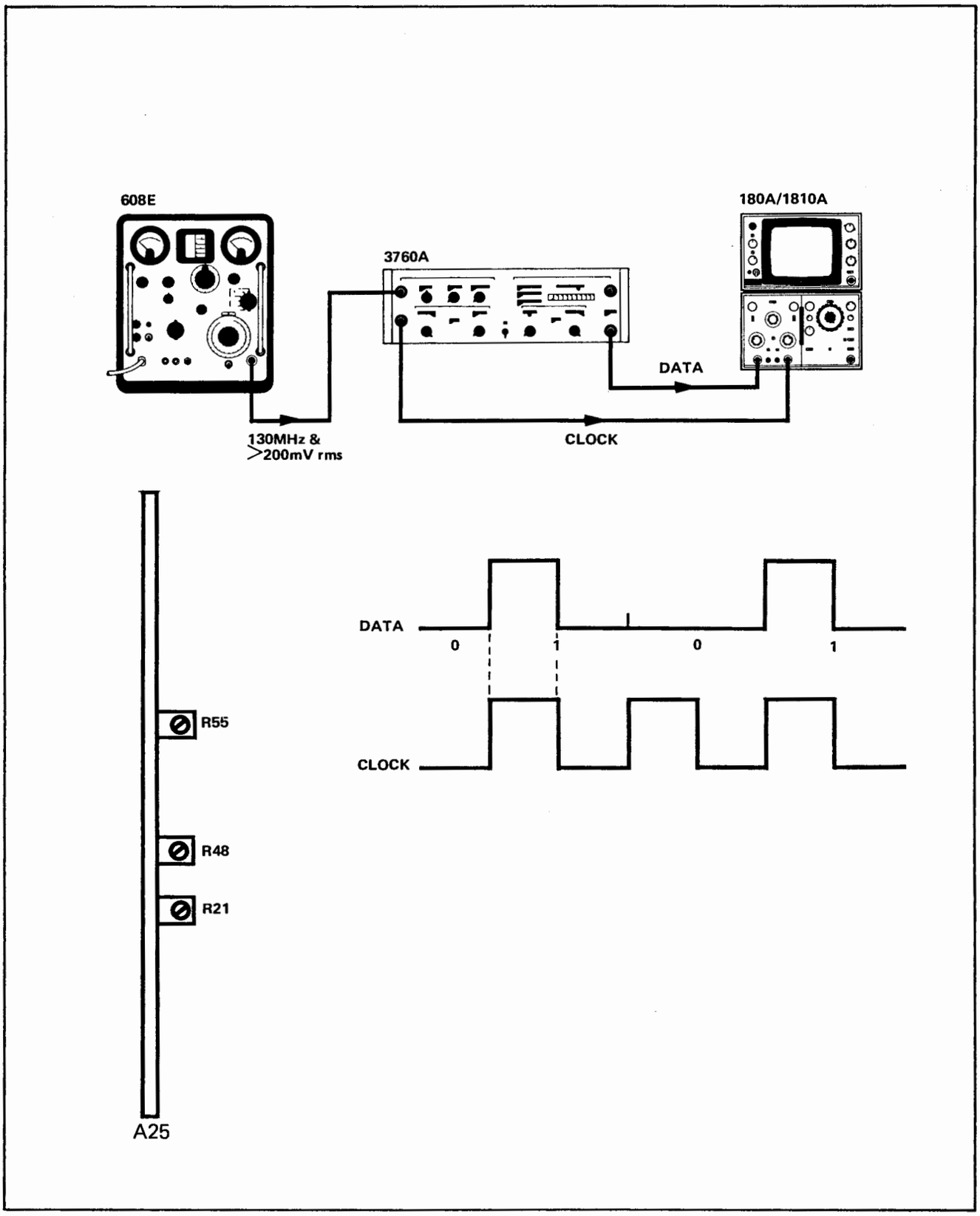


Figure 4-6 NRZ/RZ Conversion

SYNC OUTPUT LEVEL

SPECIFICATION: Amplitude: +1.0V

PROCEDURE:

1. Set the 3760A DATA MODE to PRBS NORMAL, n = 3. All other controls to the Reference Settings as in Figure 3-3.
2. Connect a 651B Test Oscillator set to 10MHz at >200mV rms to the 3760A CLOCK INPUT.
3. Connect the 3760A SYNC OUTPUT terminated in 50Ω to a 180A/1801A/1820A Oscilloscope.
4. Adjust A37R17 for a pulse amplitude of +1V.

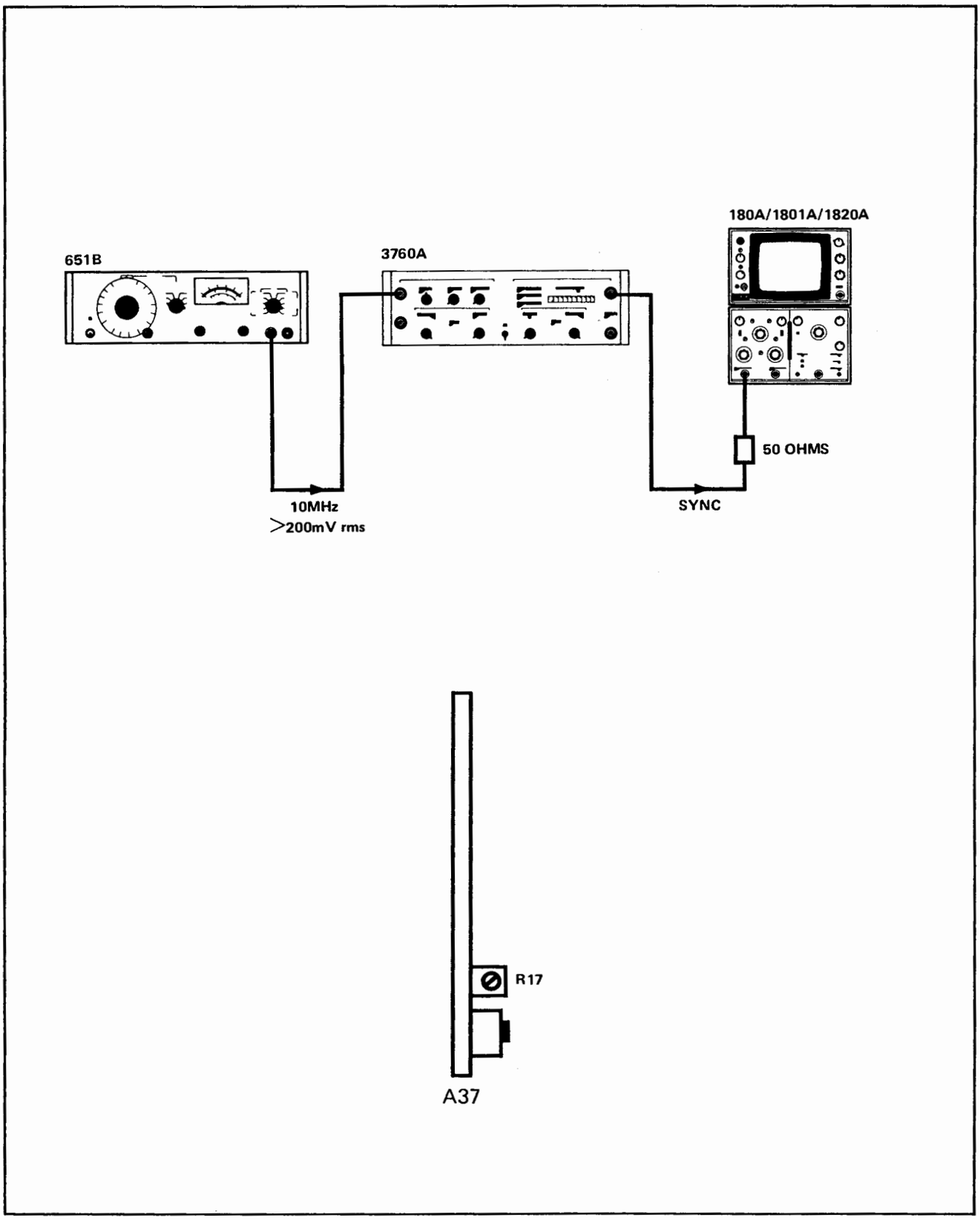


Figure 4-7 Sync Output Level

DATA OUTPUT – AMPLITUDE & PULSE SHAPE

SPECIFICATION:

Amplitude:	0.1 – 3.2V pk-pk
Rise/Fall time:	<1.4ns (10% to 90% level) <1.6ns for 75Ω versions
Overshoot:	<10% of pulse amplitude

PROCEDURE:

1. Set the 3760A Data Mode to 1010, the CLOCK TRIGGER MODE to AUTO, the DATA OUTPUT AMPLITUDE range switch to 1.6 – 3.2V and the vernier fully clockwise. All other controls to the Reference Settings as in Figure 3-3.

2. Connect a 608E VHF Signal Generator set to 50MHz at >200mV rms to the 3760A CLOCK INPUT.

3. Connect the 3760A DATA OUTPUT via an 8491A (Option 20) 20dB Coaxial Attenuator to the Channel A input of a 180A/1810A Sampling Oscilloscope.

4. Adjust A39R7 and A39R10 until the amplitude of the displayed waveform is between 3.2V pk-pk and 3.6V pk-pk balanced about 0V.

5. Adjust A39R33 and A39C17 for minimum rise and fall times on the displayed waveforms. Readjust A39C17 if necessary to reduce the overshoot to <0.32V but maintain a rise/fall time of <1.4ns (1.6ns for 75Ω versions).

6. Switch between DATA and $\overline{\text{DATA}}$ and adjust A39R3 until the width of the DATA mark is the same as the $\overline{\text{DATA}}$ mark.

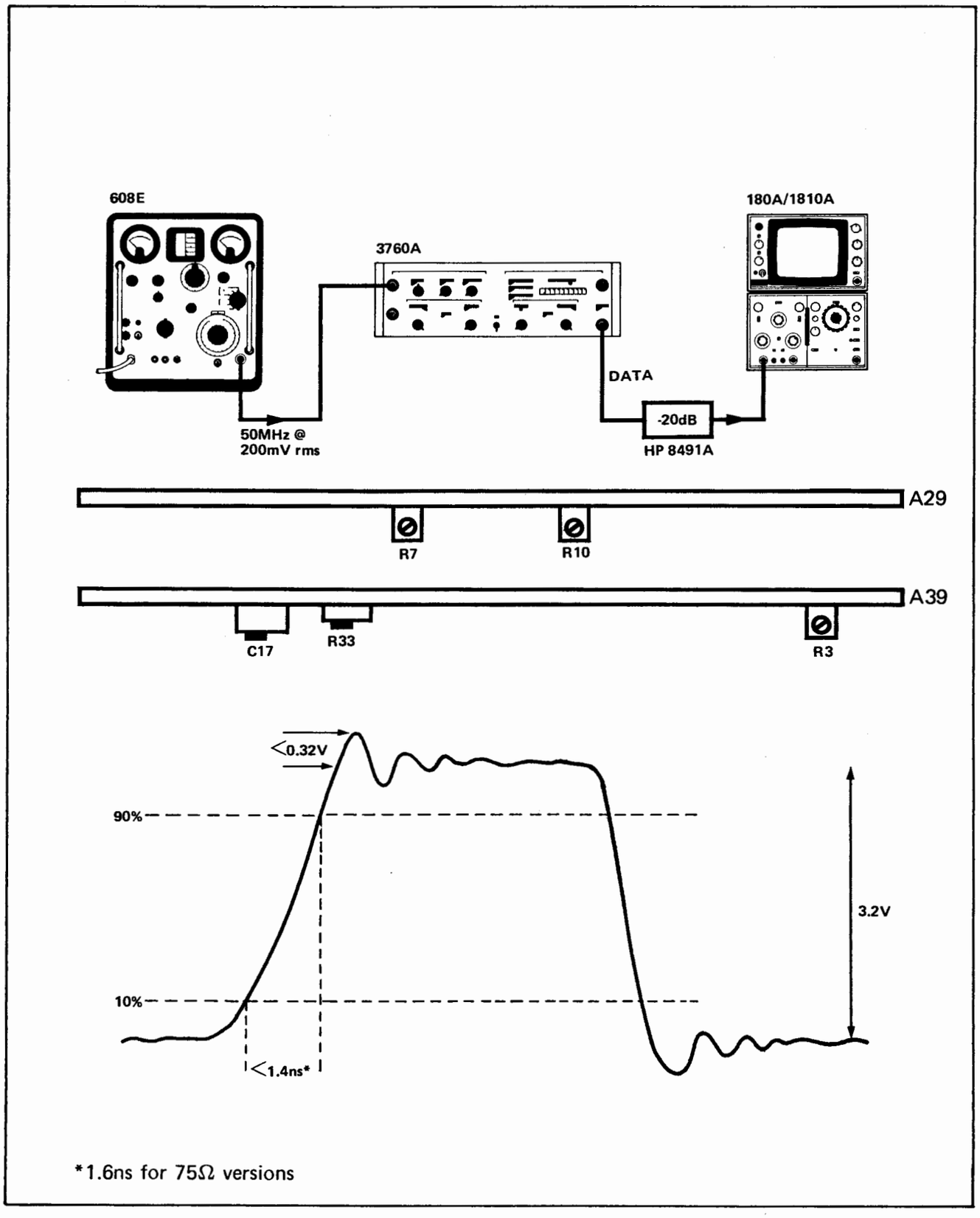


Figure 4-8 Data Output – Amplitude & Pulse Shape

SECTION V
TROUBLESHOOTING

INTRODUCTION

The purpose of this section is to allow faults to be isolated to one of the stages shown in the block diagram in Section VI. This block diagram is printed on a "throw-clear" page and should be consulted in conjunction with the Troubleshooting Procedures.

TROUBLESHOOTING PROCEDURES

In the following procedures certain assumptions are made. These are:

(i) All power supply lines including the mains are normal.

(ii) Only one fault exists.

(iii) All interconnections between assemblies are good.

Due to the obvious nature of certain faults they can be quickly isolated without the aid of a formal procedure. These include:

(i) Faults associated with the CLOCK OUTPUT.

(ii) Amplitude, dc offset, rise/fall times and overshoot of the CLOCK and DATA OUTPUTS. Note that some of these characteristics can be adjusted.

(iii) Incorrect operation of ADD ZEROS, ADD ERROR, NRZ to RZ conversion. (Assuming that the instrument operates correctly in PRBS and WORD NORMAL).

(iv) Certain faults associated with the DATA OUTPUT eg, PRBS sequences being generated instead of WORD sequences.

More complex faults associated with the DATA OUTPUT and/or SYNC OUTPUT which occur in PRBS NORMAL or WORD NORMAL modes can be isolated by using one of the following charts:

(i) CHART A. This chart should be used if the DATA OUTPUT is completely inoperative in all PRBS or WORD sequences.

(ii) CHART B. This chart should be used only if a binary output can be obtained in at least one PRBS or WORD sequence. It is irrelevant if the sequence is correct or not.

CHART A

NOTES

A-1 The fault lies in Assembly A37 or in the Data Output Stage. Monitor the DATA signal at A39-2 to isolate.
NOTE: Assemblies A38 and A39 can be replaced by assemblies A28 and A29 respectively.

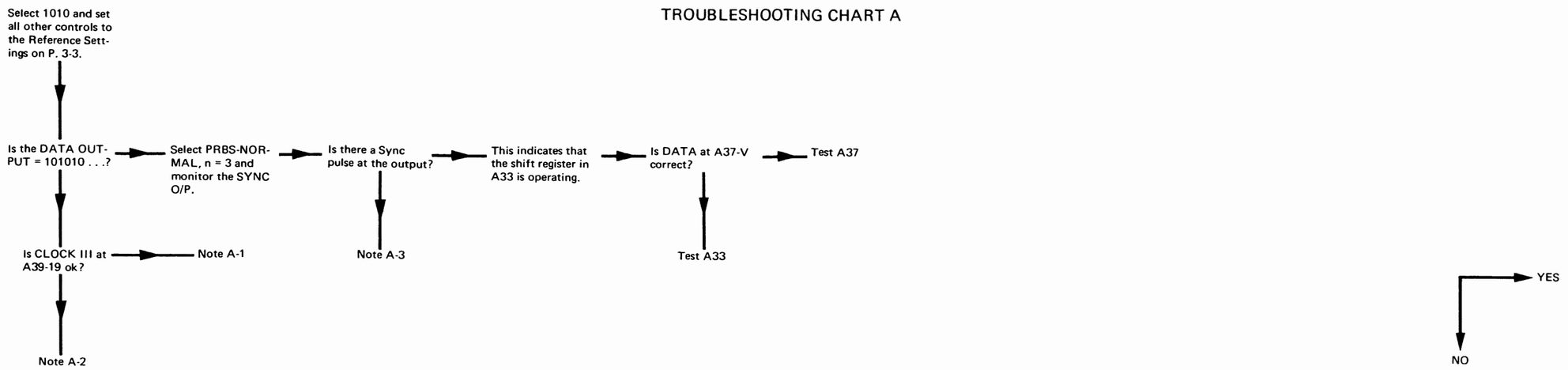
A-2 The fault lies in the Clock Module or in Assembly A31. Monitor at A31-J1 to isolate.

A-3 Inputs to the A33 Assembly should be checked against the following table:

SIGNAL	PIN	NORMAL STATE
CLOCK II	A33-V	CLOCK
CLOCK INHIBIT	A33-13	0
SET	A33-N	0
RESET	A33-11	1
SELF-START	A33-U	1
S1-S5		SEE P. 6-104

If any of these inputs are incorrect the appropriate assembly should be tested.
If all the inputs are correct, the A33 Assembly should be tested.

TROUBLESHOOTING CHART A



TROUBLESHOOTING CHART B

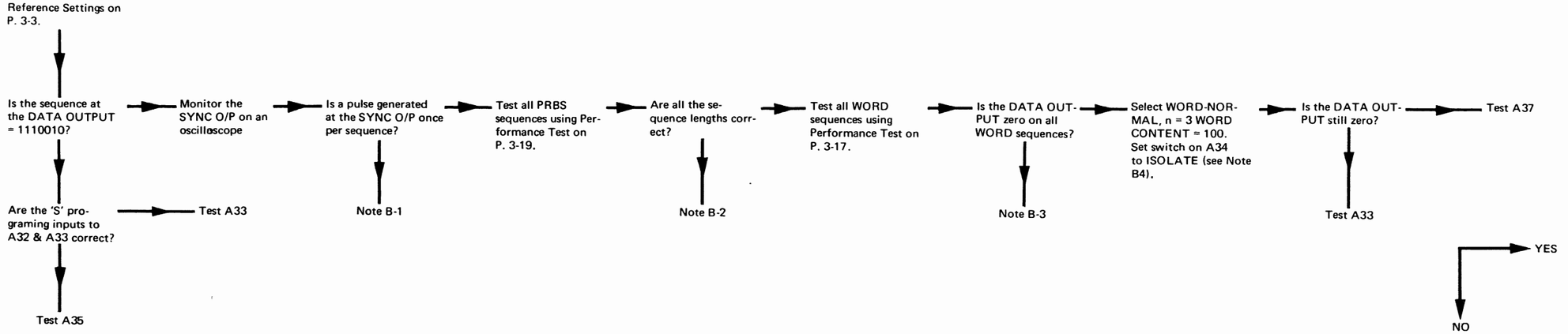


CHART B

NOTES

B-1 Trace the path of the Sync pulse from the SYNC OUTPUT back to A33-3. If there is no sync at A33-3, the Binary Sequence Generator is probably faulty but the 'B' programing inputs from A34 should be checked before testing the A33 Assembly.

B-2 The sequence lengths are measured by counting the number of clock pulses which occur between consecutive Sync pulses. Incorrect counter readings can therefore be due to a fault in the sync detection circuits.

B-3 Check the appropriate programing inputs to the Binary Sequence Generator on all faulty sequences. If these are correct then the Binary Sequence Generator is faulty.

B-4 The fault lies in either the Binary Sequence Generator or the Word Content Programer. In ISOLATE the automatic Word Content programing is stopped making it possible to examine the operation of these two stages independently. NOTE: The Sequence Length or Word switches must not be changed in ISOLATE.

B-5 If both the DATA and SYNC OUTPUT are now correct the fault lies in A34. If the SYNC OUTPUT is still incorrect then the fault probably lies in the Binary Sequence Generator however the 'B' programing inputs should be checked before testing this stage.

B-6 The Binary Sequence Generator is probably faulty but check the 'S' programing inputs before testing this stage.

2

SECTION VI
SERVICE

INTRODUCTION

The *hp* 3760A Data Generator has been designed on a modular basis and this approach has also been adopted in the preparation of this Service Section. The instrument consists of the following modules located in a standard *hp* mainframe.

(i) Front Panel Module A1.

(ii) Clock Module A2.

(iii) Data Module A3.

(iv) Power Supply Module A4.

Each module consists of a metal framework and printed circuit mother board to which the various assemblies are attached. All the information necessary for the repair and maintenance of these modules is presented in a series of Service Sheets. General information, such as overall instrument wiring diagrams etc, are given in the following pages immediately preceding the Service Sheets.

SERVICE SHEETS

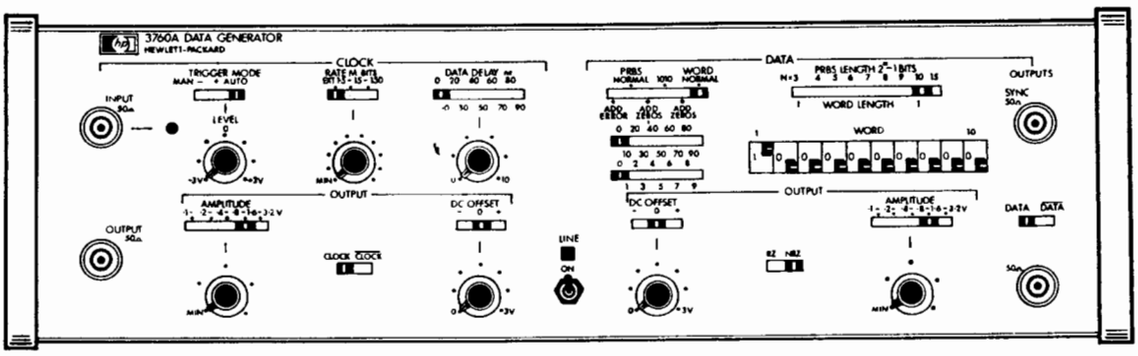
The Service Sheets are in four groups corresponding to the four modules in the instrument. Each group begins with a Module Service Sheet numbered A1, A2, A3 or A4 as appropriate which describes the module as a whole. In addition to mechanical assembly notes and wiring diagrams, these Module Service Sheets also give a replaceable parts list for items not located on the printed circuit assemblies. Following the Module Service Sheet, a series of Assembly Service Sheets describe in detail each assembly in the module. Occasionally, an Assembly Service Sheet is given a double number to indicate that it deals with two assemblies eg, Assembly Service Sheet A32/33 covers assemblies A32 and A33.

REPLACEABLE PARTS LIST

As an aid to servicing, all components located on pc assemblies are listed in their individual Assembly Service Sheets adjacent to the schematic diagram. Components located in the modules but not on a particular pc assembly are listed in the Module Service Sheet, eg, the line transformer is listed in Module Service Sheet A4. Components which cannot be associated solely with one module eg, cables connecting the module to other parts of the instrument are given in the MAIN LIST on Page 6-5. The list of abbreviations and ordering information given with this Main List applies to all Replaceable Parts Lists.

3

Front Panel



Rear Panel

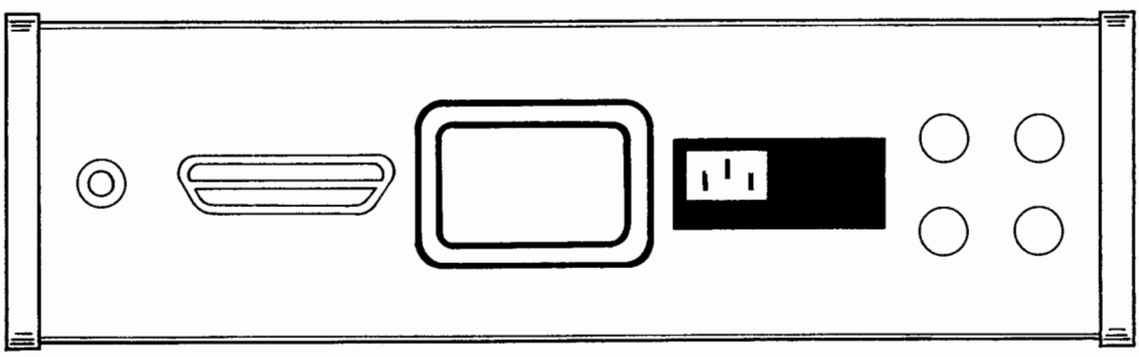


Figure 6-1 3760A Data Generator

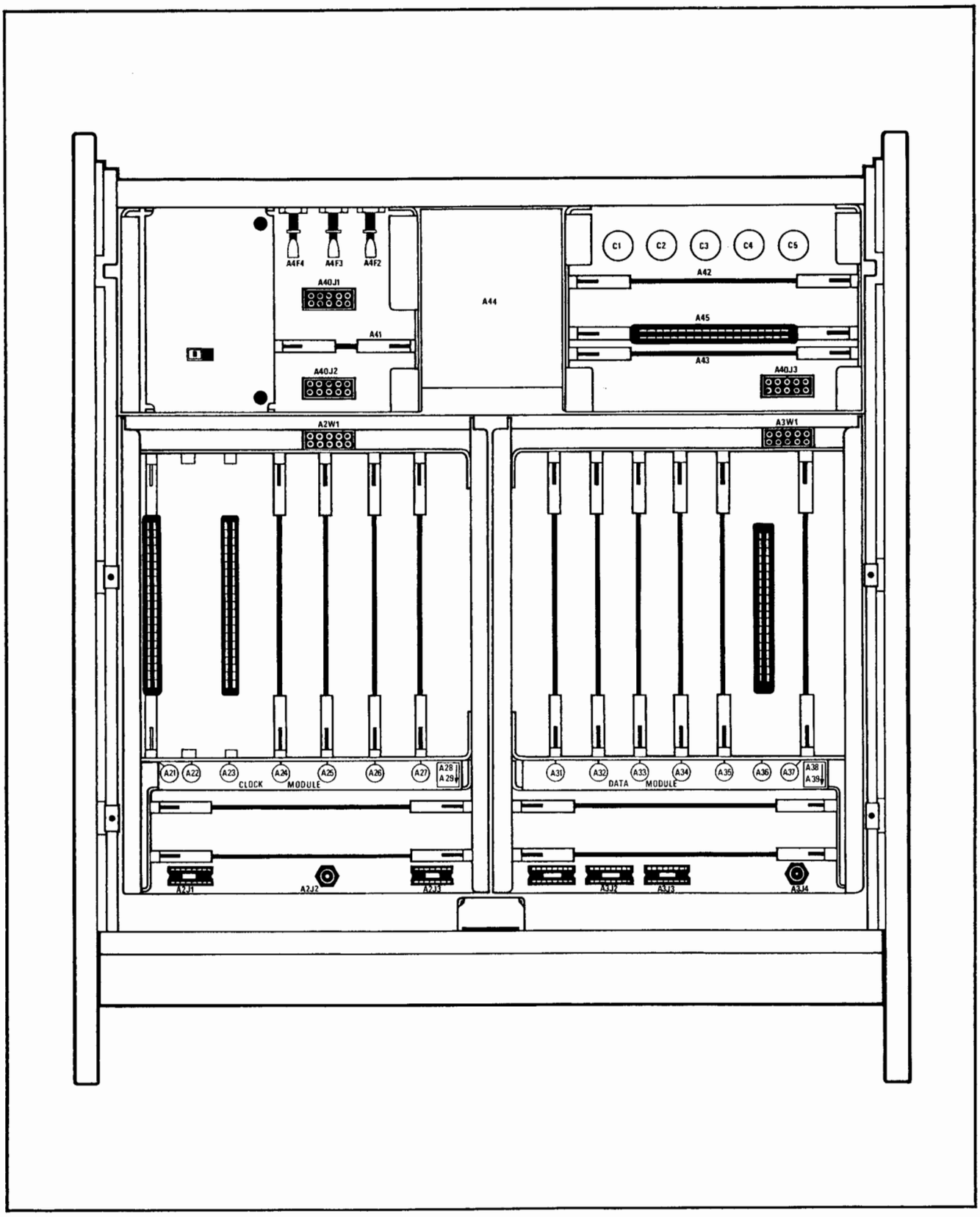
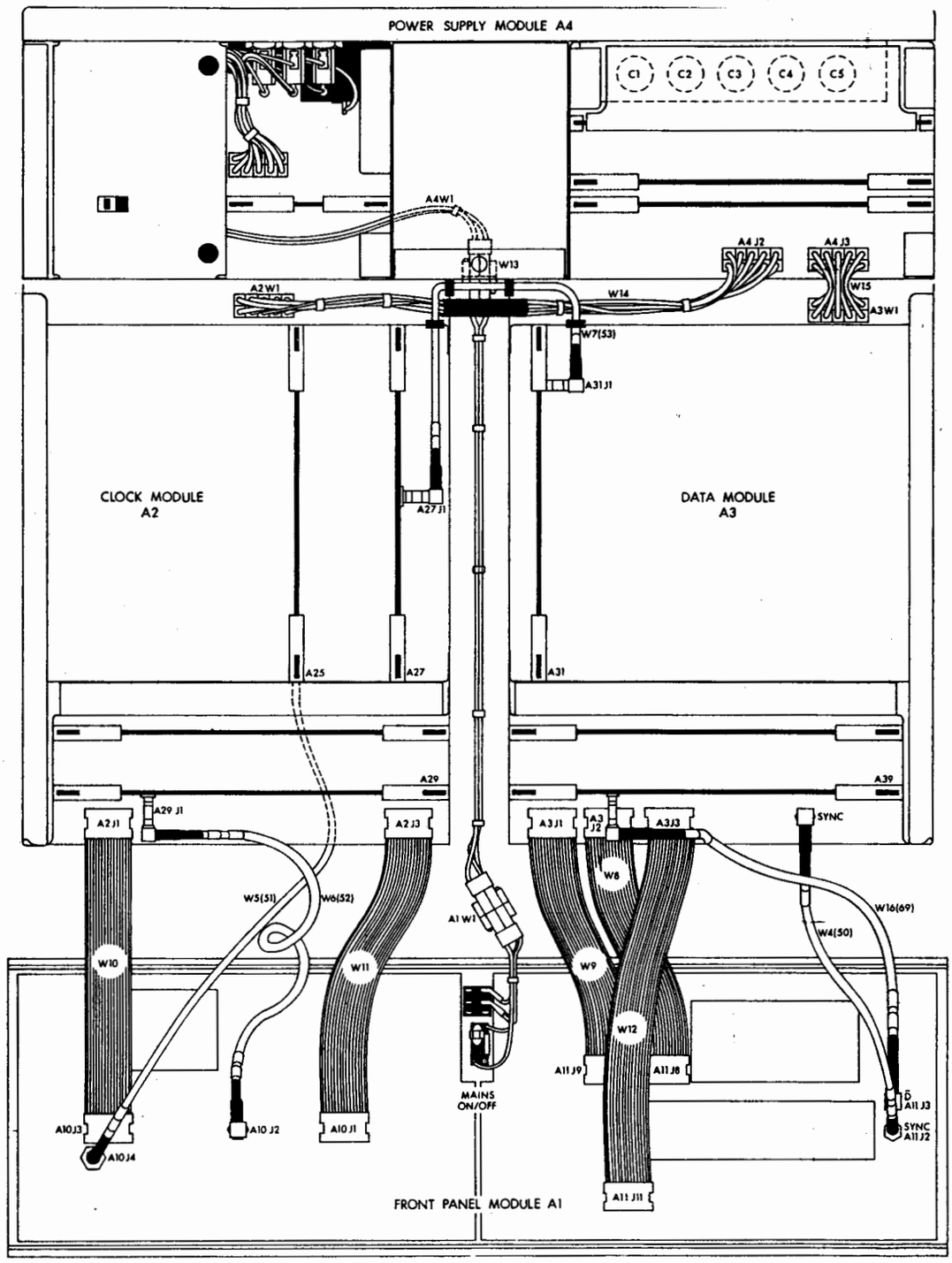


Figure 6-2 Location of Modules

4



NOTE: Stock numbers of cables shown in this diagram are given in the MAIN LIST.

Figure 6-3 3760A Wiring Diagram

REPLACEABLE PARTS – MAIN LIST

All components which cannot be associated exclusively with a particular module, eg interconnecting cables, are given in this list. All other components are listed in the appropriate Service Sheets.

Ordering Information

To order a replacement part, address the order to your local Hewlett-Packard Service Office (see lists at rear of manual for addresses). Specify the following information for each part:

(i) Model and full serial number of instrument.

(ii) Circuit reference.

(iii) Description.

To order a part not listed in the tables, give a complete description of the part including its function and location in the instrument.

List of Abbreviations

A	= amperes	MET FLM	= metal film
AL	= aluminium	MET GLA	= metal glaze
ASSY	= assembly	MET OX	= metallic oxide
CARB	= carbon	MY	= mylar
CER	= ceramic	NSR	= not separately replaceable
COAX	= coaxial		
COMP	= composition	OBD	= order by description
C/S	= countersunk	PC	= printed circuit
DIA	= diameter	P	= pico (10^{-12})
EHT	= extra high tension (high voltage)	PIV	= peak inverse voltage
		POLY	= polystyrene
F	= farads	POLYCARB	= polycarbonate
FLM	= film insulator	QTY	= quantity
FXD	= fixed	RD	= round
GE	= germanium	RT	= right
H	= henries	SI	= silicon
HEX	= hexagonal	S.T.	= selected on test
Hz	= hertz (cycles/second)	TA	= tantalum
		U(μ)	= micro (10^{-6})
K	= kilo (10^{3})	V	= volts
kHz	= kilo hertz (kilo cycles/second)	VAR	= variable
		VDCW	= dc working volts
LIN	= linear	W	= watts
LOG	= logarithmic	WW	= wire wound
M	= milli (10^{-3})	W/	= with
MEG	= mega (10^{6})		
MHz	= mega hertz (mega cycles/second)		

Replaceable Parts

Ref Desig	HP Part No	TQ	Description
	03760-95000	1	3760A SERVICE MANUAL
	03760-95002	1	3760A/61 SYSTEM OPERATING MANUAL
	5060-8740	1	KIT RACK MTG
MP500	03760-30503	1	SIDE FRAME
MP501	5060-0222	1	ASSY HANDLE SIDE
MP502	5060-8737	1	RETAINER HANDLE
MP503	5000-8709	1	PNL SIDE REAR
MP504	5060-8711	1	FRONT SIDE COVER
MP505	5000-0051	1	PLATE FLUTED AL
MP506	5060-8589	1	PNL TOP
MP507	5060-8713	1	PNL BOTTOM
MP508	5060-0767	1	ASSY FOOT
MP509	1490-0030	1	STAND TILT
MP510	03760-70500	1	YOKE ASSY
MP511	03760-10502	1	MODULE SCREEN
MP512	03760-10503	1	SUPPORT CENTRE
MP513	03760-10504	1	SUPPORT LEFT
MP514	03760-10505	1	SUPPORT RIGHT
MP515	03760-10507	1	COVER CENTRE SUPPORT
MP516	03760-30502	1	GUIDE RAIL
MP517	03760-30504	1	SPACER
S13	03760-70073	2	ASSY PC SLIDE SW
W4	03760-70050	1	CABLE ASSY COAX
W5	03760-70051	1	CABLE ASSY COAX
W6	03760-70052	1	CABLE ASSY COAX
W7	03760-70053	1	CABLE ASSY COAX
W8	03760-70054	2	CABLE ASSY 16 PIN
W9	03760-70054		CABLE ASSY 16 PIN
W10	03760-70055	2	CABLE ASSY 16 PIN
W11	03760-70055		CABLE ASSY 16 PIN
W12	03760-70056	1	CABLE ASSY 16 PIN
W13	03760-70057	1	CABLE ASSY AC POWER
W14	03760-70082	1	POWER CABLE
W15	03760-70062	2	CABLE ASSY DC POWER
W16	03760-70062		CABLE ASSY DC POWER

Abbreviations are listed in the introduction to this section

SCHEMATIC DIAGRAM SYMBOLS

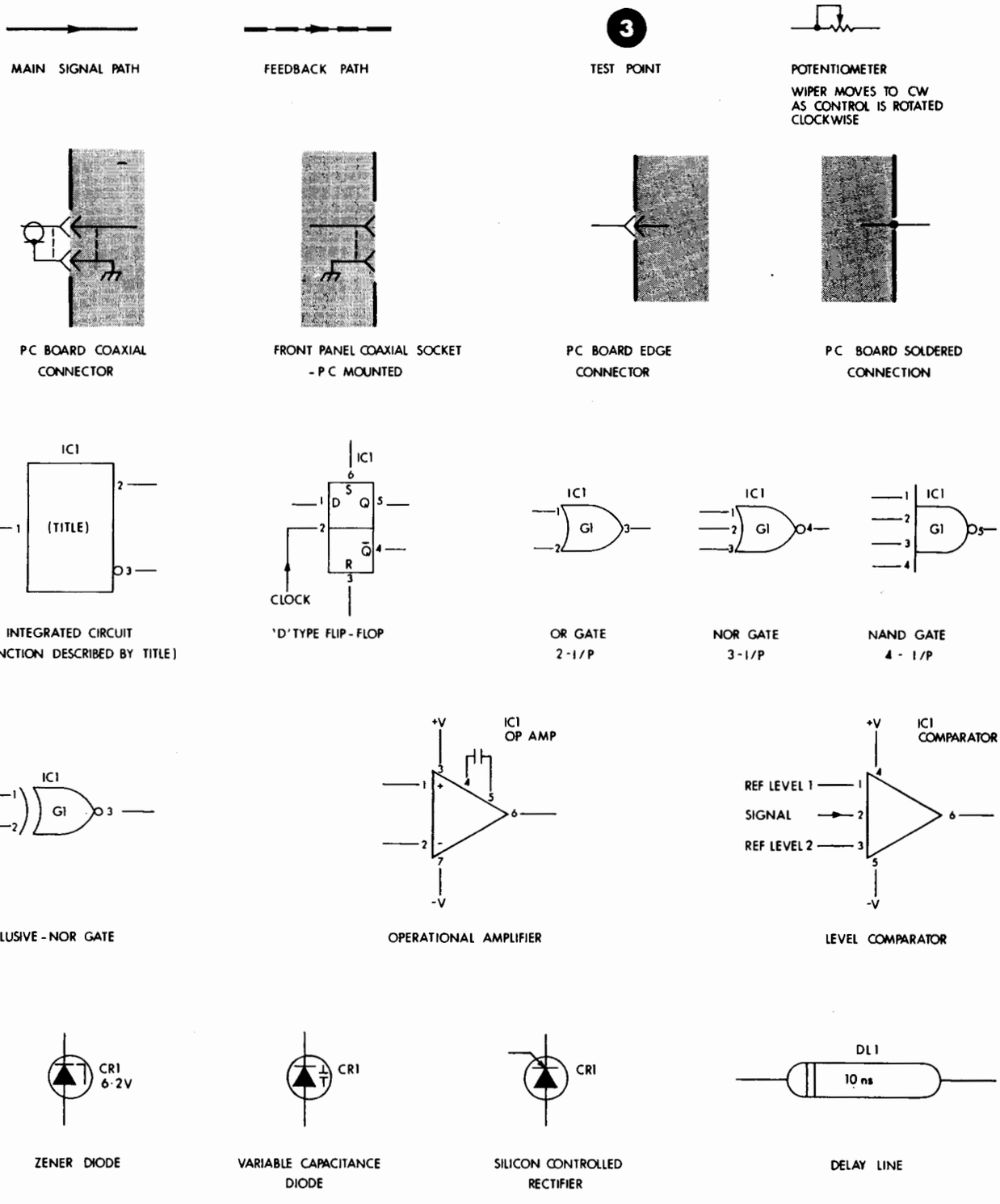


Figure 6-4 Symbols

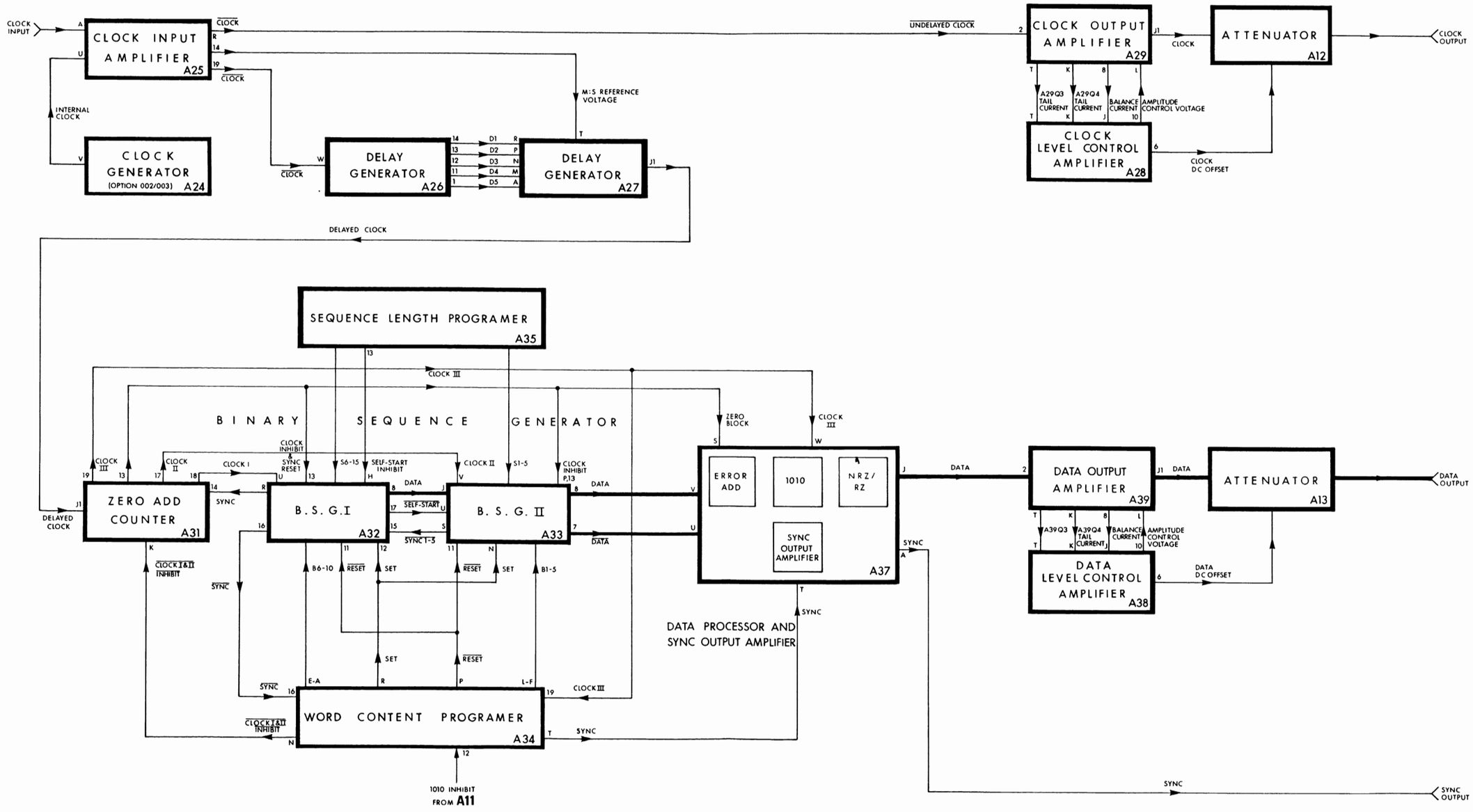
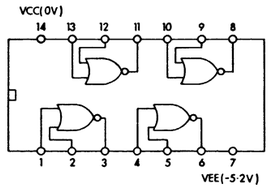


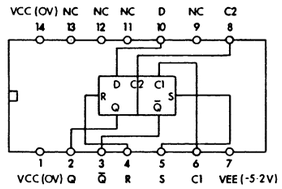
Figure 6-5 Block Diagram

Figure 6-6 I.C. Outlines

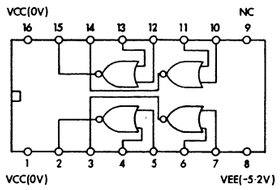
1820-0145
MC 1010 L



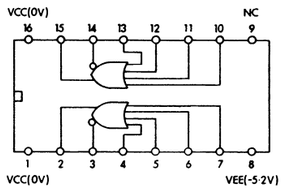
1820-0101
MC 1034 L



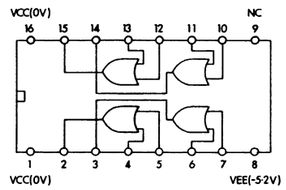
1820-0796
MC 1662 L



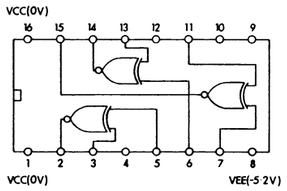
1820-0790
MC 1660 L



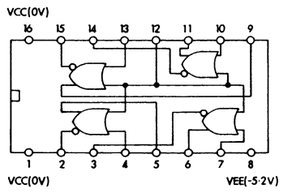
1820-0795
MC 1664 L



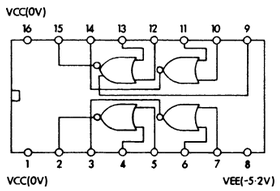
1820-0793
MC 1674 L



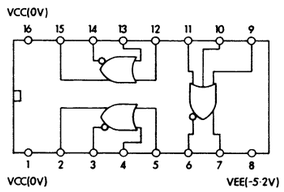
1820-0801
MC 10101L



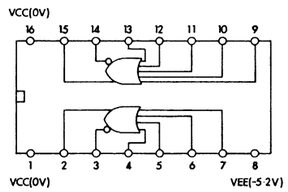
1820-0802
MC 10102 L



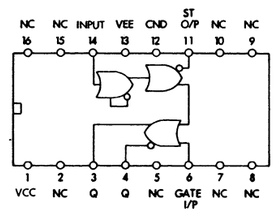
1820-0803
MC 10105 L



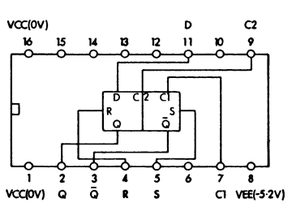
1820-0806
MC 10109 L



1820-0285
hp 849



1820-0794
MC 1670



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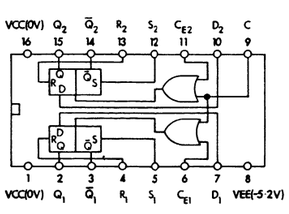
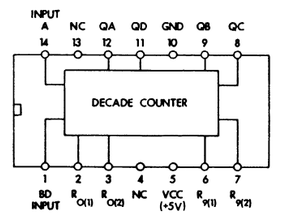
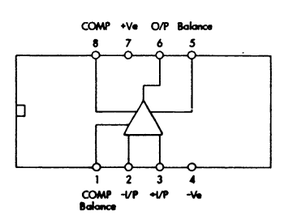
MC 10131 L



1820-0055
SN 7490

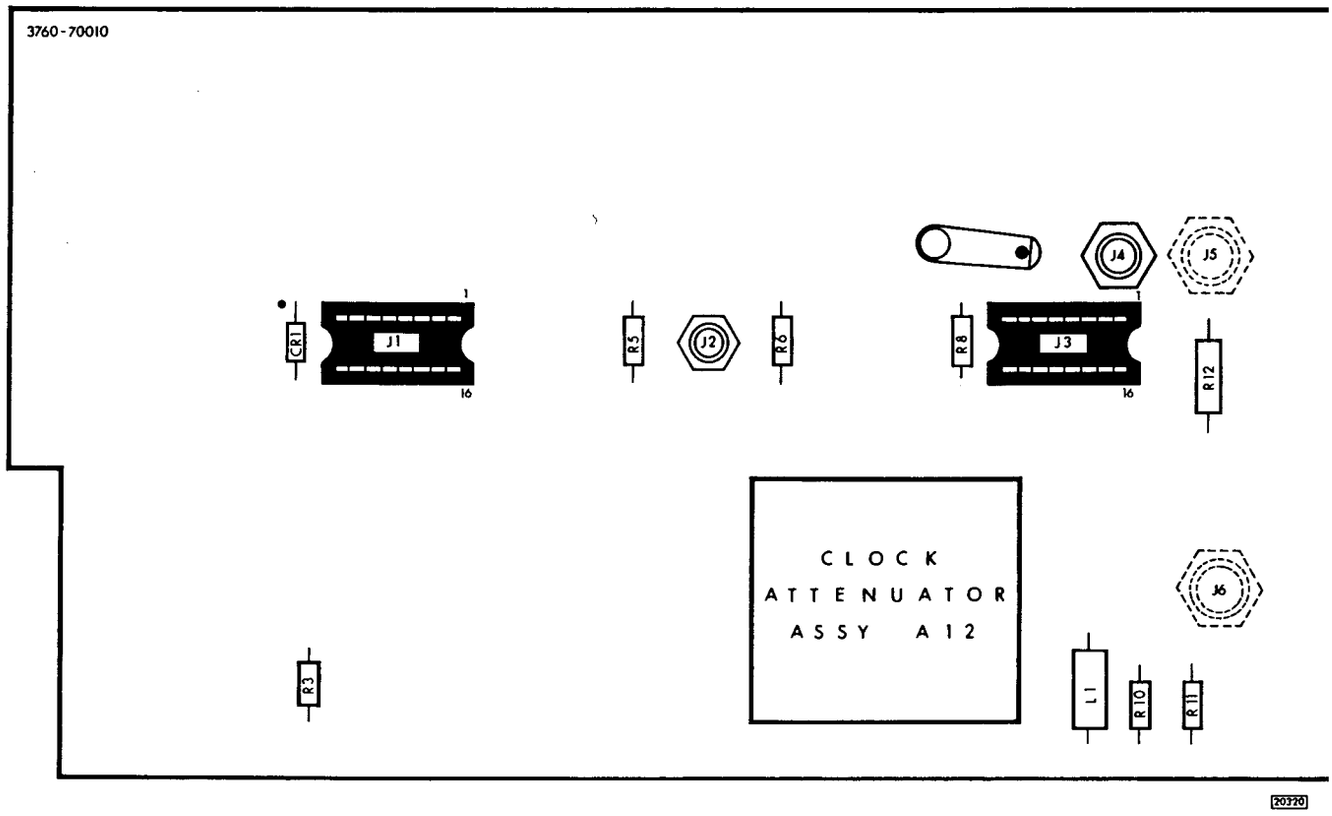


1820-0477
LM 301 A



Functional Block Diagram

A10 CLOCK FRONT PANEL ASSEMBLY



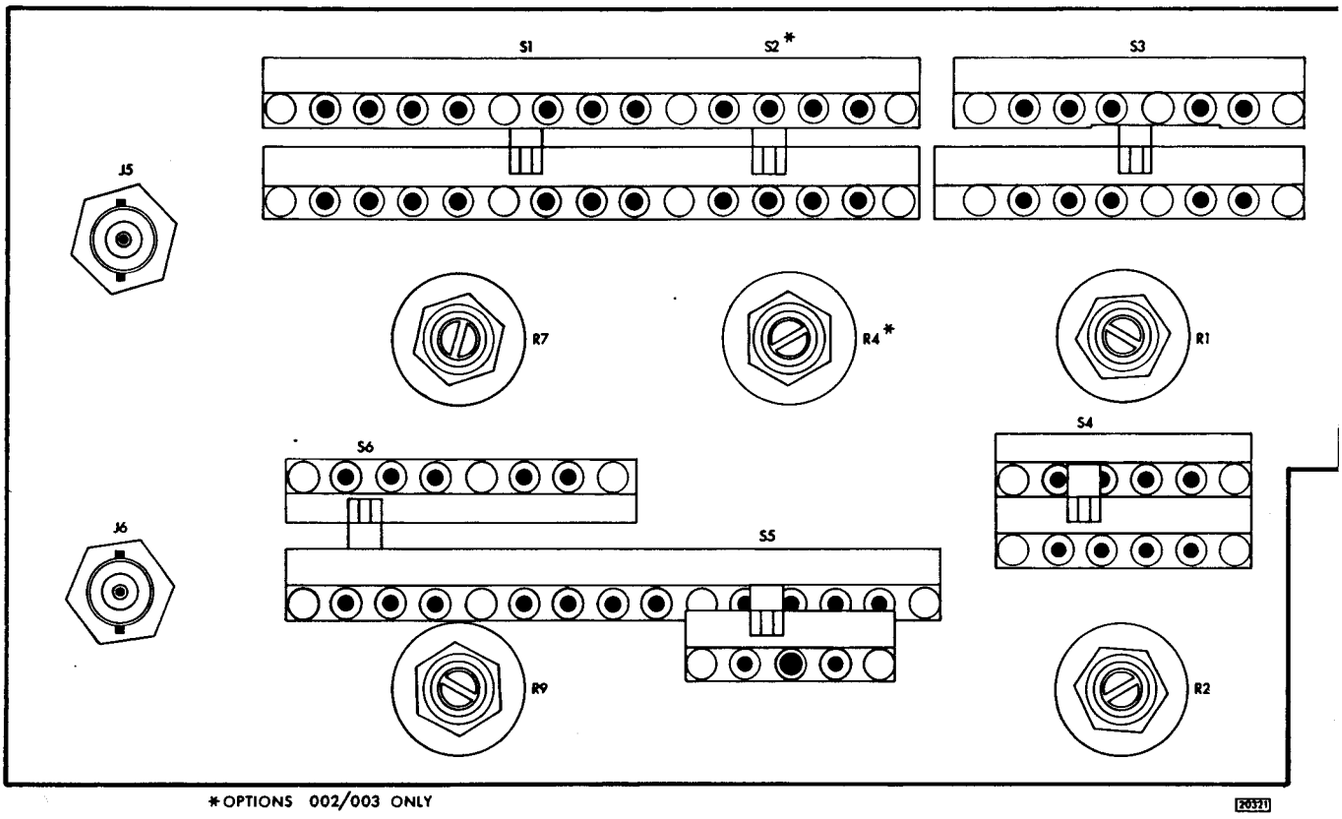


Figure A10-2 Component Location

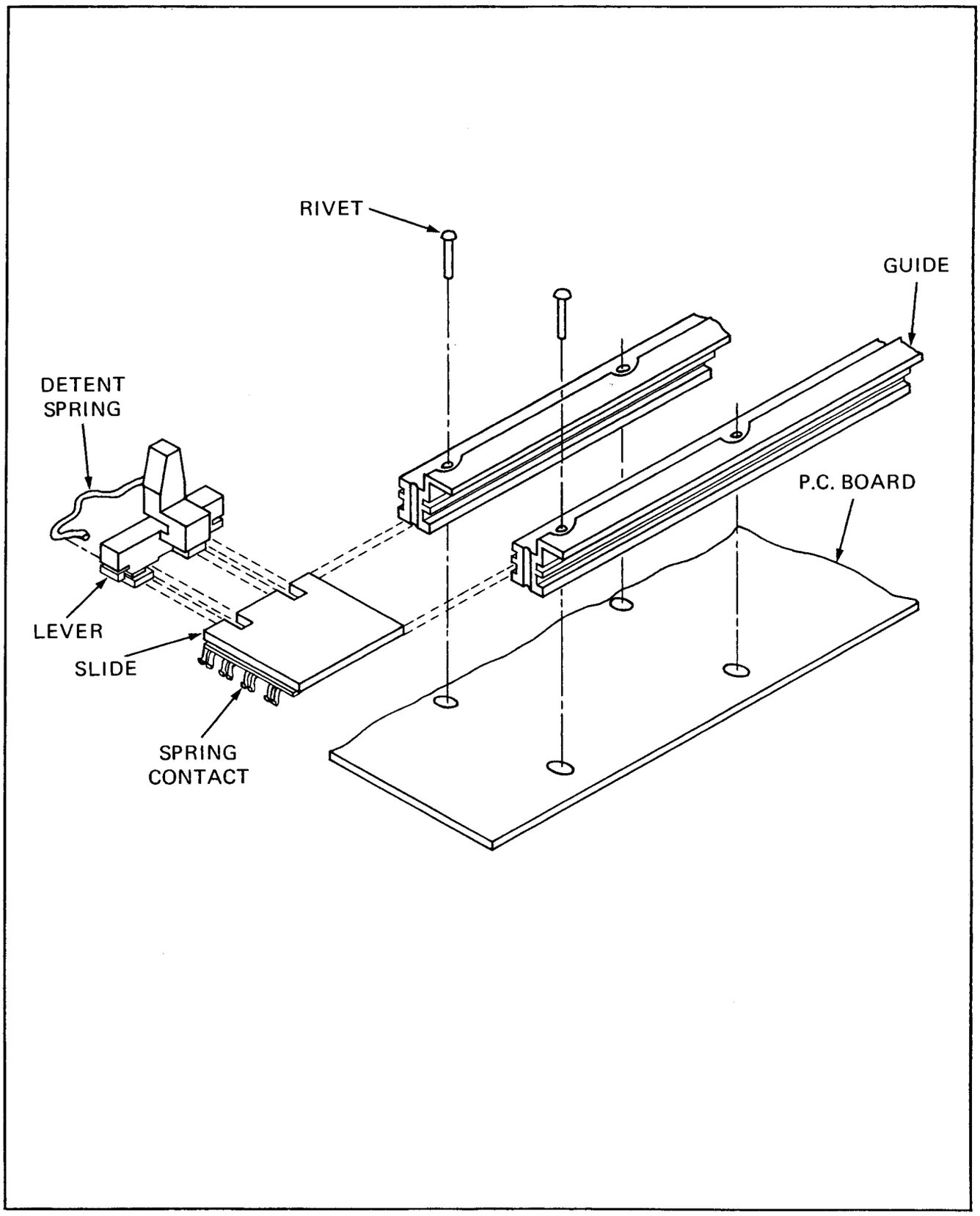


Figure A10-1 Slide Switch

SLIDE SWITCHES

In the schematic diagram, slide switches are drawn as they exist physically. In some cases this may differ from the equivalent electrical circuit shown in the Assembly Service Sheets. Where the equivalent electrical circuit is drawn, it is clearly labelled, EQUIVALENT CIRCUIT to avoid confusion.

A typical slide switch is shown in Figure A10-1 and consists of the following parts:

(i) Lever which protrudes through front panel slot.

(ii) Slide carrying spring contacts.

(iii) Detent Spring(s).

(iv) Two guide rails, screwed or riveted to pc board.

The fixed contacts of the switches are etched on the printed circuit board and if they become damaged, the board must be replaced. The spring contacts may be renewed as follows:

(i) Remove Clock Front Panel Assembly from the A1 module.

(ii) Carefully remove the slider by slipping it off the end of its guide rails. Ensure that the detent spring which fits into the side of the slider is not lost.

(iii) Separate the lever from the slide.

(iv) Fit lever and detent spring to new slider and holding the detent spring compressed slip the slider into the guide rails. Take care not to damage the spring contacts on the underside of the slider.

Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A10	03760-70010		CLOCK FRONT PANEL ASSY
	03760-70610		CLOCK FRONT PANEL ASSY OPTION 001
	03760-70015		CLOCK FRONT PANEL ASSY OPTION 002
	03760-70615		CLOCK FRONT PANEL ASSY OPTION 003
A10CR1	1901-0044	7	DIO SI
A10DS1	2140-0374	13	LAMP INCD 18V 26MA
	03760-10100	13	CONTACT LAMP
A10J1	1200-0767	10	SOCKET INTEG CIRCUIT DUAL INLINE
A10J2	1250-1255	8	CONN COAX PC BD MTG CONHEX 50 OHM
	1250-1379	4	CONN-COAX 75 OHM BNC●
A10J3	1200-0767		SOCKET INTEG CIRCUIT DUAL INLINE
A10J4	1250-0932	5	CONN COAX PC BD MTG CONHEX
A10J5	1250-1378	4	CONN-COAX 50 OHM BNC
	1250-1379		CONN-COAX 75 OHM BNC●
A10J6	1250-1378		CONN-COAX 50 OHM BNC
	1250-1379		CONN-COAX 75 OHM BNC●
A10L1	9100-1645	4	INDUCTOR 390UH 5%
	9100-1653	4	IND FXD 910UH 5%●
A10L2	03760-70209	5	INDUCTOR ASSEMBLY
A10R1	2100-3240	7	R VAR 1K OHM 10% 2W LIN
A10R2	2100-3240		R VAR 1K OHM 10% 2W LIN
A10R3	0757-0402	2	R FXD 110 OHM 1% 1/8W
A10R4	2100-3240		R VAR 1K OHM 10% 2W LIN
A10R5	0698-0083	2	R FXD 1.96K OHM 1% 1/8W
A10R6	0698-0083		R FXD 1.96K OHM 1% 1/8W
A10R7	2100-3240		R VAR 1K OHM 10% 2W LIN
A10R8	0757-0279	7	R FXD 3.16K OHM 1% 1/8W
A10R9	2100-3240		R VAR 1K OHM 10% 2W LIN
A10R10	0698-3154	7	R FXD 4.22K OHM 1% 1/8W
	0757-0439	10	R FXD 6.81K OHM 1% 1/8W●
A10R11	0698-3154		R FXD 4.22K OHM 1% 1/8W
	0757-0439		R FXD 6.81K OHM 1% 1/8W●
A10R12	0757-0715	9	R FXD 150 OHM 1% 1/4W
A10S1	03760-70076	1	ASSY PC SLIDE SW
	5040-0334	13	LEVER SWITCH
	5020-3440	25	SPRING DETENT
A10S2	03760-70074	1	ASSY PC SLIDE SW
	5040-0334		LEVER SWITCH
	5020-3440		SPRING DETENT
A10S3	03760-70075	1	ASSY PC SLIDE SW
	5040-0334		LEVER SWITCH
	5020-3440		SPRING DETENT
A10S4	03760-70071	13	ASSY PC SLIDE SW
	5040-0334		LEVER SWITCH
	5020-3440		SPRING DETENT
A10S5	03760-70071		ASSY PC SLIDE SW
	5040-0334		LEVER SWITCH
	5020-3440		SPRING DETENT
A10S6	03760-70077	2	ASSY PC SLIDE SW
	5040-0334		LEVER SWITCH
	5020-3440		SPRING DETENT
	08330-40002	1	HOLDER SPRING

●OPTIONS 001/003

Abbreviations are listed in the introduction to this section

ASSEMBLY SERVICE SHEET A10

CLOCK FRONT PANEL ASSEMBLY A10

INTRODUCTION

All front panel controls associated with the Clock Module A2 are mounted on the Front Panel Assembly. BNC connectors and potentiometers are also attached to the front panel by locking nuts which must be removed before the assembly can be separated from the A1 module.

OPTIONS

In Option 001, the impedance of the CLOCK INPUT and CLOCK OUTPUT is changed from 50 to 75Ω. The 75Ω version of the A10 Assembly is designated 03760-70610 and differs from the standard assembly (03760-70010) as follows:

(i) J5 and J6 changed to 75Ω connectors.

(ii) The values of R12, L1, R10, R11 are changed.

In Option 002, an internal Clock Generator A24 is provided. This version is designated 03760-70015 and involves the following changes:

(i) Addition of the RATE switch S2 to select clock source.

(ii) Addition of the RATE VERNIER, R4.

(iii) Removal of the wire link shown in the schematic.

Option 003 combines Options 001 and 002 and is designated 03760-70615.

Replaceable Parts

Ref Desig	HP Part No	TQ	Description	Mfr Part No
A1	03760-70010	2	CLOCK FRONT PANEL ASSY	
	03760-70610	2	CLOCK FRONT PANEL ASSY OPTION 001	
	03760-70015	2	CLOCK FRONT PANEL ASSY OPTION 002	
	03760-70615	2	CLOCK FRONT PANEL ASSY OPTION 003	
	03760-70011	2	DATA FRONT PANEL ASSY	
	03760-70611	2	DATA FRONT PANEL ASSY OPTION 001/003	
	03760-70012	2	CLOCK ATTENUATOR ASSY	
	03760-70612	2		
	03760-70013	2	DATA ATTENUATOR ASSY	
	03760-70613	2	DATA ATTENUATOR ASSY OPTION 001/003	
	03760-70014	2	LAMP DRIVER ASSY	
A1DS13	2140-0047	1	LAMP NEON 115VAC/DC	
	5040-0235	1	LAMPHOLDER BASE	
	5040-0234	1	LAMPHOLDER FROSTED LENS	
	0698-3162	1	R FXD 46.4K OHM 1% 1/8W	
A1MP10	03760-30100	1	FRONT PANEL	
	03760-30601	1	FRONT PANEL OPTION 001	
	03760-30602	1	FRONT PANEL OPTION 002	
	03760-30603	1	FRONT PANEL OPTION 003	
A1MP11	7120-1254	1	PLATE TRADEMARK	
A1MP12	0370-1099	6	KNOB POINTER	
A1MP13	0370-1099		KNOB POINTER	
A1MP14	0370-1099		KNOB POINTER	
A1MP15	0370-1099		KNOB POINTER	
A1MP16	0370-1099		KNOB POINTER	
A1MP17	0370-1099		KNOB POINTER	
A1MP18	03760-30115	1	LENS	
A1S1	3101-1732	1	SW TGL DPDT	
A1W16	03760-70061	1	CABLE ASSY AC POWER	

Abbreviations are listed in the introduction to this section

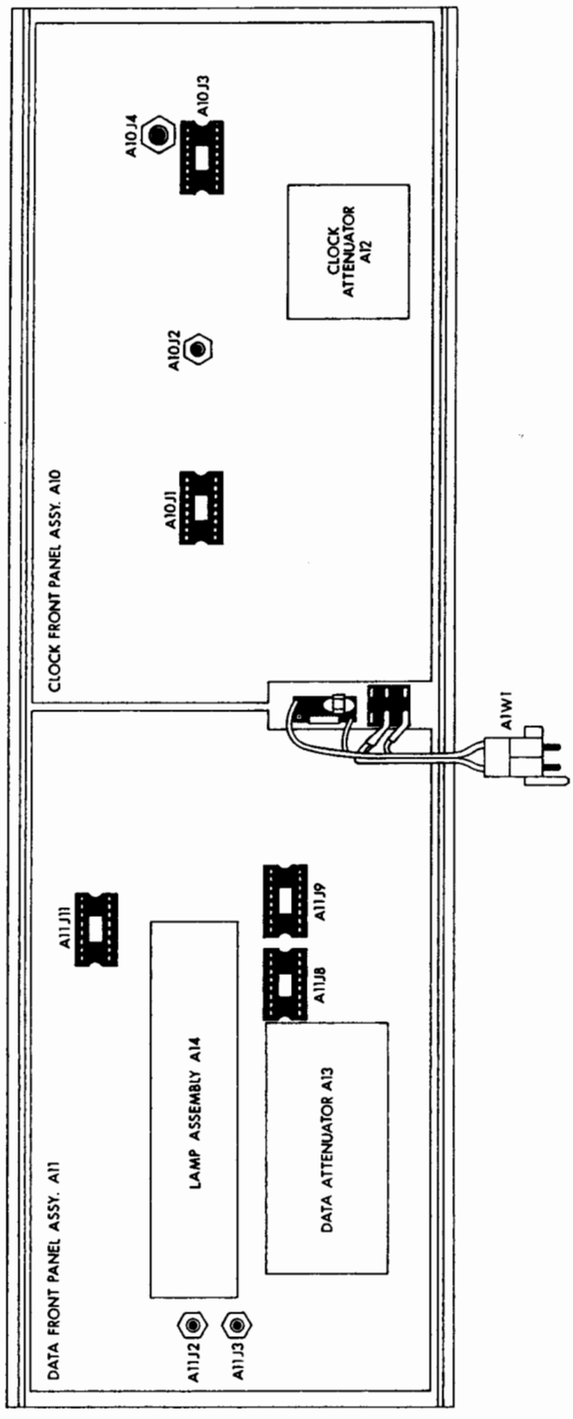


Figure A1-1 Component Location

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MODULE SERVICE SHEET A1

FRONT PANEL MODULE A1

INTRODUCTION

The Front Panel Module consists of the following assemblies:

(i) Clock Front Panel Assembly A10.
(ii) Data Front Panel Assembly A11.
(iii) Clock Attenuator A12.
(iv) Data Attenuator A13.
(v) Lamp Assembly A14.

MECHANICAL CONSTRUCTION

To remove the Front Panel Module from the instrument, proceed as follows:

WARNING

THE MAINS ON/OFF SWITCH IS LOCATED ON THE FRONT PANEL. TO PREVENT ANY POSSIBILITY OF THE USER RECEIVING A SEVERE OR FATAL ELECTRIC SHOCK, THE AC POWER LINE SHOULD BE DISCONNECTED FROM THE INSTRUMENT BEFORE THE FRONT PANEL ASSEMBLY IS REMOVED.

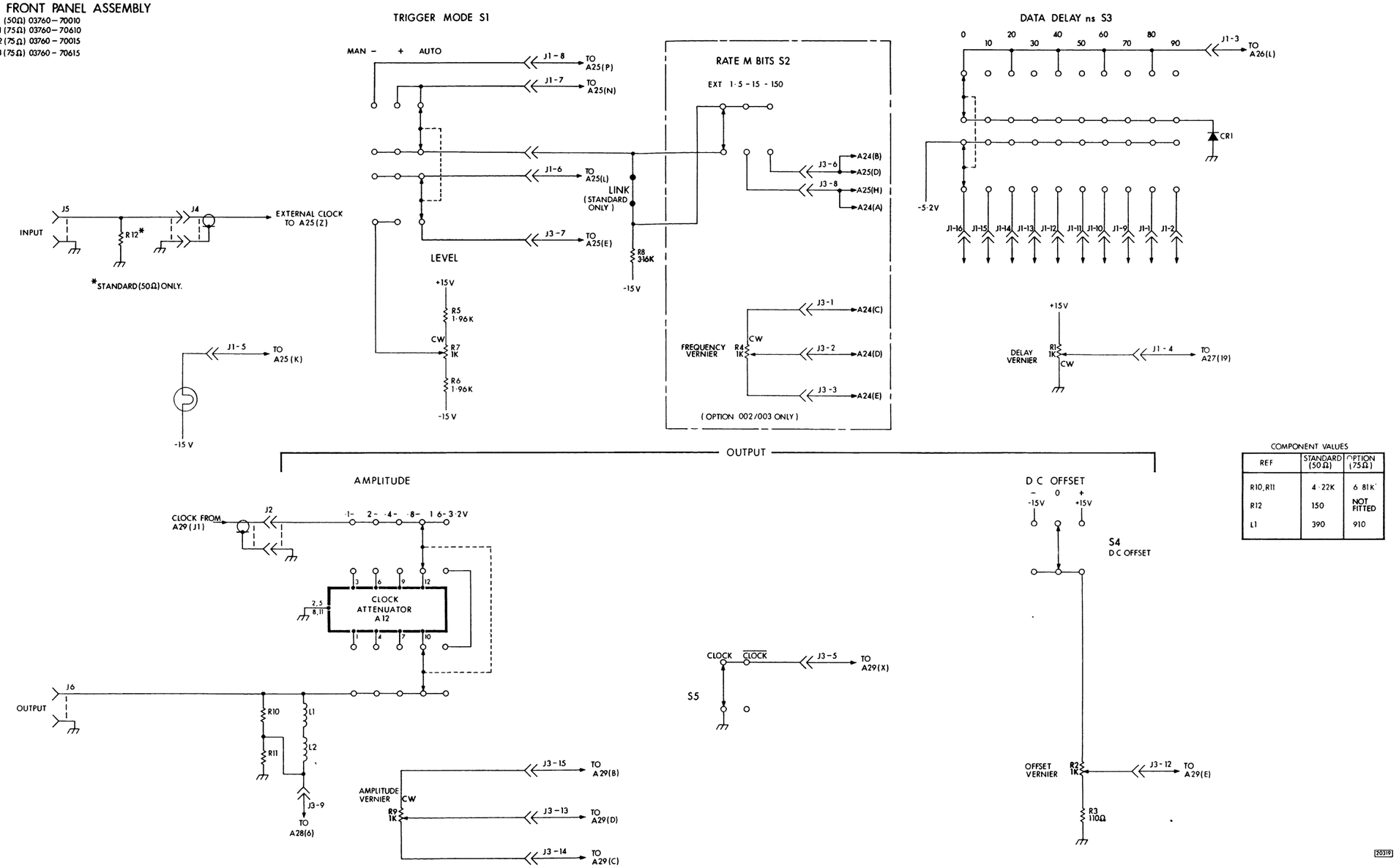
(i) Disconnect the ac power line from the instrument.
(ii) Remove top and bottom covers.
(iii) Remove four screws from front panel flanges (2 top, 2 bottom).
(iv) Pull Front Panel Module free of instrument mainframe.

Sufficient slack has been provided in the cables to allow the Front Panel Module to be serviced while still connected electrically to the instrument, but GREAT CARE should be taken to avoid contact with the back of the mains on/off switch.

Front Panel Module A1

A10 CLOCK FRONT PANEL ASSEMBLY

STANDARD (50Ω) 03760–70010
OPTION 001 (75Ω) 03760–70610
OPTION 002 (75Ω) 03760–70015
OPTION 003 (75Ω) 03760–70615



COMPONENT VALUES

REF	STANDARD (50Ω)	OPTION (75Ω)
R10, R11	4·22K	6·81K
R12	150	NOT FITTED
L1	390	910

20319

Figure A10-3 Schematic Diagram

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Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A11	03760-70011		DATA FRONT PANEL ASSY
	03760-70611		DATA FRONT PANEL ASSY OPTION 001/003
A11CR1	1901-0044		DIO SI
A11J1	1250-1378		CONN-COAX 50 OHM BNC
A11J2	1250-1255		CONN COAX PC BD MTG CONHEX 50 OHM
A11J3	1250-1255		CONN COAX PC BD MTG CONHEX 50 OHM
	1250-0932		CONN COAX PC BD MTG CONHEX●
A11J6	1250-1378		CONN-COAX 50 OHM BNC
	1250-1379		CONN-COAX 75 OHM BNC●
A11J8	1200-0767		SOCKET INTEG CIRCUIT DUAL INLINE
A11J9	1200-0767		SOCKET INTEG CIRCUIT DUAL INLINE
A11J11	1200-0767		SOCKET INTEG CIRCUIT DUAL INLINE
A11L1	9100-1645		INDUCTOR 390UH 5%
	9100-1653		IND FXD 910UH 5%●
A11L3	03760-70209		INDUCTOR ASSEMBLY
A11R1	0698-3154		R FXD 4.22K OHM 1% 1/8W
	0757-0439		R FXD 6.81K OHM 1% 1/8W●
A11R2	0757-0439		R FXD 6.81K OHM 1% 1/8W
	0757-0438	35	R FXD 5.11K OHM 1% 1/8W●
A11R5	2100-3240		R VAR 1K OHM 10% 2W LIN
A11R6	0757-0402		R FXD 110 OHM 1% 1/8W
A11R7	2100-3240		R VAR 1K OHM 10% 2W LIN
A11S1	03760-70071		ASSY PC SLIDE SW
	03760-50102	10	SWITCH INDICATOR
TO	03760-30101	10	SWITCH LEVER
	5020-3440		SPRING DETENT
A11S9	03760-70071		ASSY PC SLIDE SW
	03760-50102		SWITCH INDICATOR
	03760-30101		SWITCH LEVER
	5020-3440		SPRING DETENT
A11S10	03760-70071		ASSY PC SLIDE SW
	03760-50102		SWITCH INDICATOR
	03760-30101		SWITCH LEVER
	5020-3440		SPRING DETENT
A11S11	03760-70078	1	ASSY PC SLIDE SW
	5040-0334		LEVER SWITCH
	5020-3440		SPRING DETENT
A11S12	03760-70077		ASSY PC SLIDE SW
	5040-0334		LEVER SWITCH
	5020-3440		SPRING DETENT
	5040-0334		LEVER SWITCH
	5020-3440		SPRING DETENT
	5020-3440		SPRING DETENT
A11S14	03760-70073		ASSY PC SLIDE SW
	5040-0334		LEVER SWITCH
	5020-3440		SPRING DETENT
	5020-3440		SPRING DETENT
A11S15	03760-70071		ASSY PC SLIDE SW
	5040-0334		LEVER SWITCH
	5020-3440		SPRING DETENT
A11S16	03760-70072	1	ASSY PC SLIDE SW
	5040-0334		LEVER SWITCH
	5020-3440		SPRING DETENT
A11S17	03760-70079	1	ASSY PC SLIDE SW
	5040-0334		LEVER SWITCH
	5020-3440		SPRING DETENT

●OPTIONS 001/003

Abbreviations are listed in the introduction to this section

ASSEMBLY SERVICE SHEET A11

DATA FRONT PANEL ASSEMBLY A11

INTRODUCTION

All front panel controls associated with the Data Module A3 are mounted on the Data Front Panel Assembly. Potentiometers and BNC connectors are also attached to the front panel by locking nuts which must be removed before the assembly can be separated from the A1 module.

OPTIONS

In Option 001 the impedance of the DATA is changed from 50 to 75Ω. The 75Ω version of the A11 Assembly is designated 03760-70611 and differs from the standard assembly (03760-70011) as follows.

(i) J3 and J6 changed to 75Ω connectors.

(ii) The values of L2, R3 and R4 are changed.

NOTE: The impedance of the SYNC OUTPUT is unchanged at 50Ω.

SLIDE SWITCHES

In the schematic diagram, slide switches are drawn as they exist physically. In some cases this may differ from the equivalent electrical circuit shown in the Assembly Service Sheets. Where the equivalent circuit is drawn, it is clearly labelled, EQUIVALENT CIRCUIT, to avoid confusion.

A description and dismantling procedure for these pc switches is given in Assembly Service Sheet A10. Note that before the WORD CONTENT switch slides can be removed, the SEQUENCE LENGTH guide rails must be unscrewed from the pc board.

A11 DATA FRONT PANEL ASSEMBLY
STANDARD (50Ω) 03760 – 70011
OPTION 001 (75Ω) 03760 – 70611
OPTION 003 (75Ω) 03760 – 70611

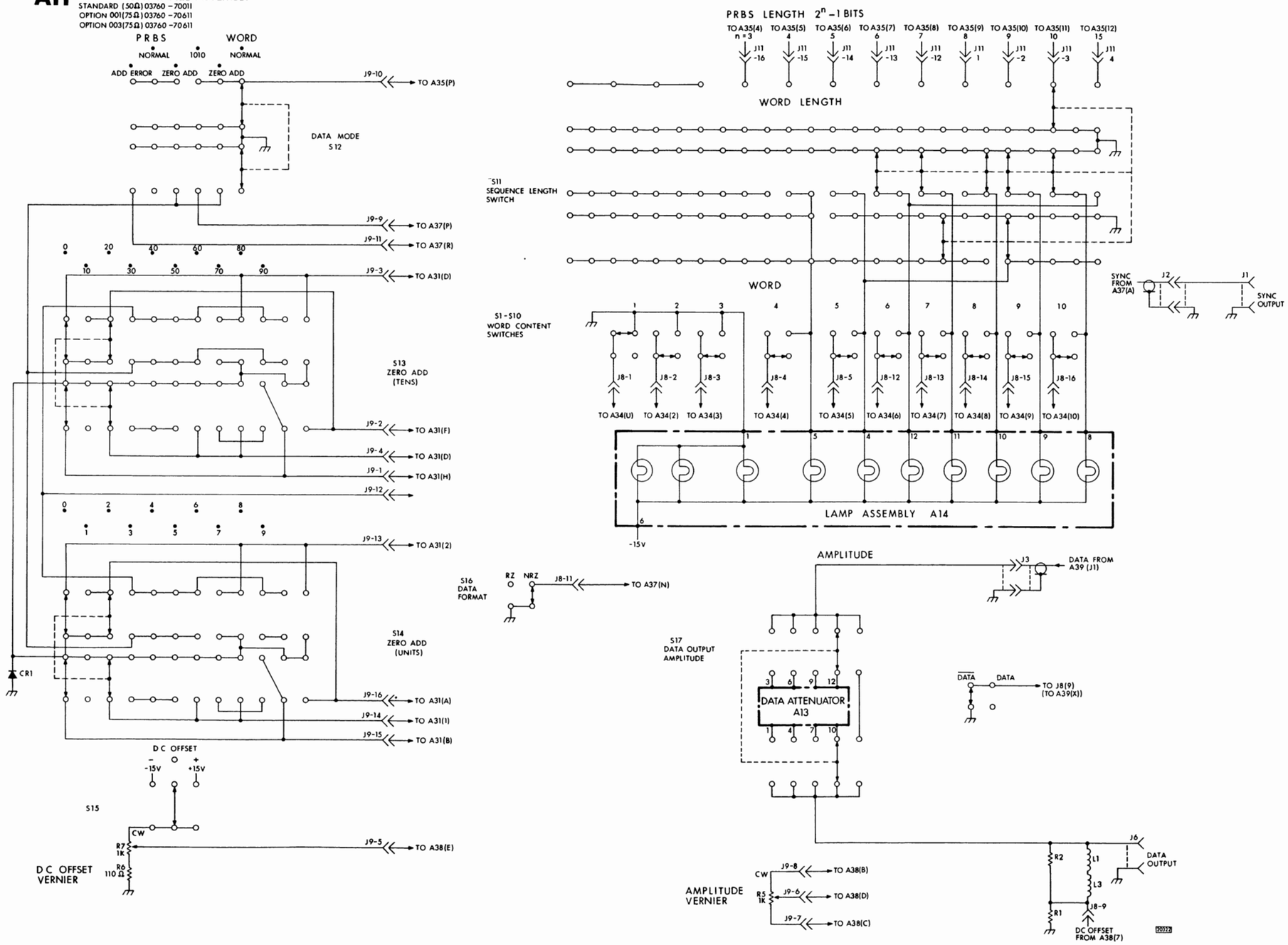
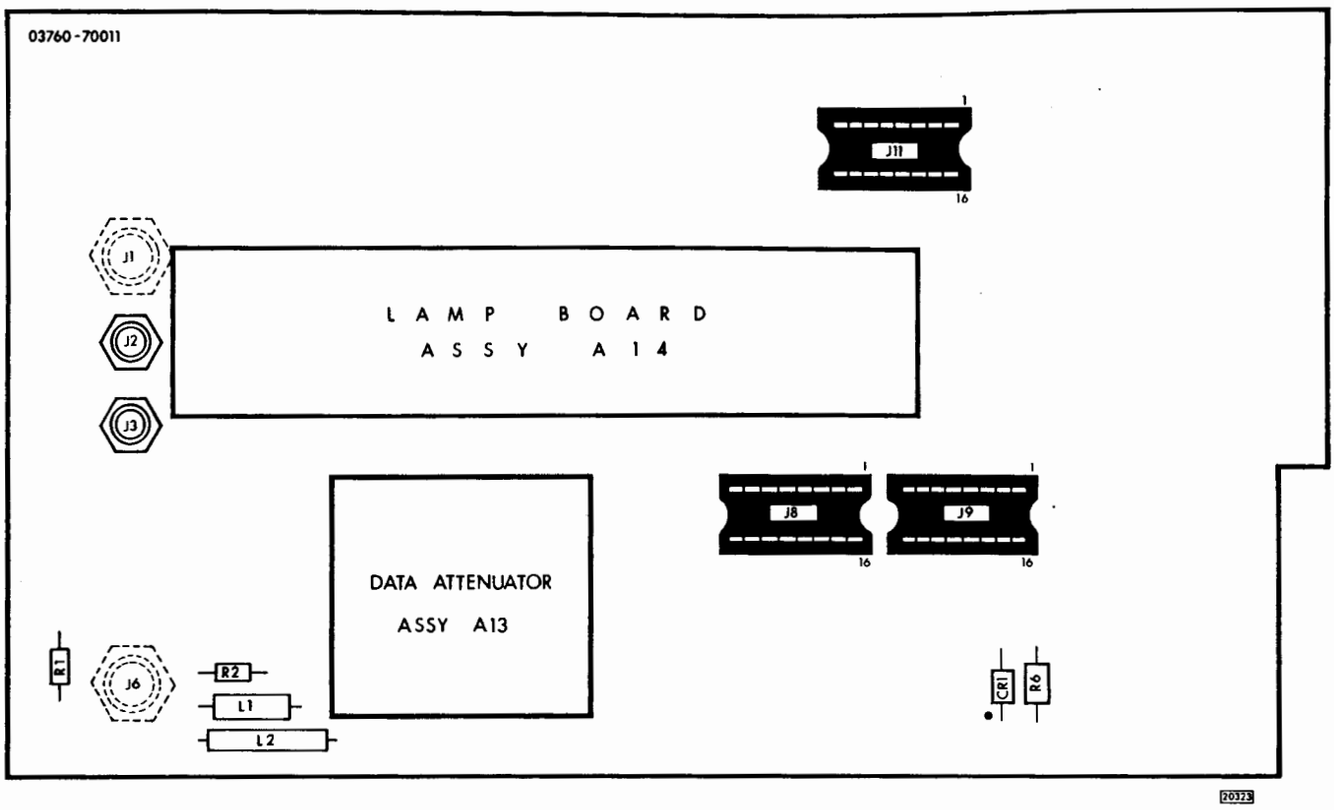


Figure A11-2 Schematic Diagram

A11 DATA FRONT PANEL ASSEMBLY



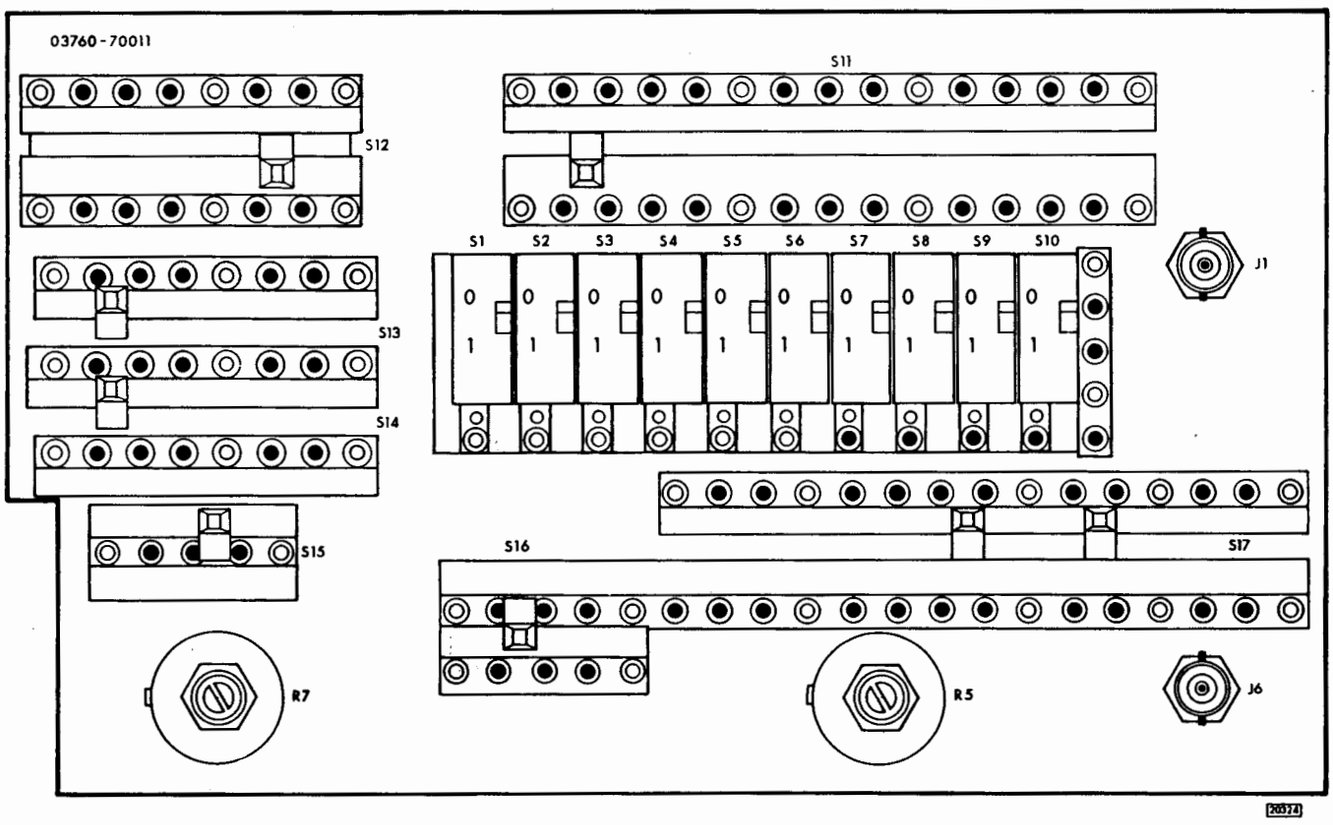


Figure A11-1 Component Location

Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A24	03760-70624		CLOCK GENERATOR ASSY OPTION 002/003
A24C1	0180-0197	10	C FXD 2.2UF 10% 20WVDC
A24C1	0180-0155	5	C FXD 2.2UF 20% 20WVDC
A24C2	0150-0093	89	C FXD 0.01UF +80-10% 100WVDC
A24C3	0180-0155		C FXD 2.2UF 20% 20WVDC
A24C3	0180-0197		C FXD 2.2UF 10% 20WVDC
A24C4	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A24C5	0160-2199	19	C FXD 30PF 5% 300WVDC
A24C6	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A24C7	0180-0197		C FXD 2.2UF 10% 20WVDC
A24C7	0180-0155		C FXD 2.2UF 20% 20WVDC
A24C8	0180-0155		C FXD 2.2UF 20% 20WVDC
A24C8	0180-0197		C FXD 2.2UF 10% 20WVDC
A24C9	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A24C10	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A24C11	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A24C12	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A24C13	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A24C14	0160-2199		C FXD 30PF 5% 300WVDC
A24C15	0160-2199		C FXD 30PF 5% 300WVDC
A24C16	0160-2199		C FXD 30PF 5% 300WVDC
A24C17	0160-2199		C FXD 30PF 5% 300WVDC
A24C18	0160-2199		C FXD 30PF 5% 300WVDC
A24C19	0160-2199		C FXD 30PF 5% 300WVDC
A24C20	0160-2199		C FXD 30PF 5% 300WVDC
A24C21	0160-3138	1	C FXD 18PF 5% 30WVDC
A24C22	0160-2141	1	C FXD 680PF 20% 1000WVDC
A24C23	0150-0050	15	C FXD 1000PF +80-20% 1000WVDC
A24C24	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A24C25	0180-0155		C FXD 2.2UF 20% 20WVDC
A24C25	0180-0197		C FXD 2.2UF 10% 20WVDC
A24C26	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A24C27	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A24CR1	1902-3182	3	DIO BKDN 12.1V 5% 400MW
A24CR2	1902-3182		DIO BKDN 12.1V 5% 400MW
A24CR3	1902-3048	3	DIO BKDN 3.48V 5% 400MW
A24CR4	1902-3048		DIO BKDN 3.48V 5% 400MW
A24CR5	1902-3104	1	DIO BKDN 5.62V 5% 400MW
A24CR6	1901-0040	56	DIO SI
A24CR7	1901-0040		DIO SI
A24CR8	1901-0040		DIO SI
A24CR9	1901-0040		DIO SI
A24CR10	1901-0040		DIO SI
A24CR11	1901-0040		DIO SI
A24CR12	1901-0040		DIO SI
A24CR13	1901-0040		DIO SI
A24IC1	1820-0477	20	IC OPER AMPL
A24IC2	1820-0477		IC OPER AMPL
A24IC3	1820-0477		IC OPER AMPL
A24IC4	1820-0477		IC OPER AMPL
A24IC5	1820-0477		IC OPER AMPL
A24IC6	1820-0477		IC OPER AMPL
A24IC7	5080-3011	1	IC PULSE GENERATOR

Abbreviations are listed in the introduction to this section

CHARGE/DISCHARGE CURRENT CONTROL

IC2 and IC3 are two independent voltage sources driven by the front panel RATE vernier. On the lower frequency range, Q6 is forward biased by the RATE switch to apply a large positive voltage to the +input of IC2. The output of this amplifier therefore saturates at approximately +10V and reverse biases CR9 thus isolating IC2 from IC1. Since Q6 is conducting, Q7 is turned off and the input from the RATE vernier is applied to the +input of IC3 via R7. The upper and lower frequency limits are set by R17 and R19 respectively.

On the high frequency range the voltage/frequency characteristic of the Pulse Generator is slightly non-linear. To compensate for this, the gain characteristic of IC2 is made non-linear by including CR7, CR8 and their associated bias networks in the feedback path of IC2. At minimum output frequency, the input from the RATE vernier is approximately -8V and due to negative feedback via R16, the -input of IC2 is also held at -8V. CR7 and CR8 are therefore reverse biased and the gain of IC2 is equal to:

$$\text{Gain} = \frac{R16 + R14}{R14}$$

As the vernier is rotated clockwise, the input voltage becomes more positive until at approximately -5.7V CR8 becomes forward biased and effectively places R12 and R13 in parallel with R16. This increases the gain of IC2 since the effective value of R14 has been reduced. As the vernier is rotated further, CR7 becomes forward biased (at approximately -5.2V) and reduces the effective value of R14 again. As the diodes do not turn on sharply, the gain characteristic of IC2 is a smooth curve of the correct shape to produce a linear relationship between input voltage and output frequency.

The voltages required at the various points in the circuit to produce the charge and discharge currents are shown in the schematic. These voltages are only approximate as they depend on the characteristics of the Pulse Generator.

To generate an output with a mark to space ratio of 1:1, the charge and discharge times must be equal (see Figure A24-1). The drive to the positive current sources is therefore made variable (by R21) to allow the mark to space of the output to be accurately set to 1:1.

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ASSEMBLY SERVICE SHEET A24

CLOCK GENERATOR A24

INTRODUCTION

This assembly is fitted as part of Options 002 and 003 and provides an internally generated clock signal in the range 1.5 to 150MHz. Also fitted to the basic instrument are the RATE switch, A10S2 which selects the clock source (EXT, 1.5 – 15 or 15 – 150M), and the RATE vernier, A10R4.

PULSE GENERATOR

The signal source consists of a pulse generator IC7 and timing capacitors C21 and C22. These capacitors are charged and discharged by a constant current and the resulting linear voltage ramp generated across them switches the output of IC7 as shown in Figure A24-1. Since the slope of the ramp is proportional to the value of the timing capacitance and charge/discharge currents, a variation in either of these will produce a change in the frequency of the output. On the 15 to 150MHz range, Q13 is reverse biased by the RATE switch and hence the timing capacitance consists of C21 only.On the 1.5 to 15MHz range, Q13 is forward biased to increase the value of the timing capacitance by 680pF. On both ranges, fine frequency control is achieved by varying the value of the charge/discharge currents applied to the timing capacitors.

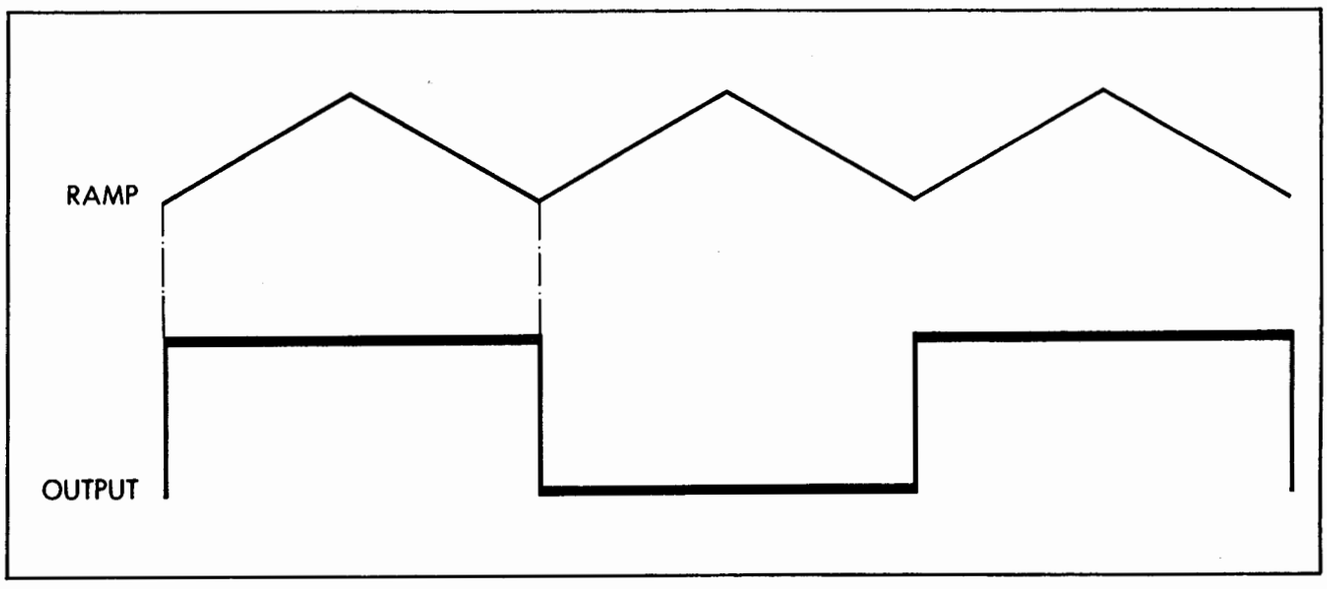

Figure A24-1 Ramp Generation

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ASSEMBLY SERVICE SHEET A20

CLOCK
MOTHERBOARD A20

GENERAL

The Clock Motherboard A20 forms the base of the Clock Module and carries the plug-in assemblies A24, A25, A26, A27, A28 and A29.

Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A20	03760-70020		CLOCK MODULE MOTHER BOARD ASSY
A20C1	0180-0098	4	C FXD 100UF 20% 20WVDC
A20C2	0180-1714	4	C FXD 330UF 10% 6WVDC
A20C3	0180-1714		C FXD 330UF 10% 6WVDC
A20C4	0180-0098		C FXD 100UF 20% 20WVDC
A20J1	1200-0767		SOCKET INTEG CIRCUIT DUAL INLINE
A20J2	1250-0932		CONN COAX PC BD MTG CONHEX
A20J3	1200-0767		SOCKET INTEG CIRCUIT DUAL INLINE
A20MP1	0403-0200	6	FOOT PLASTIC
A20MP2	0403-0200		FOOT PLASTIC
A20MP3	0403-0200		FOOT PLASTIC
A20MP4	0403-0200		FOOT PLASTIC
A20MP5	0403-0200		FOOT PLASTIC
A20W1	03760-70063		CABLE ASSY DC POWER
A20XA1	1251-1365	19	CONN-PC 44 RIB CONT
A20XA3	1251-1365		CONN-PC 44 RIB CONT
A20XA4	1251-1365		CONN-PC 44 RIB CONT
A20XA5	1251-1365		CONN-PC 44 RIB CONT
A20XA6	1251-1365		CONN-PC 44 RIB CONT
A20XA7	1251-1365		CONN-PC 44 RIB CONT
A20XA8	1251-1365		CONN-PC 44 RIB CONT
A20XA9	1251-1365		CONN-PC 44 RIB CONT

Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A2	03760-70020	2	CLOCK MODULE MOTHER BOARD ASSY
	03760-70021	1	EXTENDER BOARD
	03760-70025	2	CLOCK INPUT AMPLIFIER ASSY
	03760-70026	2	DELAY GENERATOR ASSY 1
	03760-70027	2	DELAY GENERATOR ASSY 2
	03760-70028	2	CLOCK LEVEL CONTROL AMP ASSY
	03760-70628	2	CLOCK LEVEL CON AMP ASSY OPT 001/003
	03760-70029	2	CLOCK OUTPUT AMP ASSY
	03760-70629	2	CLOCK OUTPUT AMP ASSY OPTION 001/003
	03760-70624	2	CLOCK GENERATOR ASSY OPTION 002/003
A2MP20	03760-70200	1	CLOCK MODULE CHASSIS
A2MP21	03760-10206	1	CLAMP CONNECTOR
A2MP22	03760-10207	1	SPACER
A2W1	03760-70063	3	CABLE ASSY DC POWER

Abbreviations are listed in the introduction to this section

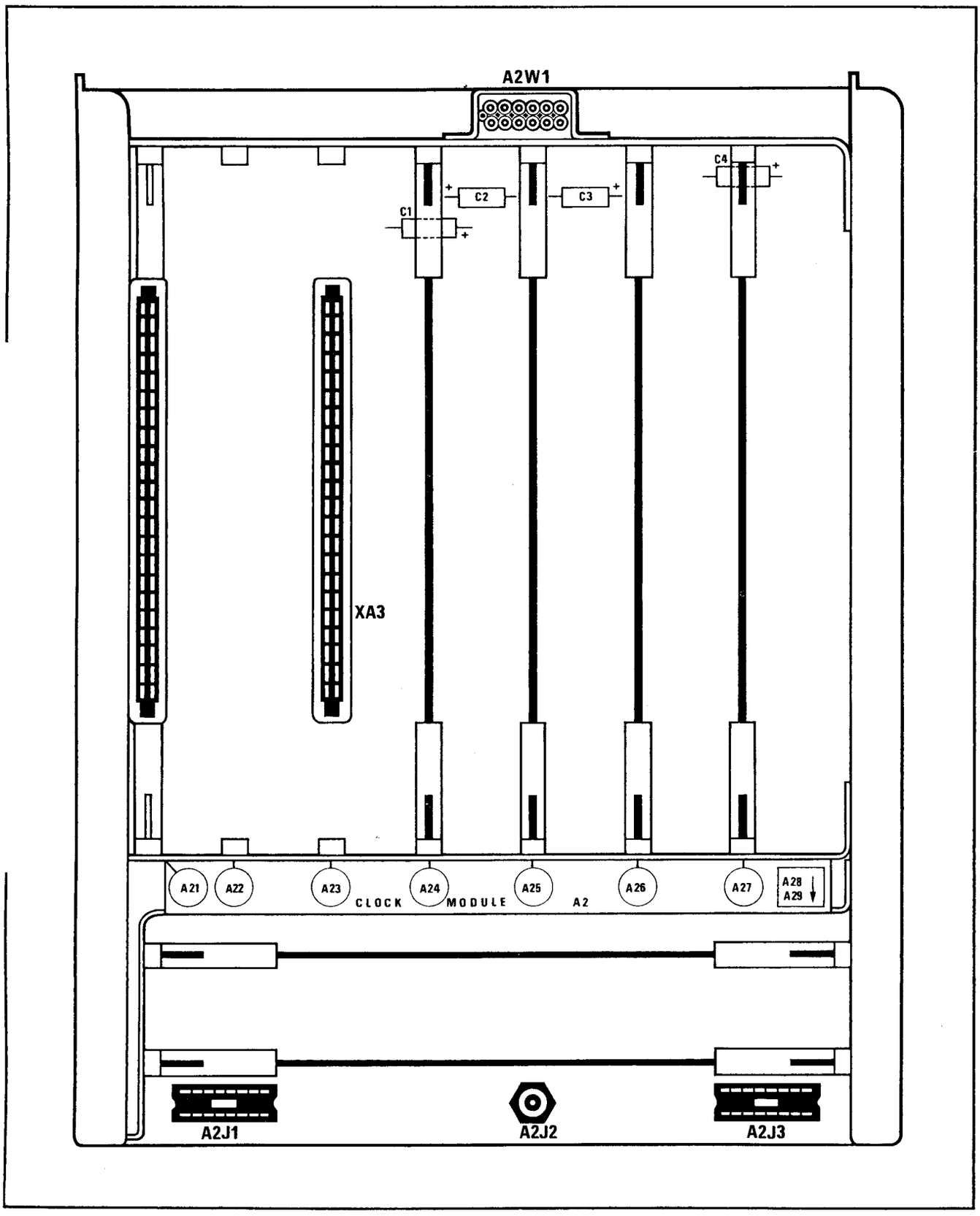

Figure A2-1 Component Location

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MODULE SERVICE SHEET A2

CLOCK MODULE A2

INTRODUCTION

The Clock Module consists of the following assemblies:

(i) Clock Generator A24 (Option 002/003 only).
(ii) Clock Input Amplifier A25.
(iii) Delay Generator I, A26.
(iv) Delay Generator II, A27.
(v) Clock Level Control Amplifier A28.
(vi) Clock Output Amplifier A29.

Note: Assembly A24 is fitted as part of Options 002 and 003 only.

MECHANICAL CONSTRUCTION

To remove the Clock Module A2 from the instrument proceed as follows:

(i) Remove top and bottom covers.
(ii) Remove module screen by turning the quick release catches.
(iii) Remove the two screws holding the Clock Mother Board A20 to the mainframe (underside).
(iv) Remove all cables and lift the module out of the instrument.

The Clock Motherboard is separated from the module by removing the six screws attaching it to the metalwork.

KED

Clock Module A2

ASSEMBLY SERVICE SHEET A14

LAMP ASSEMBLY 14

GENERAL

The lamp assembly A14 is soldered to the Data Front Panel Assembly A11 and consists of eleven sub miniature lamps and a printed circuit board. Ten of these lamps are used to give a visual indication of the settings of the WORD CONTENT switches, the eleventh is a spare. For example, with the sequence length switch set to n = 5, the first five lamps are switched on. They shine through perspex slides attached to each WORD CONTENT switch to display 0 when the switch is up or 1 when it is down.

Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A14	03760-70014		LAMP DRIVER ASSY
A14DS1	2140-0374		LAMP INCD 18V 26MA
	03760-10100		CONTACT LAMP
A14DS12	2140-0374		LAMP INCD 18V 26MA
	03760-10100		CONTACT LAMP

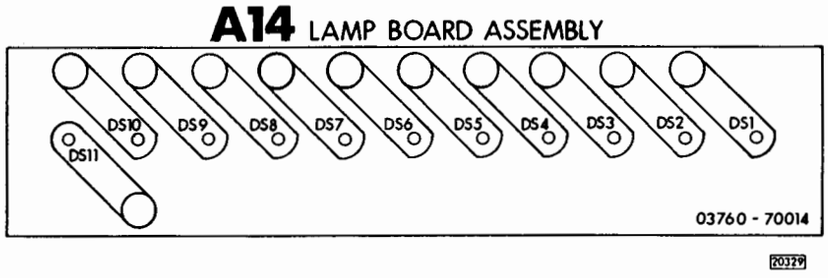

Figure A14-1 Component Location

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Replaceable Parts (continued)

Ref Desig	HP Part No	TQ	Description
A24IC8	1820-0477		IC OPER AMPL
A24IC9	1820-0796	21	IC QUAD 2-INPUT NOR GATE ECL
A24L1	03760-70208	1	INDUCTOR ASSY
A24Q2	1854-0039	11	XSTR SI NPN
A24Q2	1854-0039		XSTR SI NPN
A24Q3	1853-0036	7	XSTR SI PNP
A24Q4	1853-0036		XSTR SI PNP
A24Q5	1853-0001	1	XSTR SI PNP
A24Q6	1853-0036		XSTR SI PNP
A24Q7	1853-0036		XSTR SI PNP
A24Q8	1854-0307	1	XSTR SI NPN
A24Q9	1853-0036		XSTR SI PNP
A24Q10	1853-0036		XSTR SI PNP
A24Q11	1854-0215	2	XSTR SI NPN
A24Q12	1854-0215		XSTR SI NPN
A24Q13	1853-0036		XSTR SI PNP
A24Q15	1854-0071	10	XSTR SI NPN
A24R1	0757-0418	3	R FXD 619 OHM 1% 1/8W
A24R2	0757-0418		R FXD 619 OHM 1% 1/8W
A24R3	0698-5490	5	R FXD 2K OHM 1% 1/8W
A24R4	0757-0427	4	R FXD 1.5K OHM 1% 1/8W
A24R5	0693-4701	1	R FXD 47 10% 2W
A24R6	0757-0442	11	R FXD 10K OHM 1% 1/8W
A24R7	0757-0442		R FXD 10K OHM 1% 1/8W
A24R8	0757-0175	1	R FXD 10 OHM 1% 1/8W
A24R9	0757-0439		R FXD 6.81K OHM 1% 1/8W
A24R10	0698-0085	3	R FXD 2.61K OHM 1% 1/8W
A24R11	0757-0290	2	R FXD 6.19K OHM 1% 1/8W
A24R12	0757-0442		R FXD 10K OHM 1% 1/8W
A24R13	0698-0085		R FXD 2.61K OHM 1% 1/8W
A24R14	0698-3159	1	R FXD 26.1K OHM 1% 1/8W
A24R15	0757-0439		R FXD 6.81K OHM 1% 1/8W
A24R16	2100-2522	2	R VAR 10K OHM 10% 1/2W LIN
A24R17	2100-2522		R VAR 10K OHM 10% 1/2W LIN
A24R18	2100-2413	3	R VAR 200 OHM 10% 1/2W
A24R19	2100-2413		R VAR 200 OHM 10% 1/2W
A24R20	0698-5490		R FXD 2K OHM 1% 1/8W
A24R21	2100-2489	3	R VAR 5K OHM 10% 1/2W
A24R22	0698-3152	2	R FXD 3.48K OHM 1% 1/8W
A24R23	0757-0279		R FXD 3.16K OHM 1% 1/8W
A24R24	0757-0438		R FXD 5.11K OHM 1% 1/8W
A24R25	0698-3432	3	R FXD 26.1 OHM 1% 1/8W
A24R26	0698-3446	8	R FXD 383 OHM 1% 1/8W
A24R27	0698-3442	4	R FXD 237 OHM 1% 1/8W
A24R28	0698-3442		R FXD 237 OHM 1% 1/8W
A24R29	0698-3446		R FXD 383 OHM 1% 1/8W
A24R30	0757-0280	22	R FXD 1K OHM 1% 1/8W
A24R31	0757-0179	1	R FXD 196 OHM 1% 1/4W
A24R32	0757-0394	128	R FXD 51.1 OHM 1% 1/8W
A24R33	0698-3446		R FXD 383 OHM 1% 1/8W
A24R34	0757-0394		R FXD 51.1 OHM 1% 1/8W
A24R35	0698-4233	1	R FXD 120 OHM 5% 1/8W
A24R36	0698-3132	61	R FXD 261 OHM 1% 1/8W
A24R37	0757-0394		R FXD 51.1 OHM 1% 1/8W

Abbreviations are listed in the introduction to this section

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Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A13	03760-70013		DATA ATTENUATOR ASSY
	03760-70613		DATA ATTENUATOR ASSY OPTION 001/003
A13R1	0698-4377		R FXD 37.4 OHM 1% 1/8W
	0757-0395		R FXD 56.2 OHM 1% 1/8W●
A13R2	0757-0715		R FXD 150 OHM 1% 1/4W
	0698-7443		R FXD 226 OHM 0.5% 1/4W●
A13R3	0757-0284		R FXD 150 OHM 1% 1/8W
	0698-7443		R FXD 226 OHM 0.5% 1/4W●
A13R4	0698-8237		R FXD 93.8 OHM 1% 1/8W
	0698-4411		R FXD 140 OHM 1% 1/8W●
A13R5	0698-8243		R FXD 83.3 OHM 1% 1/4W
	0698-4408		R FXD 124 OHM 1% 1/8W●
A13R6	0698-8236		R FXD 83.3 OHM 1% 1/8W
	0698-4408		R FXD 124 OHM 1% 1/8W●
A13R7	0698-3440		R FXD 196 OHM 1% 1/8W
	0698-4448		R FXD 294 OHM 1% 1/8W●
A13R8	0698-8244		R FXD 64.3 OHM 1% 1/4W
	0698-8241		R FXD 96.4 OHM 1% 1/8W●
A13R9	0698-8238		R FXD 64.3 OHM 1% 1/8W
	0698-8241		R FXD 96.4 OHM 1% 1/8W●
A13R10	0698-8240		R FXD 398 OHM 1% 1/8W
	0757-1100		R FXD 600 OHM 1% 1/8W●
A13R11	0698-8245		R FXD 57.7 OHM 1% 1/4W
	0698-8242		R FXD 85 OHM 1% 1/8W●
A13R12	0698-8245		R FXD 57.7 OHM 1% 1/4W
	0698-8242		R FXD 85 OHM 1% 1/8W●

●OPTIONS 001/003

Abbreviations are listed in the introduction to this section

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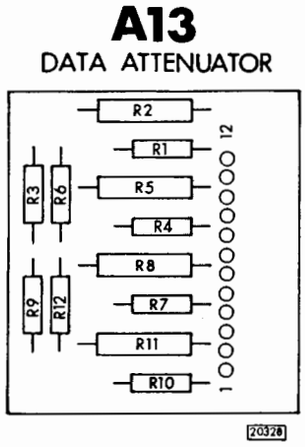

Figure A13-1 Component Location

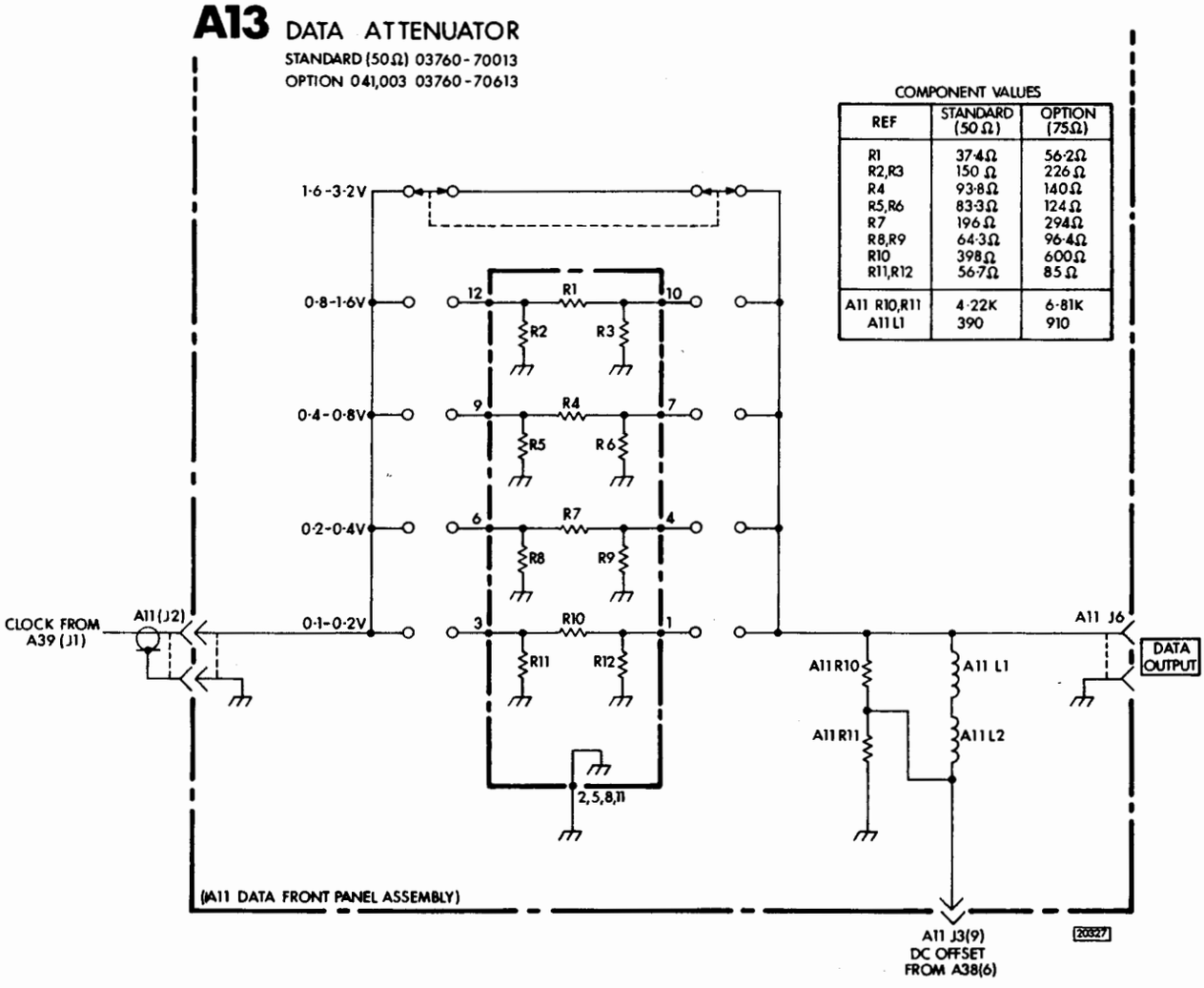

Figure A13-2 Schematic Diagram

ASSEMBLY SERVICE SHEET A13

DATA ATTENUATOR A13

GENERAL

The DATA Attenuator is mounted by solder pins to the DATA Front Panel Assembly A11. Range switching is accomplished by a pc slide switch located on the A11 assembly. Five values of attenuation are available, 0.6, 12, 18 and 24dB and since the output of the DATA Amplifier, A39 is variable between 1.6 and 3.2V pk-pk, the output amplitude ranges available are:

1.6 – 3.2V pk-pk
0.8 – 1.6V pk-pk
0.4 – 0.8V pk-pk
0.2 – 0.4V pk-pk
0.1 – 0.2V pk-pk

OPTIONS

In Options 001 and 003, the impedance of the DATA OUTPUT is changed from the standard 50Ω to 75Ω. The 75Ω version of the Attenuator is designated 03760-70613 and uses different resistor values in each of the π networks (the attenuation is still in 6dB steps).

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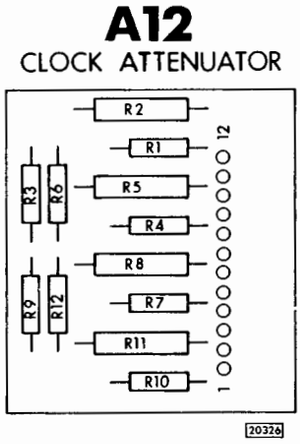

Figure A12-1 Component Location

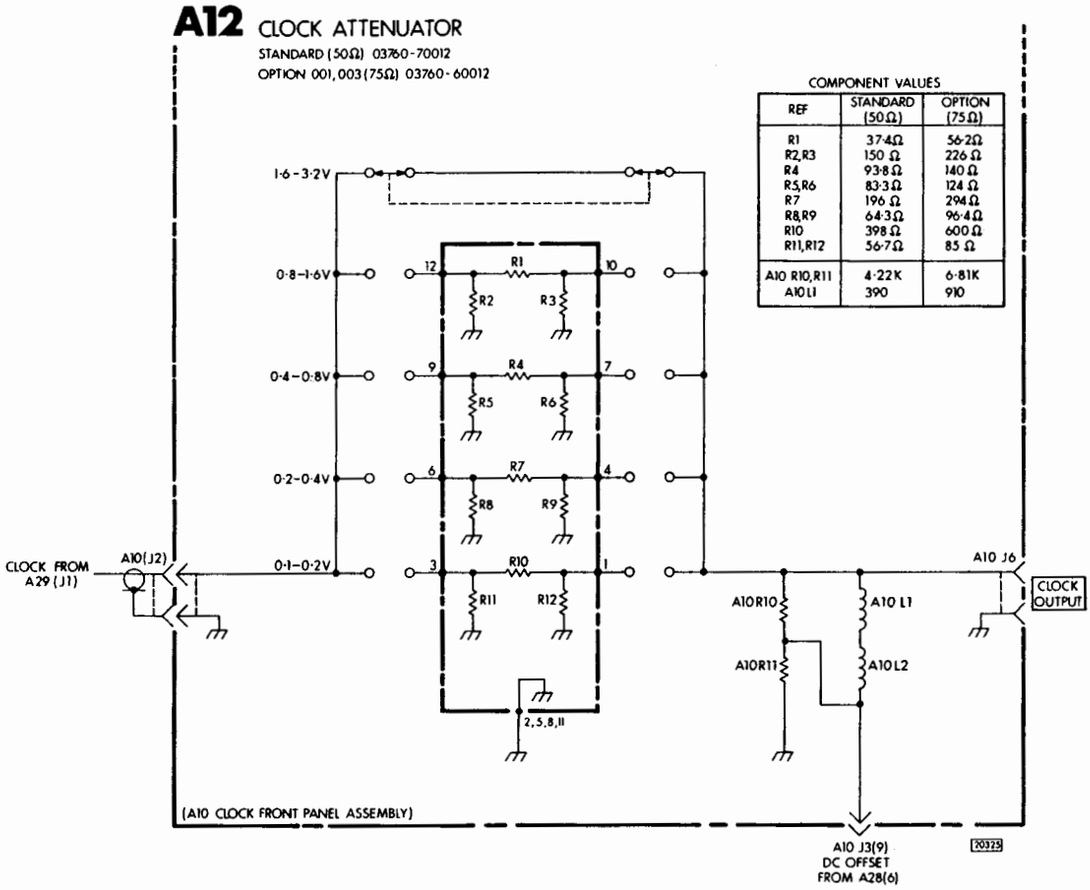

Figure A12-2 Schematic Diagram

Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A12	03760-70012		CLOCK ATTENUATOR ASSY
	03760-70612		CLOCK ATTENUATOR ASSY OPTIONS 001/003
A12R1	0698-4377	2	R FXD 37.4 OHM 1% 1/8W
	0757-0395	2	R FXD 56.2 OHM 1% 1/8W●
A12R2	0757-0715		R FXD 150 OHM 1% 1/4W
	0698-7443	4	R FXD 226 OHM 0.5% 1/4W●
A12R3	0757-0284	6	R FXD 150 OHM 1% 1/8W
	0698-7443		R FXD 226 OHM 0.5% 1/4W●
A12R4	0698-8237	2	R FXD 93.8 OHM 1% 1/8W
	0698-4411	2	R FXD 140 OHM 1% 1/8W●
A12R5	0698-8243	2	R FXD 83.3 OHM 1% 1/4W
	0698-4408	4	R FXD 124 OHM 1% 1/8W●
A12R6	0698-8236	2	R FXD 83.3 OHM 1% 1/8W
	0698-4408		R FXD 124 OHM 1% 1/8W●
A12R7	0698-3440	3	R FXD 196 OHM 1% 1/8W
	0698-4448	2	R FXD 294 OHM 1% 1/8W●
A12R8	0698-8244	2	R FXD 64.3 OHM 1% 1/4W
	0698-8241	4	R FXD 96.4 OHM 1% 1/8W●
A12R9	0698-8238	2	R FXD 64.3 OHM 1% 1/8W
	0698-8241		R FXD 96.4 OHM 1% 1/8W●
A12R10	0698-8240	2	R FXD 398 OHM 1% 1/8W
	0757-1100	2	R FXD 600 OHM 1% 1/8W●
A12R11	0698-8245	3	R FXD 57.7 OHM 1% 1/4W
	0698-8242	4	R FXD 85 OHM 1% 1/8W●
A12R12	0698-8239	1	R FXD 57.7 OHM 1% 1/8W
	0698-8242		R FXD 85 OHM 1% 1/8W●

*OPTIONS 001/003

Abbreviations are listed in the introduction to this section

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ASSEMBLY SERVICE SHEET A12

CLOCK ATTENUATOR A12

GENERAL

The Clock Attenuator is mounted by solder pins to the Clock Front Panel Assembly A10. Range switching is accomplished by a pc slide switch located on the A10 assembly. Five values of attenuation are available, 0, 6, 12, 18 and 24dB and since the output of the Clock Amplifier, A29 is variable between 1.6 and 3.2V pk-pk, the output amplitude ranges available are:

1.6 – 3.2V pk-pk
0.8 – 1.6V pk-pk
0.4 – 0.8V pk-pk
0.2 – 0.4V pk-pk
0.1 – 0.2V pk-pk

OPTIONS

In Options 001 and 003, the impedance of the CLOCK OUTPUT is changed from the standard 50Ω to 75Ω. The 75Ω version of the Attenuator is designated 03760-70612 and uses different resistor values in each of the π networks (the attenuation is still in 6dB steps).

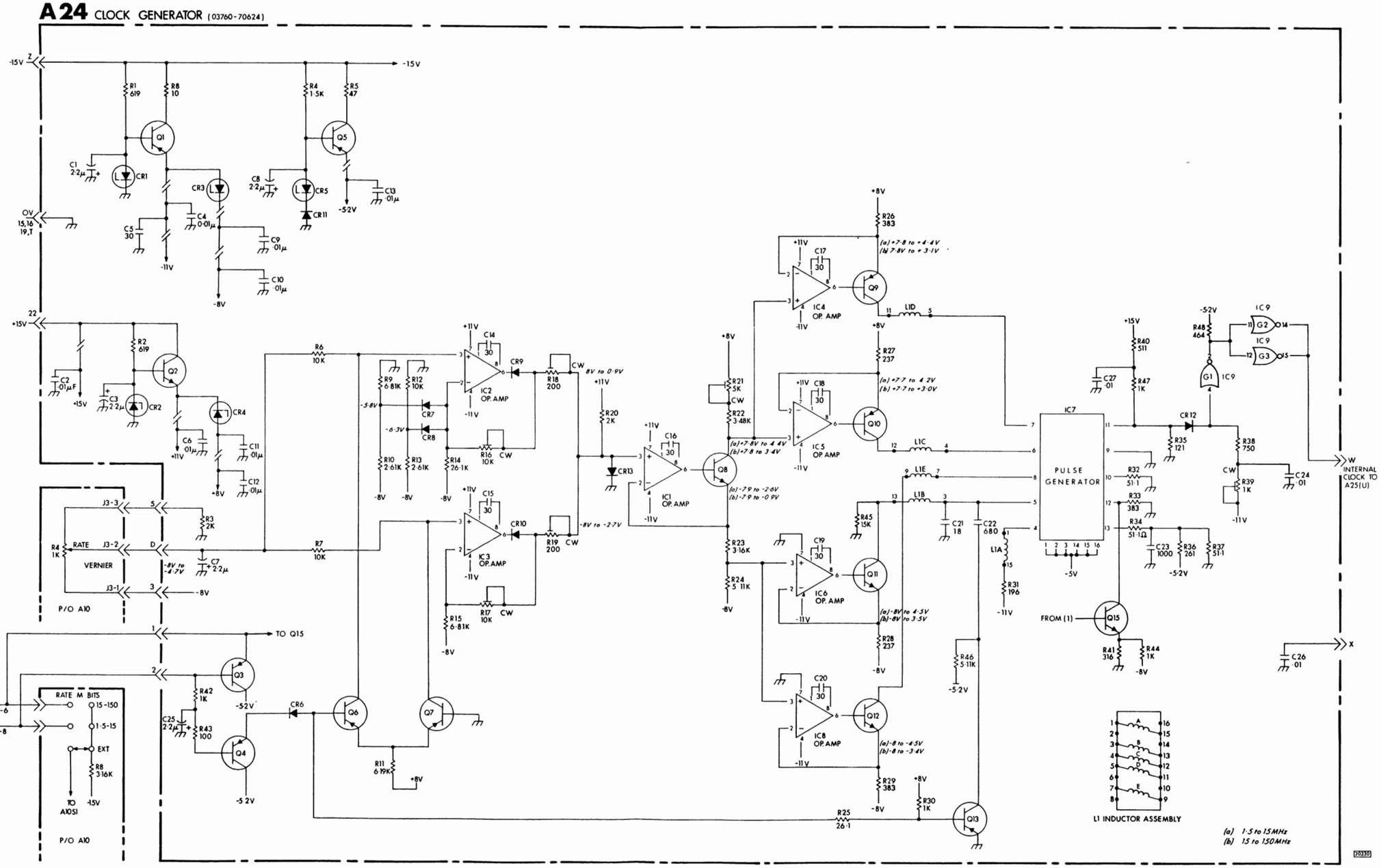

Figure A24-3 Schematic Diagram

Replaceable Parts (continued)

Ref Desig	HP Part No	TQ	Description
A24R38	0698-4251	1	R FXD 750 OHM 5% 1/8W
A24R39	2100-2633	3	R VAR 1K 10% 1/2W LIN
A24R40	0757-0416	27	R FXD 511 OHM 1% 1/8W
A24R41	0698-3444	4	R FXD 316 OHM 1% 1/8W
A24R42	0757-0280		R FXD 1K OHM 1% 1/8W
A24R43	0757-0401	14	R FXD 100 OHM 1% 1/8W
A24R44	0757-0280		R FXD 1K OHM 1% 1/8W
A24R45	0698-4282	1	R FXD 15K OHM 5% 1/8W
A24R46	0757-0438		R FXD 5.11K OHM 1% 1/8W
A24R47	0757-0280		R FXD 1K OHM 1% 1/8W
A24R48	0698-0082	5	R FXD 464 OHM 1% 1/8W

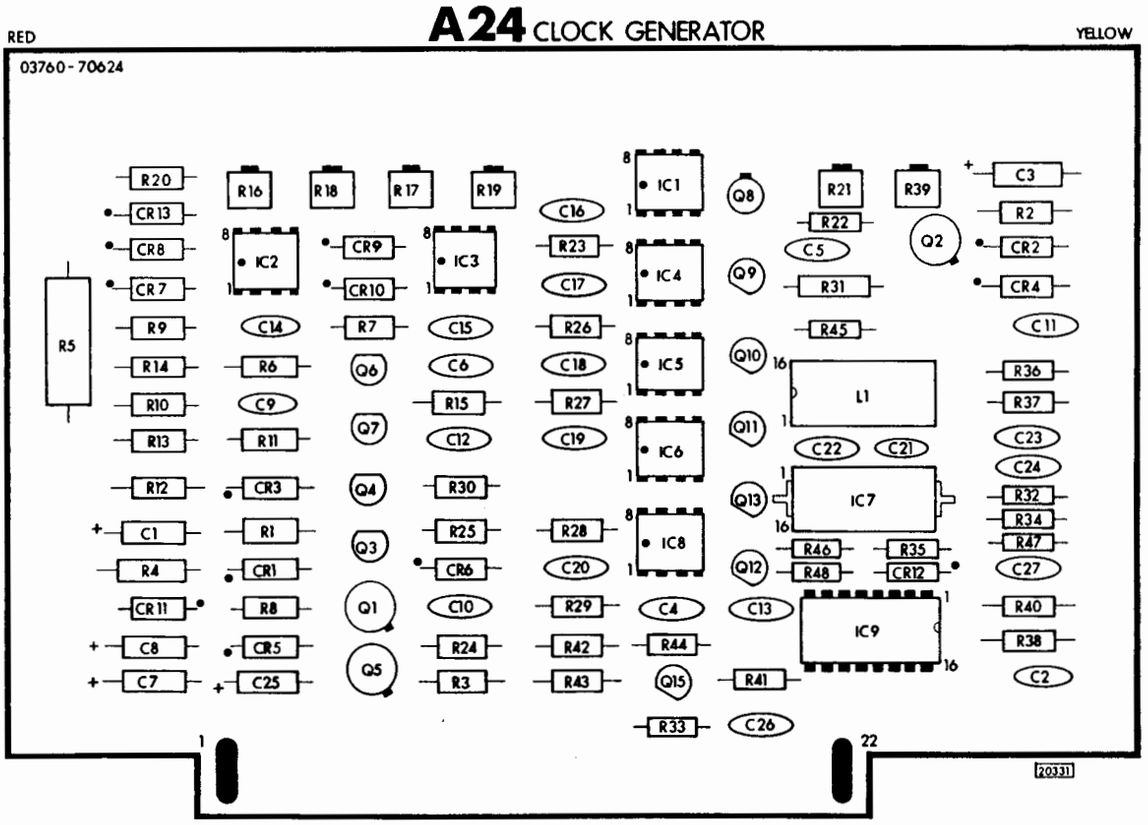

Figure A24-2 Component Location

Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A25R4	0757-0401		R FXD 100 OHM 1% 1/8W
A25R5	0757-0421	1	R FXD 825 OHM 1% 1/8W
A25R6	0698-3151	5	R FXD 2.87K OHM 1% 1/8W
A25R7	0757-0394		R FXD 51.1 OHM 1% 1/8W
A25R8	0698-3444		R FXD 316 OHM 1% 1/8W
A25R9	0698-3132		R FXD 261 OHM 1% 1/8W
A25R10	0757-0394		R FXD 51.1 OHM 1% 1/8W
A25R11	0698-3435	1	R FXD 38.3 OHM 1% 1/8W
A25R12	0757-0442		R FXD 10K OHM 1% 1/8W
A25R13	0757-0346	4	R FXD 10 OHM 1% 1/8W
A25R14	0757-0394		R FXD 51.1 OHM 1% 1/8W
A25R15	0698-3458	2	R FXD 348 OHM 1% 1/8W
A25R16	0757-0394		R FXD 51.1 OHM 1% 1/8W
A25R17	0757-0346		R FXD 10 OHM 1% 1/8W
A25R18	0757-0346		R FXD 10 OHM 1% 1/8W
A25R19	0757-0416		R FXD 511 OHM 1% 1/8W
A25R20	0698-3441	2	R FXD 215 OHM 1% 1/8W
A25R21	2100-2633		R VAR 1K 10% 1/2W LIN
A25R22	0757-0416		R FXD 511 OHM 1% 1/8W
A25R23	0757-0394		R FXD 51.1 OHM 1% 1/8W
A25R24	0757-0346		R FXD 10 OHM 1% 1/8W
A25R25	0698-3445	1	R FXD 348 OHM 1% 1/8W
A25R26	0757-0398	5	R FXD 75 OHM 1% 1/8W
A25R27	0757-0427		R FXD 1.5K OHM 1% 1/8W
A25R28	0698-4037	4	R FXD 46.4 OHM 1% 1/8W
A25R29	0698-3446		R FXD 383 OHM 1% 1/8W
A25R30	0698-3155	5	R FXD 4.64K OHM 1% 1/8W
A25R31	0698-3155		R FXD 4.64K OHM 1% 1/8W
A25R32	0698-3155		R FXD 4.64K OHM 1% 1/8W
A25R33	0698-3155		R FXD 4.64K OHM 1% 1/8W
A25R34	0757-0417	4	R FXD 562 OHM 1% 1/8W
A25R35	0757-0394		R FXD 51.1 OHM 1% 1/8W
A25R36	0757-0417		R FXD 562 OHM 1% 1/8W
A25R37	0757-0394		R FXD 51.1 OHM 1% 1/8W
A25R38	0757-0417		R FXD 562 OHM 1% 1/8W
A25R39	0757-0417		R FXD 562 OHM 1% 1/8W
A25R40	0757-0394		R FXD 51.1 OHM 1% 1/8W
A25R41	0698-3440		R FXD 196 OHM 1% 1/8W
A25R42	0757-0394		R FXD 51.1 OHM 1% 1/8W
A25R43	0757-0399	19	R FXD 82.5 OHM 1% 1/8W
A25R44	0698-3437	19	R FXD 133 OHM 1% 1/8W
A25R45	0757-0442		R FXD 10K OHM 1% 1/8W
A25R46	0757-0442		R FXD 10K OHM 1% 1/8W
A25R47	0757-0472	1	R FXD 200K OHM 1% 1/8W
A25R48	2100-2583	1	R VAR 10 OHM 20% 1/2W LIN
A25R49	0698-3132		R FXD 261 OHM 1% 1/8W
A25R50	0698-5490		R FXD 2K OHM 1% 1/8W
A25R51	0757-0403	2	R FXD 121 OHM 1% 1/8W
A25R52	0757-0419	1	R FXD 681 OHM 1% 1/8W
A25R53	0698-3442		R FXD 237 OHM 1% 1/8W
A25R54	0757-0290		R FXD 6.19K OHM 1% 1/8W
A25R55	2100-2654	1	R VAR 25K OHM 10% WW LIN 2W
A25R56	0757-0460	1	R FXD 61.9K OHM 1% 1/8W
A25S1	3102-0006	1	SW SENSITIVE SPDT PIN PLUNGER

Abbreviations are listed in the introduction to this section

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Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A25	03760-70025		CLOCK INPUT AMPLIFIER ASSY
A25C1	0180-0197		C FXD 2.2UF 10% 20WVDC
A25C2	0180-0197		C FXD 2.2UF 10% 20WVDC
A25C3	0180-0197		C FXD 2.2UF 10% 20WVDC
A25C4	0180-0197		C FXD 2.2UF 10% 20WVDC
A25C5	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A25C6	0180-0291	7	C FXD 1UF +10% 35WVDC
A25C7	0160-2145	3	C FXD 5000PF +80-20% 100WVDC
A25C8	0160-2145		C FXD 5000PF +80-20% 100WVDC
A25C9	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A25C10	0180-0291		C FXD 1UF +10% 35WVDC
A25C11	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A25C12	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A25C13	0160-2145		C FXD 5000PF +80-20% 100WVDC
A25C14	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A25C15	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A25C16	0160-2199		C FXD 30PF 5% 300WVDC
A25C17	0150-0121	8	C FXD 0.1UF +80-20% 50WVDC
A25C18	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A25C19	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A25C20	0160-2199		C FXD 30PF 5% 300WVDC
A25C21	0180-1815	1	C FXD 7.5UF 20% 20WVDC
A25C22	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A25C23	0160-2139	1	C FXD 220 PF +80 -20% 1000VDCW
A25C24	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A25C25	0180-0197		C FXD 2.2UF 10% 20WVDC
A25CR1	1901-0347	3	DIO HOT CARRIER
A25CR2	1901-0347		DIO HOT CARRIER
A25CR3	1901-0347		DIO HOT CARRIER
A25CR4	1901-0050	2	DIO SI
A25CR5	1901-0050		DIO SI
A25CR6	1901-0040		DIO SI
A25CR7	1901-0040		DIO SI
A25CR8	1901-0040		DIO SI
A25IC1	1820-0477		IC OPER AMPL
A25IC2	1820-0477		IC OPER AMPL
A25IC3	1820-0285	3	IC SCHMITT TRIGGER 250MHZ ECL
A25IC4	1820-0101	2	IC TYPE 'D' FLIP FLOP
A25IC5	1820-0796		IC QUAD 2-INPUT NOR GATE ECL
A25IC6	1820-0796		IC QUAD 2-INPUT NOR GATE ECL
A25L1	9100-1620	1	IND FXD 15UH 10%
A25Q1	1854-0345	8	XSTR NPN SILICON
A25Q2	1854-0071		XSTR SI NPN
A25Q3	1854-0345		XSTR NPN SILICON
A25Q4	1854-0345		XSTR NPN SILICON
A25Q5	1854-0345		XSTR NPN SILICON
A25Q6	1853-0018	3	XSTR-PNP SILICON
A25Q7	1853-0018		XSTR-PNP SILICON
A25Q8	1854-0009	1	XSTR SI NPN
A25R1	0757-0710	9	R FXD 75 OHM 1% 1/4W
A25R2	0757-0442		R FXD 10K OHM 1% 1/8W
A25R3	0757-0442		R FXD 10K OHM 1% 1/8W

Abbreviations are listed in the introduction to this section

TRIGGER DETECTOR

Although designed primarily to indicate correct triggering in EXT, the circuit also operates when the internal Clock Generator is used as the clock source.

The divide by two counter, FF1 is clocked by the output of G8 to produce a square wave at half the repetition rate of the clock signal. The Q and $\overline{Q}$ outputs of FF1 are integrated by the low pass filters R45, C18 and R46, C19 respectively. The resulting dc levels, equal to the mean MECL III level of approximately -1.2V are applied to the operational amplifier, IC2. Due to -ve feedback via R47 the output of this amplifier is also held at approximately -1.2V. Q8 is therefore forward biased and the front panel Trigger Lamp switched on. Note that CR8 is reverse biased and the Set input to FF1 is held inoperative at approximately -1.8V by R43 and R44.

If the clock signal fails with the Q and $\overline{Q}$ outputs of FF1 at -1.7V (logic 0) and -0.8V (logic 1) respectively, the output of the operational amplifier saturates at -14V switching Q8 and the Trigger Lamp off. If, however, the clock fails with Q1 and $\overline{Q1}$ at -0.8V and -1.7V, the output of the operational amplifier will rise towards +15V until CR8 becomes forward biased and operates the Set input of FF1. This reverses the inputs to the operational amplifier causing its output to drop to -14V thus switching the trigger lamp off.

MARK/SPACE REFERENCE VOLTAGE

As the clock signal passes through the Delay Generator (A26 and A27) its mark to space ratio is altered. The amount of error introduced is proportional to the delay and hence an automatic correcting circuit is incorporated in assembly A27. The reference voltage for this circuit, which is proportional to the mark:space ratio of the clock signal is obtained by integrating the clock signal in the low pass filter at the output of G4. R55 provides a small degree of preset adjustment.

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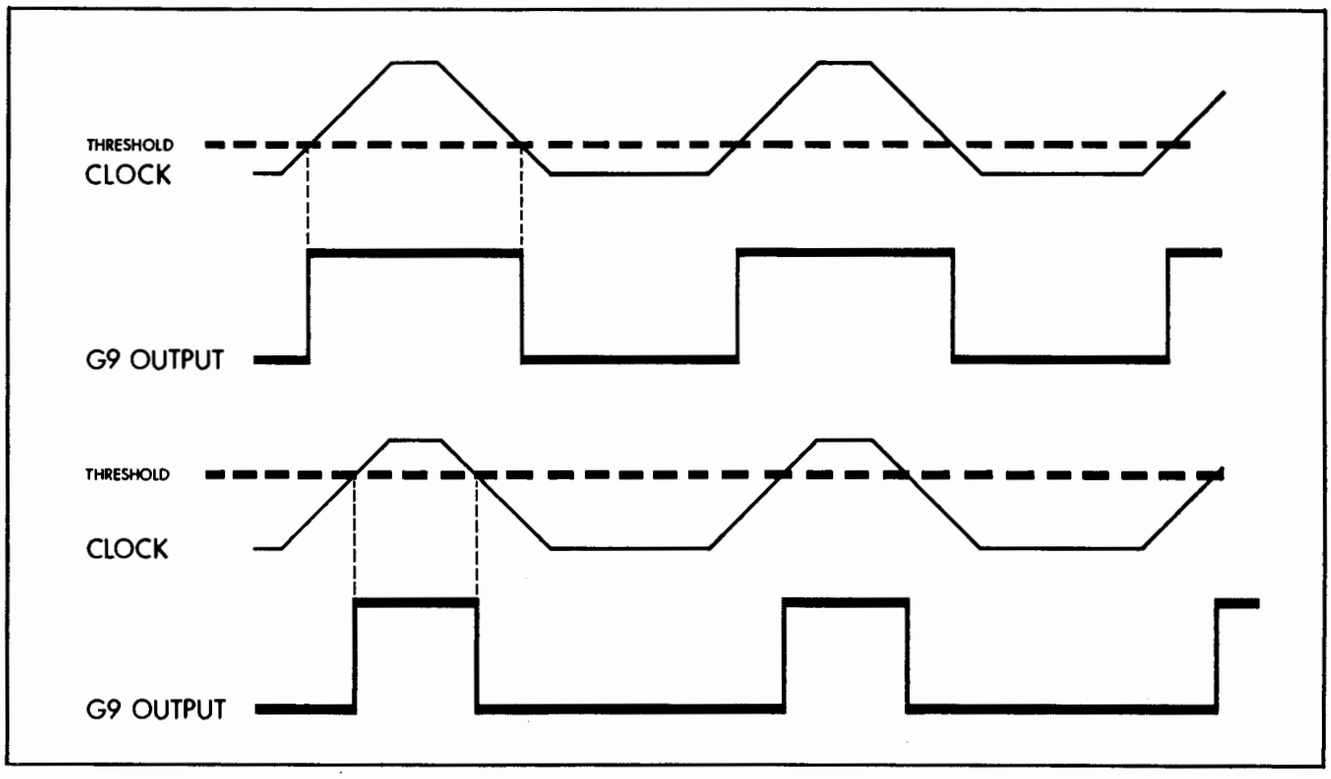

Figure A25-3 Mark:space Ratio Correction

INPUT SELECTOR LOGIC

In Options 002 and 003 an internal clock source in the form of the Clock Generator, A24, is fitted to the Clock Module. This generator produces two variable frequency outputs 1.5 – 15 and 15 – 150MHz, controlled by a front panel vernier. The RATE switch selects 1.5 – 15 or 15 – 150MHz by enabling G3 in the input selector logic. In EXT, the TRIGGER MODE switch enables G5 or G6 to give negative or positive slope triggering of the External Clock signal.

When the Clock Generator is not fitted, the RATE switch is replaced by a wire link which applies -15V to the TRIGGER MODE switch only. G3 is therefore permanently inhibited.

MANUAL CLOCK

This circuit consists of a simple latch G1 and G2, operated by the spring loaded Manual Trigger switch S1. Normally, G2 is inhibited and G1 is enabled allowing the clock signal from the external amplifier to pass through G1 to G6 (positive slope trigger). When the instrument is manually clocked the external clock signal is removed and the schmitt trigger drives G1 with a 0. The Clock Outputs, logically equal to $\overline{\text{CLOCK}}$, are therefore 1. When the switch is depressed, the output of G1 changes from 1 to 0 and produces a 0 at the outputs. Note that if the output of the schmitt trigger is 1 even with the external clock signal removed, the collector of Q6 must be connected to ground to enable the latch.

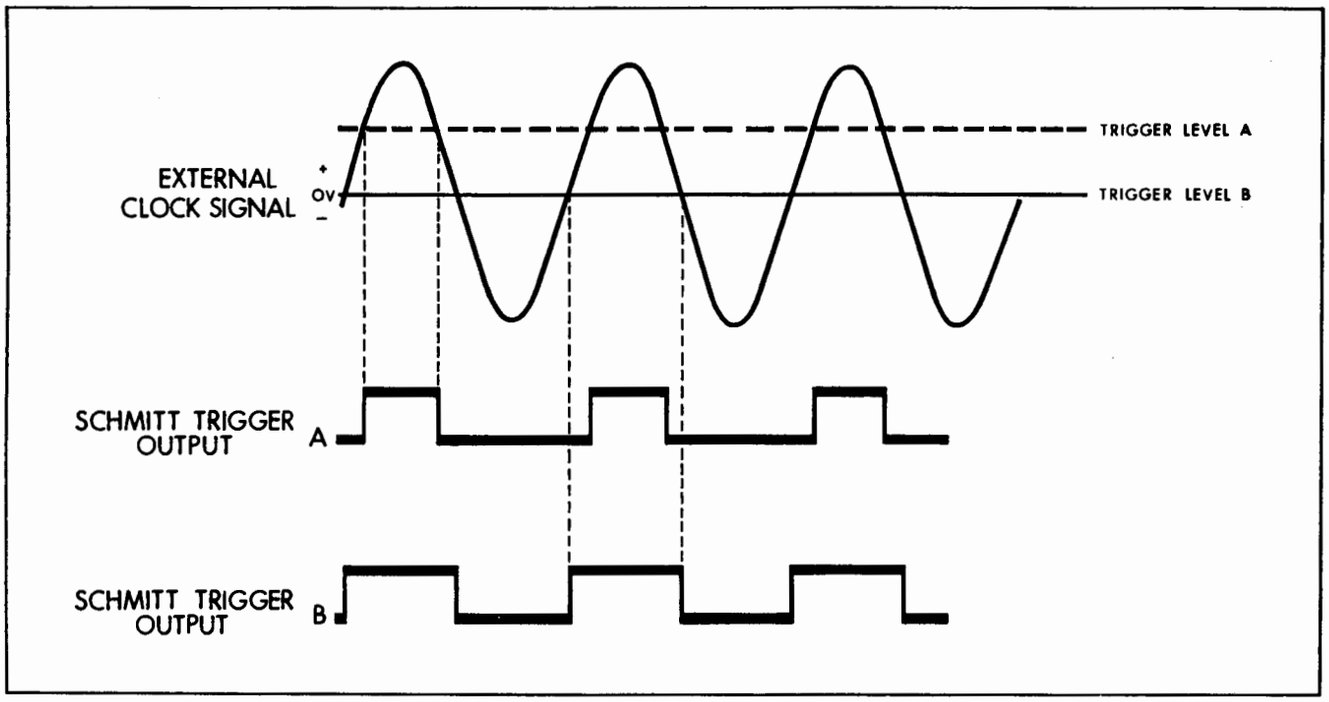

Figure A25-2 Manual Trigger

Figure A25-2 shows a sine wave input with no dc offset. As the sine wave passes through the trigger level, the collector voltages of Q1 and Q3 alternately switch high and low. It can be seen from Figure A25-2 that the mark to space ratio of the collector waveforms (and hence of the output) depends on the trigger level. For slow rise time waveforms such as sine waves, unity mark to space ratio can only be obtained when the trigger level is set to the mean dc level of the waveform (0V in this case).

In AUTO, the external clock signal is integrated by the low pass filter R2, C5, R3, C15 to obtain its mean dc value. This voltage is buffered by the operational amplifier, IC1, which due to 100% negative feedback has unity voltage gain. The output of this amplifier is applied to the base of Q3 as the trigger voltage thus ensuring that on AUTO the trigger level always lies within the swing of the input clock signal. Since sine waves have a mean level equal to their dc offset, the output of the External Clock Amplifier is always unity in AUTO with this type of input.

The differential outputs of the first emitter coupled pair drive the schmitt trigger, IC3 via two cascaded emitter coupled pairs. Due to the relatively long rise and fall times of the clock signal prior to the schmitt trigger (especially at high frequencies) the switching characteristics of the emitter coupled pairs can significantly alter its mark to space ratio. To compensate for this, a trim resistor R21 is included in the third emitter coupled pair to alter the dc offset of the signal applied to the schmitt trigger. Figure A25-3 shows how variations in dc offset (with respect to the schmitt trigger threshold) alters the mark to space ratio of the clock signal.

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ASSEMBLY SERVICE SHEET A25

CLOCK INPUT AMPLIFIER A25

A simplified block diagram of the Clock Input Amplifier is shown in Figure A25-1.

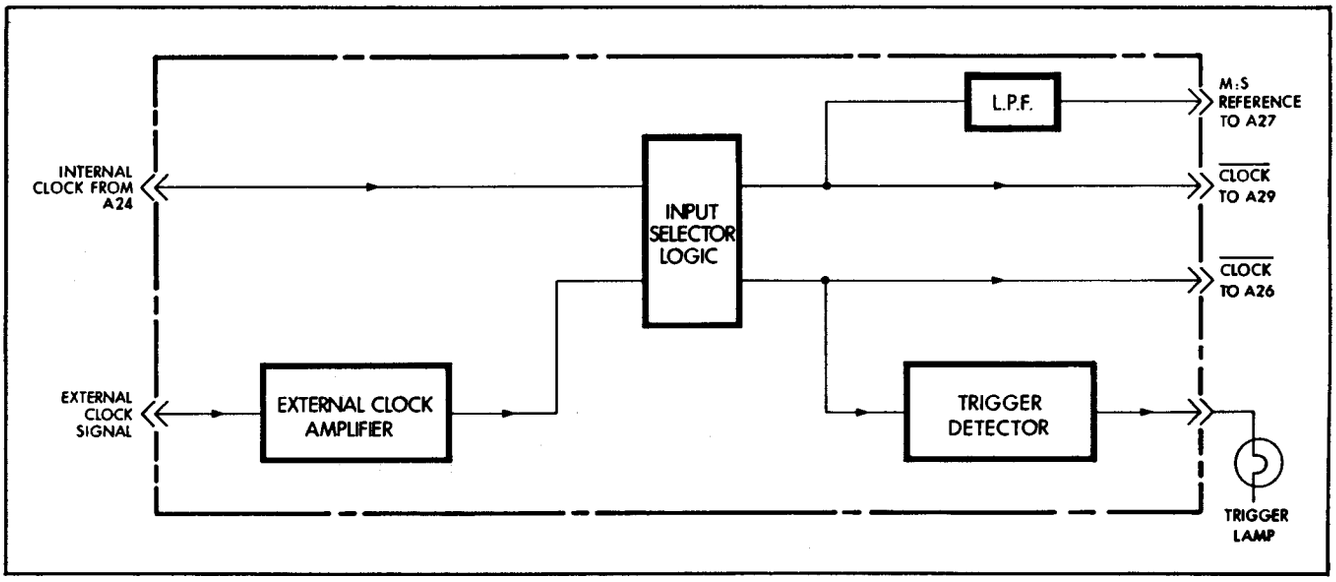

Figure A25-1 Simplified Block Diagram

EXTERNAL CLOCK AMPLIFIER

As the frequency and duty cycle of the external clock signal can vary over a wide range, the External Clock Amplifier is dc coupled. The first emitter coupled pair, Q1 and Q3, acts as a level detector, the trigger point being set by the front panel LEVEL VERNIER on MAN. or by the operational amplifier, IC1, on AUTO.

In MAN the LEVEL VERNIER applies a voltage in the range ±3V to the base of Q3. If the external clock signal is more positive than this, Q1 is forward biased and Q3 is turned off. As the clock signal passes through the trigger level, the tail current of the pair is switched from Q1 to Q3 (a differential of 300mV between the bases of Q1 and Q3 ensures that one side is fully conducting while the other is turned off). The base emitter junctions of Q1 and Q3 are protected from excessive negative inputs by CR4 and CR5 respectively while CR3 protects Q1 from large positive inputs by clamping its base at approximately +5V.

A25 CLOCK INPUT AMPLIFIER - SHEET 2 (03760 - 70025) NOTE: FOR IC POWER CONNECTION SEE PAGE 6-8

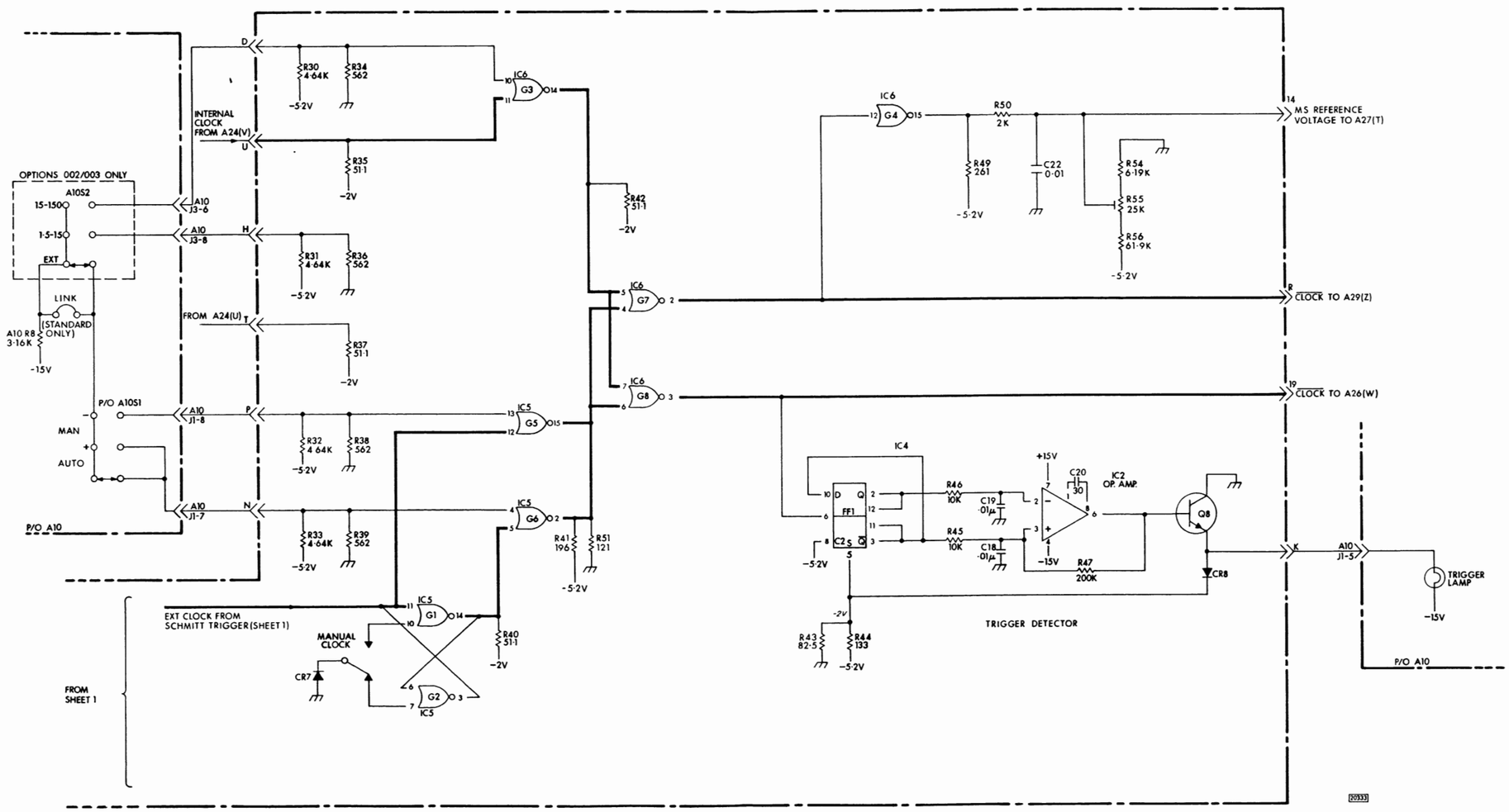

Figure A25-7 Schematic Diagram – Sheet 2

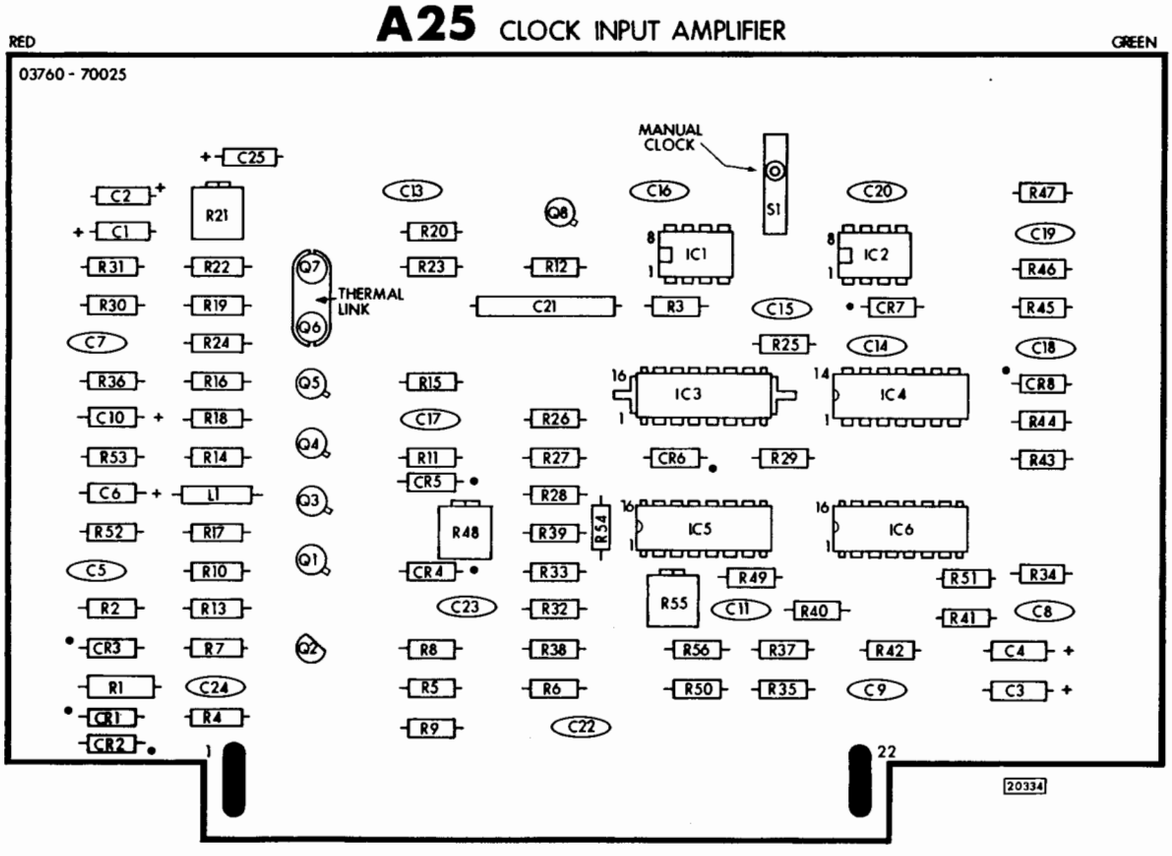

Figure A25-6 Component Location

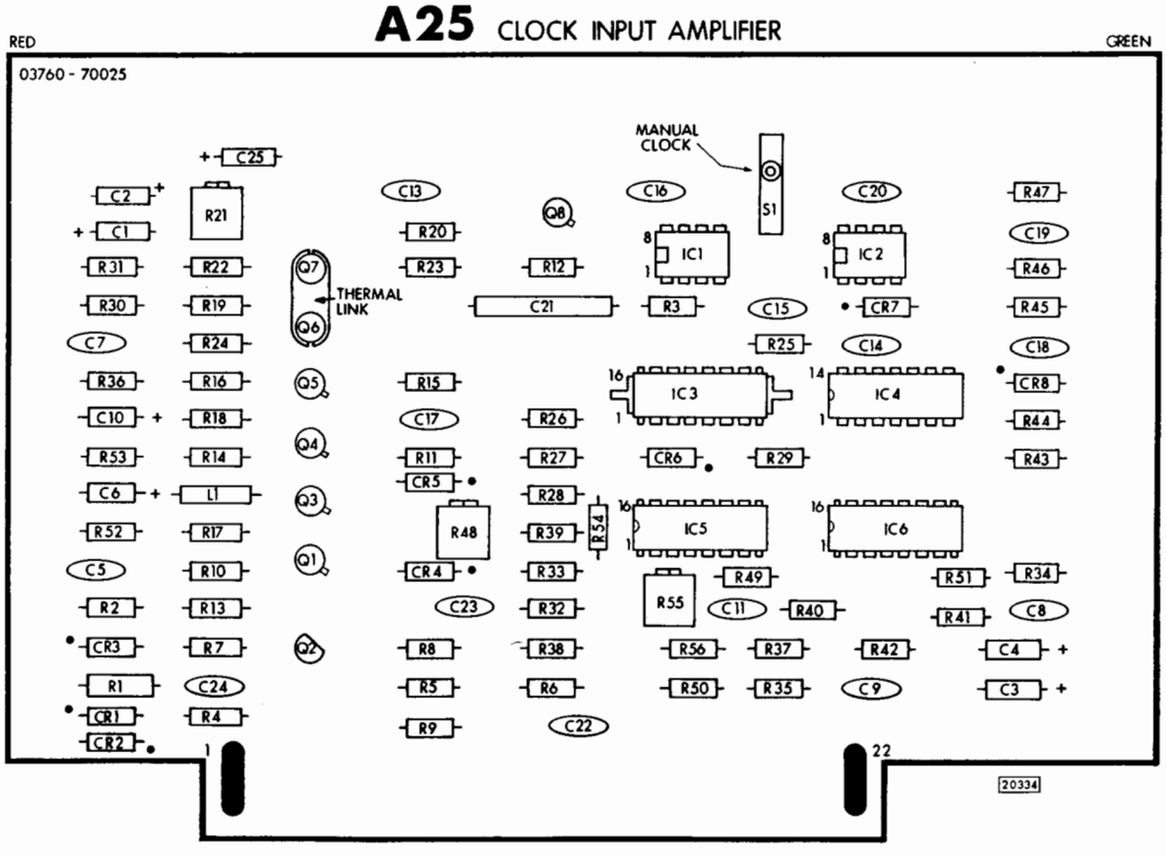

Figure A25-4 Component Location

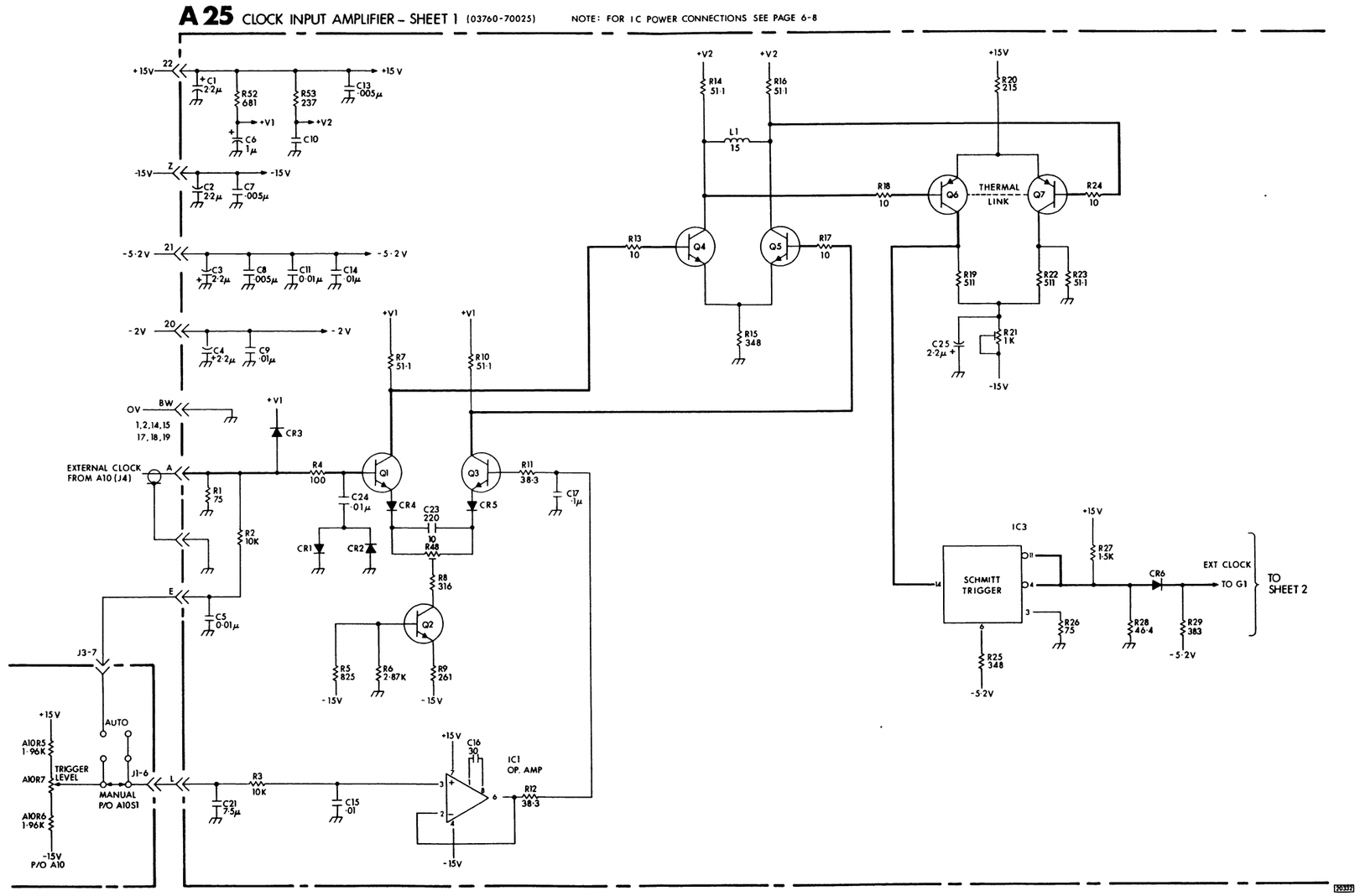

Figure A25-5 Schematic Diagram – Sheet 1

ASSEMBLY SERVICE SHEET A26

DELAY GENERATOR I A26

GENERAL

The clock signal passing through this stage to the Data Module can be delayed by an additional 10, 20, 30, 40, 50, 60 or 70ns, by the appropriate combinations of DL1, DL2, DL3 and DL4. For example when the DATA DELAY switch is set to 0, G1 is inhibited and the clock signal passes through G3, G4 and G12 to the D1 output. Note that G8, G9 and G10 are inhibited and no output appears at D2, D3 or D4. If a delay of 10nS is selected, G3 is inhibited and the clock signal now passes through G1, DL1, G4 and G12 to the D1 output, ie it has been delayed by an additional 10ns in DL1. The effective delay introduced by DL2, DL3 and DL4 is increased by approximately 1.5ns by the extra gate (for pulse regeneration) included in these lines. The D5 output which is delayed by 60 or 70ns drives one more fixed delay line in the A27 assembly to give fixed delays of 80 or 90ns.

FIXED DELAY LINES

Each delay line consists of a number of m-derived sections giving a total delay of 10ns for DL1 and 18.5ns for DL2, DL3 and DL4. These m-derived sections are formed from the equivalent constant-k sections by mutual inductance arising from close positioning of adjacent inductors in the delay lines. As each delay line is basically a low pass filter, the clock pulse shape is progressively degraded as it passes along the line. Factors which affect the pulse shape are:

(i) Cut-off frequency of the delay line.

(ii) Amplitude/Frequency response within the passband.

(iii) Group delay distortion within the passband.

The m-derived sections minimise amplitude ripple and group delay distortion within the passband and by using a large number of small sections, a high cut-off frequency is obtained. To further improve the pulse shape, regenerators in the form of MECL III NOR gates are included at the output of each delay line.

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Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A26	03760-70026		DELAY GENERATOR ASSY 1
A26C1	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A26C2	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A26C3	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A26C4	0160-2264	10	C FXD 20PF 5% 500WVDC
A26C5	0160-2264		C FXD 20PF 5% 500WVDC
A26C6	0160-2264		C FXD 20PF 5% 500WVDC
A26C7	0160-2264		C FXD 20PF 5% 500WVDC
A26C8	0160-2264		C FXD 20PF 5% 500WVDC
A26C9	0160-2264		C FXD 20PF 5% 500WVDC
A26C10	0160-2264		C FXD 20PF 5% 500WVDC
A26C11	0160-2264		C FXD 20PF 5% 500WVDC
A26C12	0160-2264		C FXD 20PF 5% 500WVDC
A26C13	0160-2264		C FXD 20PF 5% 500WVDC
A26C14	0160-2265	76	C FXD 22PF 5% 500WVDC
A26C15	0160-2265		C FXD 22PF 5% 500WVDC
TO			
A26C70	0160-2265		C FXD 22PF 5% 500WVDC
A26C71	0160-2265		C FXD 22PF 5% 500WVDC
A26C72	0160-2265		C FXD 22PF 5% 500WVDC
A26C73	0160-2265		C FXD 22PF 5% 500WVDC
A26IC1	1820-0796		IC QUAD 2-INPUT NOR GATE ECL
A26IC2	1820-0796		IC QUAD 2-INPUT NOR GATE ECL
A26IC3	1820-0796		IC QUAD 2-INPUT NOR GATE ECL
A26R1	0757-0399		R FXD 82.5 OHM 1% 1/8W
A26R2	0698-3437		R FXD 133 OHM 1% 1/8W
A26R3	0757-0428	8	R FXD 1.62K OHM 1% 1/8W
A26R4	0757-0399		R FXD 82.5 OHM 1% 1/8W
A26R5	0757-0399		R FXD 82.5 OHM 1% 1/8W
A26R6	0698-3437		R FXD 133 OHM 1% 1/8W
A26R7	0698-3437		R FXD 133 OHM 1% 1/8W
A26R8	0757-0399		R FXD 82.5 OHM 1% 1/8W
A26R9	0698-3437		R FXD 133 OHM 1% 1/8W
A26R10	0757-0399		R FXD 82.5 OHM 1% 1/8W
A26R11	0698-3437		R FXD 133 OHM 1% 1/8W
A26R12	0757-0428		R FXD 1.62K OHM 1% 1/8W
A26R13	0757-0428		R FXD 1.62K OHM 1% 1/8W
A26R14	0757-0399		R FXD 82.5 OHM 1% 1/8W
A26R15	0698-3437		R FXD 133 OHM 1% 1/8W
A26R16	0757-0428		R FXD 1.62K OHM 1% 1/8W
A26R17	0757-0428		R FXD 1.62K OHM 1% 1/8W

Abbreviations are listed in the introduction to this section

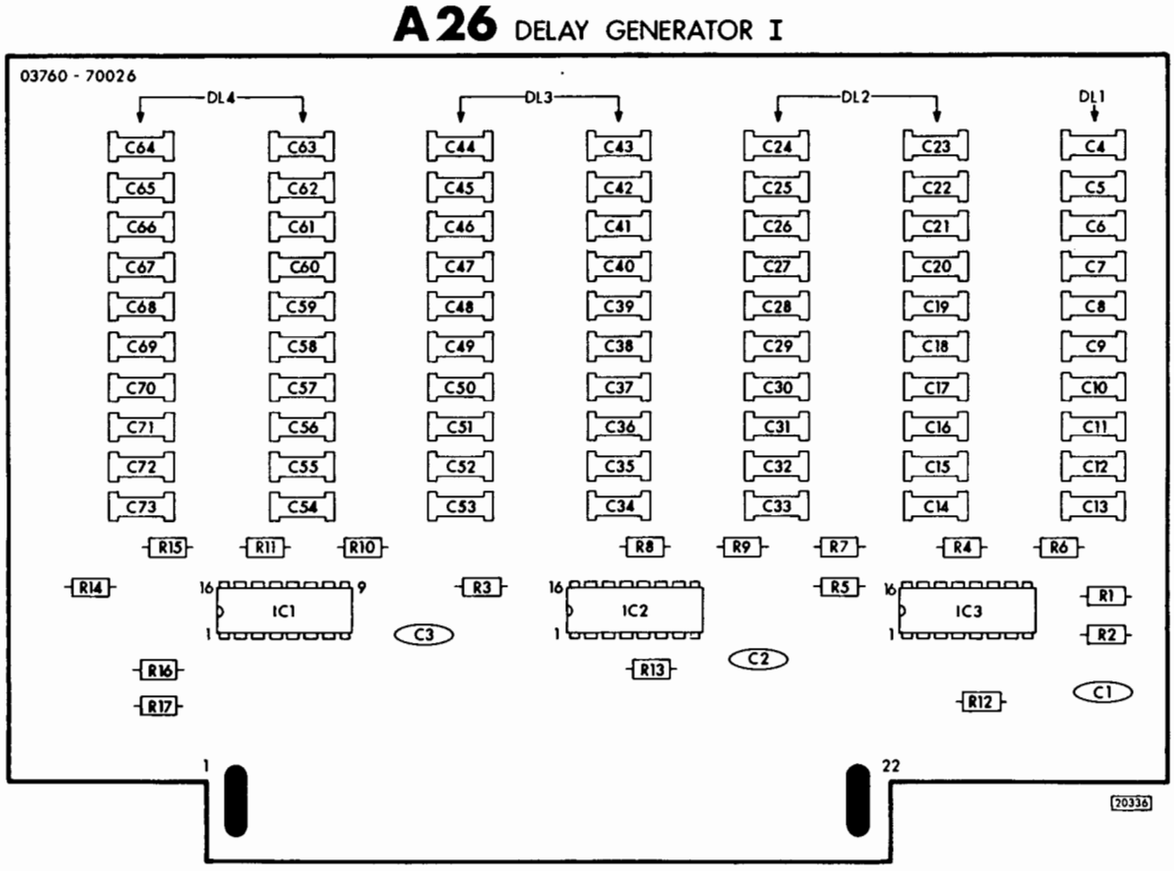

Figure A26-1 Component Location

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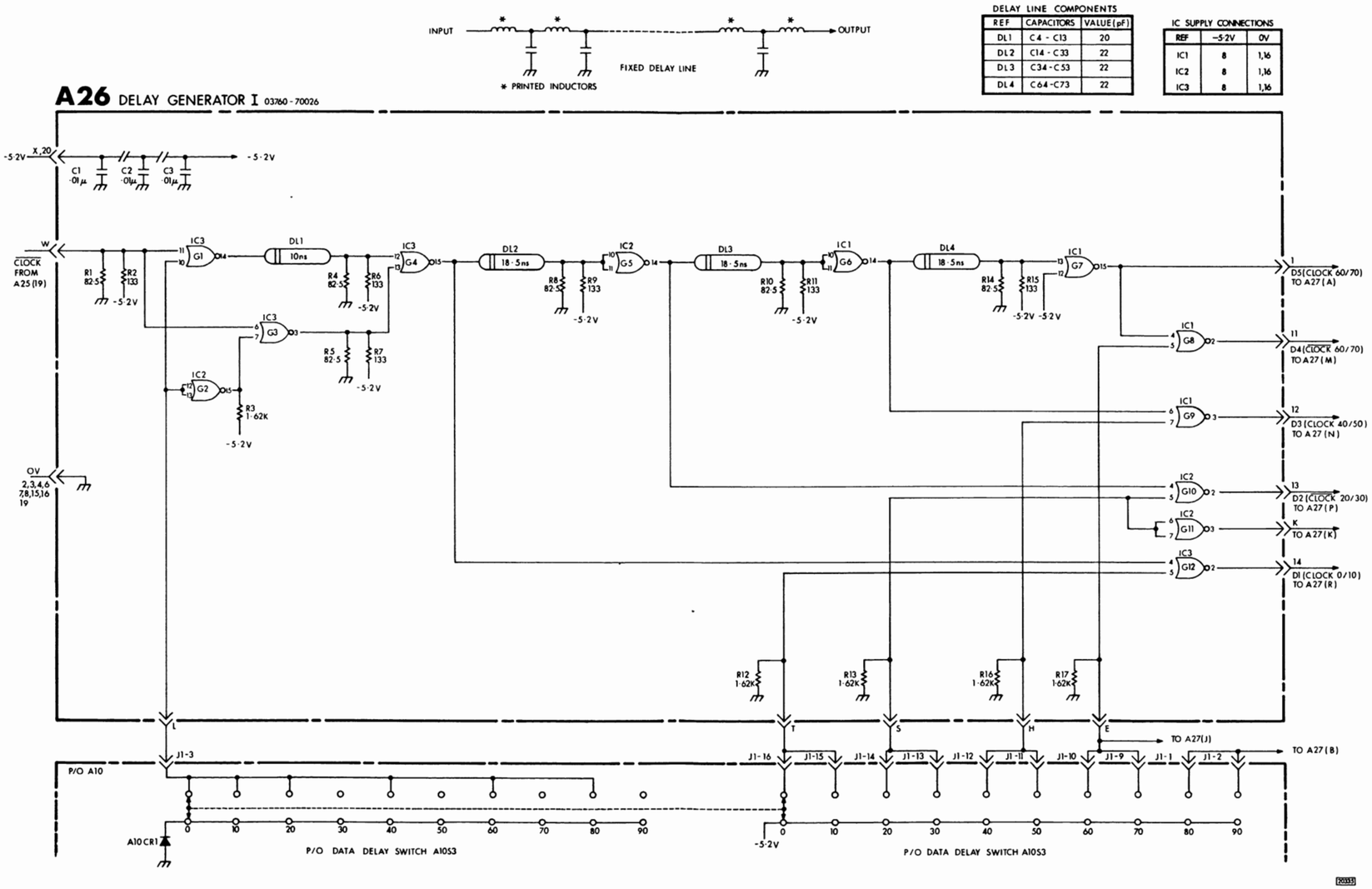

Figure A26-2 Schematic Diagram

ASSEMBLY SERVICE SHEET A27

DELAY GENERATOR II A27

GENERAL

The D5 output of A26 (CLOCK 60/70ns) drives the final fixed delay line A27DL1 to produce a clock signal delayed by 80 or 90ns at the output of G4. The Variable Delay Line gives a 10ns variation in delay and is driven by one of the fixed delay signals via G5 or G6. Note that since D1, D3 and the output of G4 are logically equal to CLOCK, these signals are inverted in G6 so that the Variable Delay Line is always driven by $\overline{\text{CLOCK}}$. When fixed delays of 20, 30, 60 or 70ns are selected, all the signal inputs to G6 are held at 0. To prevent the output of G6 being held at 1 on these ranges, it is inhibited by the DATA DELAY switch via A26G11 or A27G2.

As mentioned in Service Sheet A26, the clock pulse shape is regenerated by a MECL III gate in each delay line and although this restores the amplitude and rise time of the pulses, it also produces a change in the mark to space ratio of the pulse stream. This error is particularly severe on long delays and is corrected at the output of the Variable Delay Line by a mark to space ratio correction circuit involving IC4.

VARIABLE DELAY LINE

The 10ns variable delay is produced by an elastic coax line and bias generator. This line is formed from the same type of printed inductors as the fixed delay lines but uses varactor diodes in place of fixed capacitors to vary the electrical length of the line in proportion to the reverse bias applied to them by the DELAY VERNIER. Note that the calibration 0 – 10ns on the DELAY VERNIER refers to the relative delay produced between minimum and maximum settings of the control and not to the absolute delay introduced by this circuit.

As the bias and hence the capacity of the varactor diodes will be altered by the presence of clock pulses in the line (especially at low levels), adjacent diodes are connected in opposite directions to prevent the clock signal from modulating the electrical length of the line. This arrangement requires two differential bias supplies centred on the mean dc level of the clock pulses (approximately -1.2V).

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BIAS GENERATOR

The bias voltage is generated by the non-linear amplifier Q1 and buffers Q2 and Q3. Figure A27-1 shows how the collector voltage of Q1 must vary as the DELAY VERNIER is rotated to produce a linear scale on this control. At minimum delay, the input from the DELAY VERNIER is 0V, Q1 is forward biased and its collector voltage is approximately -1.5V. CR1 to CR4 are therefore forward biased and the collector load of Q1 consists of the parallel combination of R21 to R29. As the vernier is rotated towards maximum, the collector current of Q1 decreases and its collector voltage falls linearly until it reaches -2V. At this point (B on the curve) CR4 becomes reverse biased and effectively removes R28 and R29 from the collector load of Q1, ie, the collector load of Q1 is increased. Due to this increase, the collector voltage of Q1 falls more rapidly from B to C until at approximately -2.5V CR3 becomes reverse biased, increasing the collector load of Q1 again. Further increases occurring at -4.5 and -8.7V progressively steepen the slope of the curve as the vernier is rotated towards maximum but as the diodes do not switch off sharply, the break points are not clearly defined and the overall effect is that of a smooth curve as shown in Figure A27-1.

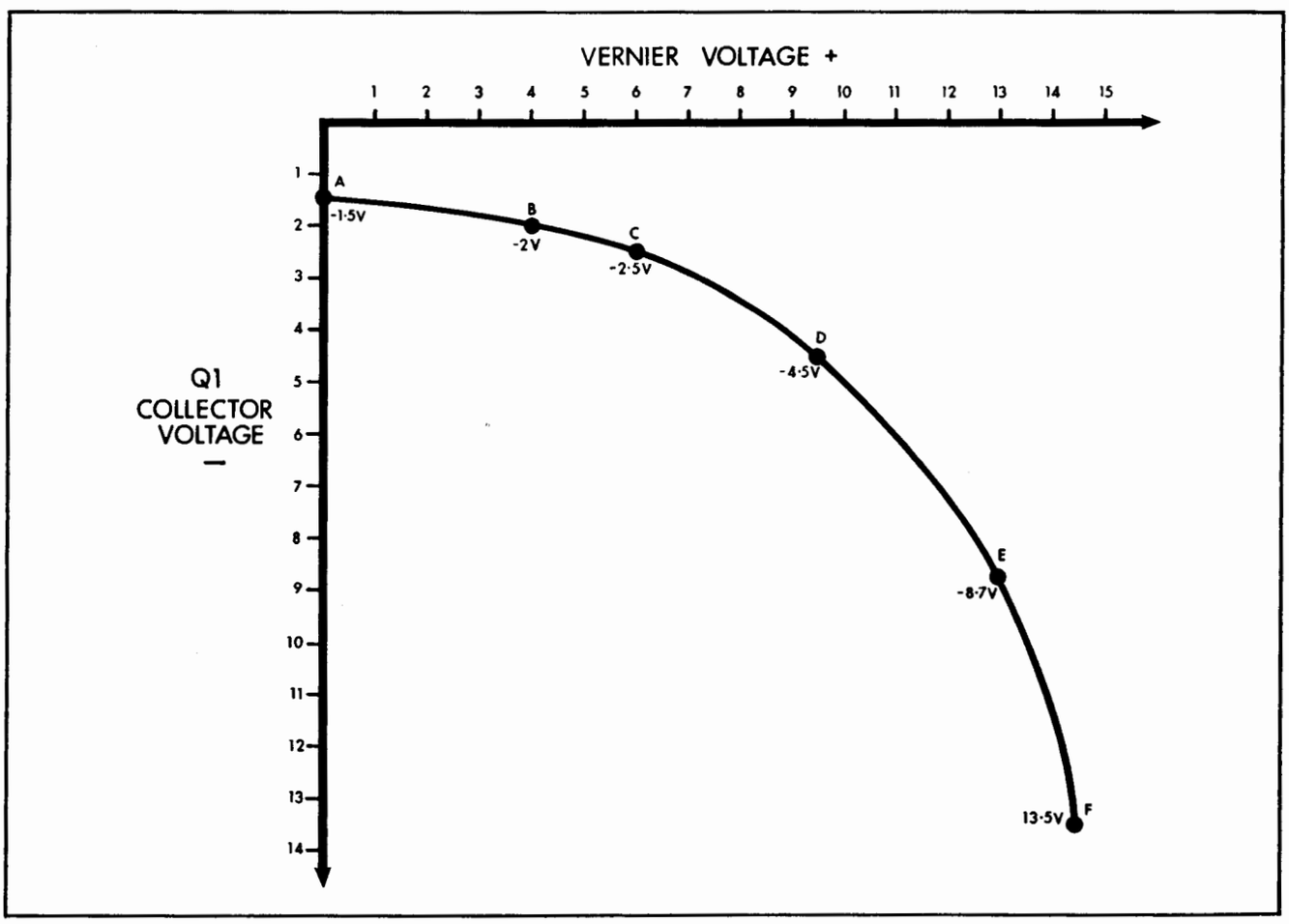

Figure A27-1 Bias Voltage

MARK:SPACE RATIO CORRECTION

As previously mentioned, the mark to space ratio of the clock pulse stream is altered by the regenerating action of the MECL III gates in the delay lines. This error is corrected by the operational amplifier IC4 which alters the dc offset of the clock signal at the input to G8. Figure A27-2 shows how a variation in this dc offset affects the mark to space ratio of the output.

The difference in duty cycles of the two clock signals is detected by IC4 as a difference in their mean dc levels. For example, if the mark to space ratio of the delayed clock signal is less than that of the original clock signal, the dc output voltage of the low pass filter R18C51 will be -ve with respect to the Mark:Space Reference Voltage. (This reference is obtained by integrating the clock signal in the Clock Input Amplifier). The output of IC4 will therefore be positive and will tend to shift the dc offset of the delayed clock signal at the input to G8 positively until the mark:space ratio of the clock at the output of G9 is the same as the undelayed clock. Figure A27-2 shows how a position shift in the dc offset produces an increase in the mark:space ratio of the clock at the output of G9.

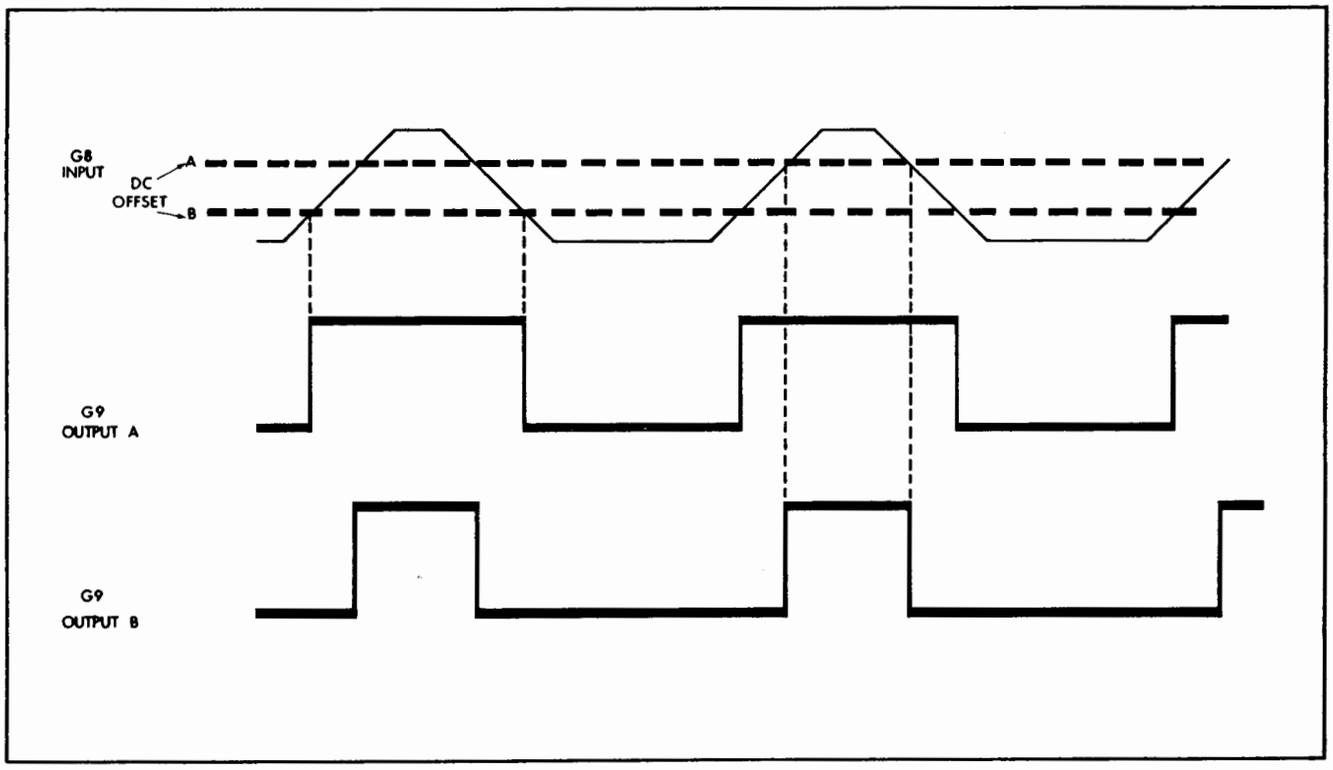

Figure A27-2 Mark:Space Ratio Correction

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Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A27	03760-70027		DELAY GENERATOR ASSY 2
A27C1	0160-2265		C FXD 22PF 5% 500WVDC
A27C2	0160-2265		C FXD 22PF 5% 500WVDC
A27C3	0160-2265		C FXD 22PF 5% 500WVDC
A27C4	0160-2265		C FXD 22PF 5% 500WVDC
A27C5	0160-2265		C FXD 22PF 5% 500WVDC
A27C6	0160-2265		C FXD 22PF 5% 500WVDC
A27C7	0160-2265		C FXD 22PF 5% 500WVDC
A27C8	0160-2265		C FXD 22PF 5% 500WVDC
A27C9	0160-2265		C FXD 22PF 5% 500WVDC
A27C10	0160-2265		C FXD 22PF 5% 500WVDC
A27C11	0160-2265		C FXD 22PF 5% 500WVDC
A27C12	0160-2265		C FXD 22PF 5% 500WVDC
A27C13	0160-2265		C FXD 22PF 5% 500WVDC
A27C14	0160-2265		C FXD 22PF 5% 500WVDC
A27C15	0160-2265		C FXD 22PF 5% 500WVDC
A27C16	0160-2265		C FXD 22PF 5% 500WVDC
A27C17	0160-2265		C FXD 22PF 5% 500WVDC
A27C18	0160-2265		C FXD 22PF 5% 500WVDC
A27C19	0160-2265		C FXD 22PF 5% 500WVDC
A27C20	0160-2265		C FXD 22PF 5% 500WVDC
A27C21	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A27C22	0150-0050		C FXD 1000PF +80-20% 1000WVDC
A27C23	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A27C24	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A27C25	0150-0050		C FXD 1000PF +80-20% 1000WVDC
A27C26	0150-0050		C FXD 1000PF +80-20% 1000WVDC
A27C27	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A27C28	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A27C29	0150-0050		C FXD 1000PF +80-20% 1000WVDC
A27C30	0150-0050		C FXD 1000PF +80-20% 1000WVDC
A27C31	0150-0050		C FXD 1000PF +80-20% 1000WVDC
A27C32	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A27C33	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A27C34	0150-0050		C FXD 1000PF +80-20% 1000WVDC
A27C35	0150-0050		C FXD 1000PF +80-20% 1000WVDC
A27C36	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A27C37	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A27C38	0150-0050		C FXD 1000PF +80-20% 1000WVDC
A27C39	0150-0050		C FXD 1000PF +80-20% 1000WVDC
A27C40	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A27C41	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A27C42	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A27C43	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A27C44	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A27C45	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A27C46	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A27C47	0180-0291		C FXD 1UF +10% 35WVDC
A27C48	0180-0291		C FXD 1UF +10% 35WVDC
A27C49	0160-2199		C FXD 30PF 5% 300WVDC
A27C50	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A27C51	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A27CR1	1901-0044		DIO SI

Abbreviations are listed in the introduction to this section

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Replaceable Parts (continued)

Ref Desig	HP Part No	TQ	Description
A27CR2	1901-0044		DIO SI
A27CR3	1901-0044		DIO SI
A27CR4	1901-0044		DIO SI
A27CR5	1901-0044		DIO SI
A27CR6	1902-3024	1	DIO BKDN 2.87V 5% 400MW
A27CR7	0122-0289	18	C V-VAR 15PF 5% 20WVDC
TO			
A27CR24	0122-0289		C V-VAR 15PF 5% 20WVDC
A27IC1	1820-0796		IC QUAD 2-INPUT NOR GATE ECL
A27IC2	1820-0790	7	IC DUAL 4-INPUT OR-NOR GATE ECL
A27IC3	1820-0796		IC QUAD 2-INPUT NOR GATE ECL
A27IC4	1820-0477		IC OPER AMPL
A27J1	1250-1255		CONN COAX PC BD MTG CONHEX 50 OHM
A27Q1	1853-0010	6	XSTR SI PNP
A27Q2	1853-0010		XSTR SI PNP
A27Q3	1854-0039		XSTR SI NPN
A27R1	0757-0399		R FXD 82.5 OHM 1% 1/8W
A27R2	0757-0394		R FXD 51.1 OHM 1% 1/8W
A27R3	0757-0394		R FXD 51.1 OHM 1% 1/8W
A27R4	0757-0394		R FXD 51.1 OHM 1% 1/8W
A27R5	0757-0394		R FXD 51.1 OHM 1% 1/8W
A27R6	0757-0394		R FXD 51.1 OHM 1% 1/8W
A27R7	0698-3437		R FXD 133 OHM 1% 1/8W
A27R8	0757-0399		R FXD 82.5 OHM 1% 1/8W
A27R9	0698-3437		R FXD 133 OHM 1% 1/8W
A27R10	0757-0428		R FXD 1.62K OHM 1% 1/8W
A27R11	0757-0394		R FXD 51.1 OHM 1% 1/8W
A27R12	2100-2633		R VAR 1K 10% 1/2W LIN
A27R13	0757-0394		R FXD 51.1 OHM 1% 1/8W
A27R14	0757-0394		R FXD 51.1 OHM 1% 1/8W
A27R15	0698-3152		R FXD 3.48K OHM 1% 1/8W
A27R16	0757-0394		R FXD 51.1 OHM 1% 1/8W
A27R17	0757-0442		R FXD 10K OHM 1% 1/8W
A27R18	0757-0442		R FXD 10K OHM 1% 1/8W
A27R19	0757-0394		R FXD 51.1 OHM 1% 1/8W
A27R20	0757-0280		R FXD 1K OHM 1% 1/8W
A27R21	0698-3154		R FXD 4.22K OHM 1% 1/8W
A27R22	0757-0441	1	R FXD 8.25K OHM 1% 1/8W
A27R23	0757-0438		R FXD 5.11K OHM 1% 1/8W
A27R24	0698-3150	3	R FXD 2.37K OHM 1% 1/8W
A27R25	0698-3155		R FXD 4.64K OHM 1% 1/8W
A27R26	0757-0420	1	R FXD 750 OHM 1% 1/8W
A27R27	0698-3151		R FXD 2.87K OHM 1% 1/8W
A27R28	0757-0407	4	R FXD 200 OHM 1% 1/8W
A27R29	0757-0280		R FXD 1K OHM 1% 1/8W
A27R30	0698-3160	1	R FXD 31.6K OHM 1% 1/8W
A27R31	0757-0279		R FXD 3.16K OHM 1% 1/8W
A27R32	0757-0279		R FXD 3.16K OHM 1% 1/8W
A27R33	0757-0427		R FXD 1.5K OHM 1% 1/8W
A27R34	0757-0428		R FXD 1.62K OHM 1% 1/8W
A27R35	0683-1065	1	R FXD 10M OHM 1/4W 5%

Abbreviations are listed in the introduction to this section

ASSEMBLY SERVICE SHEET A28

CLOCK LEVEL CONTROL AMPLIFIER A28

TAIL CURRENT CONTROL

The tail currents of the second and third emitter coupled pairs in the Clock Output Amplifier, A29, are controlled by Q1 and Q2 respectively. The collector currents of these transistors are in turn controlled by the AMPLITUDE VERNIER via the operational amplifier, IC3 and buffer Q3.

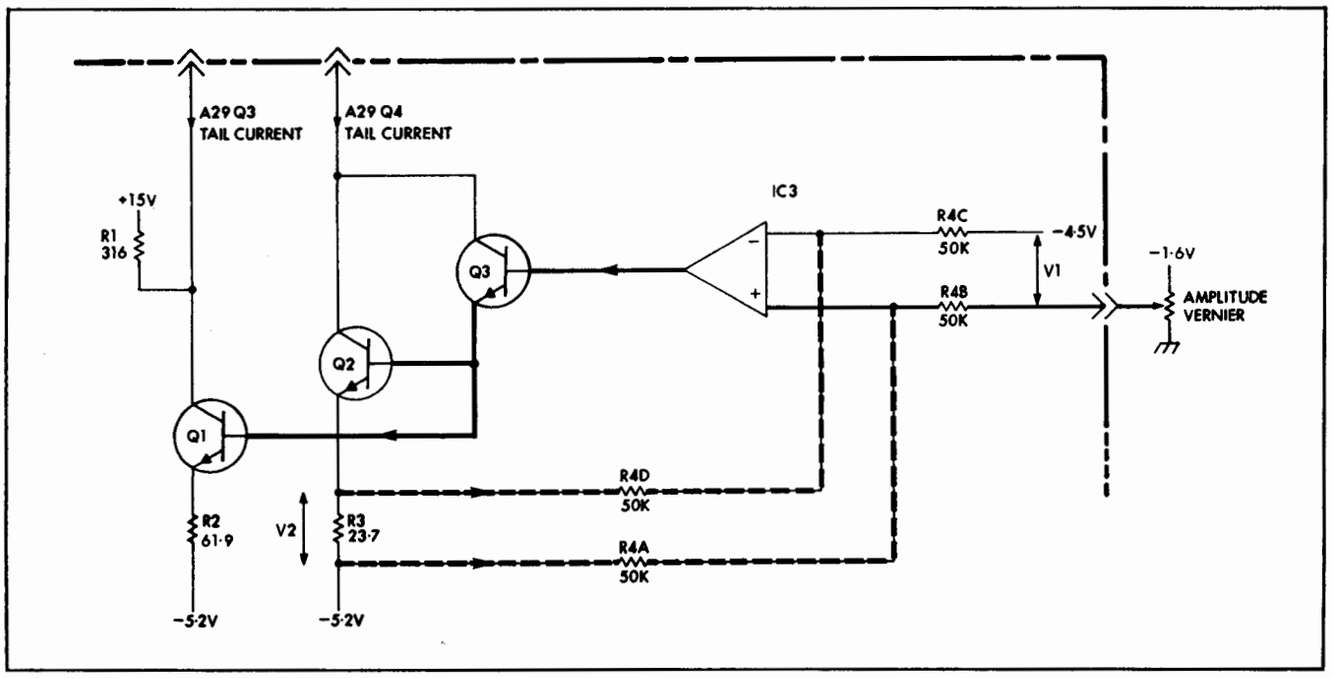

Figure A28-1 Tail Current Control

The collector current of Q2 (tail current of Q29Q4) is stabilised by monitoring the voltage drop it generates across R3 and feeding it back via precision resistors R4A and R4D to the differential inputs of IC3. The circuit is stable when the + and - inputs to IC3 are equal, ie, when differential input is 0. As R4A, B, C and D are all 50K this occurs when V2 = V1. R4C is connected to a fixed bias of -4.5V while the input from the AMPLITUDE VERNIER to R4B varies between -1.6V at minimum output to 0V at maximum. V2 (the voltage drop across R2) therefore varies between 2.9 and 4.5V producing a tail current in the third emitter coupled pair of approximately 125 to 190mA. This feedback arrangement not only gives the circuit a high degree of temperature stability but also provides immunity from ripple etc. on the -5.2V supply line.

The tail current of the first emitter coupled pair flowing through Q1 is not directly stabilised. However, as the forward base-emitter voltage drop of Q1 is almost equal to that of Q2, the voltage drop across R2 is almost equal to V2. R1 is connected to the +15V supply line to balance out the current drawn from the -15V supply by A29R16 in the Clock Amplifier. The net tail current of the second emitter coupled pair therefore varies between approximately 40mA at minimum and 70mA at maximum output amplitude.

OUTPUT AMPLITUDE CONTROL VOLTAGE

The Output Amplitude Control Voltage is generated by the operational amplifier IC2. The +input to IC2 is biased to +5.9V by a potential divider and feedback from the output via R4E stabilises the circuit with the -input also held at +5.9V. The input from the AMPLITUDE VERNIER varies between -1.6V at minimum to 0V at maximum output and since R4E and R4F are equal, the Output Amplitude Control Voltage varies between +13.4 and +11.8V.

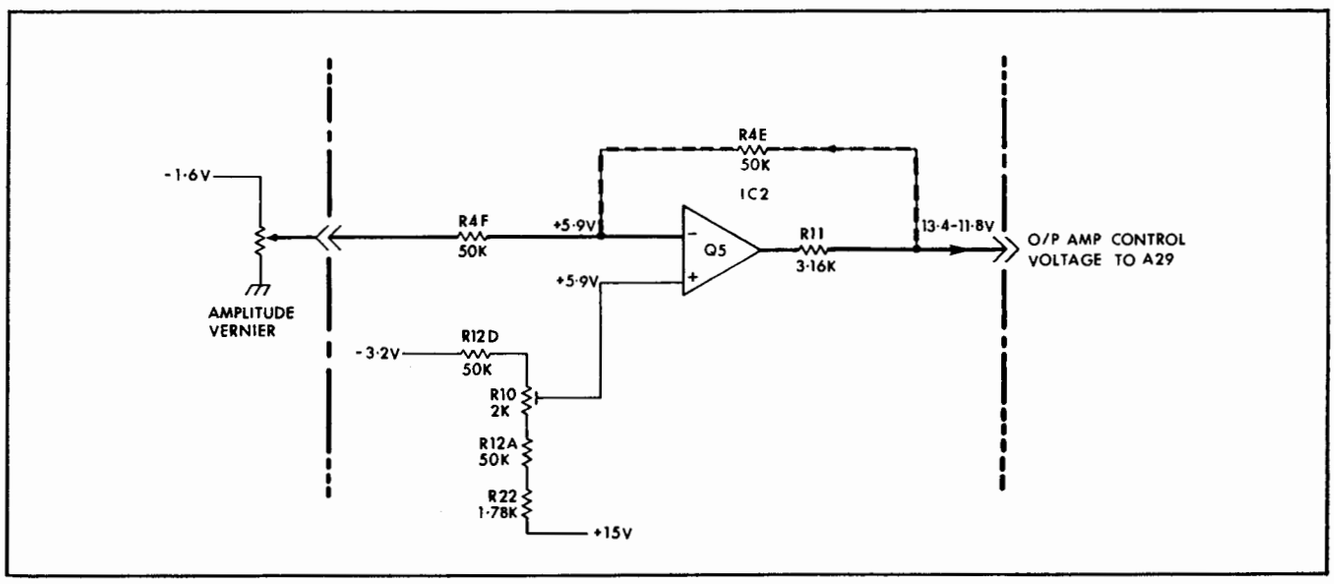

Figure A28-2 Amplitude Control Voltage

BALANCE CURRENT CONTROL

The balance current is controlled by the AMPLITUDE VERNIER via the operational amplifier IC1 and current amplifier Q4 as shown in Figure A28-3. This current, equal to half that being switched by the output transistor, A29Q7 in the Clock Amplifier, is stabilised by monitoring the voltage drop it produces across R13 and feeding it back via precision resistors to the differential inputs of IC1. This feedback stabilises the circuit with the differential inputs to IC1 equal to 0V and since R12E, F, G, and H are all equal, this occurs when V2 = V1. R12G is connected to a fixed bias of -3.2V while the input from the AMPLITUDE VERNIER to R12E varies between -1.6V at minimum output and 0V at maximum output. V2 (the voltage drop across R13) therefore varies between 1.6 and 3.2V producing a balance current varying between 32 and 64mA over the amplitude range.

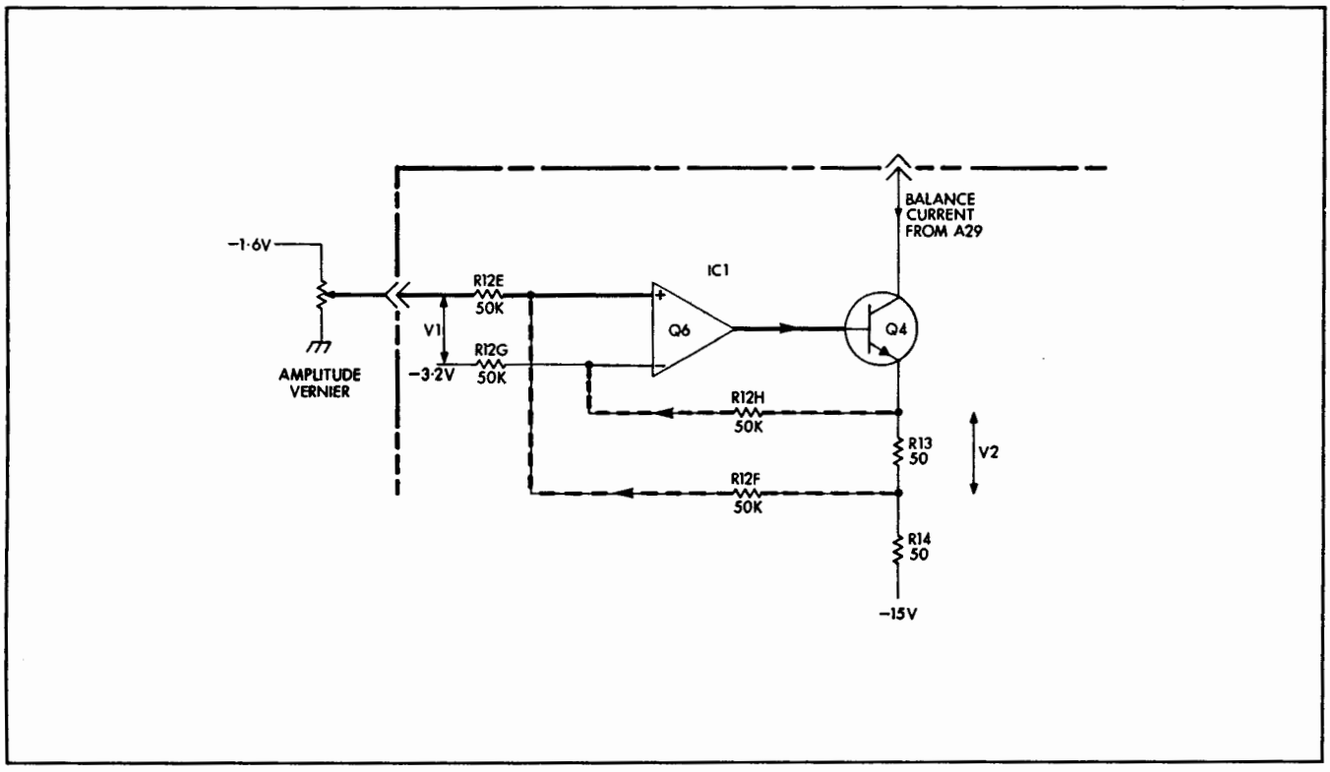

Figure A28-3 Balance Current Control

DC OFFSET AMPLIFIER

When a positive dc offset is required Q5, Q7 and Q9 are forward biased allowing a positive current proportional to the setting of the OFFSET VERNIER to flow in the load. The effective collector load of Q9 is 25Ω (50Ω load in parallel with the 50Ω output impedance of the Attenuator) and hence its collector current must vary between 0 and +120mA to generate the offset voltage range of 0 to +3V. As the output of the Clock Amplifier is balanced (no dc offset) and the output impedance of the Attenuator is always 50Ω, the offset and amplitude levels of the CLOCK OUTPUT are completely independent of one another.

Negative dc offsets are generated by forward biasing Q6, Q8 and Q10 to allow a negative current to flow in the load.

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Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A28	03760-70028		CLOCK LEVEL CONTROL AMP ASSY
	03760-70628		CLOCK LEVEL CON AMP ASSY OPT 001/003
A28C1	0160-2199		C FXD 30PF 5% 300WVDC
A28C2	0150-0121		C FXD 0.1UF +80-20% 50WVDC
A28C3	0160-2199		C FXD 30PF 5% 300WVDC
A28C4	0160-2199		C FXD 30PF 5% 300WVDC
A28C5	0150-0121		C FXD 0.1UF +80-20% 50WVDC
A28C6	0150-0121		C FXD 0.1UF +80-20% 50WVDC
A28CR1	1902-0509	2	DIO BKDN 6.2V 2% TEMP COMP
A28CR2	1901-0047	6	DIO SI
A28CR3	1901-0047		DIO SI
A28IC1	1820-0477		IC OPER AMPL
A28IC2	1820-0477		IC OPER AMPL
A28IC3	1820-0477		IC OPER AMPL
A28Q1	1854-0039		XSTR SI NPN
A28Q2	1854-0039		XSTR SI NPN
	1205-0011	8	HEAT DISSIPATOR XSTR
A28Q3	1854-0071		XSTR SI NPN
A28Q4	1854-0039		XSTR SI NPN
	1205-0011		HEAT DISSIPATOR XSTR
A28Q5	1854-0071		XSTR SI NPN
A28Q6	1853-0020	13	XSTR SI PNP
A28Q7	1853-0020		XSTR SI PNP
A28Q8	1854-0071		XSTR SI NPN
A28Q9	1853-0210	3	XSTR PNP SILICON
	1205-0011		HEAT DISSIPATOR XSTR
A28Q10	1854-0039		XSTR SI NPN
	1205-0011		HEAT DISSIPATOR XSTR
A28R1	0698-3402	2	R FXD 316 OHM 1% 1/2W
A28R2	0757-1002	2	R FXD 61.9 OHM 1% 1/4W
A28R3	0698-3392	2	R FXD 23.7 OHM 1% 1/2W
	0698-5021	2	R FXD 35.7 OHM 1% 1/2W●
A28R4	1810-0150	4	R FXD NETWORK 4X50K
A28R5	0698-6635	2	R FXD 880 OHM 1% 1/8W
A28R6	0698-4462	2	R FXD 768 OHM 1% 1/8W
A28R7	2100-2574	3	R VAR 500 OHM 10% 1/2W
A28R8	0757-0416		R FXD 511 OHM 1% 1/8W
A28R8	0757-0416		R FXD 511 OHM 1% 1/8W
A28R9	0698-4125	2	R FXD 953 OHM 1% 1/8W
A28R10	2100-2521	2	R VAR 2K OHM 10% 1/2W LIN
A28R11	0757-0279		R FXD 3.16K OHM 1% 1/8W
A28R12	1810-0150		R FXD NETWORK 4X50K
A28R13	0698-4393	2	R FXD 73.2 OHM 1% 1/8W
A28R14	0698-5068	1	R FXD 50 OHM 1% 1/8W
	0757-0398		R FXD 75 OHM 1% 1/8W●
A28R15	0698-3151		R FXD 2.87K OHM 1% 1/8W
A28R16	0757-0280		R FXD 1K OHM 1% 1/8W
A28R17	0757-0280		R FXD 1K OHM 1% 1/8W
A28R18	0757-0280		R FXD 1K OHM 1% 1/8W
A28R19	0757-0280		R FXD 1K OHM 1% 1/8W
A28R20	0698-3395	4	R FXD 34.8 OHM 1% 1/4W
	0757-1000	4	R FXD 51.1 OHM 1% 1/2W●
A28R21	0698-3395		R FXD 34.8 OHM 1% 1/4W
	0757-1000		R FXD 51.1 OHM 1% 1/2W●

●OPTIONS 001/003

Abbreviations are listed in the introduction to this section

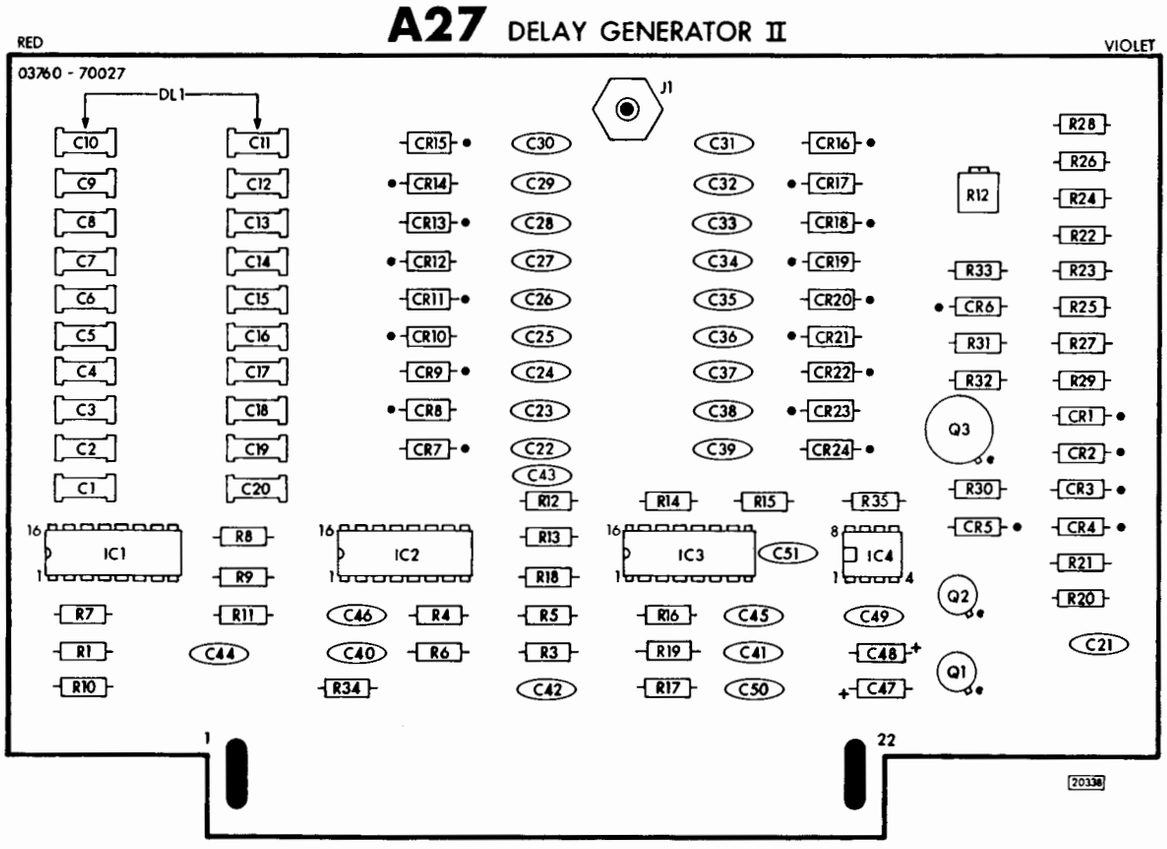

Figure A27-3 Component Location

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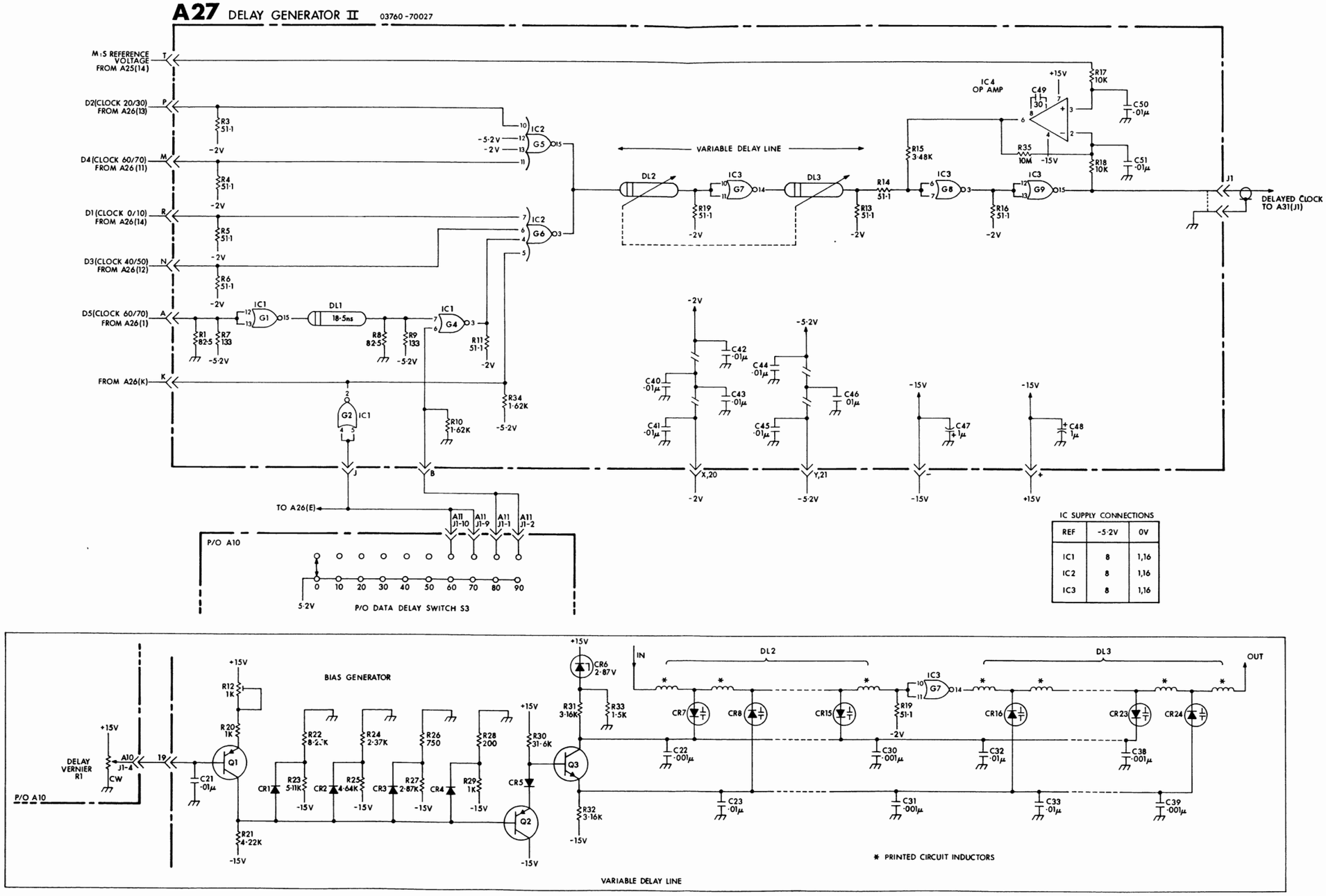


Figure A27-4 Schematic Diagram

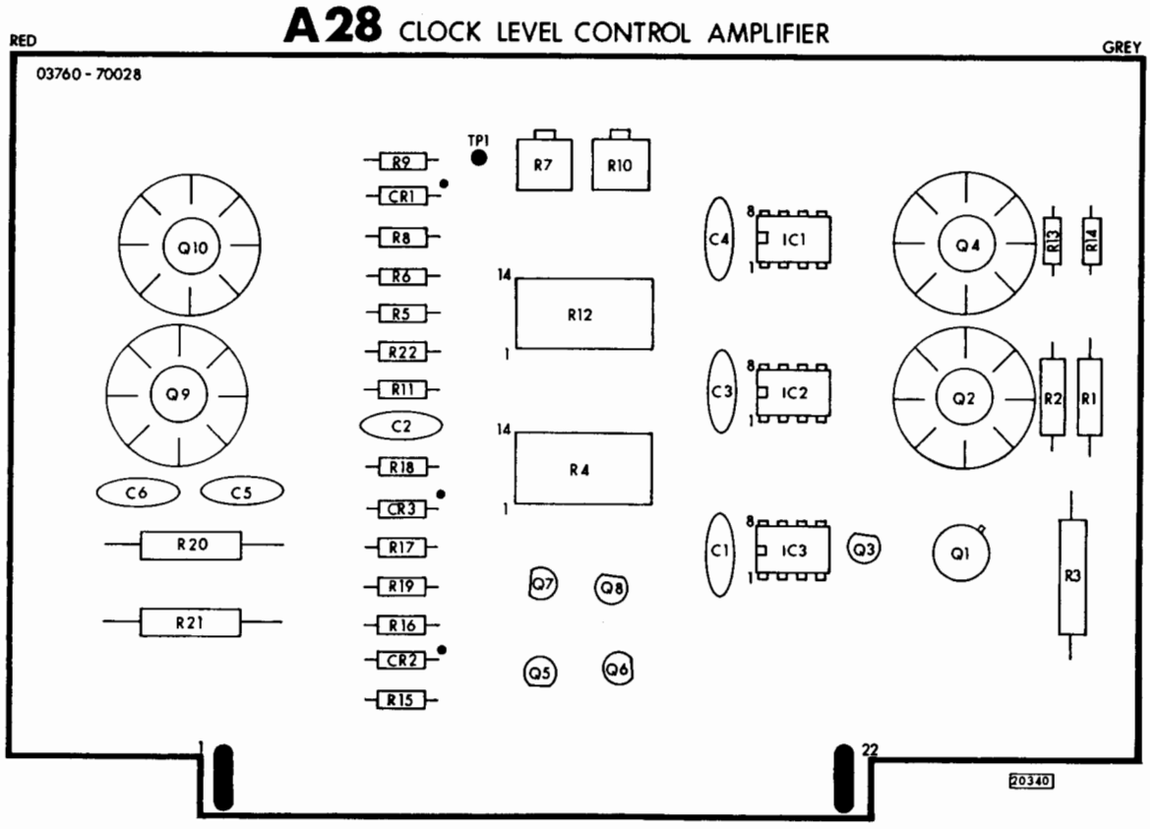
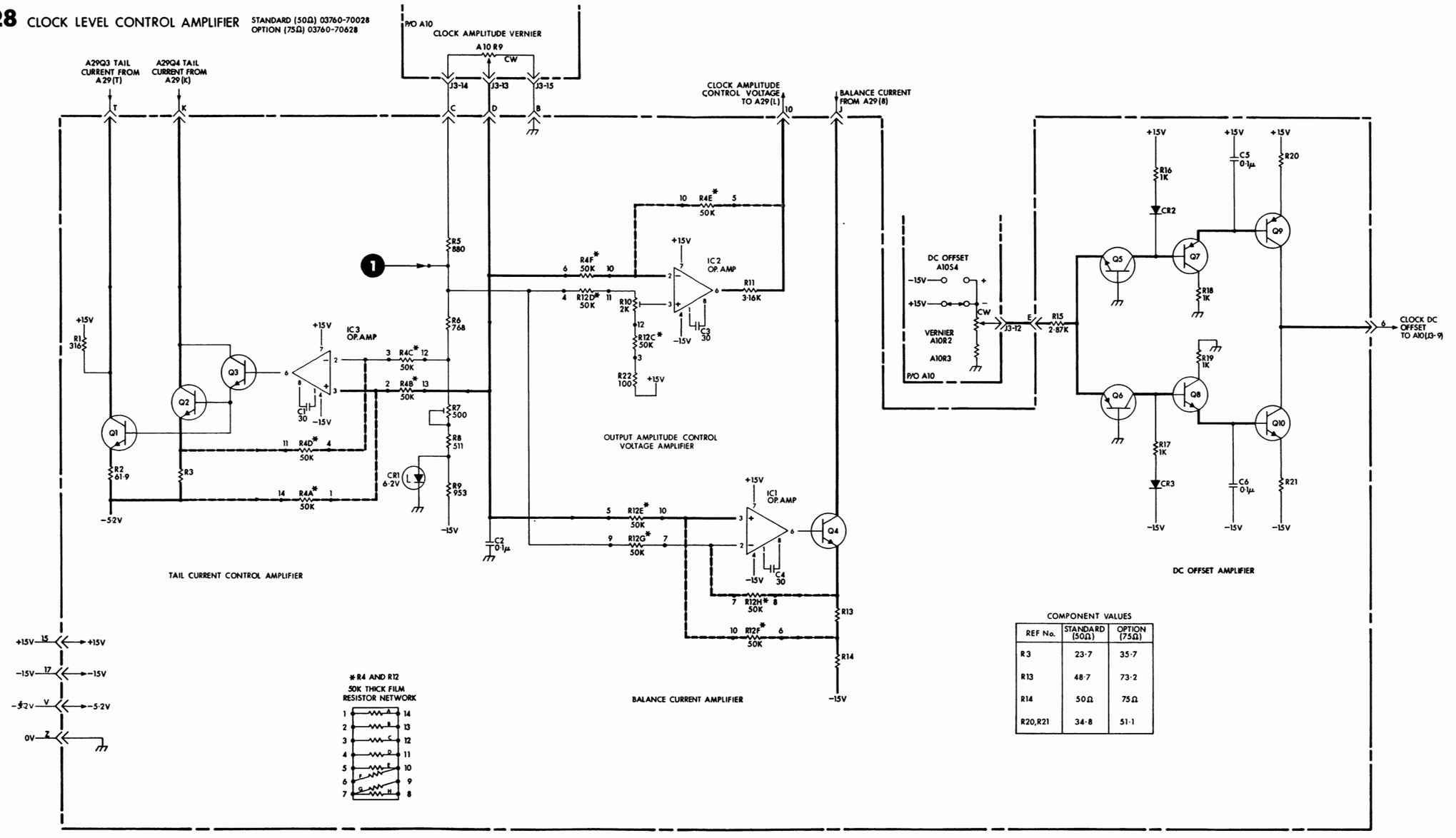


Figure A28-4 Component Location

A28 CLOCK LEVEL CONTROL AMPLIFIER

STANDARD (50Ω) 03760-70028
OPTION (75Ω) 03760-70628



COMPONENT VALUES

REF No.	STANDARD (50Ω)	OPTION (75Ω)
R3	23·7	35·7
R13	48·7	73·2
R14	50Ω	75Ω
R20,R21	34·8	51·1

Figure A28-5 Schematic Diagram

Replaceable Parts (continued)

Ref Desig	HP Part No	TQ	Description
A29R8	0757-0394		R FXD 51.1 OHM 1% 1/8W
A29R9	0757-0394		R FXD 51.1 OHM 1% 1/8W
A29R10	0757-0394		R FXD 51.1 OHM 1% 1/8W
A29R11	0757-0804	2	R FXD 200 OHM 1% 1/2W
A29R12	0757-0401		R FXD 100 OHM 1% 1/8W
A29R13	0698-4593	2	R FXD 464 OHM 1% 1/4W
A29R14	0757-0394		R FXD 51.1 OHM 1% 1/8W
A29R15	0757-0394		R FXD 51.1 OHM 1% 1/8W
A29R16	0757-0815	2	R FXD 562 OHM 1% 1/2W
A29R17	0757-0394		R FXD 51.1 OHM 1% 1/8W
A29R18	0757-0394		R FXD 51.1 OHM 1% 1/8W
A29R19	0757-0284		R FXD 150 OHM 1% 1/8W
A29R20	0757-0394		R FXD 51.1 OHM 1% 1/8W
A29R21	0757-0284		R FXD 150 OHM 1% 1/8W
A29R22	0757-0394		R FXD 51.1 OHM 1% 1/8W
A29R23	0757-0394		R FXD 51.1 OHM 1% 1/8W
A29R24	0757-1040	15	R FXD 50 OHM 1% 1/4W
A29R25	0757-0496	2	R FXD 20 OHM 1% 1/4W
	0757-1040		R FXD 50 OHM 1% 1/4W●
A29R26	0757-1040		R FXD 50 OHM 1% 1/4W
	0757-0710		R FXD 75 OHM 1% 1/4W●
A29R27	0757-1040		R FXD 50 OHM 1% 1/4W
	0757-0710		R FXD 75 OHM 1% 1/4W●
A29R28	0757-1040		R FXD 50 OHM 1% 1/4W
	0757-0710		R FXD 75 OHM 1% 1/4W●
A29R29	0757-1040		R FXD 50 OHM 1% 1/4W
A29R30	0757-0991		R FXD 20 OHM 1% 1/2W●
	0757-1040		R FXD 50 OHM 1% 1/4W
A29R31	0757-1040		R FXD 50 OHM 1% 1/4W
	0757-0710		R FXD 75 OHM 1% 1/4W●
A29R32	0757-0384	5	R FXD 20 OHM 1% 1/8W
A29R33	2100-1984	2	R VAR 100 OHM 10% 1/2W LIN
A29R34	0757-0178	7	R FXD 100 OHM 1% 1/4W
	0757-0715		R FXD 150 OHM 1% 1/4W●
A29R35	0757-0178		R FXD 100 OHM 1% 1/4W
	0757-0715		R FXD 150 OHM 1% 1/4W●
A29R36	0757-0280		R FXD 1K OHM 1% 1/8W
A29R37	0698-3404	1	R FXD 383 OHM 1% 1/2W
A29R38	0757-0178		R FXD 100 OHM 1% 1/4W
	0757-0715		R FXD 150 OHM 1% 1/4W●
A29R39	0757-0178		R FXD 100 OHM 1% 1/4W
	0757-0715		R FXD 150 OHM 1% 1/4W●
A29R40	0698-3154		R FXD 4.22K OHM 1% 1/8W
	0757-0439		R FXD 6.81K OHM 1% 1/8W●
A29R41	0698-3154		R FXD 4.22K OHM 1% 1/8W
	0757-0439		R FXD 6.81K OHM 1% 1/8W●
A29R42	0757-0399		R FXD 82.5 OHM 1% 1/8W
A29R43	0698-3132		R FXD 261 OHM 1% 1/8W
A29R44	0757-0384		R FXD 20 OHM 1% 1/8W
A29R45	0698-3444		R FXD 316 OHM 1% 1/8W
	0698-0082		R FXD 464 OHM 1% 1/8W●

●OPTIONS 001/003

Abbreviations are listed in the introduction to this section

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Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A29	03760-70029		CLOCK OUTPUT AMP ASSY
	03760-70629		CLOCK OUTPUT AMP ASSY OPTION 001/003
A29C1	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A29C2	0180-1745	1	C FXD 1.5UF 10% 20WVDC
A29C4	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A29C5	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A29C6	0160-2199		C FXD 30PF 5% 300WVDC
A29C7	0160-2266	1	C FXD 24PF 5% 500WVDC
A29C8	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A29C9	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A29C10	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A29C11	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A29C12	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A29C13	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A29C15	0150-0050		C FXD 1000PF +80-20% 1000WVDC
A29C17	0121-0046	2	C VAR 9-35PF
A29C20	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A29C23	0180-0228	1	C FXD 22UF 10% 15WVDC
A29CR1	1901-0047		DIO SI
A29CR3	1902-0048	2	DIO BKDN 6.81V 400MW
A29CR4	1901-0533		DIO SI
A29CR5	1901-0533		DIO SI
A29IC1	1820-0285		IC SCHMITT TRIGGER 250MHZ ECL
A29IC2	1820-0796		IC QUAD 2-INPUT NOR GATE ECL
A29J1	1250-1255		CONN COAX PC BD MTG CONHEX 50 OHM
	1250-0932		CONN COAX PC BD MTG CONHEX●
A29L5	9100-1645		INDUCTOR 390UH 5%
	9100-1653		IND FXD 910UH 5%●
A29L6	03760-70209		INDUCTOR ASSY
A29Q1	1854-0345		XSTR NPN SILICON
	1205-0037	4	HEAT DISSIPATOR XSTR
A29Q2	1854-0345		XSTR NPN SILICON
	1205-0037		HEAT DISSIPATOR XSTR
A29Q3	1858-0029	2	XSTR QUAD NPN SILICON
A29Q4	1858-0031	2	XSTR QUAD NPN SILICON
A29Q5	1853-0210		XSTR PNP SILICON
	03760-30200	3	HEAT DISSIPATOR XSTR
A29Q6	1854-0071		XSTR SI NPN
A29Q7	1853-0201	2	XSTR PNP SILICON
	03760-30200		HEAT DISSIPATOR XSTR
A29Q8	1853-0018		XSTR-PNP SILICON
A29R1	0757-0399		R FXD 82.5 OHM 1% 1/8W
A29R2	0698-3437		R FXD 133 OHM 1% 1/8W
A29R3	2100-2632	2	R VAR 100 OHM 10% 1/2W
A29R4	0698-4261	2	R FXD 2K OHM 5% 1/8W
A29R5	0757-0416		R FXD 511 OHM 1% 1/8W
A29R6	0698-3446		R FXD 383 OHM 1% 1/8W
A29R7	0698-3437		R FXD 133 OHM 1% 1/8W

●OPTIONS 001/003

Abbreviations are listed in the introduction to this section

BALANCE CURRENT

If no current were passed through the load by the Level Control Amplfiier, the output would switch between 0V when Q7 was off and a positive voltage when it was conducting, ie, the output would have a positive offset equal to half the amplitude of the output pulses as shown in Figure A29-1. To achieve zero dc offset, a negative "balance" current equal to half that being switched by Q7 is passed through the load via L5. Thus when Q7 is turned off, this current generates a negative voltage across the load equal to half the peak to peak value of the output pulse. When Q7 turns on, the current in the load reverses and an equal value positive voltage is developed across the load as shown in Figure A29-1.

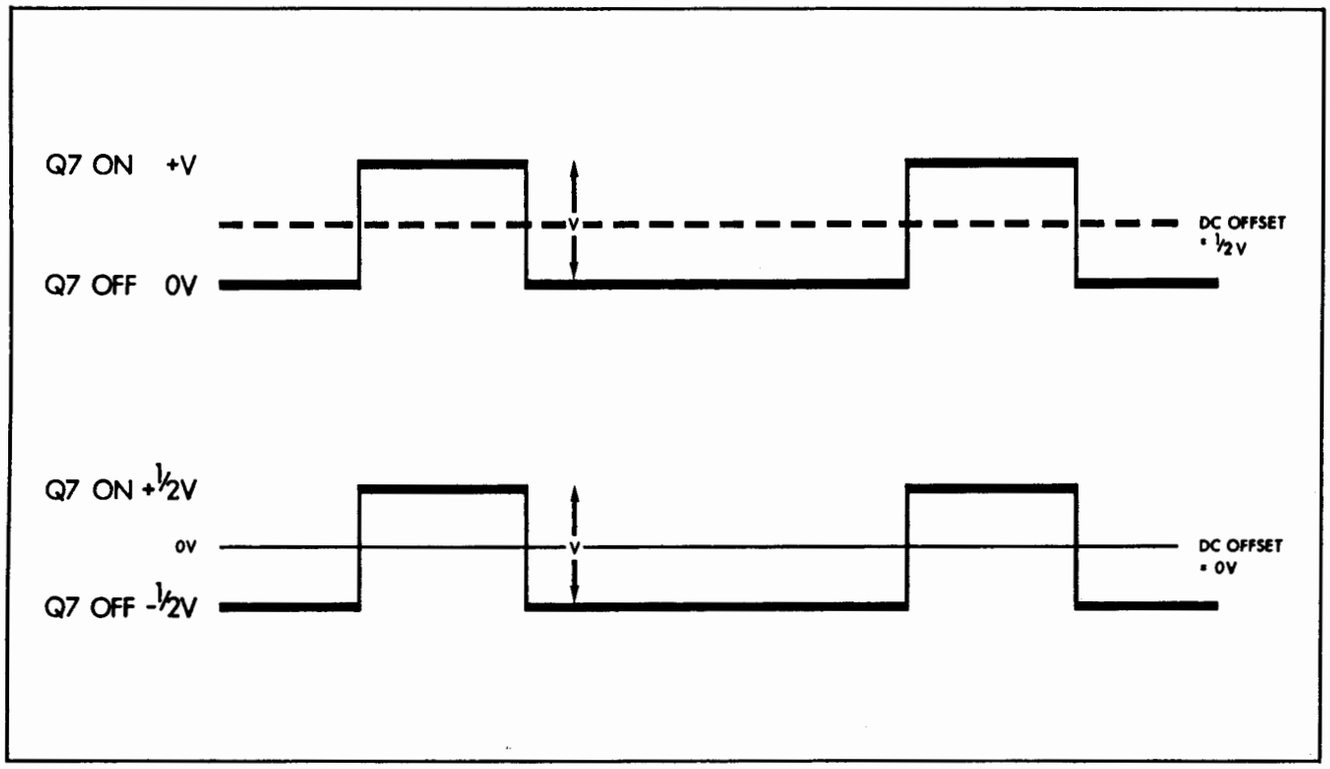

Figure A29-1 Balance Current

OVERSHOOT

Due to the fast switching action of the emitter coupled pairs a certain amount of overshoot is introduced into the switching signal. This overshoot, which appears on the output, is proportional to the amount of current being switched and to the speed at which it it switched. A small percentage overshoot ensures fast rise time pulses, however if the tail currents of the emitter coupled pairs were held constant, the amplitude of the overshoot would also remain constant and become increasingly more significant as the output amplitude was reduced. To keep the percentage overshoot approximately constant over the output amplitude range, the tail currents of the second and third emitter coupled pairs are reduced as the output amplitude is reduced. The amount of overshoot present on the output can be adjusted by C17.

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ASSEMBLY SERVICE SHEET A29

CLOCK AMPLIFIER A29

INPUT LOGIC

The output logic selection, CLOCK or $\overline{\text{CLOCK}}$ is made in the input logic of this amplifier. In the CLOCK mode the input signal, logically equal to $\overline{\text{CLOCK}}$, drives Q8 via G2 while in $\overline{\text{CLOCK}}$ it drives Q8 via G1 and G4. The dc offset of the signal applied to G4 can be altered by R42 thus allowing the mark to space ratio of the CLOCK signal to be adjusted.

The output levels of the MECL III gates G2 and G4 (-0.8V and -1.7V) are modified by the level translator Q8 to make them compatible with the logic levels of the EECL schmitt trigger (0 and -0.5V). The small variation in these levels provided by R3 allows the mark to space ratio of the input clock signal to be accurately reproduced at the output.

CURRENT AMPLIFIERS

Three cascaded emitter coupled pairs provide the current amplification required to switch the output transistor. Printed circuit inductors in series with the resistive loads of the schmitt trigger and the first emitter coupled pair counteract the "rounding-off" effect which the capacitive inputs of the following stages have on the switching signal. Two transistors in parallel are required for each side of the second and third emitter coupled pairs to switch the high currents associated with these stages. The tail currents of Q3 and Q4 are varied in proportion to the amplitude of the output by the Clock Level Control Amplifier, the reason for this is discussed later.

When Q4C and Q4D are switched on, their collector voltages lie between +12V and +10.2V depending upon the setting of the output AMPLITUDE VERNIER. As the corresponding range of voltage applied to the base of the output transistor Q7 is +13.4V to +11.8V, it is always reverse biased when Q4C and Q4D are conducting. When this side of the emitter coupled pair turns off, Q7 becomes forward biased, its collector current being determined by the voltage applied to its base and varies between 64mA at minimum output and 128mA at maximum output. As the collector load of Q7 is effectively 25Ω (R38 and R39) in parallel with the input impedance of the Attenuator) the output amplitude varies between a minimum of 1.6V pk-pk and a maximum of 3.2V pk-pk. To equalise the loading on each side of the third emitter coupled pair, Q4A and Q4B drive a dummy output stage, Q5.

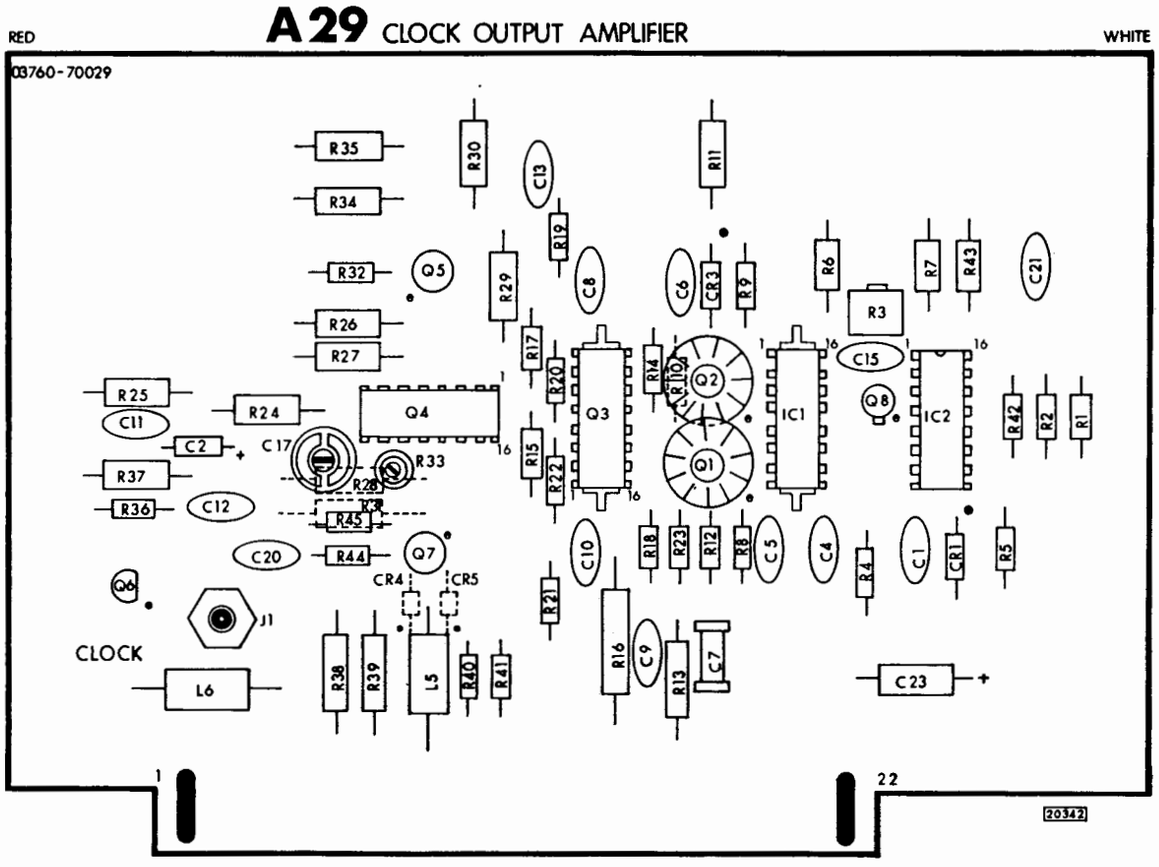
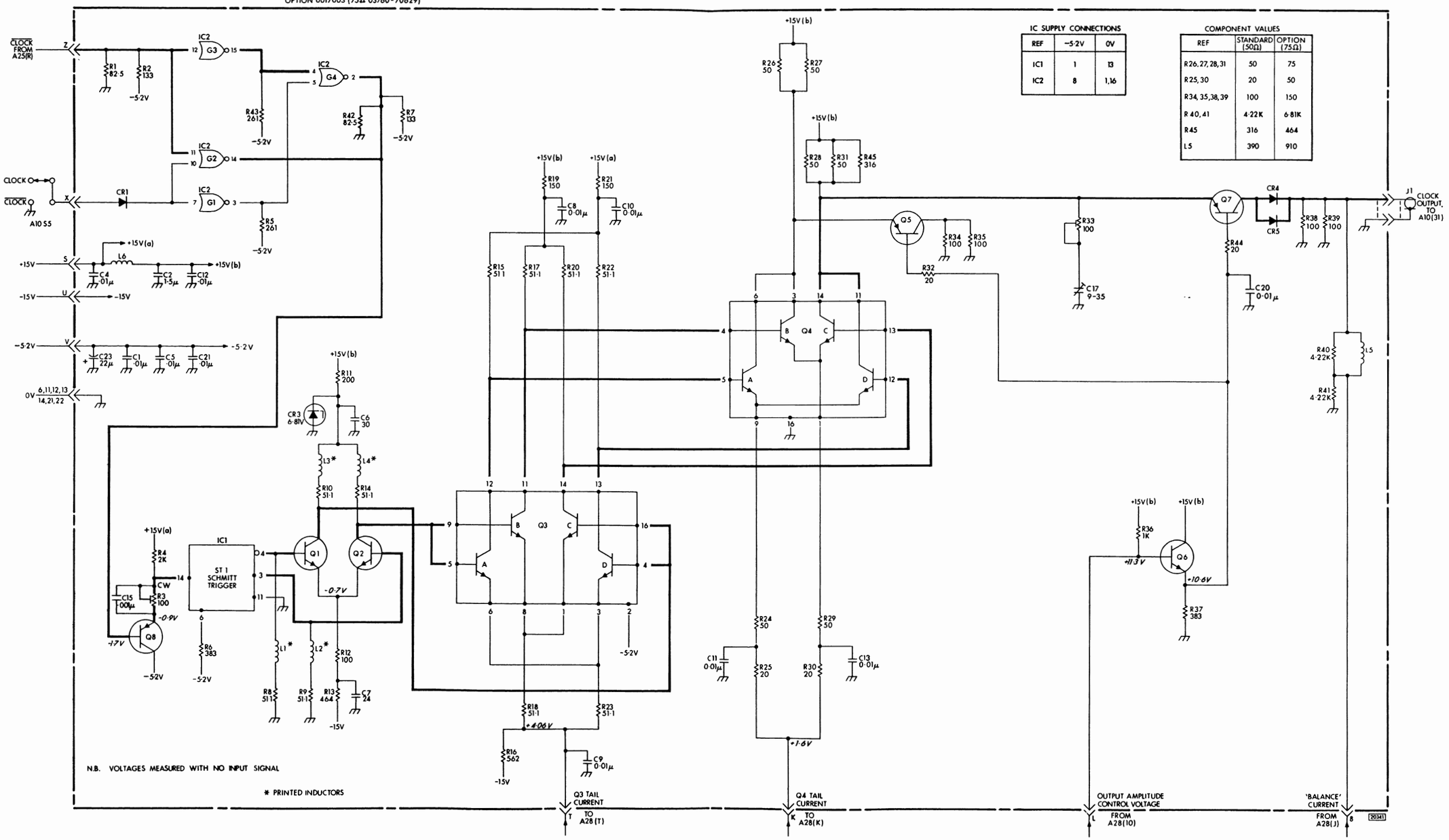


Figure A29-2 Component Location

A29 CLOCK OUTPUT AMPLIFIER

STANDARD (50Ω) 03760-70029
OPTION 001/003 (75Ω 03760-70629)



IC SUPPLY CONNECTIONS

REF	-5·2V	0V
IC1	1	13
IC2	8	1,16

COMPONENT VALUES

REF	STANDARD (50Ω)	OPTION (75Ω)
R26, 27, 28, 31	50	75
R25, 30	20	50
R34, 35, 38, 39	100	150
R 40, 41	4·22K	6·81K
R45	316	464
L5	390	910

Figure A29-3 Schematic Diagram

Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A31	03760-70031		ZERO ADD COUNTER ASSY
A31C1	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A31C2	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A31C3	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A31C4	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A31C5	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A31C5	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A31C6	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A31C7	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A31C8	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A31C9	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A31C10	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A31IC1	1820-0803	3	IC 2-3-Z-INPUT OR/NOR GATE ECL
A31IC2	1820-0817	8	IC DUAL D M/S FLIP FLOP ECL
A31IC3	1820-0817		IC DUAL D M/S FLIP FLOP ECL
A31IC4	1820-0801	2	IC QUAD 2-INPUT DR/NOR GATE
A31IC5	1820-0817		IC DUAL D M/S FLIP FLOP ECL
A31IC6	1820-0803		IC 2-3-Z-INPUT OR/NOR GATE ECL
A31IC7	1820-0794	26	IC MASTER-SLAVE FLIP FLOP ECL
A31IC8	1820-0817		IC DUAL D M/S FLIP FLOP ECL
A31IC9	1820-0796		IC QUAD 2-INPUT NOR GATE ECL
A31IC10	1820-0795	2	IC QUAD 2-INPUT OR GATE ECL
A31IC11	1820-0801		IC QUAD 2-INPUT DR/NOR GATE
A31IC12	1820-0794		IC MASTER-SLAVE FLIP FLOP ECL
A31IC13	1820-0795		IC QUAD 2-INPUT OR GATE ECL
A31J1	1250-1255		CONN COAX PC BD MTG CONHEX 50 OHM
A31R1	0698-3437		R FXD 133 OHM 1% 1/8W
A31R2	0698-3437		R FXD 133 OHM 1% 1/8W
A31R3	0698-3437		R FXD 133 OHM 1% 1/8W
A31R4	0757-0399		R FXD 82.5 OHM 1% 1/8W
A31R5	0757-0399		R FXD 82.5 OHM 1% 1/8W
A31R6 *TO* A31R25	0698-3132		R FXD 261 OHM 1% 1/8W
A31R26	0698-3132		R FXD 261 OHM 1% 1/8W
A31R27	0757-0416		R FXD 511 OHM 1% 1/8W
A31R28	0757-0416		R FXD 511 OHM 1% 1/8W
A31R29	0757-0416		R FXD 511 OHM 1% 1/8W
A31R30	0757-0416		R FXD 511 OHM 1% 1/8W
A31R31	0757-0416		R FXD 511 OHM 1% 1/8W
A31R32	0757-0416		R FXD 511 OHM 1% 1/8W
A31R33	0757-0416		R FXD 511 OHM 1% 1/8W
A31R34	0757-0416		R FXD 511 OHM 1% 1/8W
A31R35	0757-0416		R FXD 511 OHM 1% 1/8W
A31R36	0698-3132		R FXD 261 OHM 1% 1/8W
A31R37	0757-0416		R FXD 511 OHM 1% 1/8W
A31R38	0757-0416		R FXD 511 OHM 1% 1/8W
A31R39	0757-0200	1	R FXD 5.62K OHM 1% 1/8W
A31R40	0757-0399		R FXD 82.5 OHM 1% 1/8W

Abbreviations are listed in the introduction to this section

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When the counter reaches the 08 state, the 1/f divider is at zero and Q6, Q8 and Q9 are all 0, G21 therefore drives G14 with a 0. At 04, Q3 changes to 0 and the output of G14 switches to 1 and inhibits the end detection gate, G7. At 02, $\overline{Q4}$ changes to 1 and inhibits the end detection gate G9. At 01, Q2 changes to 1 and inhibits the last end detection gate G8. the wired-OR output of G7, G8 and G9 therefore changes to 0 enabling FF1. The next clock pulse clocks FF1 and since the sync input is low, Q1 switches to 0 and ends the zero block. This last clock pulse also registers in the h/f divider reducing its count to zero before G10 is inhibited by $\overline{Q1}$. The programing gates are now enabled and the counter is re-programed ready for the next zero block.

From the previous explanation it can be seen that for the zero block to end when the counter reaches zero, the Sync Input must be low. To ensure that this happens, the Zero Add signal is also used to reset the sync to 0 in the Binary Sequence Generator. In WORD modes when a new word is being loaded by the Word Content Programer, it is necessary to prevent the Binary Sequence Generator from being clocked. This is achieved by driving G1 with a 0 to set FF1 thus causing the Zero Block output to go high and inhibit the clock signals in the Binary Sequence Generator.

PROGRAMING

As mentioned previously, the appropriate number of clock pulses to be counted are initially programed into the counter. This programing can be illustrated by considering the example 25.

At the end of the zero block, the programing gates are enabled by Q1 via G11. As can be seen from Figure A31-5 with the ZERO ADD switch set to 5, the input to G15 is 1 and the Reset input to FF3 is held at 0, Q3 therefore remains in its count 0 state, ie, at 1. The inputs to G12, G16 and G18 are 0 and hence the Q outputs of FF2, FF4 and FF5 are set to 1. The high frequency divider has therefore been programed to the count 5 state, ie, 1111. The low frequency divider is programed in a similar manner into the count 2 state, 0001. When a sync pulse arrives at the input, it inhibits the programing gates via G11 and they remain inhibited by Q1 during the zero block.

UNITS	1	2	A	B
0	1	1	1	1
1	0	0	1	0
2	1	0	1	0
3	0	0	0	0
4	1	0	0	0
5	0	1	0	0
6	1	1	0	0
7	0	1	0	1
8	1	1	0	1
9	0	1	1	0

TENS	D	E	F	H
0	1	1	1	1
1	0	0	1	0
2	1	0	1	0
3	0	0	0	0
4	1	0	0	0
5	0	1	0	0
6	1	1	0	0
7	0	1	0	1
8	1	1	0	1
9	0	1	1	0

Figure A31-5 Programing Inputs

OVERALL OPERATION

When no zero block is being generated in ZERO ADD, the programing gates are enabled since the Q output of FF1 is 0. Also since the end detection gates G7, G8 and G9 are inhibited by $\overline{Q1}$ the Set input to FF1 is held at 0.

When the Sync Input goes high, the programing gates are inhibited leaving the counter programed to the required count. With the Sync high, the next clock pulse causes FF1 to change state. The Zero Block Output therefore switches to 1 and inhibits the data stream in the Data Processor. This signal also inhibits the clock signals in the Binary Sequence Generator and ensures that the sync is reset to 0. Simultaneously, the end detection gates are enabled by Q1 and if the counter is not at 01, the output of these gates changes to 1 to hold FF1 in the set condition for the duration of the zero block.

S6

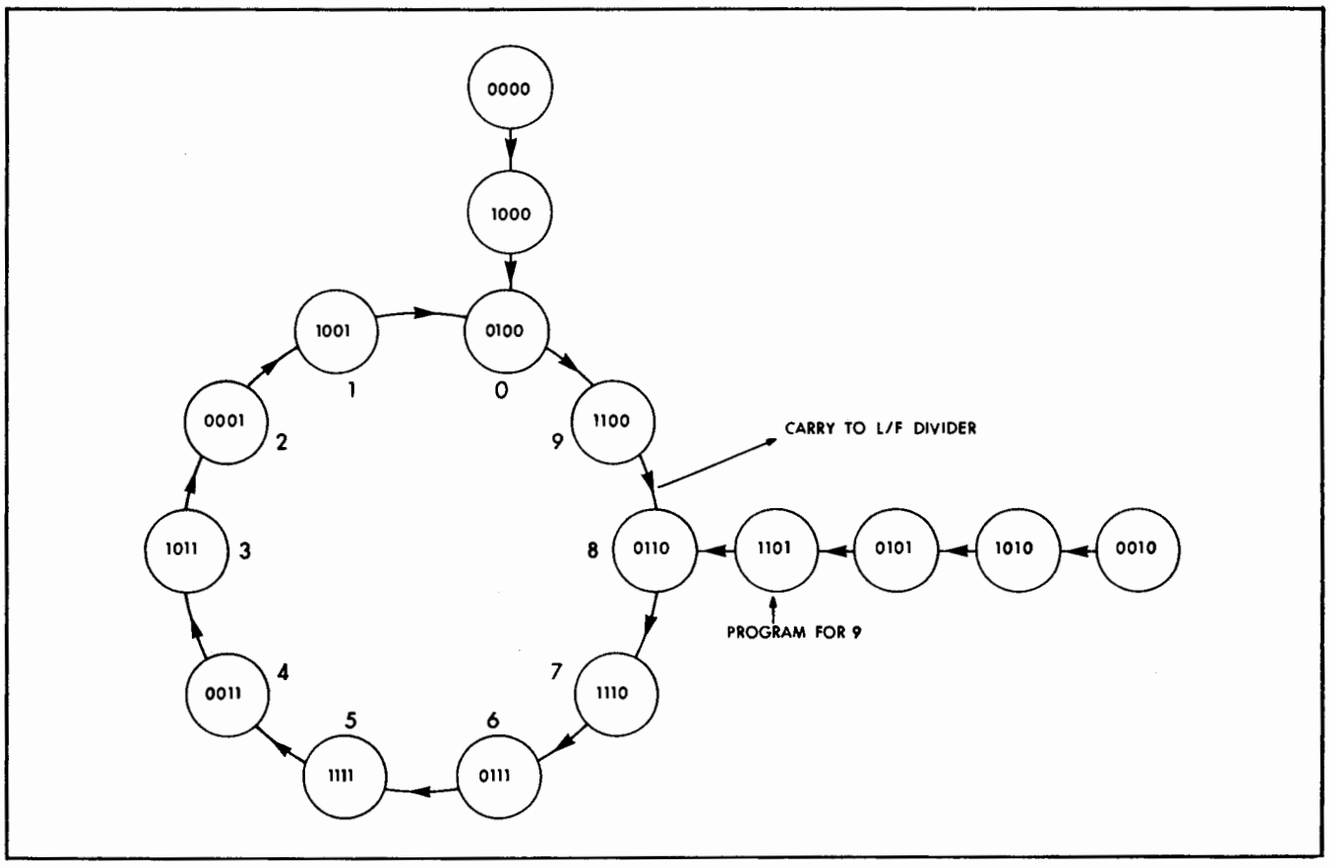
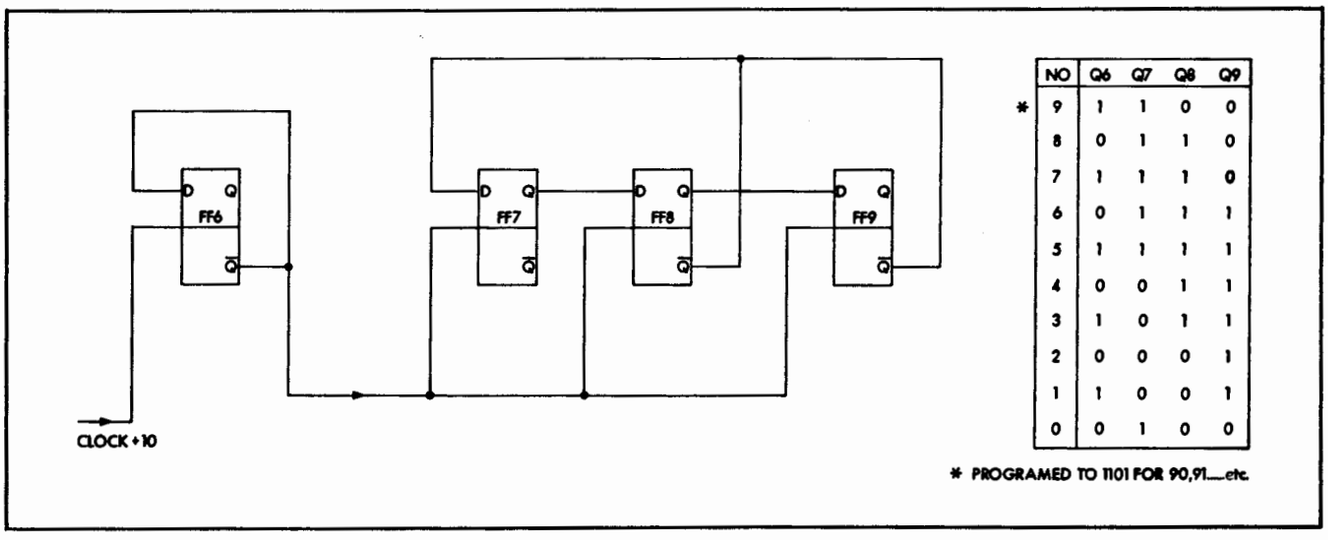


Figure A31-3 State Diagram

The low frequency divider consists of a ÷2 stage, FF6, which clocks a synchronous ÷5 stage, the truth table of which is shown in Figure A31-4 and is identical to that of the h/f divider. When this divider reaches count zero, Q6, Q8 and Q9 are all 0 and the $\overline{Q}$ output of G21 inhibits G19 and G20 holding the clock input to FF6 at 1 to prevent further clocking of this stage.



	NO	Q6	Q7	Q8	Q9
*	9	1	1	0	0
	8	0	1	1	0
	7	1	1	1	0
	6	0	1	1	1
	5	1	1	1	1
	4	0	0	1	1
	3	1	0	1	1
	2	0	0	0	1
	1	1	0	0	1
	0	0	1	0	0

* PROGRAMED TO 1101 FOR 90,91....etc.

Figure A31-4 Low Frequency Divider

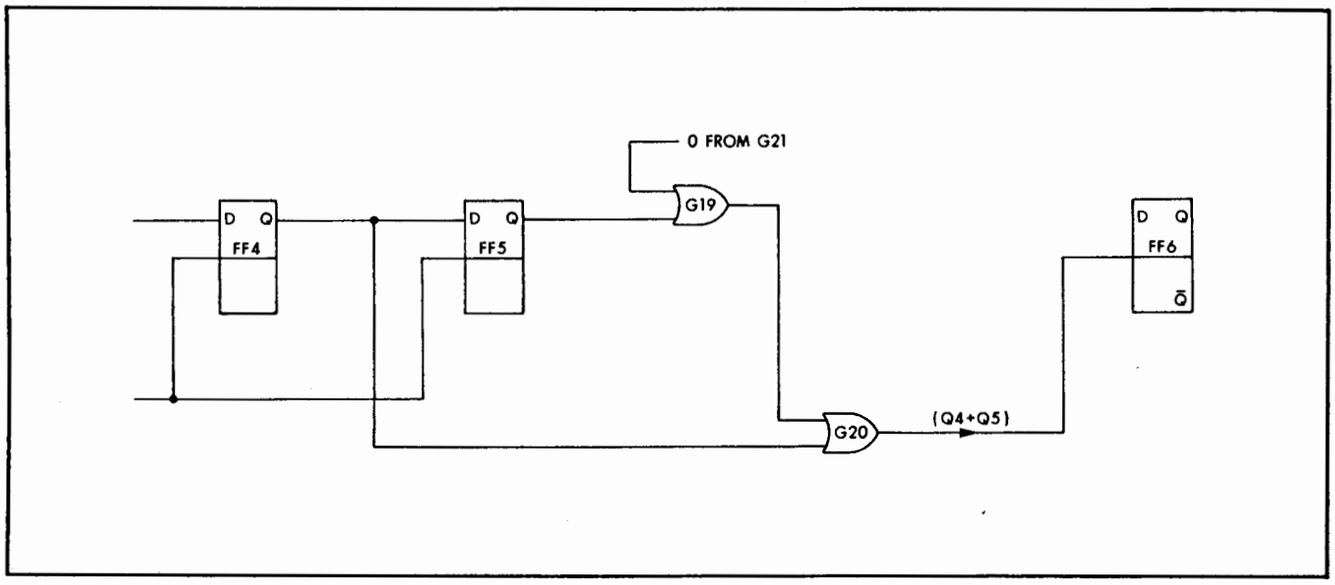


Figure A31-2 L/F Clock Signal

A carry input to the low frequency divider logically equal to (Q4 + Q5), is produced at the output of G20. Reference to the truth table given in Figure A31-1 shows that at count 0 and 9, Q4 and Q5 are both 0 and hence the output of G20 is also 0. When the h/f divider changes from 9 to 8, Q4 switches to 1 and G20 clocks the l/f divider, reducing the count stored in it by one.

When the h/f divider is cycling normally, the state corresponding to 9 is 1100. If the program for 9 also set up this state, the l/f divider would be falsely clocked when the count first changed from 9 to 8. To prevent this, the programing for 9 sets up the state 1101 in the divider. As can be seen from the State Diagram in Figure A31-3, the first clock pulse changes the count to 8 (0110) as normal but no carry input to the l/f divider is generated as one input to G20 is always 1. If G20 were connected directly to Q5, a spike could be produced on the l/f clocking line during the transition from 9 to 8 (this would occur if Q4 changed faster than Q5). To prevent this the output of Q5 is delayed by G19 to ensure that Q4 has completely changed from 0 to 1 before the 1 to 0 change at Q5 reaches G20.

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ASSEMBLY SERVICE SHEET A31

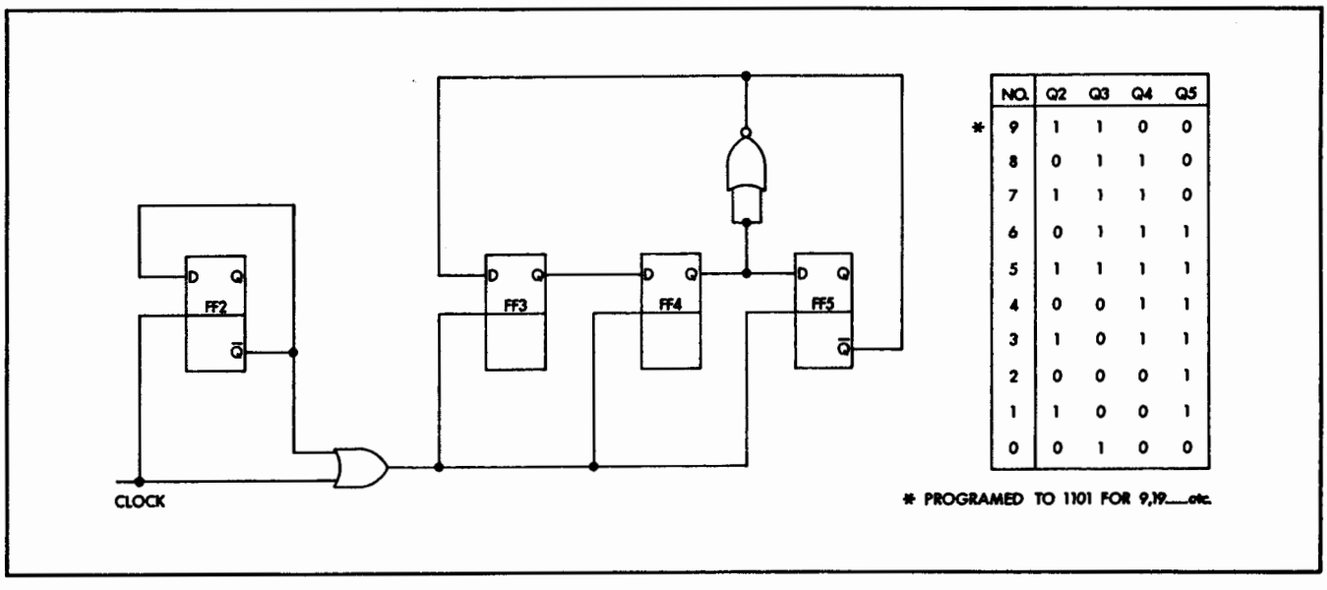
ZERO ADD COUNTER A31

INTRODUCTION

When triggered by a sync pulse, the Zero Add Counter inhibits the data stream in the Data Processor to hold the Data Output at 0. It also stops the Binary Sequence Generator by inhibiting its clock signals (Clock I & II) thus ensuring that no part of the sequence being generated is lost during the zero block. The number of zeros added to the data stream is controlled by a clock pulse counter which is programed by front panel selector switches. When the required number of clock pulses have registered in this counter, the Binary Sequence Generator is enabled again and the sequence continues from the point at which it was stopped. To simplify decoding the number of clock pulses to be counted is initially programed into the counter which then counts down to zero. For example if 25 zeros are to be inserted, the counter is initially programed to 25 and then allowed to count down to 00. The delays experienced by the sync pulse and data streams while being processed in the various circuits in the instrument have been adjusted so that in WORD, the zero block is added to the data stream between words.

CLOCK PULSE COUNTER

The Clock Pulse Counter consists of two decade dividers in series. The first, a high frequency divider consists of a divide by two stage, FF2, followed by a synchronous divide by five stage, FF3, FF4 and FF5. The truth table and simplified circuit diagram of this divider is shown in Figure A31-1.



	NO.	Q2	Q3	Q4	Q5
*	9	1	1	0	0
	8	0	1	1	0
	7	1	1	1	0
	6	0	1	1	1
	5	1	1	1	1
	4	0	0	1	1
	3	1	0	1	1
	2	0	0	0	1
	1	1	0	0	1
	0	0	1	0	0

* PROGRAMED TO 1101 FOR 9,19....etc.

Figure A31-1 H/F Divider

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ASSEMBLY SERVICE SHEET A30

DATA
MOTHERBOARD A30

INTRODUCTION The Data Motherboard A30 forms the base of the Data Module A3 and carries the plug-in assemblies, A31, A32, A33, A34, A35, A37, A38, A39.

Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A30	03760-70030		DATA MODULE MOTHER BOARD ASSY
A30C1	0180-0098		C FXD 100UF 20% 20WVDC
A30C2	0180-1714		C FXD 330UF 10% 6WVDC
A30C3	0180-1714		C FXD 330UF 10% 6WVDC
A30C4	0180-0098		C FXD 100UF 20% 20WVDC
A30J1	1200-0767		SOCKET INTEG CIRCUIT DUAL INLINE
A30J2	1200-0767		SOCKET INTEG CIRCUIT DUAL INLINE
A30J3	1200-0767		SOCKET INTEG CIRCUIT DUAL INLINE
A30J4	1250-1255		CONN COAX PC BD MTG CONHEX 50 OHM
A30XA1	1251-1365		CONN-PC 44 RIB CONT
A30XA2	1251-1365		CONN-PC 44 RIB CONT
A30XA3	1251-1365		CONN-PC 44 RIB CONT
A30XA4	1251-1365		CONN-PC 44 RIB CONT
A30XA5	1251-1365		CONN-PC 44 RIB CONT
A30XA6	1251-1365		CONN-PC 44 RIB CONT
A30XA7	1251-1365		CONN-PC 44 RIB CONT
A30XA8	1251-1365		CONN-PC 44 RIB CONT
A30XA9	1251-1365		CONN-PC 44 RIB CONT

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Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A3	03760-70030	2	DATA MODULE MOTHER BOARD ASSY
	03760-70031	2	ZERO ADD COUNTER ASSY
	03760-70032	2	BINARY SEQUENCE GENERATOR ASSY 1
	03760-70033	2	BINARY SEQUENCE GENERATOR ASSY 2
	03760-70034	2	WORD CONTENT PROGRAMER ASSY
	03760-70035	2	SEQUENCE LENGTH PROGRAMER ASSY
	03760-70037	2	DATA PROCESSOR/SYNC OUTPUT AMP ASSY
	03760-70038	2	DATA LEVEL CONTROL AMP ASSY
	03760-70638	2	DATA LEVEL CONTROL AMP ASSY OPT 001/3
	03760-70039	2	DATA OUTPUT AMP ASSY
	03760-70639	2	DATA OUTPUT AMP ASSY OPTION 001/003
A3MP30	03760-70300	1	DATA MODULE CHASSIS
A3MP31	03760-10306	1	CLAMP CONNECTOR
A3MP32	03760-10307	1	SPACER
A3W1	03760-70063		CABLE ASSY DC POWER

Abbreviations are listed in the introduction to this section

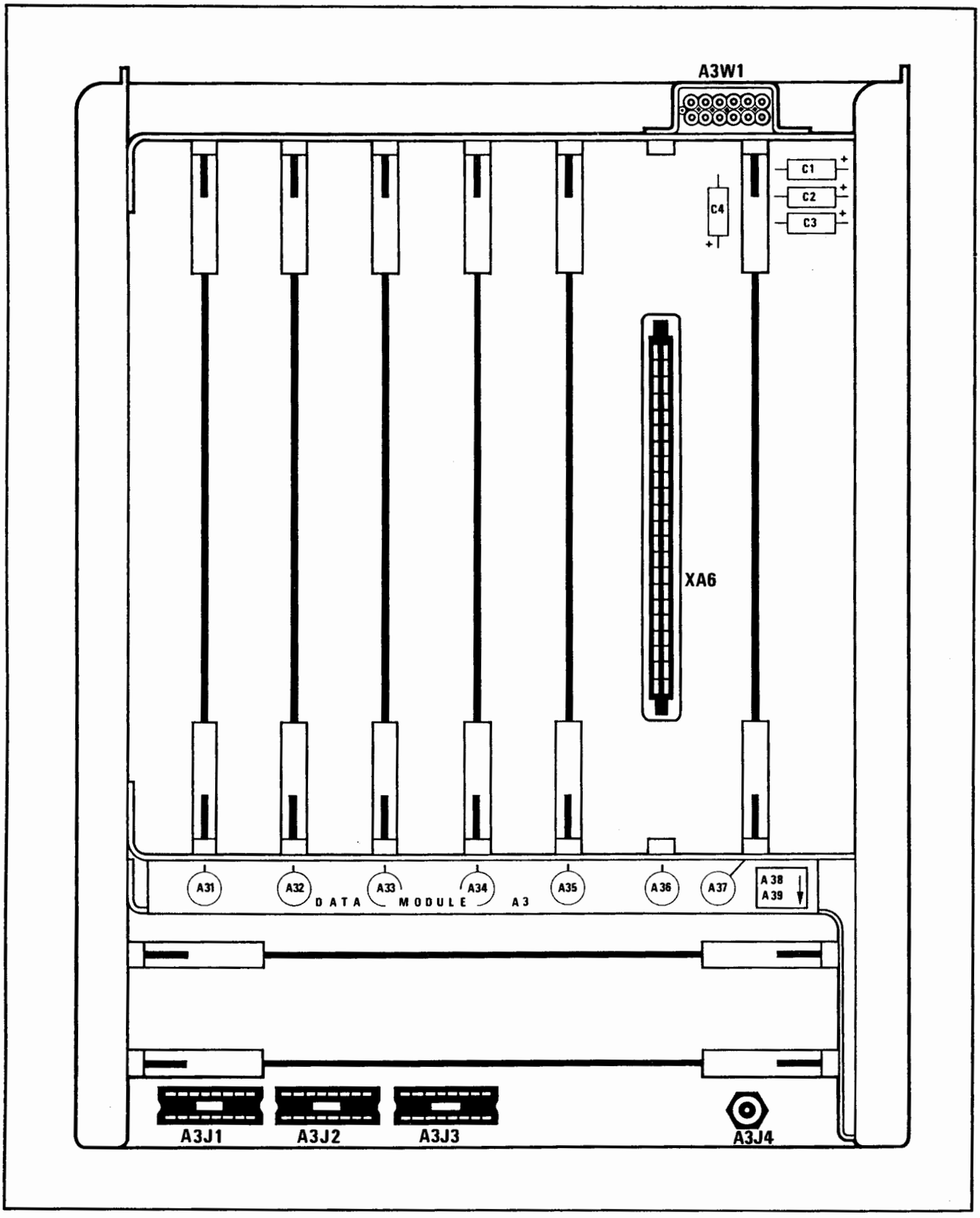

Figure A3-1 Component Location

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MODULE SERVICE SHEET A3

DATA MODULE A3

INTRODUCTION

The Data Module consists of the following assemblies:

(i) Zero Add Counter A31.

(ii) Binary Sequence Generator I A32.

(iii) Binary Sequence Generator II A33.

(iv) Word Content Programer A34.

(v) Sequence Length Programer A35.

(vi) Data Processor/Sync Output Amplifier A37.

(vii) Data Level Control Amplifier A38.

(viii) Data Output Amplifier A39.

MECHANICAL CONSTRUCTION

To remove the Data Module A3 from the instrument proceed as follows:

(i) Remove top and bottom covers.

(ii) Remove module screen by turning the quick release catches.

(iii) Remove the two screws holding the Data Mother Board A30 to the mainframe (underside).

(iv) Remove all cables and lift the module out of the instrument.

The Data Motherboard is separated from the module by removing the six screws attaching it to the metalwork.

Data Module A3

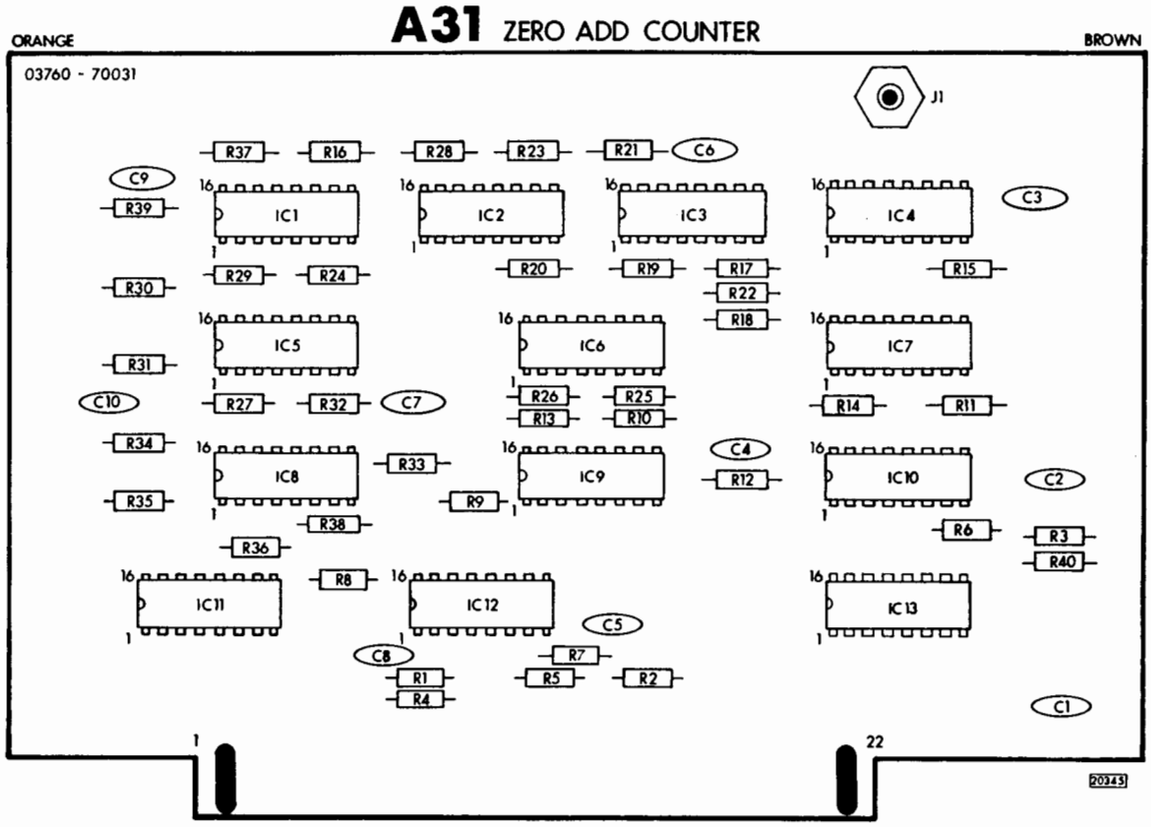

Figure A31-8 Component Location

UNITS	1	2	A	B
0	1	1	1	1
1	0	0	1	0
2	1	0	1	0
3	0	0	0	0
4	1	0	0	0
5	0	1	0	0
6	1	1	0	0
7	0	1	0	1
8	1	1	0	1
9	0	1	1	0

TENS	D	E	F	H
0	1	1	1	1
I	1	0	1	0
2	1	0	1	0
3	0	0	0	0
4	1	0	0	0
5	0	1	0	0
6	1	1	0	0
7	0	1	0	1
8	1	1	0	1
9	0	1	1	0

NOTE

THESE TABLES SHOW THE STATES OF THE PROGRAMING LINES AND NOT THE COUNTER STATES

Figure A31-9 Programing Inputs

A31 ZERO ADD COUNTER - SHEET 2 03760-70031

NOTE: FOR POWER SUPPLY CONNECTIONS SEE PAGE 6-8

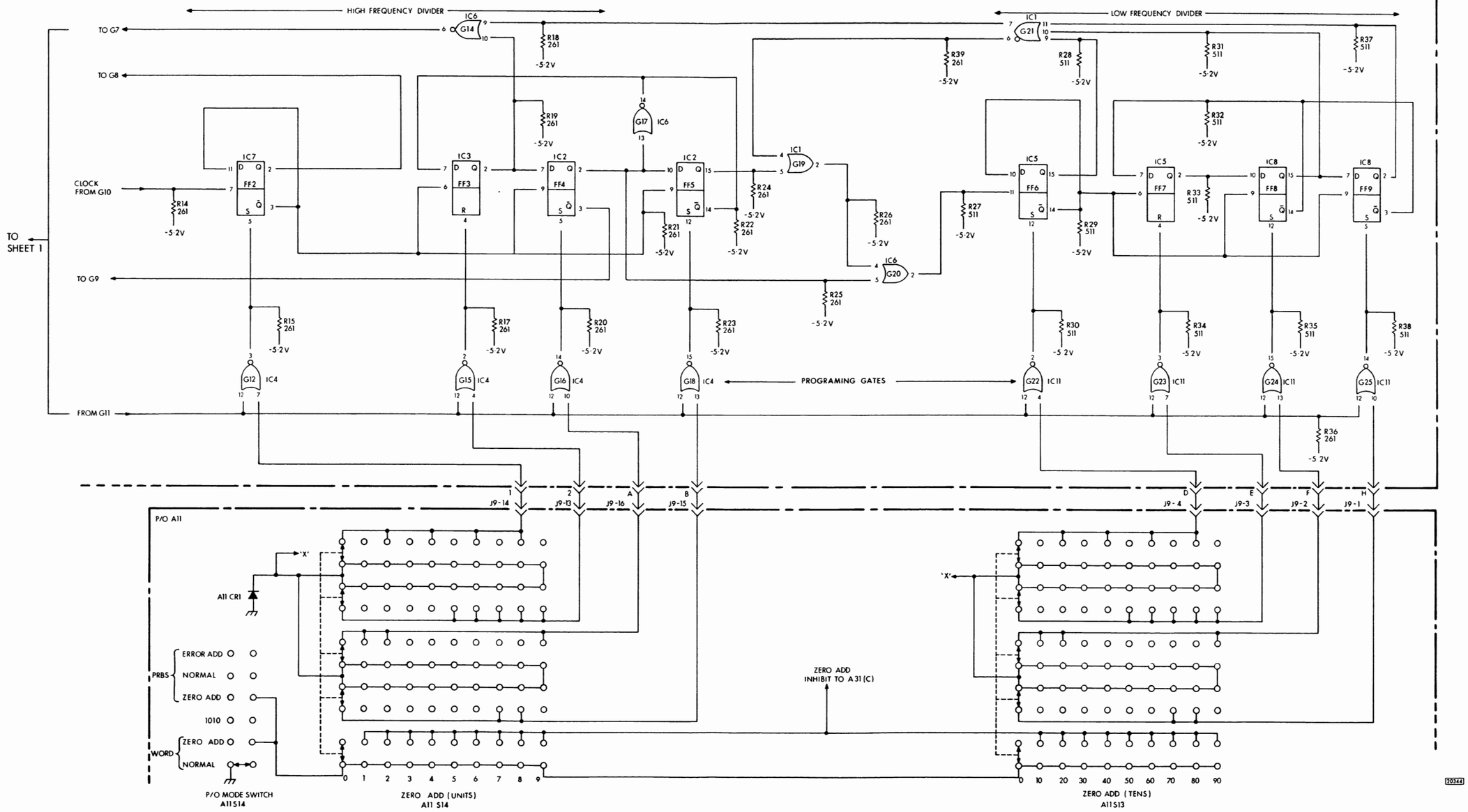

Figure A31-10 Schematic Diagram Sheet 2

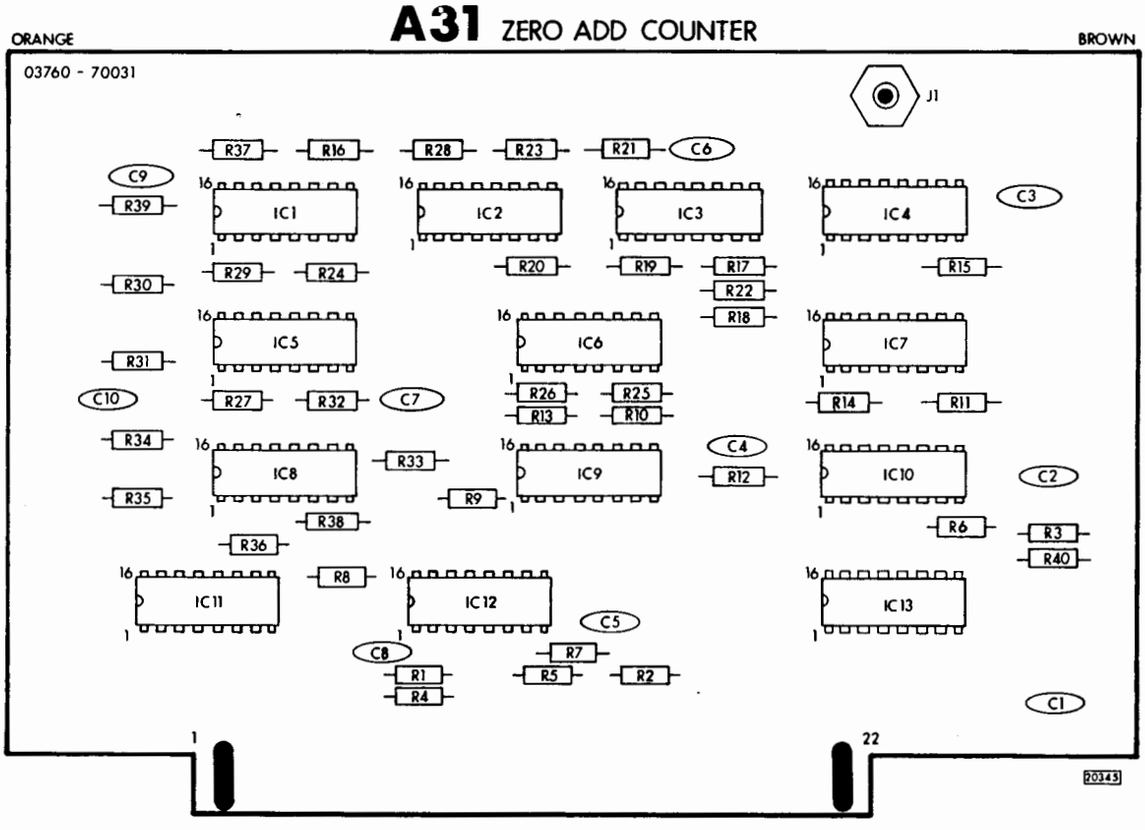

Figure A31-6 Component Location

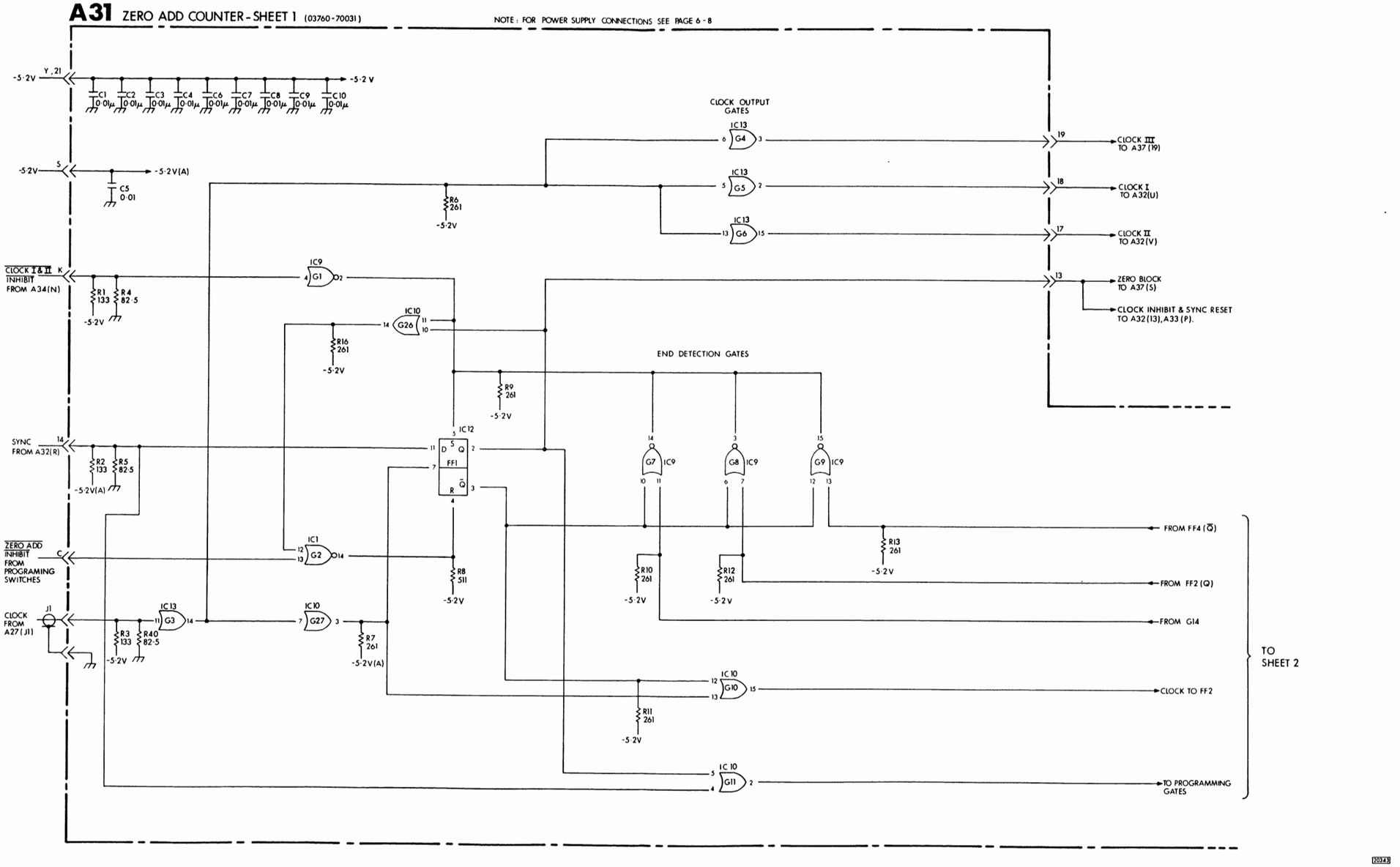

Figure A31-7 Schematic Diagram Sheet 1

Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A32	03760-70032		BINARY SEQUENCE GENERATOR ASSY 1
A32C2	0160-0640	1	C FXD 10PF 5% 30WVDC
A32IC1	1820-0796		IC QUAD 2-INPUT NOR GATE ECL
A32IC2	1820-0794		IC MASTER-SLAVE FLIP FLOP ECL
A32IC3	1820-0794		IC MASTER-SLAVE FLIP FLOP ECL
A32IC4	1820-0794		IC MASTER-SLAVE FLIP FLOP ECL
A32IC5	1820-0794		IC MASTER-SLAVE FLIP FLOP ECL
A32IC6	1820-0793	4	IC TRIPLE 2-INPUT EXCLUSIVE NOR GATE
A32IC7	1820-0794		IC MASTER-SLAVE FLIP FLOP ECL
A32IC8	1820-0796		IC QUAD 2-INPUT NOR GATE ECL
A32IC9	1820-0790		IC DUAL 4-INPUT OR-NOR GATE ECL
A32IC10	1820-0794		IC MASTER-SLAVE FLIP FLOP ECL
A32IC11	1820-0793		IC TRIPLE 2-INPUT EXCLUSIVE NOR GATE
A32IC12	1820-0794		IC MASTER-SLAVE FLIP FLOP ECL
A32IC13	1820-0796		IC QUAD 2-INPUT NOR GATE ECL
A32IC14	1820-0796		IC QUAD 2-INPUT NOR GATE ECL
A32IC15	1820-0794		IC MASTER-SLAVE FLIP FLOP ECL
A32IC16	1820-0794		IC MASTER-SLAVE FLIP FLOP ECL
A32IC17	1820-0794		IC MASTER-SLAVE FLIP FLOP ECL
A32IC18	1820-0794		IC MASTER-SLAVE FLIP FLOP ECL
A32IC18	1820-1132	1	IC TYPE D FLIP FLOP
A32IC19	1820-0790		IC DUAL 4-INPUT OR-NOR GATE ECL
A32IC20	1820-0794		IC MASTER-SLAVE FLIP FLOP ECL
A32R1 *TO* A32R40	0757-0394		R FXD 51.1 OHM 1% 1/8W
A32R41	0757-0316	1	R FXD 42.2 OHM 1% 1/8W

Abbreviations are listed in the introduction to this section

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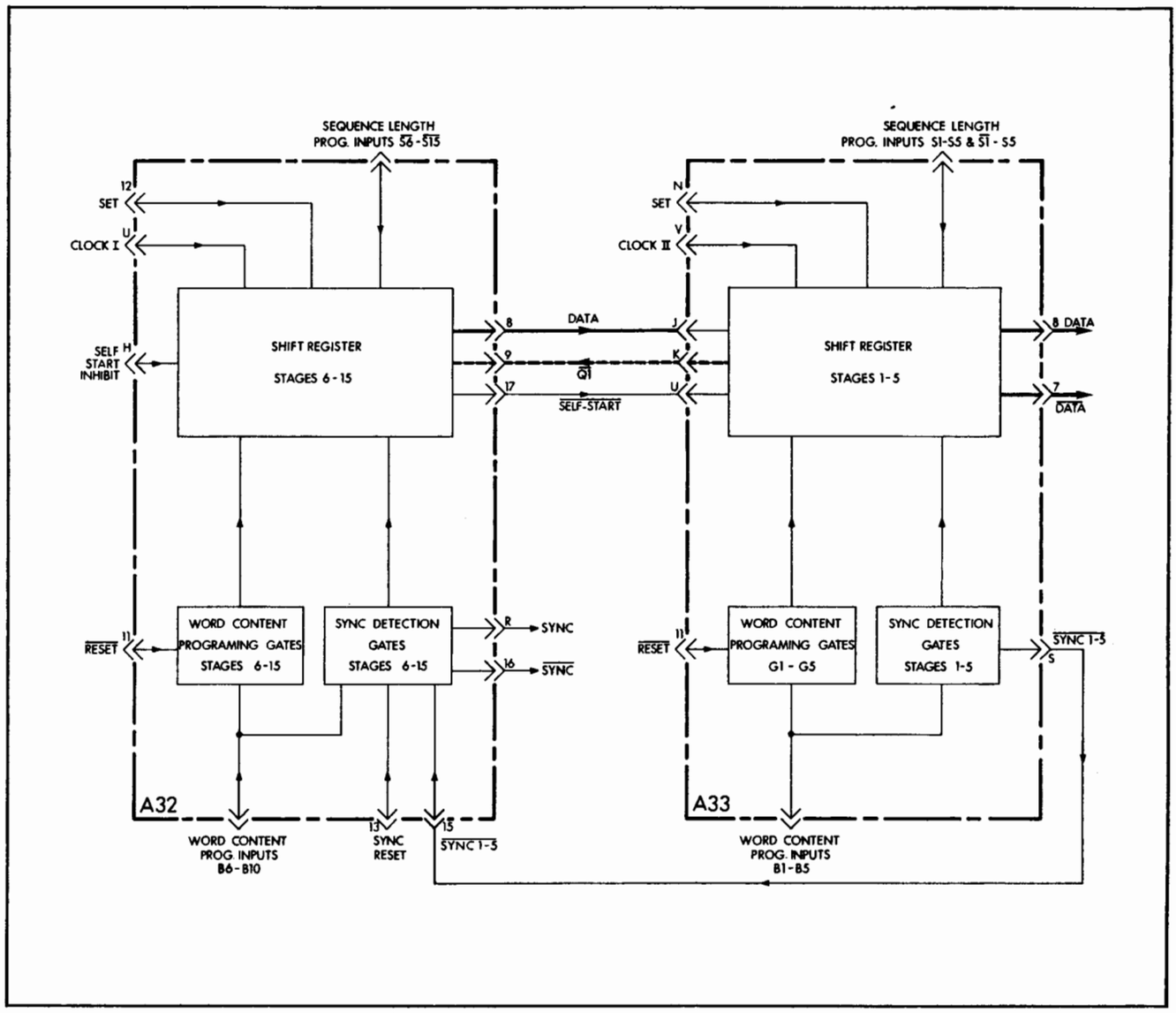

Figure A32/33-7 Block Diagram

PRBS Mode

In PRBS, the circuit operation is similar to that in WORD. For example, when n = 7 the PRBS sequence contains all possible seven bit words except 0000000. Thus by selecting the appropriate word on the front panel switches, the sync pulse can be placed anywhere in the sequence. In the n = 15 PRBS, stages 11 to 15 must always be 0 to produce sync and so sync detection is limited to words in the sequence whose last five bits are all 0. However, the sync pulse can still occur in a large number of positions since the first ten bits can still be selected.

SELF-START CIRCUIT

As explained earlier the all 0's state represents a hazard in this type of generator. To overcome this, a self start circuit which detects the all 0's state and introduces a 1 into the shift register is incorporated.

G26, G31, G32, G35 and G43 monitor the shift register stages and should the all 0's state occur, the output of G39 is changed to 1. This 1 drives the Set input of FF5 via G37 and G38 to introduce a 1 into the shift register. As soon as Q5 changes to 1 the self start circuit becomes inoperative and the input to FF5 changes back to 0.

Due to the physical distance between some stages and the self start gates, significant time delays can occur between these stages changing state and the effect of the changes reaching G39. These delays can cause spikes at the output of G39 resulting in false triggering of the Set input to FF5. To prevent this, a spike suppression circuit consisting of the low pass filter R6, C1 is included at the output of G39.

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WORD CONTENT PROGRAMING

In the simplified Word Generator already described it was shown that the word generated was that formed by the initial states of the stages in the shift register. In the 3760A, a change in data mode or sequence length which alters the content of the word is detected by the Word Content Programer which stops the shift register by inhibiting its clock signals (CLOCK I and II). Simultaneously, it generates a 1 on the SET line to clear the shift register of the previous sequence. The SET pulse lasts for two clock periods and when it ends, the $\overline{\text{RESET}}$ line is switched from 1 to 0 to enable the word content programing gates G1 to G10. If a stage is to be programed to 1, the corresponding 'B' input from the Word Content Programer is 1, the output of the programing gate is therefore 0 and the flip-flop remains set ie with its Q output at 1. If a 0 is selected, the B input is 0 and the output of the programing gate becomes 1, the flip-flop is therefore reset to 0. The bit programing inputs for unused stages are automatically held at 0 and hence these stages are always reset to 0. Due to a relatively long time constant associated with the Word Content Programer, the word loading cycle is repeated a number of times before the shift register resumes normal operation (see Assembly Service Sheet A34).

SYNC DETECTION

Sync detection occurs when the sequence formed by the shift register stages is the same as the word formed by the WORD CONTENT switches. For example if the WORD CONTENT switches are set to 1011, sync detection occurs at the instant when Q1 to Q5 are 1011 respectively.

Word Mode

Sync detection in WORD will be considered in detail first. The programing inputs, B1 to B10 are applied to one input of the sync detection gates G11 to G20 respectively. The other input to these gates is driven by the $\overline{\text{Q}}$ output of the associated flip-flop in the shift register. Consider the seven bit word 1101001, B1 to B7 are 1101001 respectively and for one clock period in every data cycle, the Q outputs of FF1 to FF7 are also 1101001. The $\overline{\text{Q}}$ outputs of FF1 to FF7 are therefore 0010110 during this time and hence the inputs to the Exclusive – NOR gates, G1 to G7 are simultaneously different for one clock period in every data cycle. The resulting 0 produced at the wired-OR output of gates G1 to G5 in B.S.G. II is clocked through FF18 to B.S.G. I where it is combined with stages 6 to 15 sync. Note, that the unused stages are held at 0 and are therefore permanently in sync. The combined signal (logically $\overline{\text{SYNC}}$) is clocked through FF17 and appears at the outputs two clock periods after detection.

In ZERO ADD, the Sync input to the Zero Add Counter must change back to 0 before the end of the zero block otherwise a continuous zero block will be generated. (This condition can only occur accidentally, ie, at switch on). For this reason, the Zero Block signal is applied to the Set input of FF17 to reset the SYNC signal to 0 at the beginning of the zero block.

(ii) Figure A32/33-6 shows the coupling circuit between FF3 and FF2 in which G48 is inhibited by S2 and may be ignored. The combined output of G47 and G49 is:

$$= \overline{\overline{Q1} + Q3} + \overline{Q1 + \overline{Q3}}$$

$$= (Q1 \,.\, \overline{Q3}) + (\overline{Q1} \,.\, Q3)$$

$$= Q1 \oplus Q3$$

G47 and G49 therefore form an Exclusive-OR gate, driving FF2 with the mod. 2 addition of the feedback from FF1 and the output of FF3 as required by the polynomial.

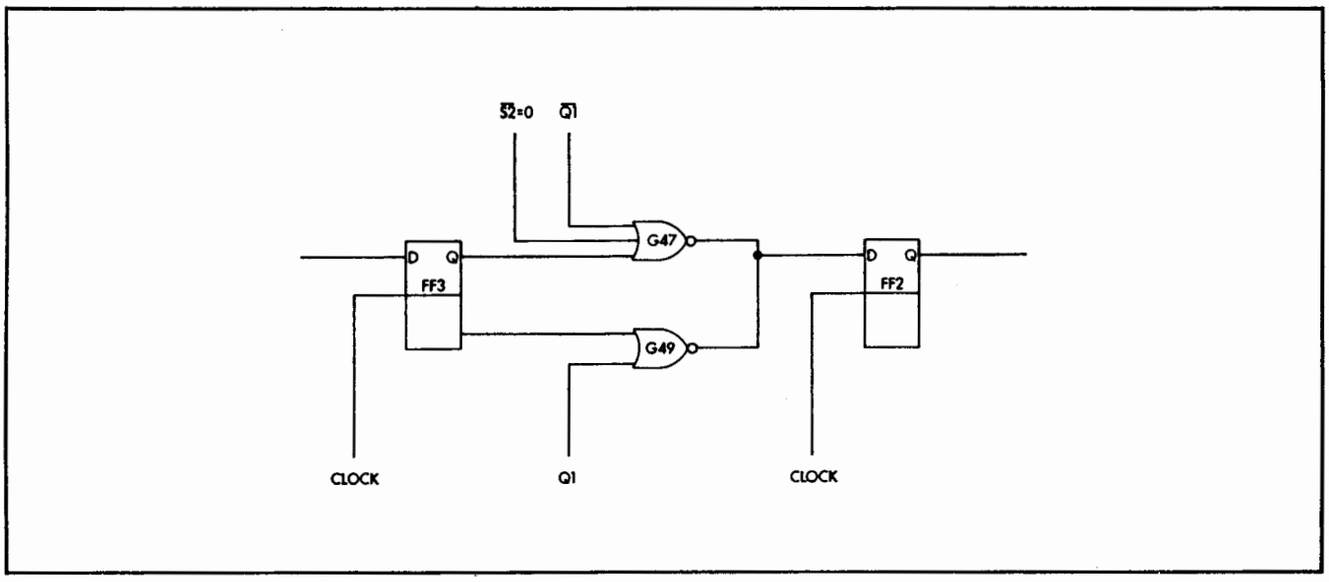

Figure A32/33-6 Exclusive-OR Gate Coupling

(iii) G50 is inhibited by S1 and the coupling between FF2 and FF1 is via G51 and G52. The combined output of these gates is:

$$= \overline{\overline{Q2} + \overline{Q1 + \overline{Q2}}}$$

$$= Q2 + (\overline{Q1} \,.\, Q2)$$

$$= Q2\,(1 + \overline{Q1})$$

$$= Q2$$

The input to FF1 is therefore logically equal to Q2 only, ie, no feedback is applied to FF1.

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The operation of sequence length programing in PRBS can be illustrated by considering the n = 3 sequence. From the simplified n = 3 PRBS generator shown in Figure A32/33-2 it can be seen that three types of interstage coupling are necessary in the shift register. These are:

(i) Feedback from the output stage (FF1) to the Nth stage (stage 3 in this case).

(ii) Exclusive-OR gate coupling where the input to a stage consists of the modulo 2 addition of the output from the previous stage and the feedback from the first stage (stages 3 & 2 in this case).

(iii) Direct coupling between adjacent stages (stages 2 and 1 in this case).

As can be seen from the Polynomials, Exclusive-OR gate coupling is only required between adjacent stages from FF1 to FF4 and hence a single gate acting as a feedback tap is sufficient for stages 5 to 10. Also, as there is no provision for sequence lengths of n = 11 to 14, no feedback at all is required to stages 11 to 14 and hence these stages are coupled directly together.

(i) From the table of PRBS sequence length programing inputs given in Figure A32/33-4 it can be seen that when n = 3, inputs $\overline{S15}$ to $\overline{S5}$ are all 1. $\overline{Q15}$ and Q14 to Q5 are therefore held at 0 (see Word Length Programing). $\overline{Q5}$ inhibits G41 and G42 and since $\overline{S4}$ is 1, G40 is also inhibited and the input to FF4 is held at 0. $\overline{Q4}$ inhibits G45 and G46 and the feedback loop from FF1 to FF3 is completed via G44 which is enabled by Q4 and $\overline{S3}$. This is shown in Figure A32/A33-5.

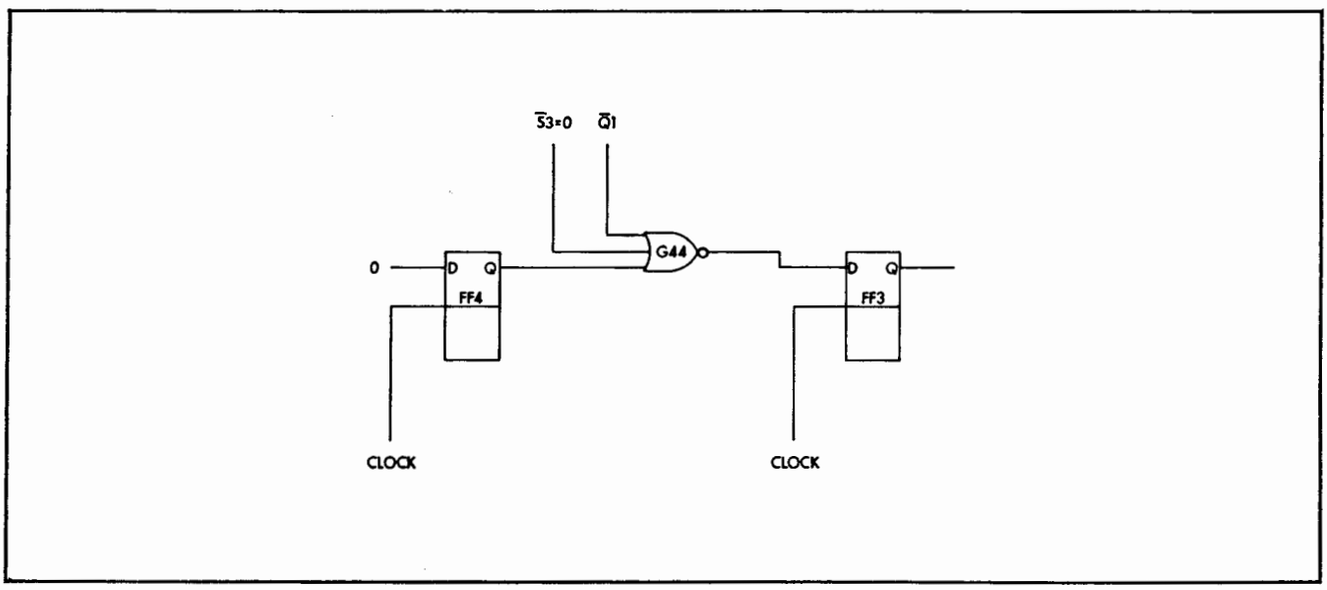

Figure A32/33-5 Interstage Coupling

n \ $\overline{S}$	15	10	9	8	7	6	5	4	3	2	1
3	1	1	1	1	1	1	1	1	0	0	1
4	1	1	1	1	1	1	1	0	0	1	1
5	1	1	1	1	1	1	0	1	1	0	1
6	1	1	1	1	1	0	1	1	1	1	0
7	1	1	1	1	0	1	1	1	1	1	0
8	1	1	1	0	1	1	1	0	0	0	1
9	1	1	0	1	1	1	1	0	1	1	1
10	1	0	1	1	1	1	1	1	0	1	1
15	0	1	1	1	1	1	1	1	1	1	0

Figure A32/33-4 PRBS Programming

PRBS Length

The programing inputs shown in Figure A32/33-4 set up the correct feedback conditions in the shift register for the generation of the following PRBS sequences:

$n = 3 \quad D^3 + D^2 + 1 = 0$
$n = 4 \quad D^4 + D^3 + 1 = 0$
$n = 5 \quad D^5 + D^2 + 1 = 0$
$n = 6 \quad D^6 + D + 1 = 0$
$n = 7 \quad D^7 + D + 1 = 0$
$n = 8 \quad D^8 + D^4 + D^3 + D^2 + 1 = 0$
$n = 9 \quad D^9 + D^4 + 1 = 0$
$n = 10 \quad D^{10} + D^3 + 1 = 0$
$n = 15 \quad D^{15} + D + 1 = 0$

These polynomials define the sequences being generated by indicating the positions of the feedback taps in the register. For example in the n = 3 sequence described earlier, the polynomial is $D^3 + D^2 + 1 = 0$, which means that feedback is applied from the output to stages 3 and 2 to produce this PRBS.

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SEQUENCE LENGTH PROGRAMING

The length and type of sequence being generated is controlled by the SEQUENCE LENGTH and DATA MODE switches respectively via the Sequence Length Programer, A35.

n \ $\overline{S}$	15	10	9	8	7	6	5	4	3	2	1
3	1	1	1	1	1	1	1	1	0	1	1
4	1	1	1	1	1	1	1	0	1	1	1
5	1	1	1	1	1	1	0	1	1	1	1
6	1	1	1	1	1	0	1	1	1	1	1
7	1	1	1	1	0	1	1	1	1	1	1
8	1	1	1	0	1	1	1	1	1	1	1
9	1	1	0	1	1	1	1	1	1	1	1
10	1	0	1	1	1	1	1	1	1	1	1
15	1	1	1	1	1	1	1	1	1	1	1

Figure A32/33-3 Word Length Programming

Word Length

The operation of the sequence length programing in WORD can be illustrated by considering the n = 4 case. From the table shown in Figure A32/33-3 it can be seen that when n = 4 $\overline{S15}$ is 1, FF15 is therefore set and its $\overline{Q}$ output is held at 0. The sequence length programing gates G27, G28, G29, G33, G34 and G36 are inhibited by inputs $\overline{S10}$ to $\overline{S5}$ respectively and hence the outputs of these gates are all 0. This allows the 0 at $\overline{Q}15$ to be clocked along the register and results in the Q outputs of FF14 to FF5 being held at 0. G41 and G42 are inhibited by $\overline{Q5}$ and the feedback loop is completed via G40 which is enabled by both Q5 and $\overline{S4}$. G44 is inhibited by $\overline{S3}$ and FF4 is coupled to FF3 via G45 and G46. The combined output of these gates is:

$$= \overline{\overline{Q4}} + \overline{(Q1 + \overline{Q4})}$$

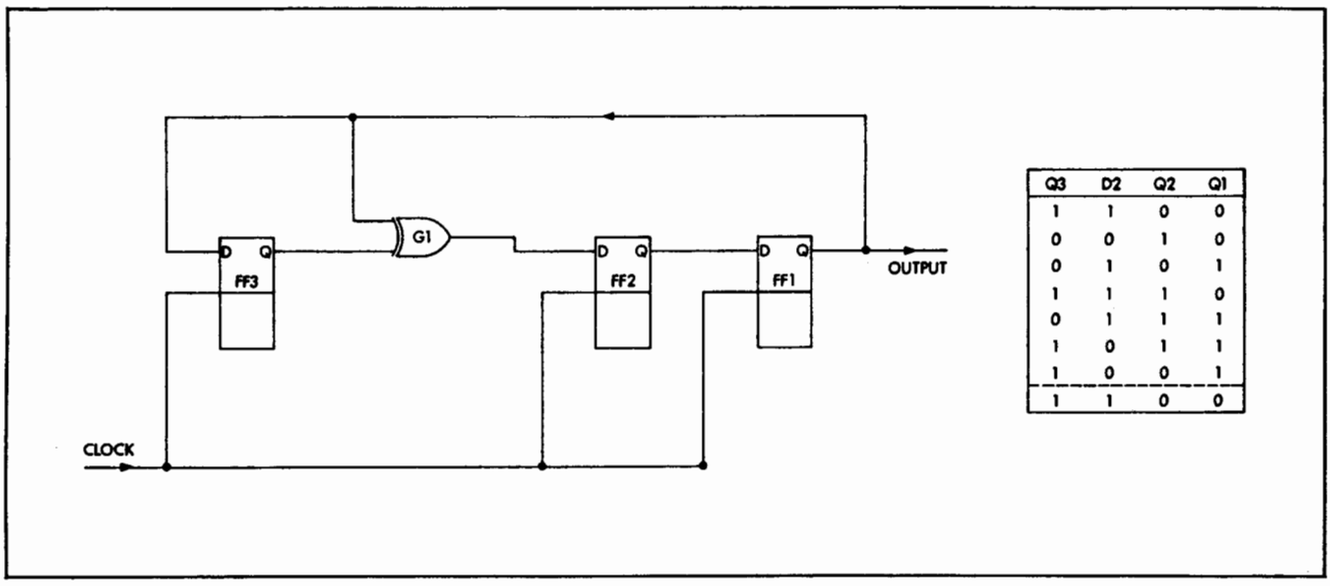
$$= Q4 + (Q4 \cdot \overline{Q1})$$

$$= Q4\ (1 + \overline{Q1})$$

$$= \underline{\underline{Q4}}$$

Thus the input to FF3 is logically equal to Q4 only ie no feedback is applied to FF3. The other adjacent stages are similarly coupled to each other and the overall circuit becomes logically equivalent to the word generator shown in Figure A32/33-1.

PRBS GENERATION



Q3	D2	Q2	Q1
1	1	0	0
0	0	1	0
0	1	0	1
1	1	1	0
0	1	1	1
1	0	1	1
1	0	0	1
1	1	0	0

Figure A32/33-2 PRBS Generation

A simple three stage PRBS Generator is shown in Figure A32/33-2. Assume that the initial conditions in the shift register are Q3 = 1, Q2 = 0 and Q1 = 0. Since the inputs to the exclusive – OR gate, G1, are different it drives the D input of FF2 with a 1. The first clock pulse shifts the 0 at D3 to Q3, the 1 at D2 to Q2 and the 0 at D1 to Q1 (and the output). Both inputs to G1 are now the same, ie 0 and hence D2 is driven by a 0. Subsequent clocking produces the truth table shown in Figure A32/33-2. After seven clock pulses, the shift register returns to its initial conditions and further clocking generates the repeated PRBS 0010111 at the output.

A hazard which exists in this type of generator can be illustrated by considering the initial conditions Q3 = 0, Q2 = 0 and Q1 = 0. Both inputs to G1 are the same and hence D2 is driven by a 0. The input and output of each stage is therefore 0 and clocking will only generate a continuous run of 0's at the output. This "all 0's state" never occurs naturally when the generator is cycling although it could occur at switch on unless a protection circuit is included in the generator.

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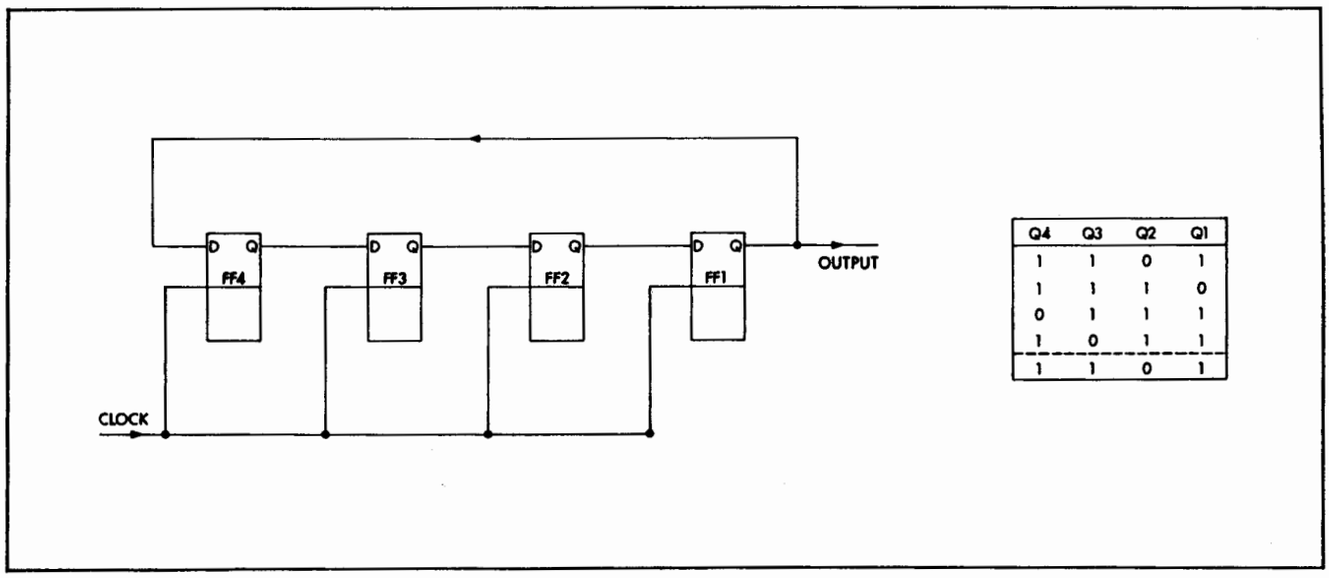
ASSEMBLY SERVICE SHEET A32/A33

BINARY SEQUENCE GENERATOR A32/A33

INTRODUCTION

The Binary Sequence Generator consists of a 15 stage shift register with associated programing and sync detection circuits. Stages 1 to 5 are contained on assembly A33 (B.S.G. II) while stages 6 to 15 are on assembly A32 (B.S.G. I). The number of stages in use and feedback conditions are controlled by the Sequence Length Programer to suit the WORD or PRBS being generated. Only one fixed PRBS per sequence length is available but the word content is selectable on front panel switches and is programed into the shift register by the Word Content Programer.

WORD GENERATION



Q4	Q3	Q2	Q1
1	1	0	1
1	1	1	0
0	1	1	1
1	0	1	1
1	1	0	1

Figure A32/33-1 Word Generation

A simple word generator is shown in Figure A32/33-1. Assume that initially FF1 to FF4 are 1011 respectively as shown in the first line of the truth table. If the generator is now clocked, each clock pulse will shift this pattern one stage to the right and hence the word formed at the output will be 1011, ie, the word initially formed by the shift register states.

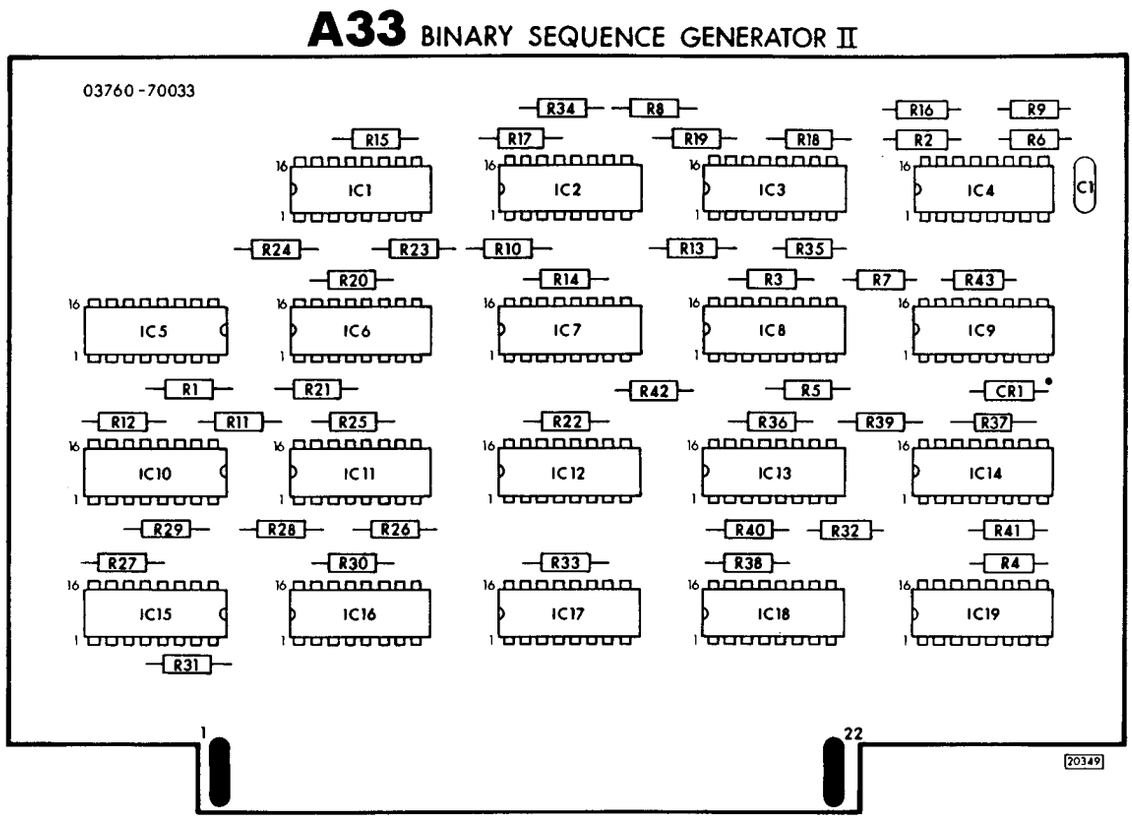


Figure A32/33-11 Component Location

WORD MODES

n \ S	15	10	9	8	7	6	5	4	3	2	1
3	1	1	1	1	1	1	1	1	0	1	1
4	1	1	1	1	1	1	1	0	1	1	1
5	1	1	1	1	1	1	0	1	1	1	1

PRBS MODES

n \ S	15	10	9	8	7	6	5	4	3	2	1
3	1	1	1	1	1	1	1	1	0	0	1
4	1	1	1	1	1	1	1	0	0	1	1
5	1	1	1	1	1	1	0	1	1	0	1

Figure A32/33-12 Programing Inputs

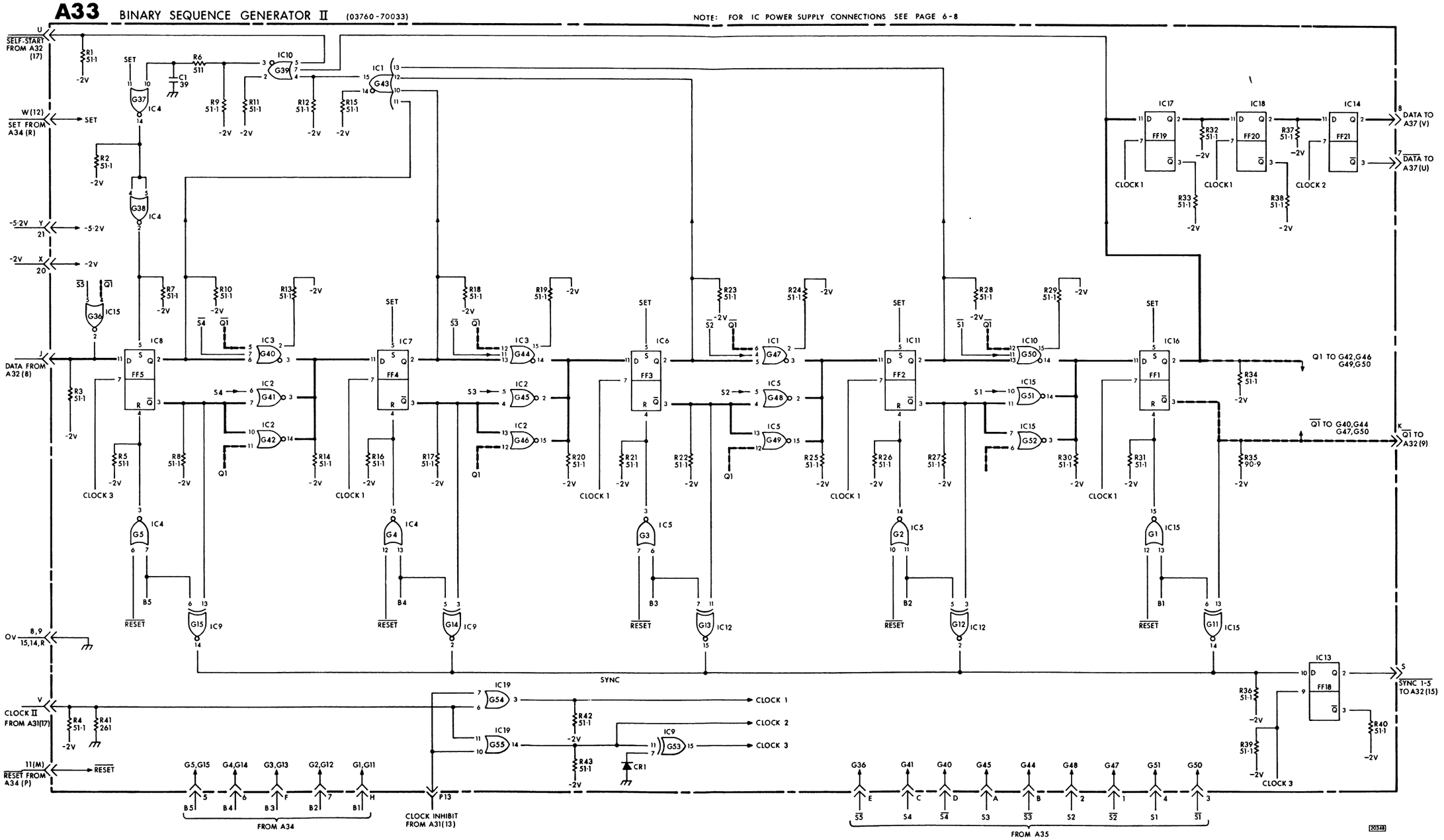


Figure A32/33-13 Schematic Diagram

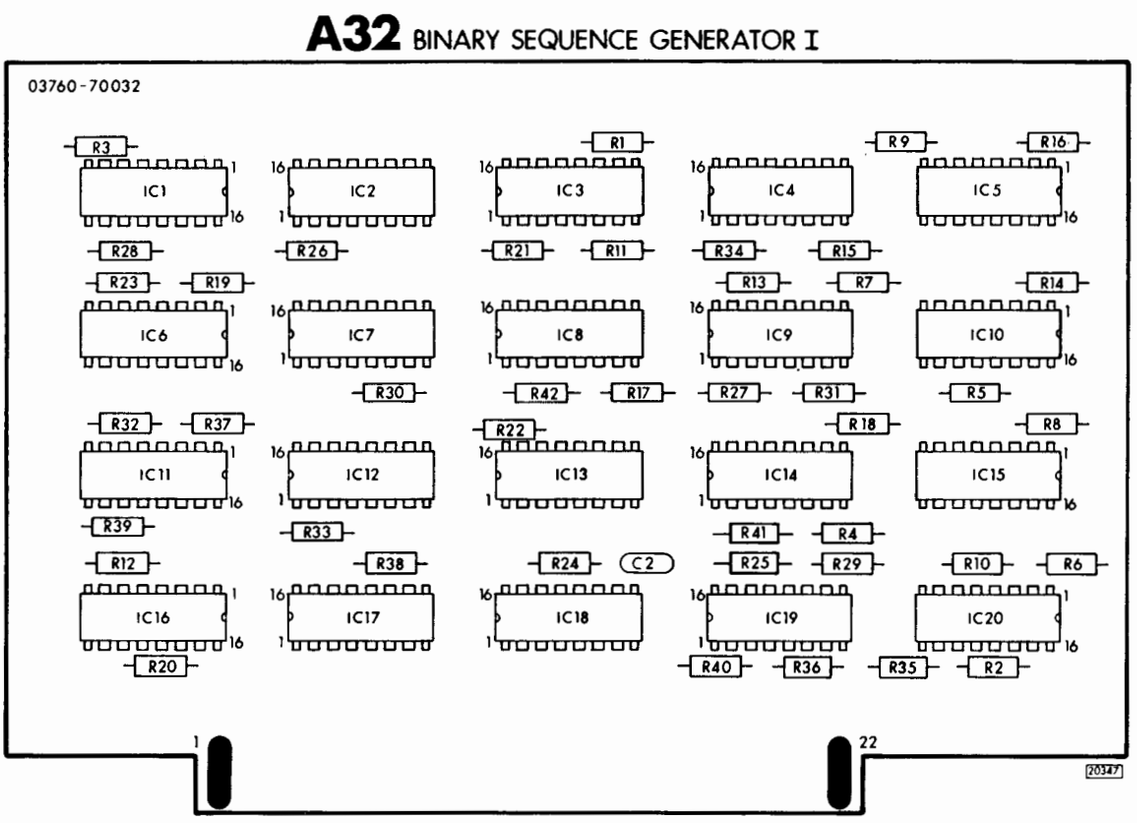


Figure A32/33-8 Component Location

WORD

n \ S	15	10	9	8	7	6	5	4	3	2	1
6	1	1	1	1	1	0	1	1	1	1	1
7	1	1	1	1	0	1	1	1	1	1	1
8	1	1	1	0	1	1	1	1	1	1	1
9	1	1	0	1	1	1	1	1	1	1	1
10	1	0	1	1	1	1	1	1	1	1	1
15	1	1	1	1	1	1	1	1	1	1	1

PRBS

n \ S	15	10	9	8	7	6	5	4	3	2	1
6	1	1	1	1	1	0	1	1	1	1	0
7	1	1	1	1	0	1	1	1	1	1	0
8	1	1	1	1	0	1	1	0	0	0	1
9	1	1	0	1	1	1	1	0	1	1	1
10	1	0	1	1	1	1	1	1	0	1	1
15	0	1	1	1	1	1	1	1	1	1	0

Figure A32/33-9 Programing Inputs

A32 BINARY SEQUENCE GENERATOR 03760-70032

NOTE: FOR IC POWER SUPPLY CONNECTIONS SEE PAGE 6-8

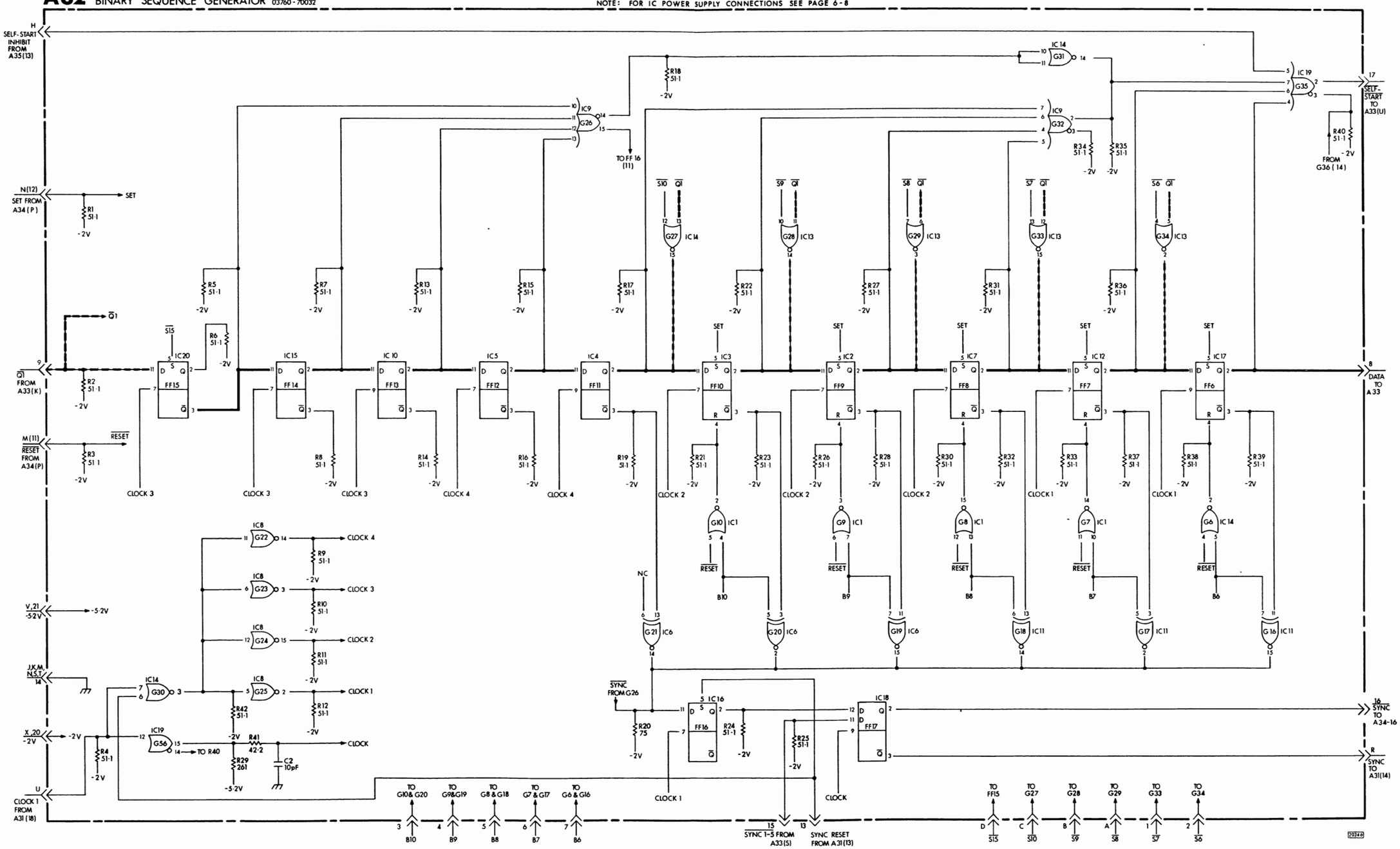


Figure A32/33-10 Schematic Diagram

Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A34	03760-70034		WORD CONTENT PROGRAMER ASSY
A34C1	0150-0096	2	C FXD 0.05UF +80-20% 100WVDC
A34C2	0150-0096		C FXD 0.05UF +80-20% 100WVDC
A34C3	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A34C4	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A34C5	0180-0291		C FXD 1UF +10% 35WVDC
A34C6	0180-0291		C FXD 1UF +10% 35WVDC
A34C7	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A34CR1 TO A34CR10	1901-0040		DIO SI
A34CR11	1901-0040		DIO SI
A34CR12	1902-3182		DIO BKDN 12.1V 5% 400MW
A34CR13	1902-0049	3	DIO BKDN 6.19V 400MW
A34CR14	1901-0040		DIO SI
A34IC1	1820-0125	1	IC DUAL COMPARITOR
A34IC2	1820-0802	1	IC QUAD 2-INPUT NOR GATE ECL
A34IC3	1820-0817		IC DUAL D M/S FLIP FLOP ECL
A34IC4	1820-0796		IC QUAD 2-INPUT NOR GATE ECL
A34IC5	1820-0101		IC TYPE 'D' FLIP FLOP
A34IC6	1820-0817		IC DUAL D M/S FLIP FLOP ECL
A34R1	0757-0438		R FXD 5.11K OHM 1% 1/8W
A34R2	0757-0438		R FXD 5.11K OHM 1% 1/8W
A34R3	0757-0438		R FXD 5.11K OHM 1% 1/8W
A34R4	0757-0438		R FXD 5.11K OHM 1% 1/8W
A34R5	0757-0438		R FXD 5.11K OHM 1% 1/8W
A34R6	0757-0438		R FXD 5.11K OHM 1% 1/8W
A34R7	0757-0438		R FXD 5.11K OHM 1% 1/8W
A34R8	0757-0438		R FXD 5.11K OHM 1% 1/8W
A34R9	0757-0438		R FXD 5.11K OHM 1% 1/8W
A34R10	0757-0438		R FXD 5.11K OHM 1% 1/8W
A34R11	0698-3132		R FXD 261 OHM 1% 1/8W
A34R12	0698-5490		R FXD 2K OHM 1% 1/8W
A34R13	0698-3132		R FXD 261 OHM 1% 1/8W
A34R14	0698-5490		R FXD 2K OHM 1% 1/8W
A34R15	0757-0438		R FXD 5.11K OHM 1% 1/8W
A34R16	0757-0403		R FXD 121 OHM 1% 1/8W
A34R17	0698-4037		R FXD 46.4 OHM 1% 1/8W
A34R18	0698-3446		R FXD 383 OHM 1% 1/8W
A34R19	0698-3132		R FXD 261 OHM 1% 1/8W
A34R20	0698-3132		R FXD 261 OHM 1% 1/8W
A34R21	0698-3441		R FXD 215 OHM 1% 1/8W
A34R22	0757-0280		R FXD 1K OHM 1% 1/8W
A34R23	0757-0280		R FXD 1K OHM 1% 1/8W
A34R24	0757-0422	1	R FXD 909 OHM 1% 1/8W
A34R25	0698-3132		R FXD 261 OHM 1% 1/8W
A34R26	0698-3132		R FXD 261 OHM 1% 1/8W
A34R27	0698-3132		R FXD 261 OHM 1% 1/8W
A34R28	0757-0399		R FXD 82.5 OHM 1% 1/8W
A34R29	0698-3132		R FXD 261 OHM 1% 1/8W
A34R30	0698-3132		R FXD 261 OHM 1% 1/8W
A34R31	0698-3437		R FXD 133 OHM 1% 1/8W
A34S1	3101-1162	1	SW SLIDE SPDT PC BD MTG

Abbreviations are listed in the introduction to this section

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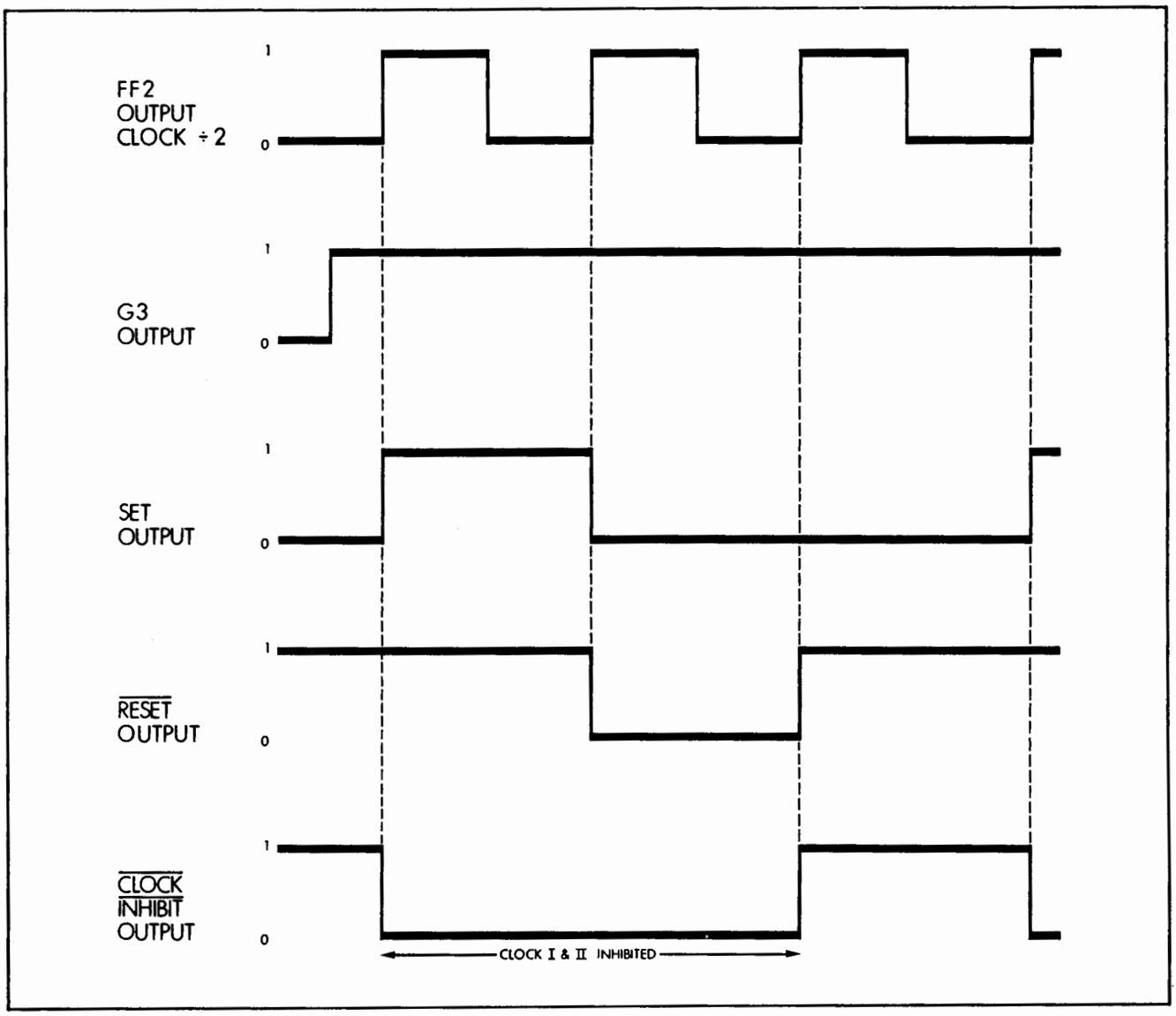

Figure A34-1 Timing Diagram

SET AND RESET PULSE GENERATORS

The main clock signal, CLOCK III, drives the Set and Reset pulse generators via the divide by two stage FF2. In WORD, the MODE switch enables G3 via G1 and while the word content is correct, the output of G3 is 0 (G2 output is 1). This produces logic 0 at the Set output, and logic 1 at the $\overline{\text{RESET}}$ and CLOCK INHIBIT outputs.

When a new word is selected, the sync fails causing the output of G3 to go high. When the Q output of FF2 (CLOCK ÷2) next goes high FF3 changes state switching the SET output from 0 to 1. Simultaneously the $\overline{\text{CLOCK INHIBIT}}$ output goes low and inhibits the clock signals in the Binary Sequence Generator. This prevents the shift register from being clocked during the word loading cycle. Two clock periods later the Q output of FF2 again switches from 0 to 1 changing the Q output of FF4 to 1. This resets FF3 but maintains the $\overline{\text{CLOCK INHIBIT}}$ output at 0. Simultaneously the $\overline{\text{RESET}}$ output goes low to complete the word content programing in the Binary Sequence Generator. Two clock periods later FF4 is clocked by FF2 and the $\overline{\text{RESET}}$ and $\overline{\text{CLOCK INHIBIT}}$ outputs switch back to 1.

Although the word content is now correct, no sync pulses have been generated and so the output of G3 is still 1. The next clock pulse therefore initiates another word loading cycle. To end these cycles, a relatively long uninterrupted sync pulse stream is required at the input to stabilise the dc input to the comparator within the reference levels again. (The time taken is dependent on the time constant of the low pass filter). Although the clock signals to the Binary Sequence Generator are enabled for a short time during each word loading cycle this cannot be relied on to establish a steady sync pulse stream (especially at high frequencies). Consequently, FF1 is also clocked by the Q output of FF4 (RESET) to bring the input to the comparator back within the reference levels and so end the word loading cycles.

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ASSEMBLY SERVICE SHEET A34

WORD CONTENT PROGRAMER A34

INTRODUCTION

Word content as selected on the front panel WORD CONTENT switches is programed into the Binary Sequence Generator via the Word Content Programer A34. The state to which each stage in the shift register is programed is determined by the appropriate WORD CONTENT switch and is 1 when the switch is closed. Unused stages are automatically programed to 0 as the WORD CONTENT switches are connected to ground via the SEQUENCE LENGTH switch. When the word being generated is the same as that formed by the WORD CONTENT switches, a sync pulse is produced by the Binary Sequence Generator once per sequence (see Assembly Service Sheet A32/33). The absence of sync is therefore used as an indication that the word being generated is incorrect and that a new word must be loaded. The SET and $\overline{\text{RESET}}$ pulses required by the Binary Sequence Generator to load new words are also generated in this assembly.

SYNC PULSE DETECTOR

The divide by 2 counter, FF1 is clocked by the sync pulse stream to produce a square wave output at half the repetition rate of the sync. This waveform is integrated by the low pass filter R12, C1, R14, C2 to obtain its mean dc level. Since the waveform has unity mark to space ratio, the output of the filter is the mean MECL level of approximately -1.3V, regardless of the sync pulse repetition rate. This voltage is applied to the voltage comparator, IC1, which has an upper reference voltage of -1.15 and a lower reference voltage of -1.5V applied to it. While sync pulses are being generated, the input to the comparator lies between these reference levels and its output is approximately 0V. However, if the word content changes and sync is lost, the output of the comparator switches to +5V. A potential divider reduces the output levels of the comparator from 0 and +5V to approximately -2V and -0.5V respectively. The output of G2 is therefore logic 1 when the correct word is being generated, changing to 0 when a new word has to be generated.

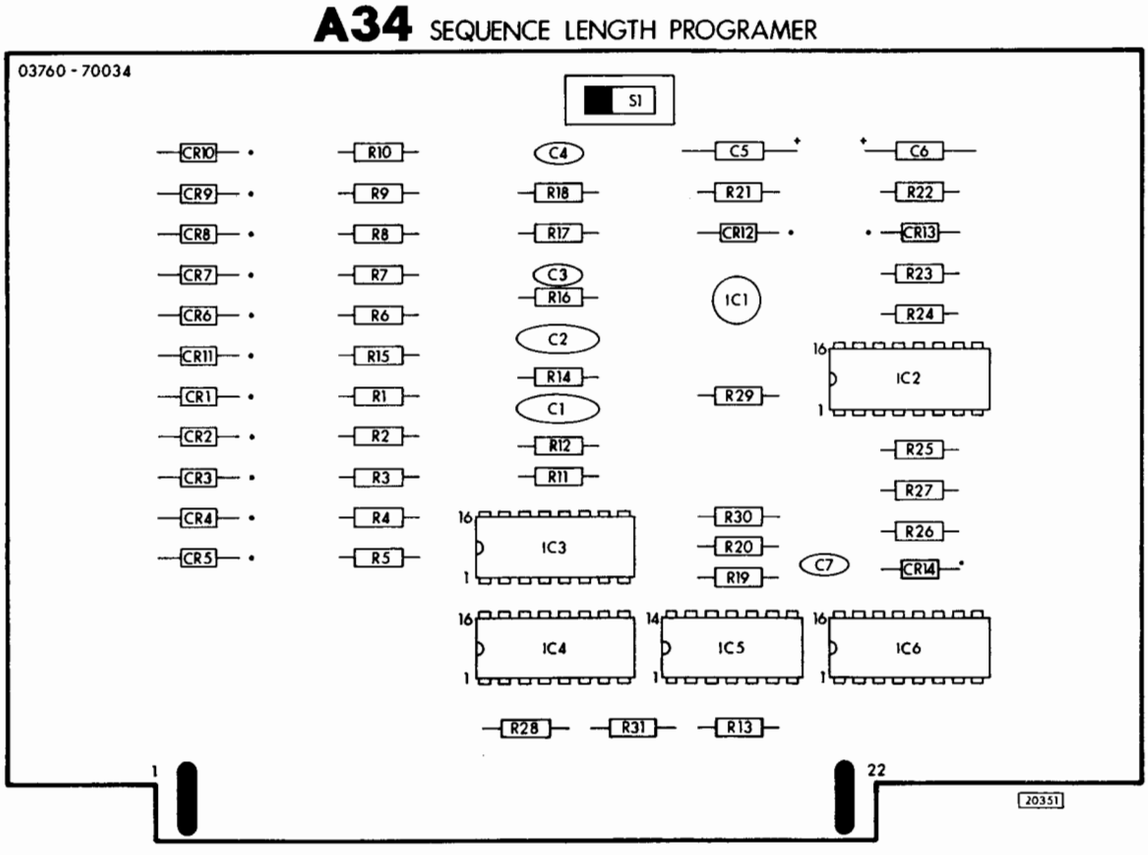

Figure A34-2 Component Location

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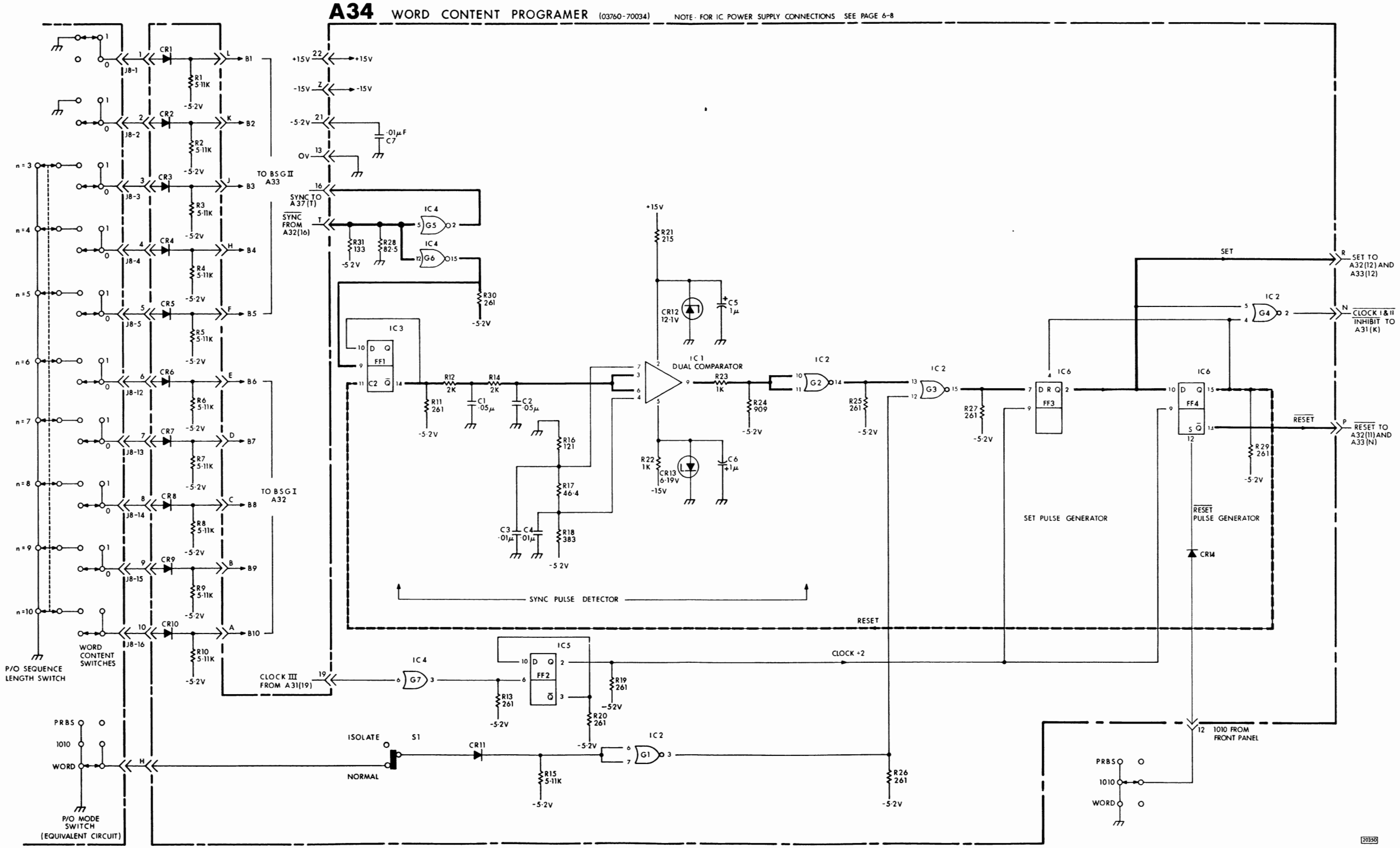

Figure A34-3 Schematic Diagram

ASSEMBLY SERVICE SHEET A35

SEQUENCE LENGTH PROGRAMER A35

INTRODUCTION

The feedback arrangements in the Binary Sequence Generator are controlled by the DATA MODE and SEQUENCE LENGTH switches via the logic in the Sequence Length Programer. Two different sets of programing inputs are required for each sequence length, one for WORD and another for PRBS.

WORD LENGTH PROGRAMING

In WORD modes, CR23 is grounded by the MODE switch, G12 and G14 are therefore inhibited. The output of G3 (0) inhibits the NAND gates G4, G15 and G16 but enables the NOR gates G11 and G13. The states of the Programing Outputs are therefore controlled by the Sequence Length switch via G5 to G11 and G13.

The complete range of programing inputs is given in Figure A35-2. Note that should n = 15 be selected in WORD, G5 is inhibited by G2 and the programing becomes the same as n = 10, the longest permissible word length.

PRBS PROGRAMING

In PRBS, the Mode switch enables G12 and G14, and G3 enables the NAND gates, G4, G15 and G16 but inhibits the NOR gates G11 and G13. PRBS sequence length programing is therefore controlled by G4 to G10, G12, G14, G15 and G16. Note that in n = 15, G2 is inhibited by G3 and has no effect on the Programing Outputs. The complete range of Programing Outputs are given in Figure A35-2.

1010

When the DATA MODE switch is set to the Maximum Change Sequence, 1010, CR23 is grounded by the MODE switch and the Binary Sequence Generator is programed to WORD. The DATA OUTPUT, however is the maximum change sequence 1010 generated in the Data Processor.

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Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A35	03760-70035		SEQUENCE LENGTH PROGRAMER ASSY
A35C1	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A35CR1	1901-0040		DIO SI
A35CR2	1901-0040		DIO SI
A35CR3	1901-0040		DIO SI
A35CR4	1901-0040		DIO SI
A35CR5	1901-0040		DIO SI
A35CR6	1901-0040		DIO SI
A35CR7	1901-0040		DIO SI
A35CR8	1901-0040		DIO SI
A35CR9	1901-0040		DIO SI
A35CR10	1901-0040		DIO SI
A35CR11	1901-0040		DIO SI
A35CR12	1901-0040		DIO SI
A35CR13	1901-0040		DIO SI
A35CR14	1901-0040		DIO SI
A35CR15	1901-0040		DIO SI
A35CR16	1901-0040		DIO SI
A35CR17	1901-0040		DIO SI
A35CR18	1901-0040		DIO SI
A35CR19	1901-0040		DIO SI
A35CR20	1901-0040		DIO SI
A35CR21	1901-0040		DIO SI
A35CR22	1901-0040		DIO SI
A35CR23	1901-0040		DIO SI
A35IC1	1820-0473	1	IC QUAD 2-INPUT NAND GATE
A35IC2	1820-0145	4	IC OPER AMPL
A35IC3	1820-0145		IC OPER AMPL
A35IC4	1820-0145		IC OPER AMPL
A35IC5	1820-0145		IC OPER AMPL
A35R1	0757-0438		R FXD 5.11K OHM 1% 1/8W
A35R2	0757-0438		R FXD 5.11K OHM 1% 1/8W
A35R3	0757-0438		R FXD 5.11K OHM 1% 1/8W
A35R4	0757-0438		R FXD 5.11K OHM 1% 1/8W
A35R5	0757-0438		R FXD 5.11K OHM 1% 1/8W
A35R6	0757-0438		R FXD 5.11K OHM 1% 1/8W
A35R7	0757-0438		R FXD 5.11K OHM 1% 1/8W
A35R8	0757-0438		R FXD 5.11K OHM 1% 1/8W
A35R9	0757-0438		R FXD 5.11K OHM 1% 1/8W
A35R10	0757-0438		R FXD 5.11K OHM 1% 1/8W
A35R11	0757-0438		R FXD 5.11K OHM 1% 1/8W
A35R12	0757-0438		R FXD 5.11K OHM 1% 1/8W
A35R13	0757-0438		R FXD 5.11K OHM 1% 1/8W
A35R14	0757-0438		R FXD 5.11K OHM 1% 1/8W

Abbreviations are listed in the introduction to this section

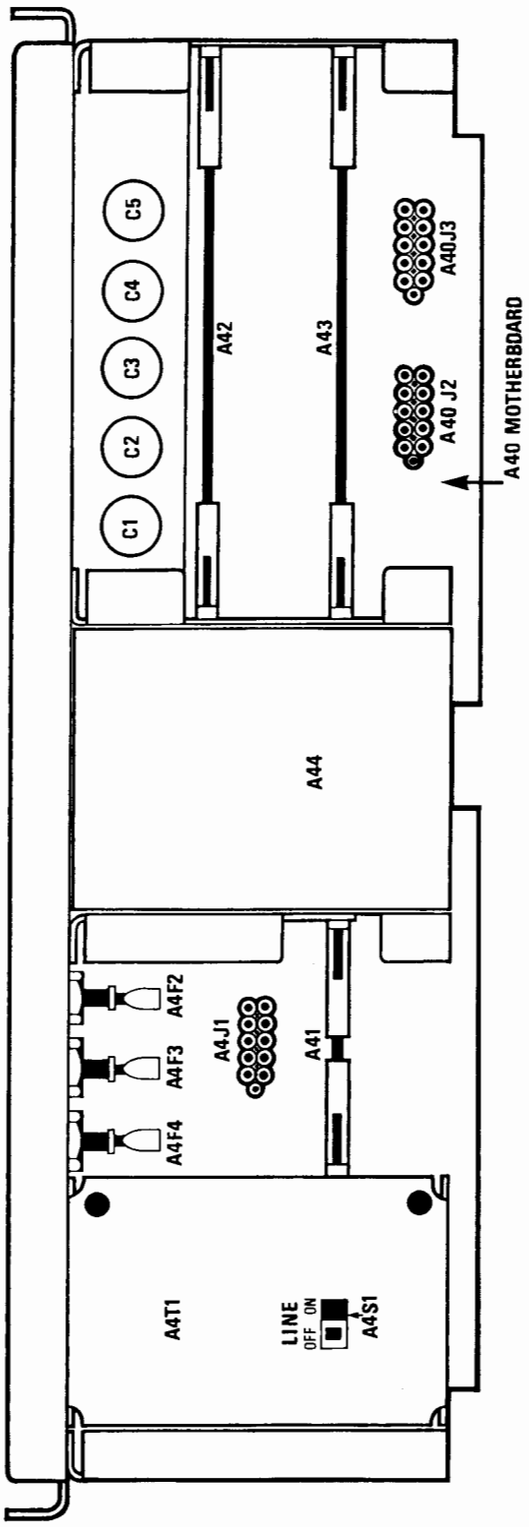

Figure A4-1 Component Location

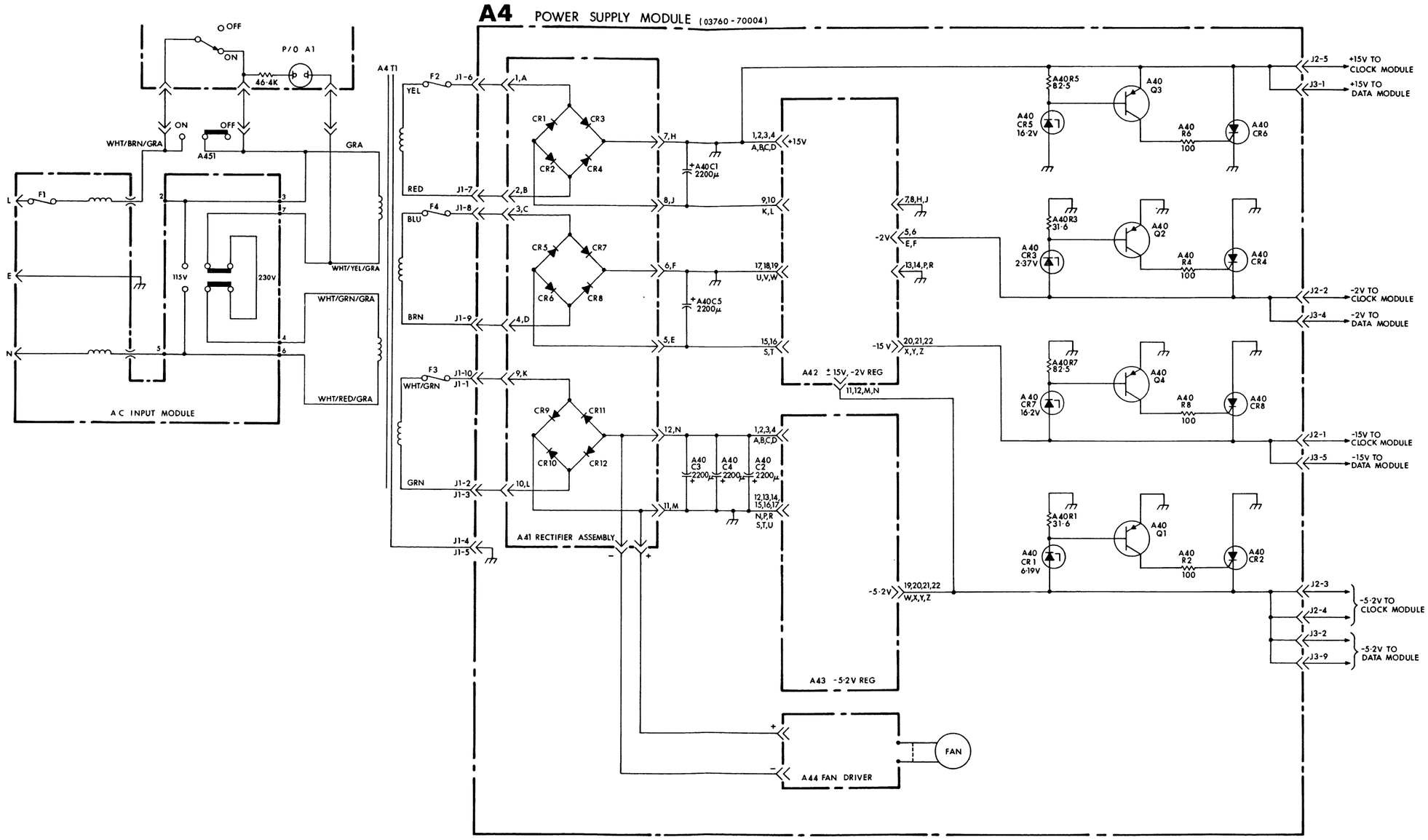

Figure A4-2 Schematic Diagram

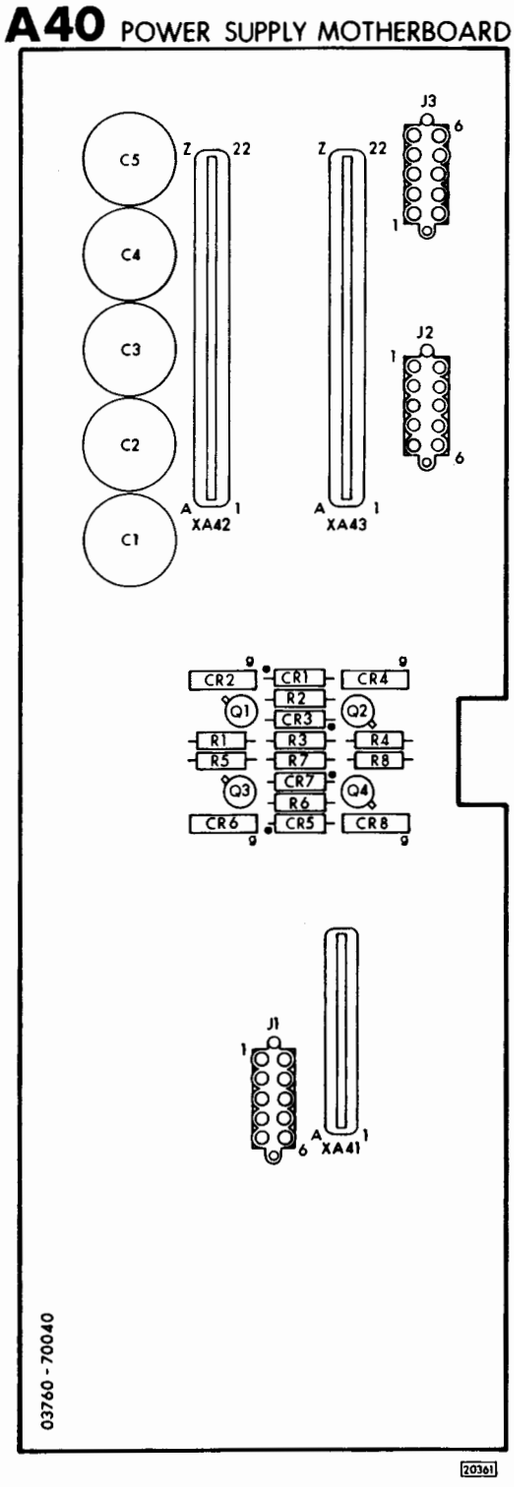

Figure A40-1 Component Location

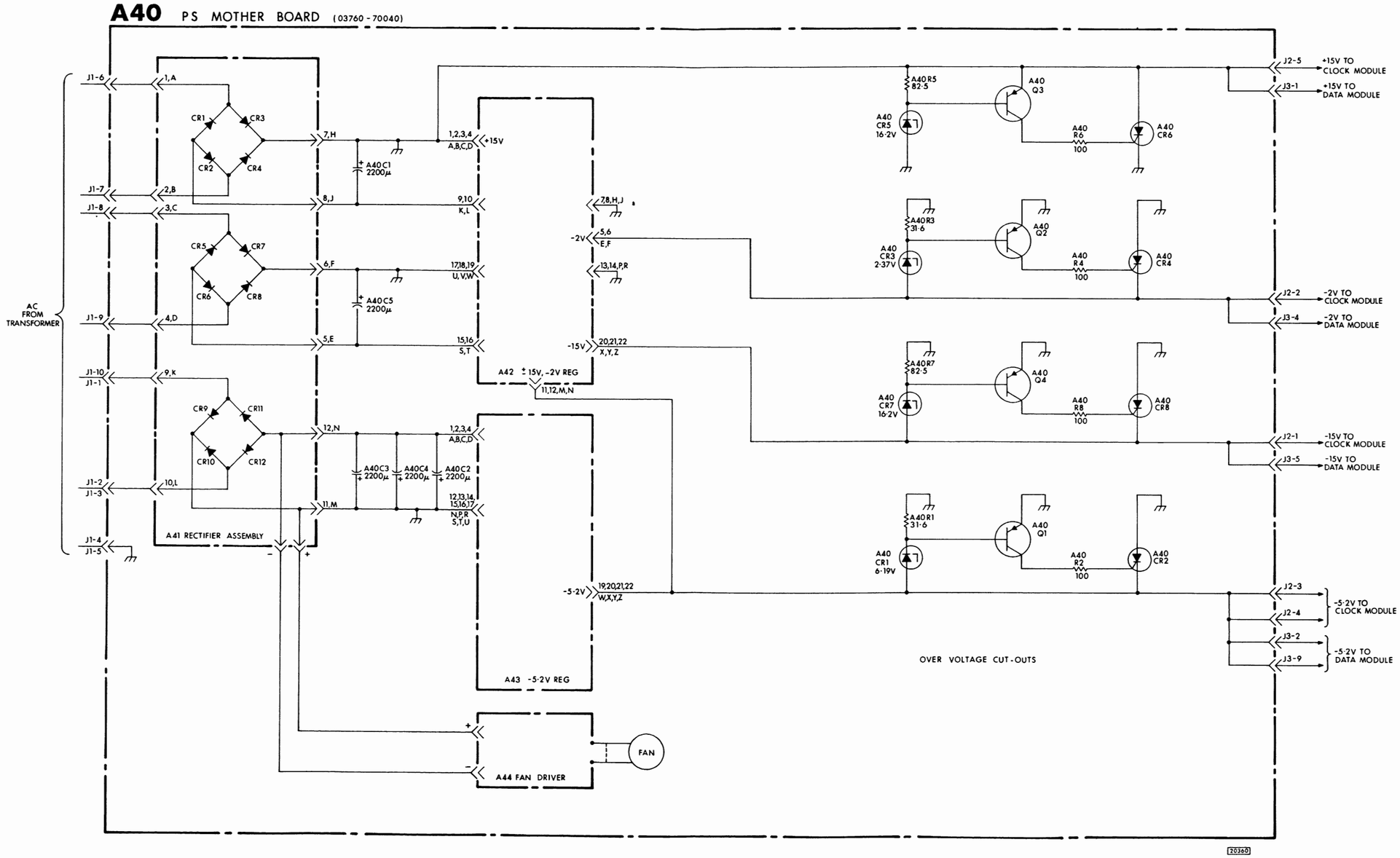

Figure A40-2 Schematic Diagram

ASSEMBLY SERVICE SHEET A40

POWER SUPPLY MOTHERBOARD A40

GENERAL

The Power Supply Motherboard forms the base of the Power Supply Module and carries the dc smoothing capacitors, overvoltage cut-outs and the plug-in assemblies A41, A42, A43.

OVERVOLTAGE CUT-OUTS

An overvoltage cut-out is fitted to each dc power supply line. The respective operating voltages are given below.

DC SUPPLY LINE	CUT-OUT VOLTAGE
+15V	+16.2V
-15V	-16.2V
-5.2V	-6.2V
-2V	-2.4V

Apart from the differences in operating voltage, the circuits are identical and hence only the -5.2V cut-out is described in detail. When the potential of the -5.2V line exceeds approximately -6.2V, the zener diode, CR1 turns on and forward biases Q1. This gates the silicon controlled rectifier, CR2 on and effectively places a short circuit across the supply line. The increase in output current produced when CR2 turns on operates the overcurrent cut-out and switches the regulator off. Since the SCR latches on when triggered, the instrument must be switched off to reset the overvoltage cut-out.

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Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A40	03760-70040		POWER SUPPLY MOTHERBOARD ASSY
	0403-0200		FOOT PLASTIC
A40C1	03761-70402	5	C FXD 2200UF +50-10% 40WVDC
A40C2	03761-70402		C FXD 2200UF +50-10% 40WVDC
A40C3	03761-70402		C FXD 2200UF +50-10% 40WVDC
A40C4	03761-70402		C FXD 2200UF +50-10% 40WVDC
A40C5	03761-70402		C FXD 2200UF +50-10% 40WVDC
A40CR1	1902-0049		DIO BKDN 6.19V 400MW
A40CR2	1884-0066	4	THYRISTOR JEDEC ZN443
A40CR3	1902-3002	1	DIO BRKDWN 2.37V 5% 400MW
A40CR4	1884-0066		THYRISTOR JEDEC ZN443
A40CR5	1902-0184	2	DIO BKDN 16.2V 5% 400MW
A40CR6	1884-0066		THYRISTOR JEDEC ZN443
A40CR7	1902-0184		DIO BKDN 16.2V 5% 400MW
A40CR8	1884-0066		THYRISTOR JEDEC ZN443
A40J1	1251-3257	3	CONN-PC 10 RIB CONT
A40J2	1251-3257		CONN-PC 10 RIB CONT
A40J3	1251-3257		CONN-PC 10 RIB CONT
A40Q1	1853-0010		XSTR SI PNP
A40Q2	1853-0010		XSTR SI PNP
A40Q3	1853-0010		XSTR SI PNP
A40Q4	1853-0010		XSTR SI PNP
A40R1	0757-0180	2	R FXD 31.6 OHM 1% 1/8W
A40R2	0757-0401		R FXD 100 OHM 1% 1/8W
A40R3	0757-0180		R FXD 31.6 OHM 1% 1/8W
A40R4	0757-0401		R FXD 100 OHM 1% 1/8W
A40R5	0757-0399		R FXD 82.5 OHM 1% 1/8W
A40R6	0757-0401		R FXD 100 OHM 1% 1/8W
A40R7	0757-0399		R FXD 82.5 OHM 1% 1/8W
A40R8	0757-0401		R FXD 100 OHM 1% 1/8W
A40XA41	1251-1626	1	CONN-PC 24 RIB CONT
A40XA42	1251-1365		CONN-PC 44 RIB CONT
A40XA43	1251-1365		CONN-PC 44 RIB CONT

Abbreviations are listed in the introduction to this section

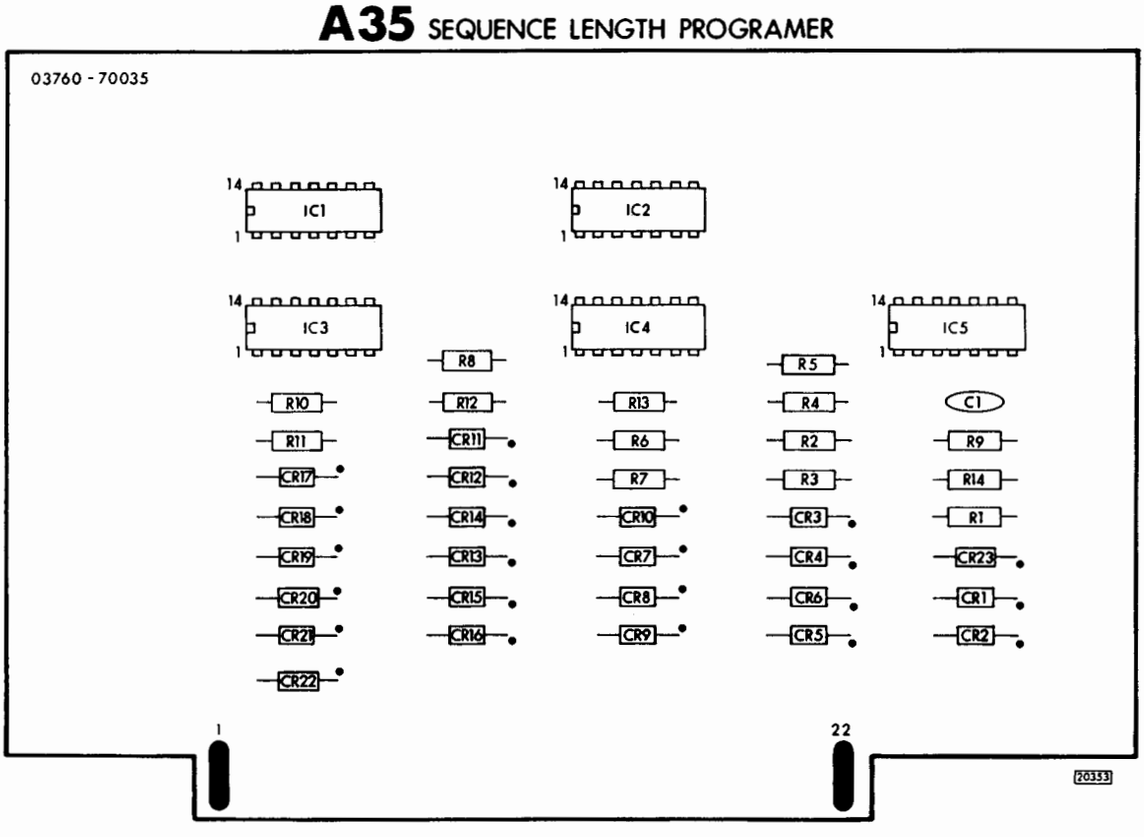

Figure A35-1 Component Location

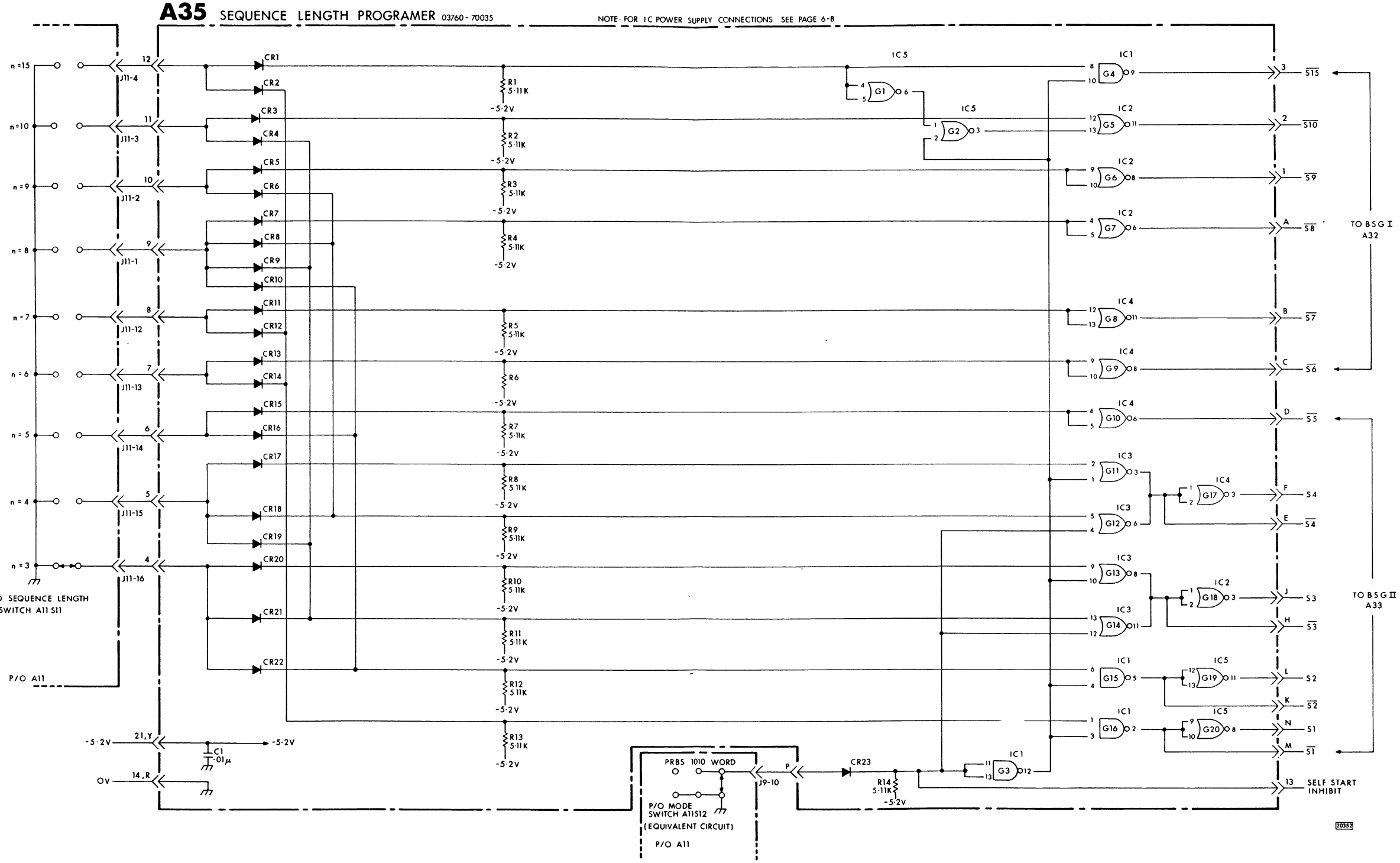

Figure A35-2 Schematic Diagram

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ASSEMBLY SERVICE SHEET A37

DATA PROCESSOR/ SYNC OUTPUT AMPLIFIER A37

GENERAL

The Data Processor and Sync Output Amplifier are located on the A37 assembly. The Data Processor carries out the following modifications to the data stream produced by the Binary Sequence Generator:

(i) Addition of two consecutive errors to every 4000th PRBS sequence.

(ii) Insertion of the zero block generated by the Zero Add Counter, A31, into the data stream.

(iii) It replaces the data generated by the Binary Sequence Generator by the maximum change sequence 1010.

(iv) Conversion of the data format from Non-Return to Zero (NRZ) to Return to Zero (RZ).

ZERO ADD

In ZERO ADD, the MODE switch inhibits G4 via G2 to hold the Q and $\overline{Q}$ outputs of FF4 at 0 and 1 respectively. G9 is therefore inhibited by $\overline{Q4}$ and since the 1010 control input is 0 in this mode, the wired – OR output of G8 and G9 is DATA (between zero blocks). When a zero block is inserted into the data stream, the ZERO BLOCK signal switches from 0 to 1 and inhibits G8 for the required number of clock periods (the length of the block is timed by the Zero Add Counter A31).

MAXIMUM CHANGE SEQUENCE 1010

In 1010, the mode switch inhibits G8 to prevent the normal data stream reaching FF5 (G9 is inhibited by $\overline{Q4}$ as in ZERO ADD). The MODE switch also enables G12 via G10 to provide a feedback path from the Q output of FF5 to its D input. This flip-flop now operates as a divide by two counter producing a square wave at half the clock rate ie the Maximum Change Sequence 1010. In all other modes, G12 is inhibited and the normal data stream is clocked through FF5 without modification to appear at its $\overline{Q}$ output as $\overline{DATA}$.

NRZ/RZ CONVERSION

In NRZ, G11 is inhibited and the data stream at the output of FF5 ($\overline{DATA}$) passes through G13 to appear at the output as DATA. In RZ, G11 is enabled to allow the clock to be combined with the data stream in G13. The output of G13 is therefore:

$$\overline{\overline{DATA} + \overline{CLOCK}}$$
$$= DATA \ . \ CLOCK$$

The output is therefore only 1 when both the data and clock are 1, ie the data stream has been converted to the Return to Zero format, RZ (see Figure A37-1). Since the propogation delay of FF5 is greater than G11 (approximately 1ns), a small delay line is included at the output of G11 to maintain synchronism between the clock and data streams.

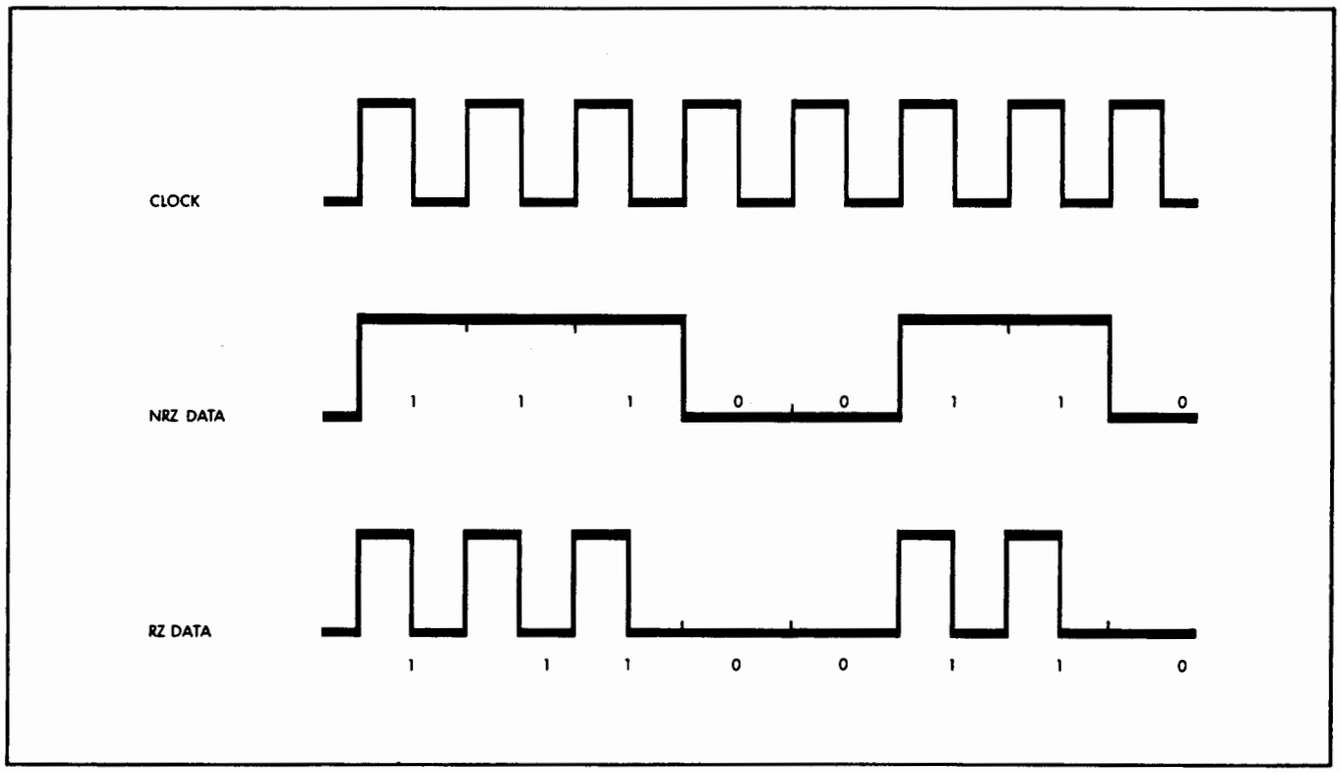

Figure A37-1 NRZ/RZ Conversion

ERROR ADD

The errors are added to the data stream by changing two consecutive bits in every 4000 sequences to their logic complement. The timing of the errors is controlled by a counter consisting of two ÷2 stages (FF2 and FF6) and three TTL decade dividers in series. The logic levels are converted from MECL to TTL by the schmitt trigger Q4 and Q5 and then back to MECL by CR9 and CR10 at the output of the decade dividers.

In PRBS-ADD ERRORS, CR4 is grounded by the mode switch to hold the output of G2 at 0. Once every 4000 sequences the output of DD3 goes high and clocks FF3, this occurs coincident with the positive going edge

of the SYNC pulse. When clocked by DD3 the Q output of FF3 changes to 0 (this flip-flop was set by FF4 after the addition of the previous errors) and since this change is coincident with the arrival of the $\overline{\text{SYNC}}$ pulse, the output of G4 changes to 1. Since the output of G4 remains high for the duration of the $\overline{\text{SYNC}}$ pulse ie for one clock period, the CLOCK ÷2 signal will change state once during this time. If the change is from 0 to 1, FF4 changes state to inhibit G8 and enable G9. The wired – OR output of G8 and G9 therefore changes from DATA to $\overline{\text{DATA}}$, thus introducing an error into the data stream. Q4 also sets FF3 whose Q output changes to 1 and inhibits G4. Consequently when FF4 is clocked again it changes state and the wired-OR output of G8 and G9 reverts to DATA. Since FF4 is clocked at half the rate of the main clock signal, the data stream is logically $\overline{\text{DATA}}$ for two bits ie two consecutive errors are added to the data stream.

If the CLOCK ÷2 signal had changed from 1 to 0 during the $\overline{\text{SYNC}}$ pulse then obviously FF4 would not have changed state and no errors would have been inserted. One sequence later however the phase of the CLOCK ÷2 signal relative to the $\overline{\text{SYNC}}$ pulse will have changed since there are an odd number of bits in every PRBS sequence ($2^n - 1$). The errors are therefore inserted one sequence after the output of DD3 goes high.

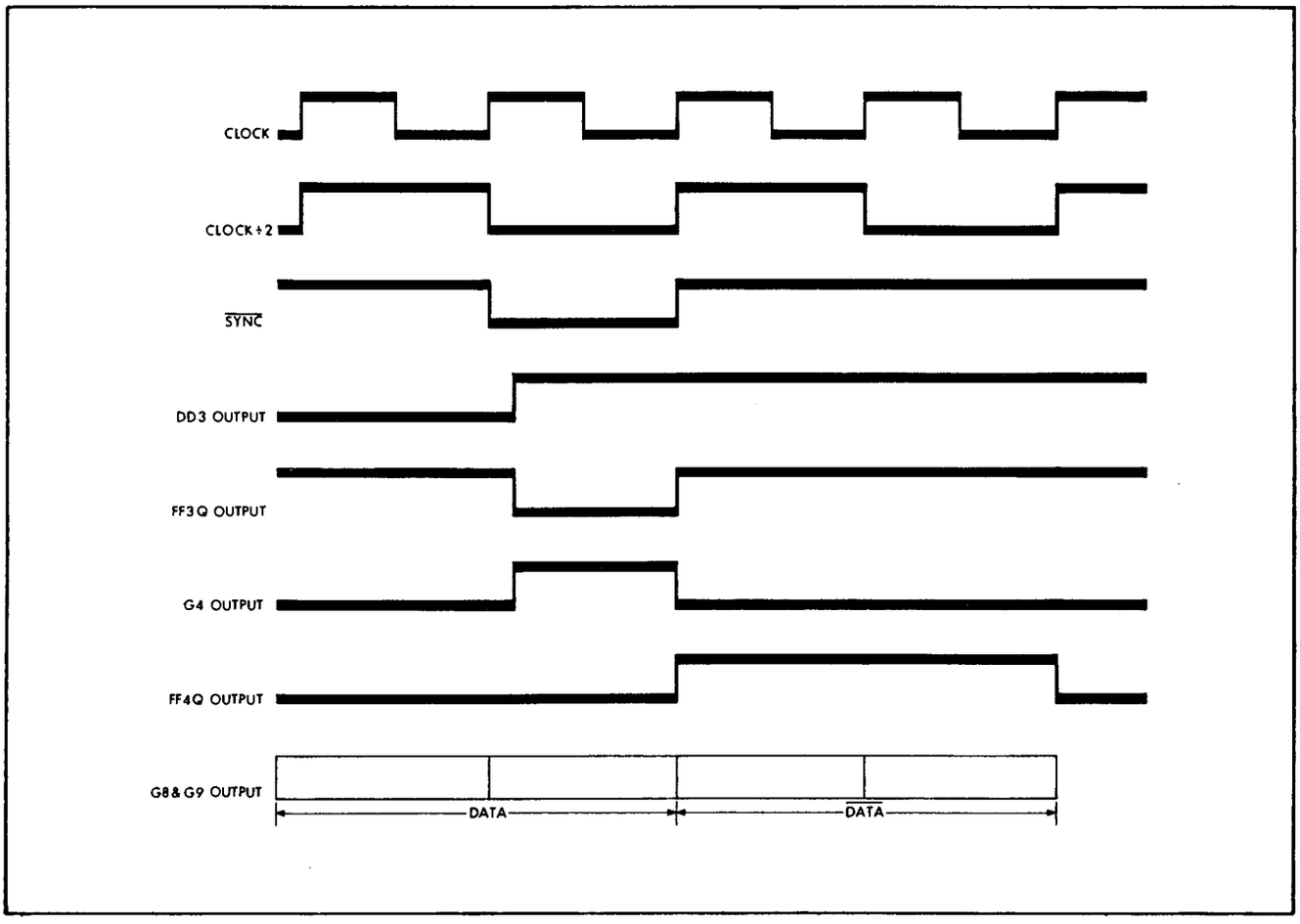

Figure A37-2 Error Add

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SYNC OUTPUT AMPLIFIER

The sync pulse stream is retimed at the input to the Data Processor/Sync Output Amplifier by FF1. With the internally mounted Sync Mode switch, S1, set to NORMAL, FF1 drives the Sync Output Amplifier via G5 to produce an output pulse with a width equal to one clock period. In the ÷2 position, S1 enables G6 and the Sync Output Amplifier is driven by FF2. This flip-flop has feedback from its $\overline{Q}$ output to its D input and therefore operates as a ÷2 counter producing a square wave output whose mark and space times are equal to one sequence length.

The sync output amplifier consists of an emitter coupled pair Q1 and Q2 driven by the complementary outputs of G7 and followed by a common base stage, Q3. In the absence of a sync pulse, G7 turns Q1 on and Q2 off. Q3 is therefore reverse biased and the sync output is 0V. When a sync pulse arrives, G7 switches Q1 off and Q2 on, Q3 is now forward biased and a positive going pulse is produced at the sync output. The output pulse amplitude is proportional to the collector current of Q3 which in turn is proportional to the "on" collector voltage of Q2. This voltage is adjusted by R17 to set the sync output to +1V.

Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A37	03760-70037		DATA PROCESSOR/SYNC OUTPUT AMP ASSY
A37C3	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A37C4	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A37C5	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A37C6	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A37C7	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A37C8	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A37C10	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A37C11	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A37C12	0140-0210	1	C FXD 270PF 5% 300WVDC
A37C13	0160-2261	2	C FXD 15PF 5% 500WVDC
A37C14	0160-2261		C FXD 15PF 5% 500WVDC
A37C15	0160-2201	1	C FXD 51PF 5% 300WVDC
A37C16	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A37C17	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A37C18	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A37C19	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A37CR1	1902-3139	1	DIO BKDN 8.25V 5% 400MW
A37CR2	1901-0040		DIO SI
A37CR3	1901-0040		DIO SI
A37CR4	1901-0040		DIO SI
A37CR5	1901-0040		DIO SI
A37CR6	1901-0040		DIO SI
A37CR8	1902-0049		DIO BKDN 6.19V 400MW
A37CR9	1902-3048		DIO BKDN 3.48V 5% 400MW
A37CR10	1901-0040		DIO SI
A37CR11	1901-0040		DIO SI
A37IC1	1820-0055	3	IC DECADE COUNTER
A37IC2	1820-0055		IC DECADE COUNTER
A37IC3	1820-0055		IC DECADE COUNTER
A37IC4	1820-0803		IC 2-3-2-INPUT OR/NOR GATE ECL
A37IC5	1820-0817		IC DUAL D M/S FLIP FLOP ECL
A37IC6	1820-0817		IC DUAL D M/S FLIP FLOP ECL
A37IC7	1820-0796		IC QUAD 2-INPUT NOR GATE ECL
A37IC8	1820-0790		IC DUAL 4-INPUT OR-NOR GATE ECL
A37IC9	1820-0794		IC MASTER-SLAVE FLIP FLOP ECL
A37IC10	1820-0796		IC QUAD 2-INPUT NOR GATE ECL
A37IC11	1820-0794		IC MASTER-SLAVE FLIP FLOP ECL
A37IC12	1820-0794		IC MASTER-SLAVE FLIP FLOP ECL
A37Q1	1854-0247	2	XSTR NPN SILICON
A37Q2	1854-0247		XSTR NPN SILICON
A37Q3	1854-0218	1	XSTR SI NPN
A37Q4	1853-0034	2	XSTR SI PNP
A37Q5	1853-0034		XSTR SI PNP
A37R1	0757-0394		R FXD 51.1 OHM 1% 1/8W
A37R2	0757-0394		R FXD 51.1 OHM 1% 1/8W
A37R3	0757-1020	1	R FXD 133 OHM 1% 1/4W
A37R4	0698-3132		R FXD 261 OHM 1% 1/8W
A37R5	0698-3132		R FXD 261 OHM 1% 1/8W
A37R7	0698-3132		R FXD 261 OHM 1% 1/8W
A37R8	0698-3132		R FXD 261 OHM 1% 1/8W
A37R9	0698-3132		R FXD 261 OHM 1% 1/8W
A37R10	0698-3132		R FXD 261 OHM 1% 1/8W

Abbreviations are listed in the introduction to this section

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Replaceable Parts (continued)

Ref Desig	HP Part No	TQ	Description
A37R11	0698-3132		R FXD 261 OHM 1% 1/8W
A37R12	0698-3132		R FXD 261 OHM 1% 1/8W
A37R13	0757-0394		R FXD 51.1 OHM 1% 1/8W
A37R14	0757-0394		R FXD 51.1 OHM 1% 1/8W
A37R15	0757-0401		R FXD 100 OHM 1% 1/8W
A37R15	0698-5132	1	R FXD 990K OHM 5% 1/4W
A37R16	0757-0394		R FXD 51.1 OHM 1% 1/8W
A37R17	2100-2413		R VAR 200 OHM 10% 1/2W
A37R18	0757-0416		R FXD 511 OHM 1% 1/8W
A37R19	0757-0394		R FXD 51.1 OHM 1% 1/8W
A37R20	0757-1040		R FXD 50 OHM 1% 1/4W
A37R21	0698-4037		R FXD 46.4 OHM 1% 1/8W
A37R22	0757-0401		R FXD 100 OHM 1% 1/8W
A37R23	0698-4037		R FXD 46.4 OHM 1% 1/8W
A37R24	0698-3132		R FXD 261 OHM 1% 1/8W
A37R25	0757-0276	1	R FXD 61.9 OHM 1% 1/8W
A37R26	0757-0416		R FXD 511 OHM 1% 1/8W
A37R27	0698-0082		R FXD 464 OHM 1% 1/8W
A37R28	0757-0394		R FXD 51.1 OHM 1% 1/8W
A37R29	0757-0394		R FXD 51.1 OHM 1% 1/8W
A37R30	0757-0394		R FXD 51.1 OHM 1% 1/8W
A37R31	0698-3132		R FXD 261 OHM 1% 1/8W
A37R32	0698-3132		R FXD 261 OHM 1% 1/8W
A37R33	0698-3132		R FXD 261 OHM 1% 1/8W
A37R34	0698-3437		R FXD 133 OHM 1% 1/8W
A37R35	0698-3132		R FXD 261 OHM 1% 1/8W
A37R36	0698-3132		R FXD 261 OHM 1% 1/8W
A37R37	0698-3132		R FXD 261 OHM 1% 1/8W
A37R38	0698-3132		R FXD 261 OHM 1% 1/8W
A37R39	0698-3132		R FXD 261 OHM 1% 1/8W
A37R40	0698-3437		R FXD 133 OHM 1% 1/8W
A37R41	0757-0399		R FXD 82.5 OHM 1% 1/8W
A37R42	0698-3132		R FXD 261 OHM 1% 1/8W
A37R43	0698-3132		R FXD 261 OHM 1% 1/8W
A37R44	0698-3132		R FXD 261 OHM 1% 1/8W
A37R45	0698-3132		R FXD 261 OHM 1% 1/8W
A37R46	0698-3132		R FXD 261 OHM 1% 1/8W
A37R47	0698-3132		R FXD 261 OHM 1% 1/8W
A37R48	0757-0405	1	R FXD 162 OHM 1% 1/8W

Abbreviations are listed in the introduction to this section

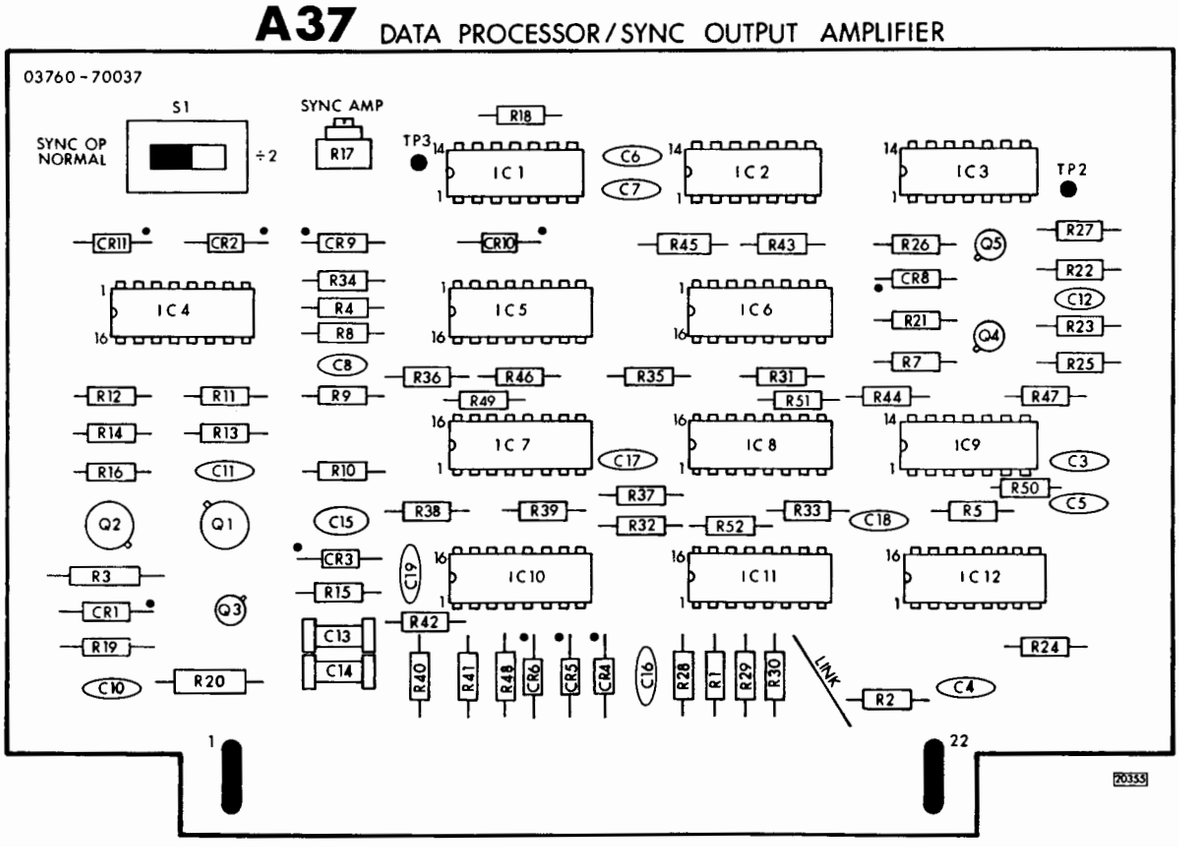

Figure A37-3 Component Location

A37 DATA PROCESSOR / SYNC OUTPUT AMPLIFIER (03760-70037)

NOTE: FOR IC POWER SUPPLY CONNECTIONS SEE PAGE 6-8

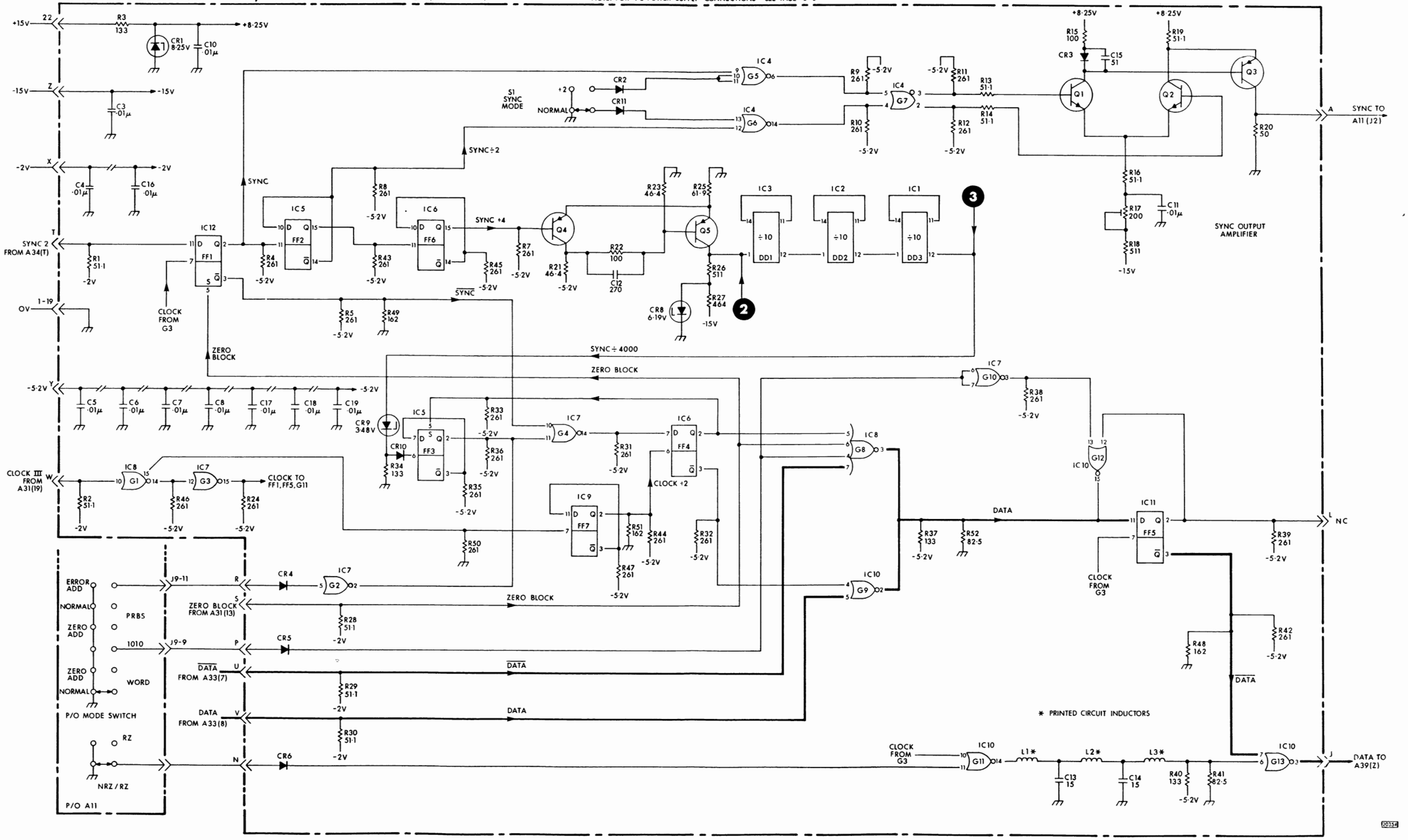

Figure A37-4 Schematic Diagram

ASSEMBLY SERVICE SHEET A38

DATA LEVEL CONTROL AMPLIFIER A38

TAIL CURRENT CONTROL

The tail currents of the second and third emitter coupled pairs in the Data Output Amplifier, A39, are controlled by Q1 and Q2 respectively. The collector currents of these transistors are in turn controlled by the AMPLITUDE VERNIER via the operational amplifier, IC3 and buffer Q3.

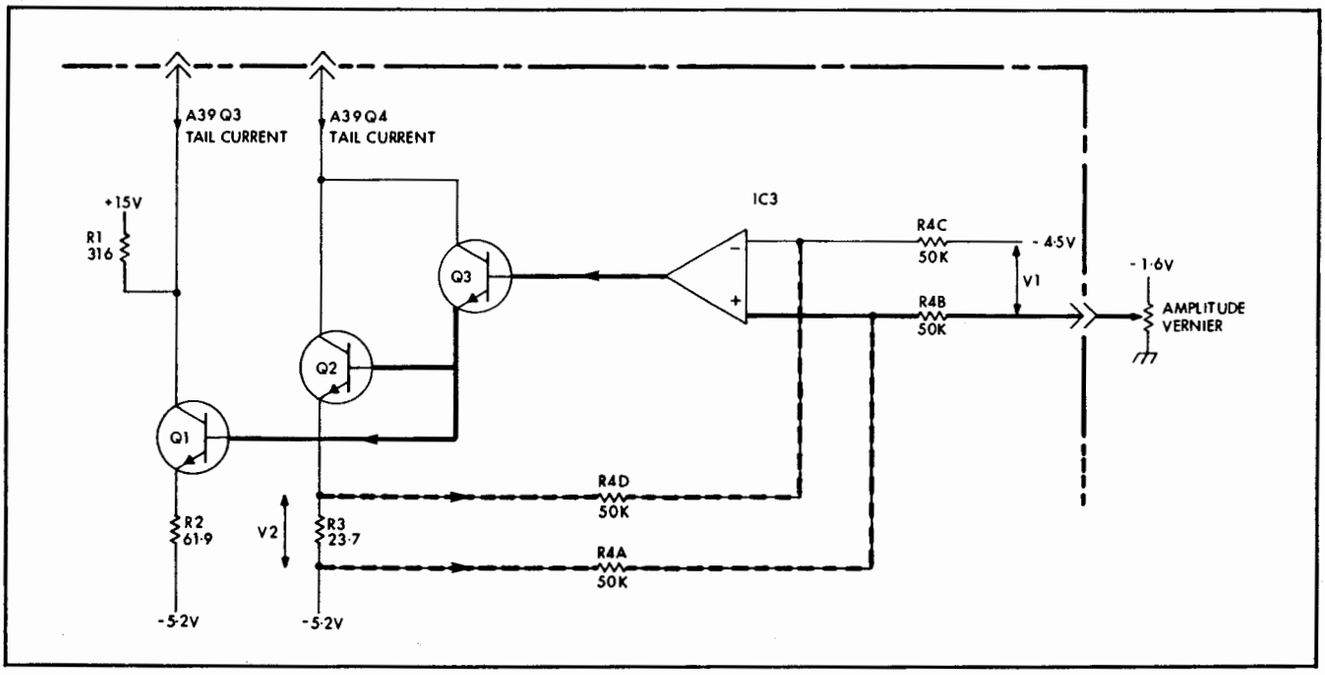

Figure A38-1 Tail Current Control

The collector current of Q2 (tail current of A39Q4) is stabilised by monitoring the voltage drop it generates across R3 and feeding it back via precision resistors R4A and R4D to the differential inputs of IC3. The circuit is stable when the + and - inputs to IC3 are equal, ie, when the differential input is 0. As R4A, B, C and D are all 50K this occurs when V2 = V1. R4C is connected to a fixed bias of -4.5V while the input from the AMPLITUDE VERNIER to R4B varies between -1.6V at minimum output to 0V at maximum. V2 (the voltage drop across R2) therefore varies between 2.9 and 4.5V producing a tail current in the third emitter coupled pair of approximately 125 to 190mA. This feedback arrangement not only gives the circuit a high degree of temperature stability but also provides immunity from ripple etc. on the -5.2V supply line.

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The tail current of the first emitter coupled pair flowing through Q1 is not directly stabilised. However, as the forward base-emitter voltage drop of Q1 is almost equal to that of Q2, the voltage drop across R2 is almost equal to V2. R1 is connected to the +15V supply line to balance out the current drawn from the -15V supply to A39R16 in the Data Amplifier. The net tail current of the second emitter coupled pair therefore varies between approximately 40mA at minimum and 70mA at maximum output amplitude.

OUTPUT AMPLITUDE CONTROL VOLTAGE

The Output Amplitude Control Voltage is generated by the operational amplifier IC2. The +input to IC2 is biased to +5.9V by a potential divider and feedback from the output via R4E stabilises the circuit with the -input also held at +5.9V. The input from the AMPLITUDE VERNIER varies between -1.6V at minimum to 0V at maximum output and since R4E and R4F are equal, the Output Amplitude Control Voltage varies between +13.4 and +11.8V.

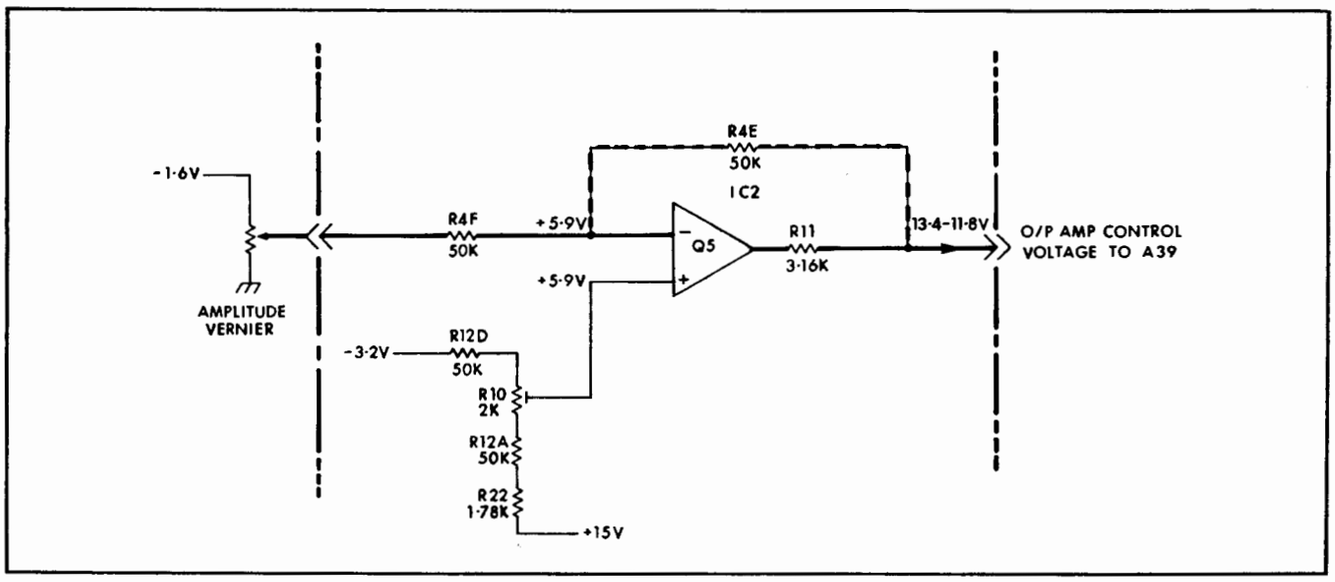


Figure A38-2 Amplitude Control Voltage

BALANCE CURRENT CONTROL

The Balance Currents are controlled by the AMPLITUDE VERNIER via the operational amplifier IC1 and the current amplifier Q4. This current, equal to half that being switched by the output transistor, A38Q7 in the Data Output Amplifier, is stabilised by monitoring the voltage drop it produces across R13 and feeding it back via precision resistors to the differential inputs of IC1. This feedback stabilises the circuit with the differential inputs of IC1 equal to 0V and since R12E, F, G and H are all equal, this occurs when V2 = V1. R12G is connected to a fixed bias of -3.2V while the input from the AMPLITUDE VERNIER to R12E varies between -1.6V at minimum and 0V at maximum output. V2 (the voltage drop across R13) therefore varies between 1.6 and 3.2V producing a Balance Current varying between 32 and 64mA over the amplitude range.

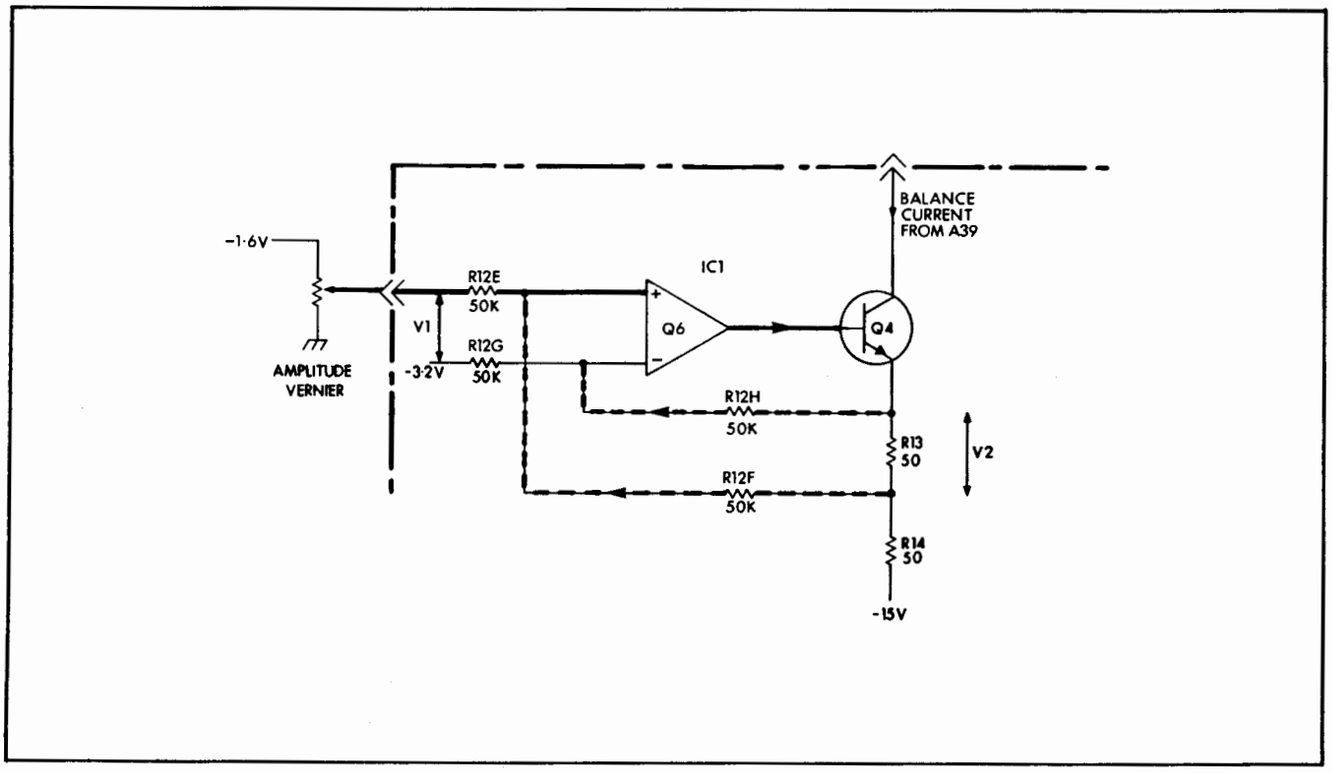


Figure A38-3 Balance Current Control

DC OFFSET AMPLIFIER

When a positive dc offset is required, Q5, Q7 and Q9 are forward biased allowing positive currents proportional to the setting of the DC OFFSET VERNIER to flow in the load. The effective collector load of Q9 is 25Ω (50Ω load in parallel with the 50Ω output impedance of the Attenuator) and hence its collector current must vary between 0 and 120mA to generate the offset voltage range of 0 to +3V. As the output of the Data Amplifier is balanced (no dc offset) and the output impedance of the Attenuator is always 50Ω, the offset and amplitude levels of the DATA OUTPUT are completely independent of one another.

Negative offsets are generated by forward biasing Q6, Q8 and Q10 to allow negative currents to flow in the load.

Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A38	03760-70038		DATA LEVEL CONTROL AMP ASSY
	03760-70638		DATA LEVEL CONTROL AMP ASSY OPT 001/3
A38C1	0160-2199		C FXD 30PF 5% 300WVDC
A38C2	0150-0121		C FXD 0.1UF +80-20% 50WVDC
A38C3	0160-2199		C FXD 30PF 5% 300WVDC
A38C4	0160-2199		C FXD 30PF 5% 300WVDC
A38C5	0150-0121		C FXD 0.1UF +80-20% 50WVDC
A38C6	0150-0121		C FXD 0.1UF +80-20% 50WVDC
A38CR1	1902-0509		DIO BKDN 6.2V 2% TEMP COMP
A38CR2	1901-0047		DIO SI
A38CR3	1901-0047		DIO SI
A38IC1	1820-0477		IC OPER AMPL
A38IC2	1820-0477		IC OPER AMPL
A38IC3	1820-0477		IC OPER AMPL
A38Q1	1854-0039		XSTR SI NPN
A38Q2	1854-0039		XSTR SI NPN
	1205-0011		HEAT DISSIPATOR XSTR
A38Q3	1854-0071		XSTR SI NPN
A38Q4	1854-0039		XSTR SI NPN
	1205-0011		HEAT DISSIPATOR XSTR
A38Q5	1854-0071		XSTR SI NPN
A38Q6	1853-0020		XSTR SI PNP
A38Q7	1853-0020		XSTR SI PNP
A38Q8	1854-0071		XSTR SI NPN
A38Q9	1853-0210		XSTR PNP SILICON
	1205-0011		HEAT DISSIPATOR XSTR
A38Q10	1205-0011		HEAT DISSIPATOR XSTR
A38Q10	1854-0039		XSTR SI NPN
A38R1	0698-0087		R FXD 316 OHM 1% 1/4W
A38R2	0698-7660		R FXD 61.9 OHM 1% 1/4W
A38R3	0698-3392		R FXD 23.7 OHM 1% 1/2W
	0698-5021		R FXD 35.7 OHM 1% 1/2W●
A38R4	1810-0150		R FXD NETWORK 4X50K
A38R5	0698-6635		R FXD 880 OHM 1% 1/8W
A38R6	0698-4462		R FXD 768 OHM 1% 1/8W
A38R7	2100-2574		R VAR 500 OHM 10% 1/2W
A38R8	0757-0416		R FXD 511 OHM 1% 1/8W
A38R8	0757-0416		R FXD 511 OHM 1% 1/8W
A38R9	0698-4125		R FXD 953 OHM 1% 1/8W
A38R10	2100-2521		R VAR 2K OHM 10% 1/2W LIN
A38R11	0757-0279		R FXD 3.16K OHM 1% 1/8W
A38R12	1810-0150		R FXD NETWORK 4X50K
A38R13	0757-0398		R FXD 75 OHM 1% 1/8W
A38R13	0698-4393		R FXD 73.2 OHM 1% 1/8W
A38R14	0698-4381	1	
	0757-0398		R FXD 75 OHM 1% 1/8W●
A38R15	0698-3151		R FXD 2.87K OHM 1% 1/8W
	0698-3151		R FXD 2.87K OHM 1% 1/8W●
A38R16	0757-0280		R FXD 1K OHM 1% 1/8W
A38R17	0757-0280		R FXD 1K OHM 1% 1/8W
A38R18	0757-0280		R FXD 1K OHM 1% 1/8W
A38R19	0757-0280		R FXD 1K OHM 1% 1/8W
A38R20	0698-3395		R FXD 34.8 OHM 1% 1/4W
	0757-1000		R FXD 51.1 OHM 1% 1/2W●
A38R21	0698-3395		R FXD 34.8 OHM 1% 1/4W
	0757-1000		R FXD 51.1 OHM 1% 1/2W●
A38R22	0757-0401		R FXD 100 OHM 1% 1/8W
	0757-0401		R FXD 100 OHM 1% 1/8W●

●OPTIONS 001/003

Abbreviations are listed in the introduction to this section

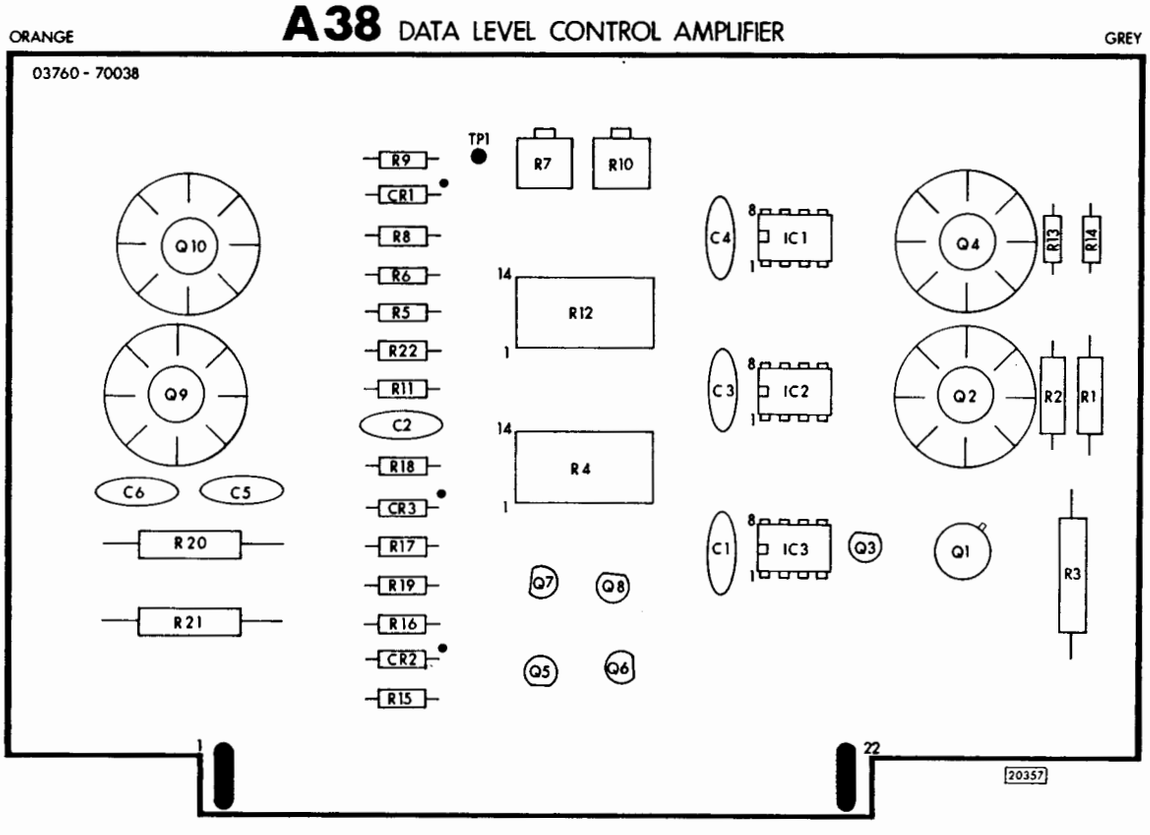
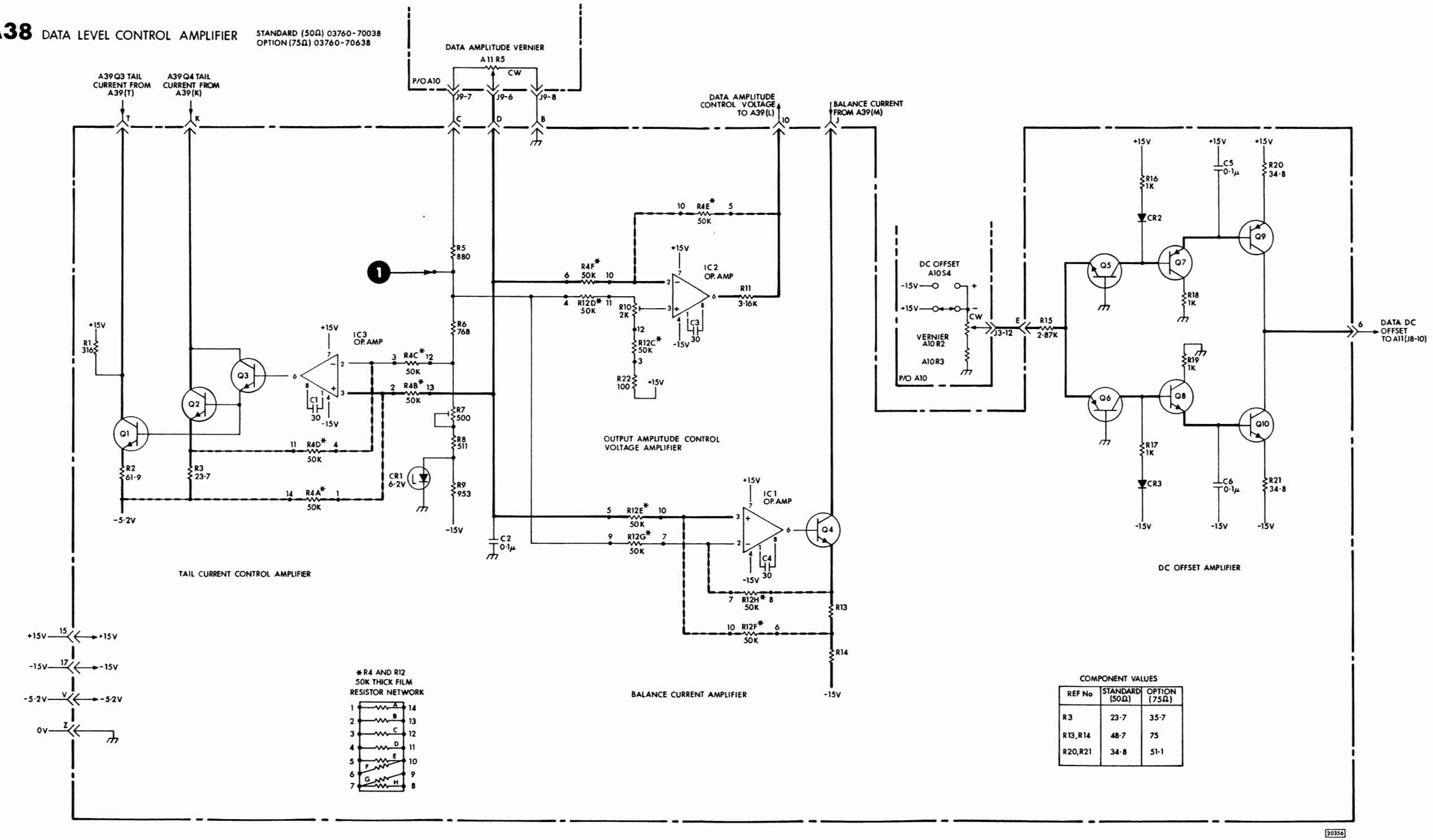


Figure A38-4 Component Location

A38 DATA LEVEL CONTROL AMPLIFIER

STANDARD (50Ω) 03760-70038
OPTION (75Ω) 03760-70638



COMPONENT VALUES

REF No	STANDARD (50Ω)	OPTION (75Ω)
R3	23·7	35·7
R13, R14	48·7	75
R20, R21	34·8	51·1

Figure A38-5 Schematic Diagram

ASSEMBLY SERVICE SHEET A39

DATA AMPLIFIER A39

INPUT LOGIC

The output logic selection, DATA or $\overline{\text{DATA}}$ is made in the input logic of this amplifier. In the DATA mode the input signal, logically equal to CLOCK, drives Q8 via G2 while in $\overline{\text{DATA}}$ it drives Q8 via G1 and G4. The dc offset of the signal applied to G4 can be altered by R42 thus allowing the width of the data mark to be adjusted.

The output levels of the MECL III gates G2 and G4 (-0.8V and -1.7V) are modified by the level translator Q8 to make them compatible with the logic levels of the EECL schmitt trigger (0 and -0.5V). The small variation in these levels provided by R3 allows the mark to space ratio of the input data signal to be accurately reproduced at the output.

CURRENT AMPLIFIERS

Three cascaded emitter coupled pairs provide the current amplification required to switch the output transistor. Printed circuit inductors in series with the resistive loads of the schmitt trigger and the first emitter coupled pair counteract the "rounding-off" effect which the capacitive inputs of the following stages have on the switching signal. Two transistors in parallel are required for each side of the second and third emitter coupled pairs to switch the high currents associated with these stages. The tail currents of Q3 and Q4 are varied in proportion to the amplitude of the output by the Data Level Control Amplifier, the reason for this is discussed later.

When Q4C and Q4D are switched on, their collector voltages lie between +12V and +10.2V depending upon the setting of the output AMPLITUDE VERNIER. As the corresponding range of voltage applied to the base of the output transistor Q7 is +13.4V to +11.8V, it is always reverse biased when Q4C and Q4D are conducting. When this side of the emitter coupled pair turns off, Q7 becomes forward biased, its collector current being determined by the voltage applied to its base and varies between 64mA at minimum output and 128mA at maximum output. As the collector load of Q7 is effectively 25Ω (R38 and R39) in parallel with the input impedance of the Attenuator) the output amplitude varies between a minimum of 1.6V pk-pk and a maximum of 3.2V pk-pk. To equalise the loading on each side of the third emitter coupled pair, Q4A and Q4B drive a dummy output stage, Q5.

BALANCE CURRENT

If no current were passed through the load by the Data Level Control Amplifier, the output would switch between 0V when Q7 was off and a positive voltage when Q7 was switched on, ie the output would have a positive dc offset equal to half the amplitude of the output pulses as shown in Figure A39-1. To achieve zero dc offset, a negative balance current equal to half that being switched by Q7 is passed through the load via L5. Thus when Q7 is turned off, this current generates a negative voltage across the load equal to half the peak to peak value of the output pulse. When Q5 is turned on, the current in the load reverses and an equal value positive voltage is developed across the load as shown in Figure A39-1.

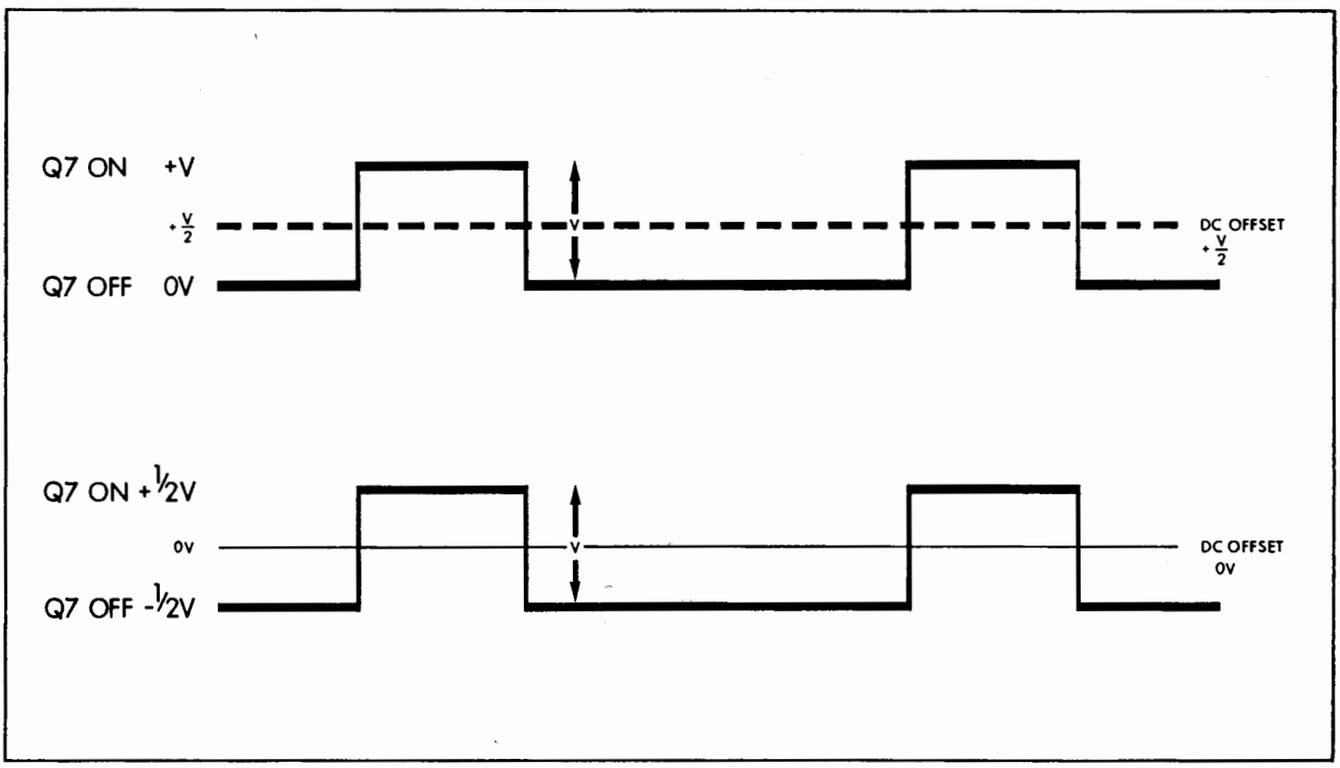


Figure A39-1 Balance Current

OVERSHOOT

Due to the fast switching action of the emitter coupled pairs a certain amount of overshoot is introduced into the switching signal. This overshoot which appears on the output, is proportional to the amount of current being switched and to the speed at which it is switched. A small percentage overshoot ensures fast rise time pulses, however if the tail currents of the emitter coupled pairs were held constant, the amplitude of the overshoot would also remain constant and become increasingly more significant as the output amplitude was reduced. To keep the percentage overshoot approximately constant over the output amplitude range, the tail currents of the second and third emitter coupled pairs are reduced as the output amplitude is reduced. The amount of overshoot present on the output can be adjusted by C17.

Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A39	03760-70029		DATA OUTPUT AMP ASSY
	03760-70629		DATA OUTPUT AMP ASSY OPTION 001/003
A39C1	0150-0093		C FXD 0.01UF +80 -10% 100WVDC
A39C2	0180-1745		C FXD 1.5UF 10% 20WVDC
A39C4	0150-0093		C FXD 0.01UF +80 -10% 100WVDC
A39C5	0150-0093		C FXD 0.01UF +80 -10% 100WVDC
A39C6	0160-2199		C FXD 30PF 5% 300WVDC
A39C7	0160-2266		C FXD 24PF 5% 500WVDC
A39C8	0150-0093		C FXD 0.01UF +80 -10% 100WVDC
A29C9	0150-0093		C FXD 0.01UF +80 -10% 100WVDC
A39C10	0150-0093		C FXD 0.01UF +80 -10% 100WVDC
A39C11	0150-0093		C FXD 0.01UF +80 -10% 100WVDC
A39C12	0150-0093		C FXD 0.01UF +80 -10% 100WVDC
A39C13	0150-0093		C FXD 0.01UF +80 -10% 100WVDC
A39C15	0150-0050		C FXD 1000PF +80 -20% 1000WVDC
A39C17	0121-0046		C VAR 9-35PF
A39C20	0150-0093		C FXD 0.01UF +80 -10% 100WVDC
A39C23	0180-0228		C FXD 22UF 10% 15WVDC
A39CR1	1901-0047		DIO SI
A39CR3	1902-0048		DIO BKDN 6.81V 400MW
A39CR4	1901-0533		DIO SI
A39CR5	1901-0533		DIO SI
A39IC1	1820-0285		IC SCHMITT TRIGGER 250MHz ECL
A39IC2	1820-0796		IC QUAD 2-INPUT NOR GATE ECL
A39J1	1250-1255		CONN COAX PC BD MTG CONHEX 50 OHM
	1250-0932		CONN COAX PC BD MTG CONHEX ●
A39L5	9100-1645		INDUCTOR 390UH 5%
	9100-1653		IND FXD 910UH 5% ●
A39L6	03760-70209		IND ASSY
A39Q1	1854-0345		XSTR NPN SILICON
	1205-0037		HEAT DISSIPATOR XSTR
A39Q2	1854-0345		XSTR NPN SILICON
	1205-0037		HEAT DISSIPATOR XSTR
A39Q3	1858-0029		XSTR QUAD NPN SILICON
A39Q4	1858-0031		XSTR QUAD NPN SILICON
A39Q5	1853-0210		XSTR PNP SILICON
	03760-30200		HEAT DISSIPATOR XSTR
A39Q6	1854-0071		XSTR SI NPN
A39Q7	1853-0201		XSTR PNP SILICON
	03760-30200		HEAT DISSIPATOR XSTR
A39Q8	1853-0018		XSTR-PNP SILICON
A39R1	0757-0399		R FXD 82.5 OHM 1% 1/8W
A39R2	0698-3437		R FXD 133 OHM 1% 1/8W
A39R3	2100-2632		R VAR 100 OHM 10% 1/2W
A39R4	0698-4261		R FXD 2K OHM 5% 1/8W
A39R5	0757-0416		R FXD 511 OHM 1% 1/8W
A39R6	0698-3446		R FXD 383 OHM 1% 1/8W
A39R7	0698-3437		R FXD 133 OHM 1% 1/8W

●OPTIONS 001/003

Abbreviations are listed in the introduction to this section

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Replaceable Parts (continued)

Ref Desig	HP Part No	TQ	Description
A39R8	0757-0394		R FXD 51.1 OHM 1% 1/8W
A39R9	0757-0394		R FXD 51.1 OHM 1% 1/8W
A39R10	0757-0394		R FXD 51.1 OHM 1% 1/8W
A39R11	0757-0804		R FXD 200 OHM 1% 1/2W
A39R12	0757-0401		R FXD 100 OHM 1% 1/8W
A39R13	0698-4593		R FXD 464 OHM 1% 1/4W
A39R14	0757-0394		R FXD 51.1 OHM 1% 1/8W
A39R15	0757-0394		R FXD 51.1 OHM 1% 1/8W
A29R16	0757-0815		R FXD 562 OHM 1% 1/2W
A39R17	0757-0394		R FXD 51.1 OHM 1% 1/8W
A39R18	0757-0394		R FXD 51.1 OHM 1% 1/8W
A39R19	0757-0284		R FXD 150 OHM 1% 1/8W
A39R20	0757-0394		R FXD 51.1 OHM 1% 1/8W
A39R21	0757-0284		R FXD 150 OHM 1% 1/8W
A29R22	0757-0394		R FXD 51.1 OHM 1% 1/8W
A29R23	0757-0394		R FXD 51.1 OHM 1% 1/8W
A39R24	0757-1040		R FXD 50 OHM 1% 1/4W
A39R25	0757-0496		R FXD 20 OHM 1% 1/4W
	0757-1040		R FXD 50 OHM 1% 1/4W ●
A39R26	0757-1040		R FXD 50 OHM 1% 1/4W
	0757-0710		R FXD 75 OHM 1% 1/4W ●
A39R27	0757-1040		R FXD 50 OHM 1% 1/4W
	0757-0710		R FXD 75 OHM 1% 1/4W ●
A39R28	0757-1040		R FXD 50 OHM 1% 1/4W
	0757-0710		R FXD 75 OHM 1% 1/4W●
A39R29	0757-1040		R FXD 50 OHM 1% 1/4W
A39R30	0757-0991		R FXD 20 OHM 1% 1/2W
	0757-1040		R FXD 50 OHM 1% 1/4W ●
A39R31	0757-1040		R FXD 50 OHM 1% 1/4W
	0757-0710		R FXD 75 OHM 1% 1/4W ●
A39R32	0757-0384		R FXD 20 OHM 1% 1/8W
A39R33	2100-1984		R VAR 100 OHM 10% 1/2W LIN
A39R34	0757-0178		R FXD 100 OHM 1% 1/4W
	0757-0715		R FXD 150 OHM 1% 1/4W ●
A39R35	0757-0178		R FXD 100 OHM 1% 1/4W
	0757-0715		R FXD 150 OHM 1% 1/4W ●
A39R36	0757-0280		R FXD 1K OHM 1% 1/8W
A39R37	0698-3404		R FXD 383 OHM 1% 1/2W
A39R38	0757-0178		R FXD 100 OHM 1% 1/4W
	0757-0715		R FXD 150 OHM 1% 1/4W ●
A39R39	0757-0178		R FXD 100 OHM 1% 1/4W
	0757-0715		R FXD 150 OHM 1% 1/4W ●
A39R40	0698-3154		R FXD 4.22K OHM 1% 1/8W
	0757-0439		R FXD 6.81K OHM 1% 1/8W ●
A39R41	0698-3154		R FXD 4.22K OHM 1% 1/8W
	0757-0439		R FXD 6.81K OHM 1% 1/8W ●
A39R42	0757-0399		R FXD 82.5 OHM 1% 1/8W
A39R43	0698-3132		R FXD 261 OHM 1% 1/8W
A39R44	0757-0384		R FXD 20 OHM 1% 1/8W
A39R45	0698-3444		R FXD 316 OHM 1% 1/8W
	0698-0082		R FXD 464 OHM 1% 1/8W ●

*OPTIONS 001/003

Abbreviations are listed in the introduction to this section

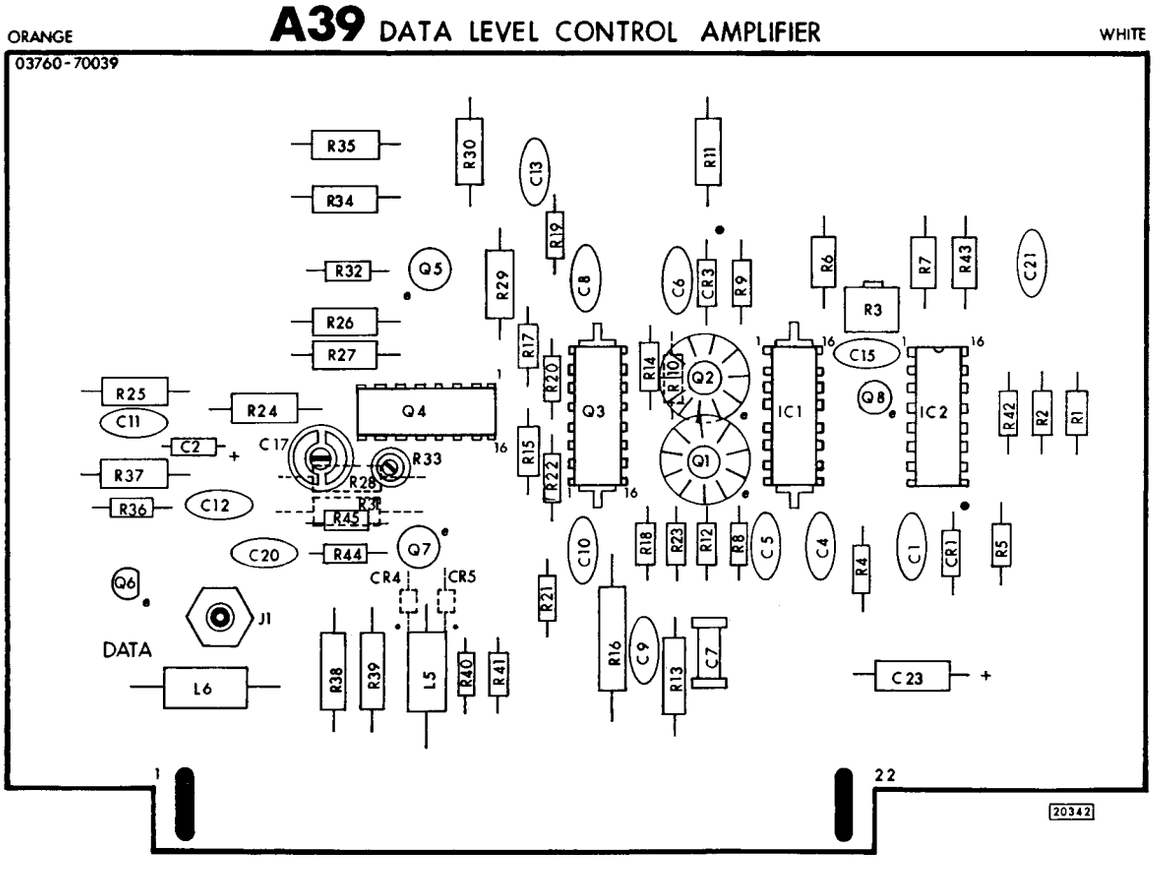
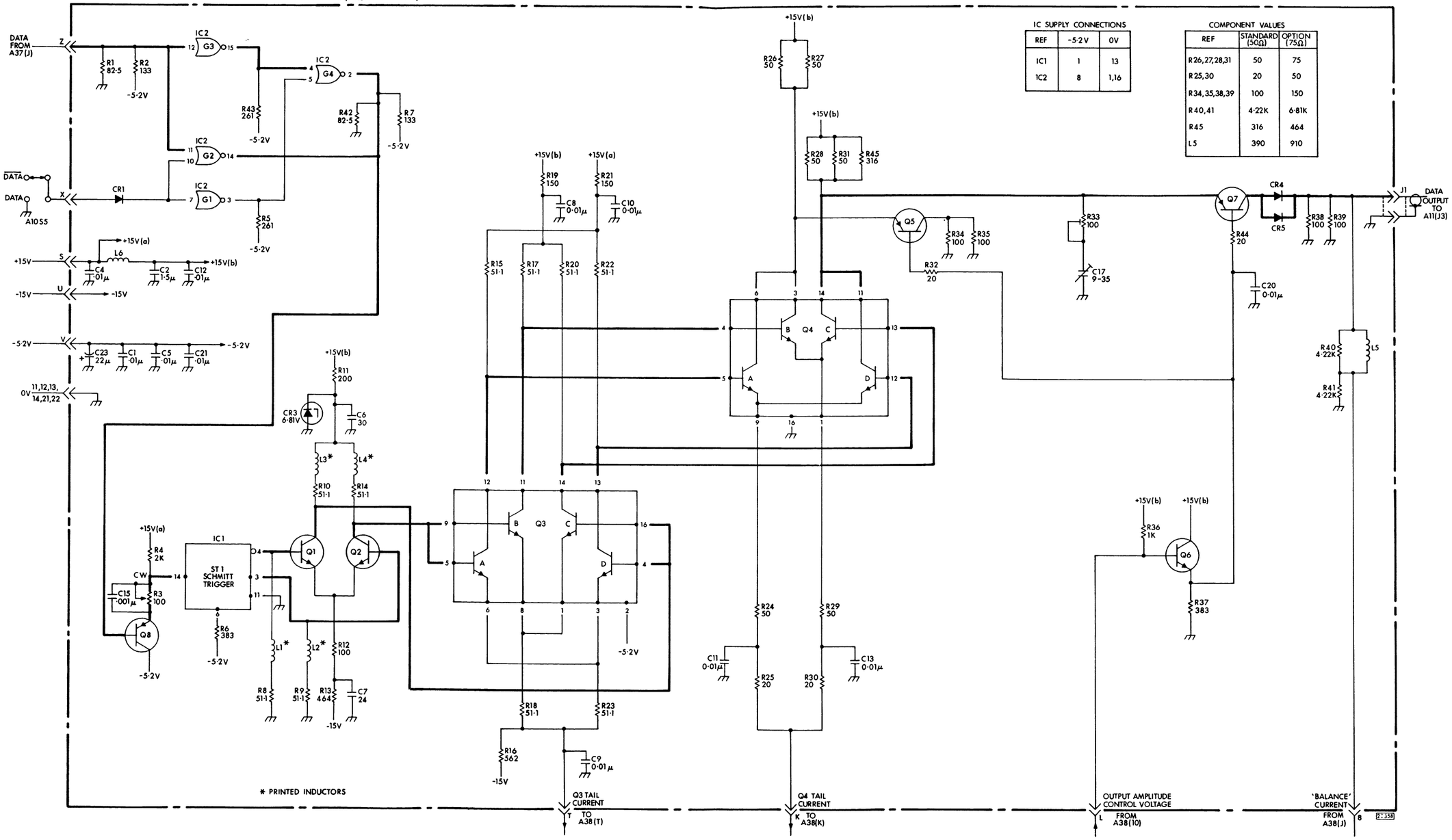


Figure A39-2 Component Location

A39 DATA OUTPUT AMPLIFIER

STANDARD (50Ω) 03760-70039
OPTION 001/003 (75Ω 03760-70639)



IC SUPPLY CONNECTIONS

REF	-5·2V	0V
IC1	1	13
IC2	8	1,16

COMPONENT VALUES

REF	STANDARD (50Ω)	OPTION (75Ω)
R26,27,28,31	50	75
R25,30	20	50
R34,35,38,39	100	150
R40,41	4·22K	6·81K
R45	316	464
L5	390	910

Figure A39-3 Schematic Diagram

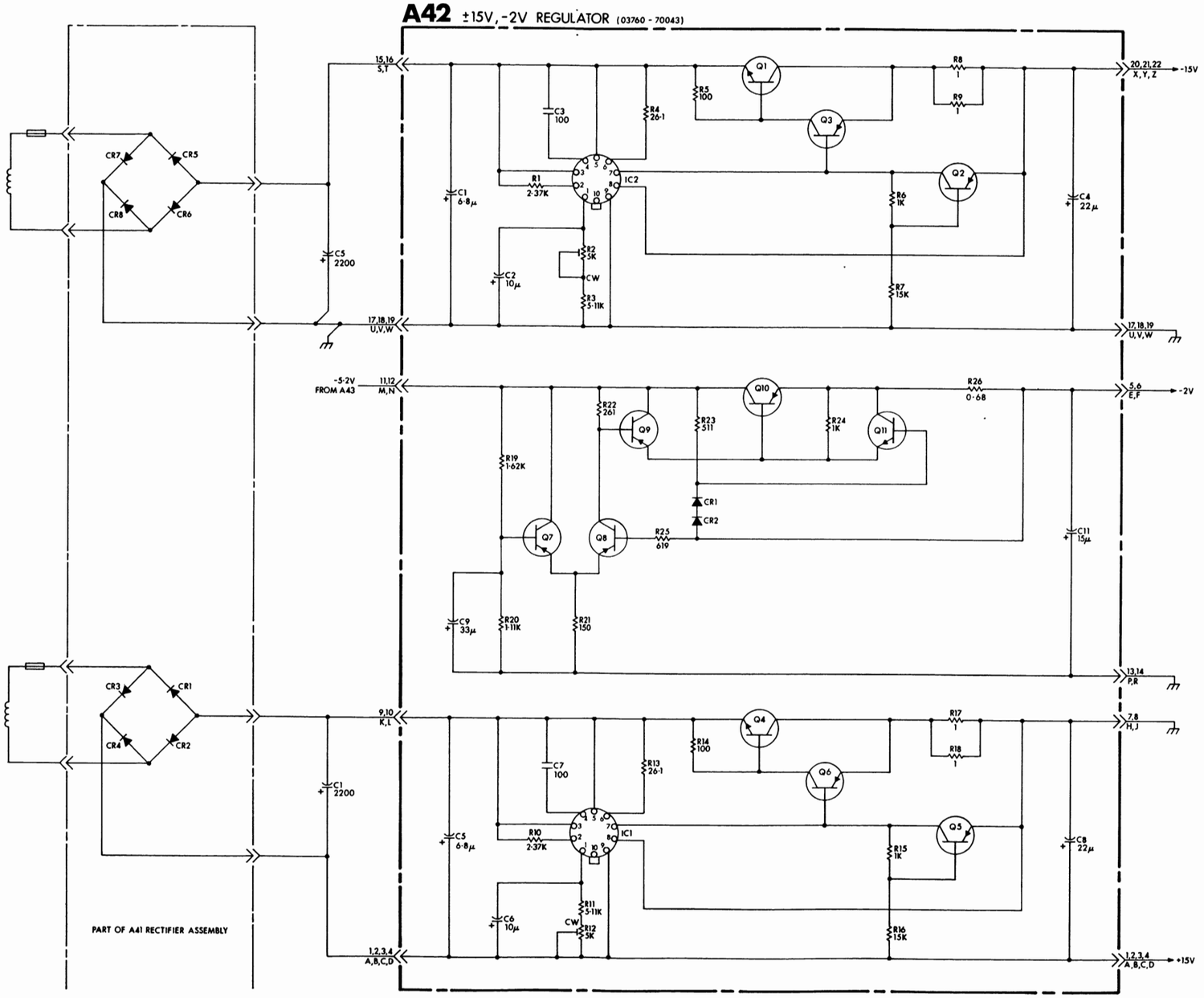


Figure A42-3 Schematic Diagram

Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A42	03760-10417		HEAT SINK
A42	03760-70042		15V REGULATOR ASSY
A42	03760-10417	2	HEAT SINK BRACKET
A42C1	0180-0116	3	C FXD 6.8UF 10% 35WVDC
A42C2	0180-0374	2	C FXD 10UF 10% 20WVDC
A42C3	0150-0050		C FXD 1000PF +80-20% 1000WVDC
A42C4	0180-0160	2	C FXD 22UF 20% 35VDCW
A42C5	0180-0116		C FXD 6.8UF 10% 35WVDC
A42C6	0180-0374		C FXD 10UF 10% 20WVDC
A42C7	0150-0050		C FXD 1000PF +80-20% 1000WVDC
A42C8	0180-0160		C FXD 22UF 20% 35VDCW
A42C9	0180-0229	3	C FXD 33UF 10% 10WVDC
A42C11	0180-1746	2	C FXD 15UF 10% 20WVDC
A42CR1	1901-0040		DIO SI
A42CR2	1901-0040		DIO SI
A42IC1	1826-0004	2	IC LIN, NEG VOLT REGULATOR
A42IC2	1826-0004		IC LIN, NEG VOLT REGULATOR
A42Q1	2100-0147	1	R VAR 10K OHM 10%
A42Q1	1854-0519	2	XSTR NPN SILICON
	1205-0056	1	HEAT DISSIPATOR TO-3 TRANSISTOR
A42Q2	1853-0020		XSTR SI PNP
A42Q3	1853-0038	4	XSTR SI PNP
A42Q4	1854-0519		XSTR NPN SILICON
A42Q5	1853-0020		XSTR SI PNP
A42Q6	1853-0038		XSTR SI PNP
A42Q7	1853-0020		XSTR SI PNP
A42Q8	1853-0020		XSTR SI PNP
A42Q9	1853-0020		XSTR SI PNP
A42Q10	1853-0052	1	XSTR SI PNP
	0340-0162	1	INSULATOR XSTR
A42Q11	1854-0071		XSTR SI NPN
A42R1	0698-3150		R FXD 2.37K OHM 1% 1/8W
A42R2	2100-2489		R VAR 5K OHM 10% 1/2W
A42R3	0757-0438		R FXD 5.11K OHM 1% 1/8W
A42R4	0698-3432		R FXD 26.1 OHM 1% 1/8W
A42R5	0757-0401		R FXD 100 OHM 1% 1/8W
A42R6	0757-0280		R FXD 1K OHM 1% 1/8W
A42R7	0757-0446	2	R FXD 15K OHM 1% 1/8W
A42R8	0811-1666	4	R FXD 1 OHM 5% 2W
A42R9	0811-1666		R FXD 1 OHM 5% 2W
A42R10	0698-3150		R FXD 2.37K OHM 1% 1/8W
A42R11	0757-0438		R FXD 5.11K OHM 1% 1/8W
A42R12	2100-2489		R VAR 5K OHM 10% 1/2W
A42R13	0698-3432		R FXD 26.1 OHM 1% 1/8W
A42R14	0757-0401		R FXD 100 OHM 1% 1/8W
A42R15	0757-0280		R FXD 1K OHM 1% 1/8W
A42R16	0757-0446		R FXD 15K OHM 1% 1/8W
A42R17	0811-1666		R FXD 1 OHM 5% 2W
A42R18	0811-1666		R FXD 1 OHM 5% 2W
A42R19	0757-0428		R FXD 1.62K OHM 1% 1/8W
A42R20	0757-0424	1	R FXD 1.1K OHM 1% 1/8W
A42R21	0757-0284		R FXD 150 OHM 1% 1/8W
A42R22	0698-3132		R FXD 261 OHM 1% 1/8W
A42R23	0757-0416		R FXD 511 OHM 1% 1/8W
A42R24	0757-0280		R FXD 1K OHM 1% 1/8W
A42R25	0757-0418		R FXD 619 OHM 1% 1/8W
A42R26	0811-1553	1	R FXD WW .680HM 5% 2W

Abbreviations are listed in the introduction to this section

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±15V REGULATORS

As these circuits are identical only the -15V regulator will be described in detail. To boost the current handling capability of the LM304, a current amplifier consisting of Q1 and Q2 has been included in the circuit. Overcurrent protection for Q1 and Q2 is provided by Q3 which turns on when the voltage drop across R8 and R9 exceeds a preset level. This removes the drive to Q2 thus turning the series regulator Q1 off.

-2V REGULATOR

The reference voltage to the error amplifier, Q7 & Q8 is set by the ratio of R19 and R20. Q8 drives the series regulator Q10 via Q9 and feedback to the base of Q8 stabilizes the output at V_{REF} ie, -2V. Overcurrent protection is provided by Q11 which turns on if the voltage drop across the sense resistor R26 exceeds a preset value. This effectively short circuits the base emitter of Q10 thus turning the series regulator off.

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ASSEMBLY SERVICE SHEET A42

±15V & -2V REGULATOR A42

INTRODUCTION

The +15V and -15V power supplies are stabilized by identical linear regulators based on the LM304A Negative Voltage Regulator. The -2V supply is obtained from the -5.2V supply and is stabilized by the linear regulator consisting of Q7 to Q11.

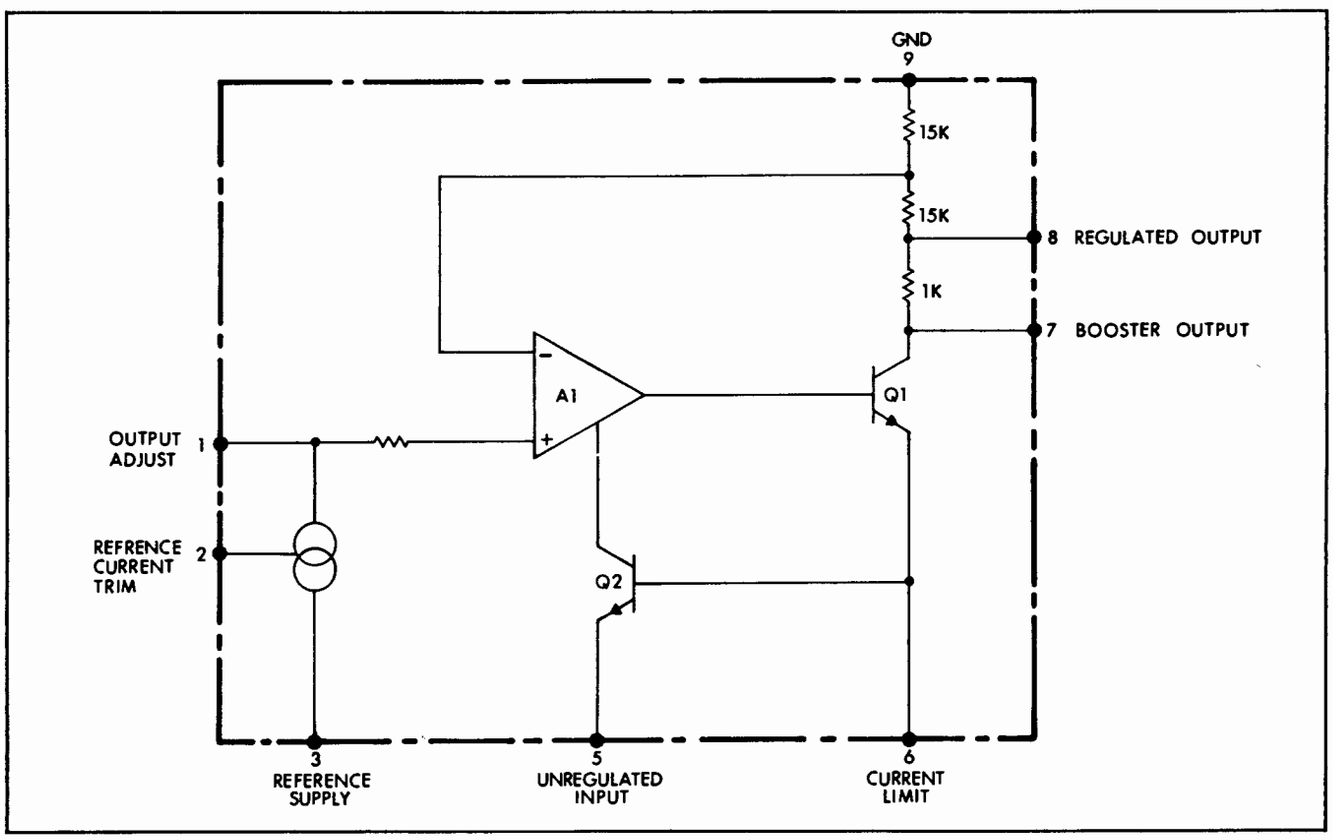

Figure A42-1 LM304A Voltage Regulator

LM304A VOLTAGE REGULATOR

The reference current for the LM304A Voltage Regulator is obtained from an internal constant current source supplied via Pin 3. An external resistor connected between Pin 1 and ground sets the reference voltage V_{REF} at the +input to the error amplifier A1. Feedback from the output to the -input of A1 stabilizes the output voltage at a value equal to $2V_{REF}$ (only half Vo is fed back.)

The regulator can be protected from short circuits by connecting a resistor between Pin 6 and the unregulated input at Pin 5. If the voltage drop across the resistor (proportional to output current) exceeds approximately 0.6V, Q2 is turned on to limit the output current to a safe value.

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ASSEMBLY SERVICE SHEET A41

RECTIFIER
ASSEMBLY A41

COMPONENT LOCATION

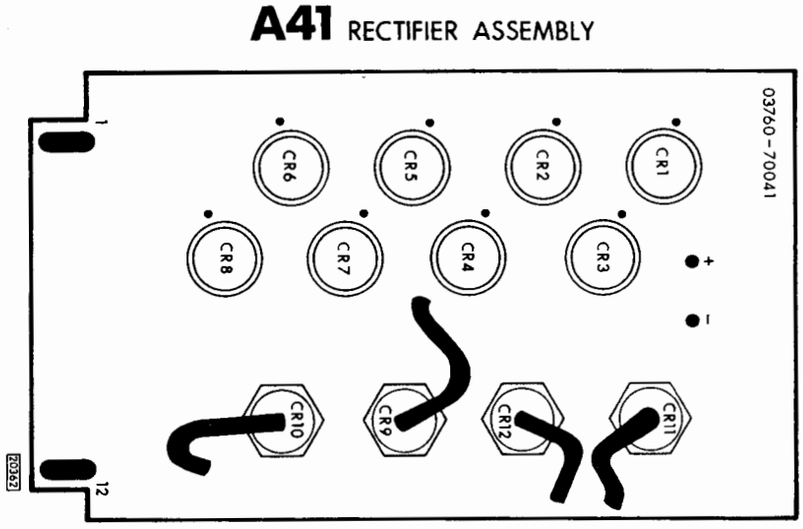

Figure A41-1 Component Location

Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A41	03760-70041		RECTIFIER ASSY
A41CR1	1901-0200	8	DIO SI
A41CR2	1901-0200		DIO SI
A41CR3	1901-0200		DIO SI
A41CR4	1901-0200		DIO SI
A41CR5	1901-0200		DIO SI
A41CR6	1901-0200		DIO SI
A41CR7	1901-0200		DIO SI
A41CR8	1901-0200		DIO SI
A41CR9	1901-0496	4	DIO-SILICON 100PIV 1ZA
A41CR10	1901-0496		DIO-SILICON 100PIV 1ZA
A41CR11	1901-0496		DIO-SILICON 100PIV 1ZA
A41CR12	1901-0496		DIO-SILICON 100PIV 1ZA

MECHANICAL CONSTRUCTION

To remove the Power Supply Module from the instrument proceed as follows:

(i) Remove top and bottom instrument covers.

(ii) Remove Module Screen by turning quick release catches.

(iii) Unplug the two cables connecting the Power Supply Module to the Clock and Data Modules.

(iv) Unplug the AC cable to the front panel mains on/off switch (underside).

(v) Remove the four screws holding the Power Supply Mother Board A40 to the instrument mainframe.

(vi) Remove the four screws holding the rear panel to the instrument side frames.

(vii) The module can now be withdrawn from the instrument.

The module can now be plugged into the ac mains supply and switched on using the auxiliary mains on/off switch mounted on the transformer cover.

Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A4	03760-70040	2	POWER SUPPLY MOTHERBOARD ASSY
	03760-70041	2	RECTIFIER ASSY
	03760-70042	2	15V REGULATOR ASSY
	03760-70043	2	5.2V/2V REGULATOR ASSY
	03760-70044	2	FAN DRIVER ASSY
	03760-70045	1	EXTENDER BOARD
A4B1	03760-0490	1	FAN
	03760-0217	1	FAN BLADE
	03760-10406	1	FAN HOUSING TOP
	03760-10407	1	FAN HOUSING BOTTOM
A4E1	5060-1188	1	LINE MODULE
A4F1	2110-0304	1	FUSE SLOW BLOW 1.5A 250V
	2100-0381	1	FUSED TIMED 1.5A 250V
A4F2	2110-0365	2	FUSE SLOW BLOW 4AT 250V
A4F3	2110-0051	1	FUSE SLOW BLOW 10A 250V
A4F4	2110-0365		FUSE SLOW BLOW 4AT 250V
A4MP40	03760-70400	1	POWER SUPPLY MODULE CHASSIS
A4MP41	03760-70411	1	FILTER FAN
A4MP42	03760-10405	1	SUPPORT XFMR BOTTOM
A4MP43	03760-70408	1	SUPPORT XFMR TOP
A4MP44	03760-10410	1	CLAMP CAPACITOR
A4T1	9100-0633	1	XFMR MAINS
A4W1	03760-70058	1	CABLE ASSY TRANSFORMER SECONDARY
A4W2	03760-70059	1	CABLE ASSY AC POWER
A4XF1	1400-0084	3	FUSEHOLDER
A4XF2	1400-0084		FUSEHOLDER
A4XF3	1400-0084		FUSEHOLDER

MODULE SERVICE SHEET A4

POWER SUPPLY MODULE A4

GENERAL

The following printed circuit assemblies are located in the Power Supply Module:

(i) Power Supply Mother Board A40.

(ii) Rectifier Assembly A41.

(iii) ±15V, -2V Regulator A42.

(iv) -5.2V Regulator A43.

(v) Fan Driver Assembly A44.

In addition to these printed circuit assemblies the following major components are also located in this module:

(i) AC Input Module.

(ii) Line Transformer.

(iii) Fan.

The mains on/off switch AISI and neon lamp are mounted on the Front Panel and are connected to the Power Supply Module via a three core cable. A4SI, mounted on top of the transformer cover is connected in parallel with AISI and allows the Power Supply Module to be operated outside the instrument. Normally, with the Power Supply Module fitted to the instrument this switch should always be in the OFF position.

AC INPUT MODULE

The 3760A has been designed to operate from 90 – 125V or 200 – 250V, 40 to 400Hz ac supply lines. The operating voltage is selected by a slide switch in the AC Input Module which is mounted on the rear panel. The line fuse is also located in this module and the appropriate ratings are given below.

LINE VOLTAGE	SLIDE SWITCH	F1
90 – 125V	115V	3.0A Timed
200 – 250V	230V	1.5A Timed

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Power Supply Module A4

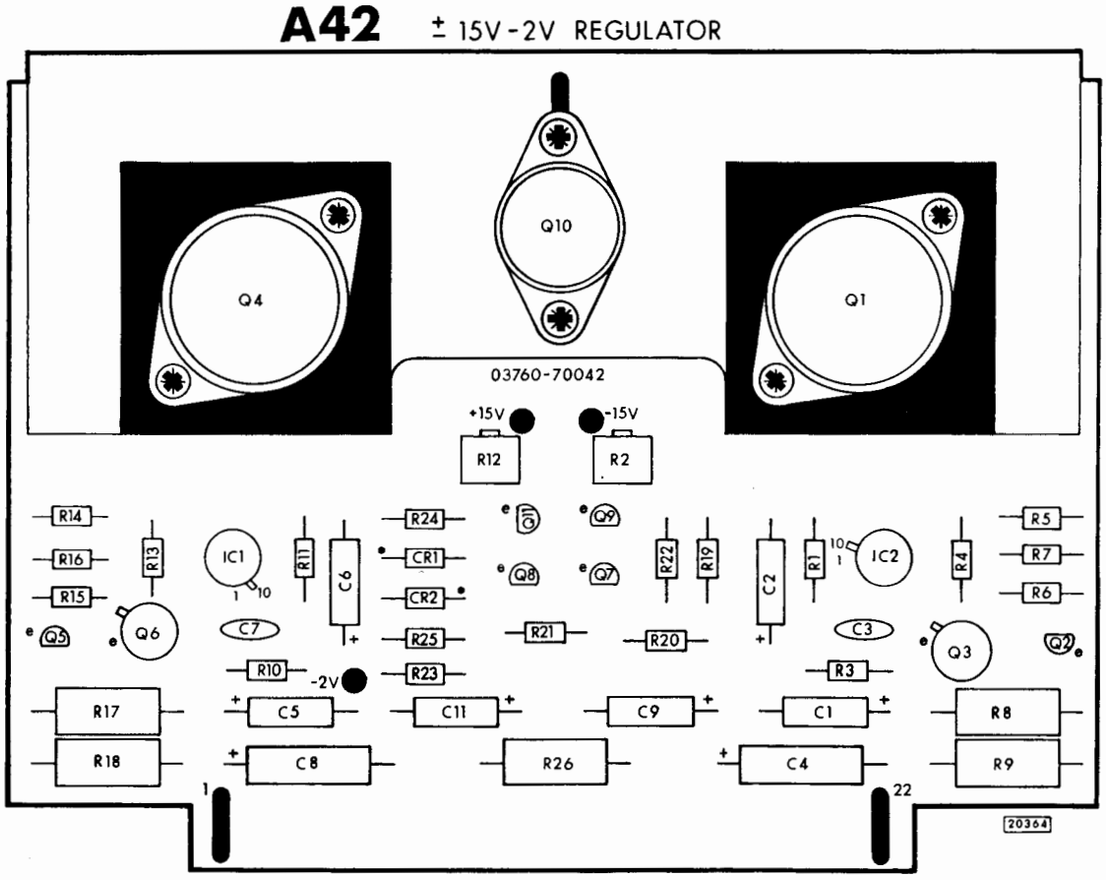

Figure A42-2 Component Location

ASSEMBLY SERVICE SHEET A43

-5.2V REGULATOR A43

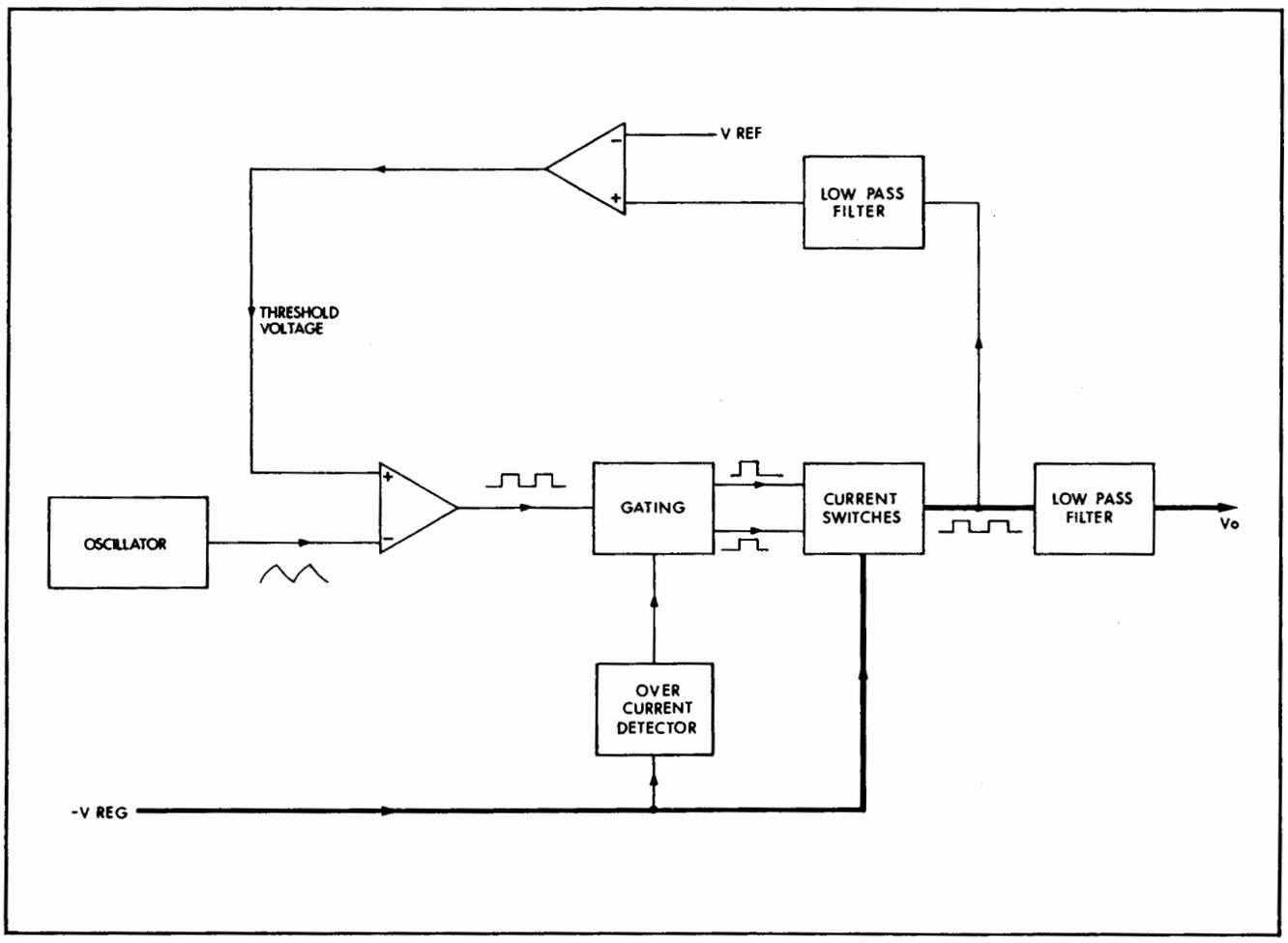

Figure A43-1 Block Diagram

INTRODUCTION

The threshold of the level detector is controlled by the error amplifier and is therefore proportional to the difference between the dc output and the reference voltage. The oscillator generates a ramp which drives the level detector to produce a pulse train whose mark:space ratio is controlled by the threshold voltage. The dc output is obtained by integrating the output of the current switches in a low pass filter and is therefore proportional to the mark:space ratio of the switching signal. This mark:space ratio is automatically adjusted by the error amplifier so that the output is always equal to the reference voltage ie, -5.2V.

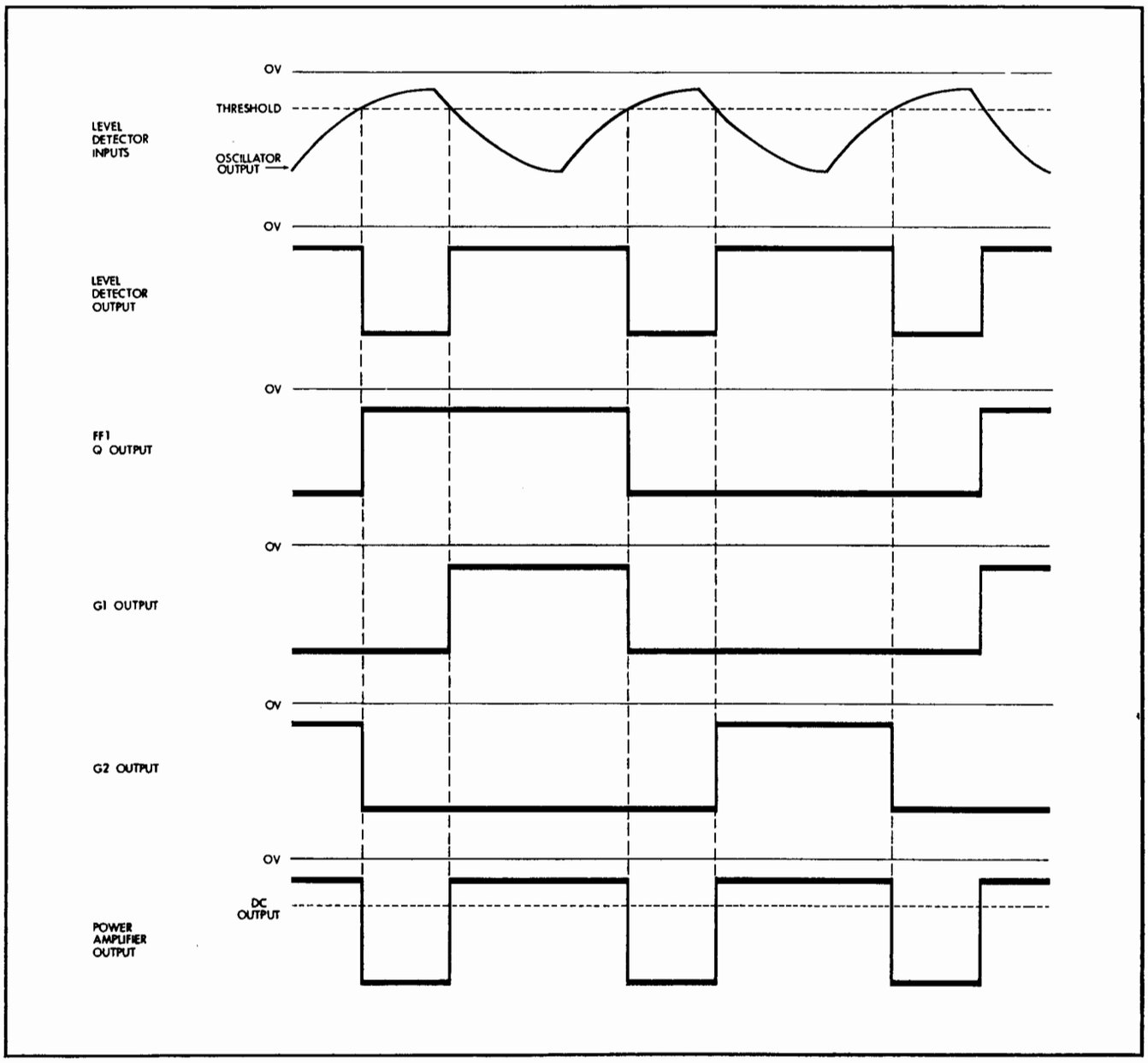

Figure A43-2 Timing Diagram

IC4 is a free running oscillator operating at approximately 30kHz. The exponential voltage generated across the timing capacitor C3 is applied to the level detector IC3. The threshold of IC3 is controlled by the error amplifier IC5 and is therefore proportional to the difference between the dc output and the reference voltage. The output of IC3 switches as the voltage across C3 passes through this threshold and hence the output consists of a pulse train whose mark:space ratio is proportional to the difference between the output and reference voltages. Note that as the gain of the error amplifier is very high only a few millivolts difference between its inputs is required to produce saturation at its output.

The output of the level detector drives the ÷2 counter FF1 whose outputs alternately enable G1 and G2. The level detector also drives G1 and G2 directly so that the current switches are alternately switched on for a time determined by the mark:space ratio of the switching signal (see Figure A43-2).

The current switches produce a train of width modulated pulses which are filtered by L1, L2, C9, C10 and C11 to produce a dc at the output. Diodes CR7 and CR8 clamp the collectors of Q5 and Q6 at approximately 0.7V when both current switches are off.

The output level is stabilised by -ve feedback via the filter R19, C7 to the error amplifier. For example, if the output voltage falls for any reason, the error amplifier alters the threshold of the level detector so that the duty cycle of the switching signal is increased thus restoring the dc output level to -5.2V.

Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A43	03760-70043		5.2V/2V REGULATOR ASSY
	03760-10411	2	CLAMP TOROID
	03760-10411		CLAMP TOROID
A43C12	0180-0097	1	C FXD 47UF 10% 35WVDC
A43C1	0180-1746		C FXD 15UF 10% 20WVDC
A43C2	0180-0229		C FXD 33UF 10% 10WVDC
A43C3	0160-0154	1	C FXD 2200PF 10% 200WVDC
A43C4	0160-2199		C FXD 30PF 5% 300WVDC
A43C5	0150-0050		C FXD 1000PF +80-20% 1000WVDC
A43C6	0150-0121		C FXD 0.1UF +80-20% 50WVDC
A43C7	0180-0291		C FXD 1UF +10% 35WVDC
A43C8	0180-0116		C FXD 6.8UF 10% 35WVDC
A43C9	0180-0159	3	C FXD 220UF 20% 10WVDC
A43C10	0180-0159		C FXD 220UF 20% 10WVDC
A43C11	0180-0159		C FXD 220UF 20% 10WVDC
A43CR1	1902-3070	2	DIO BKDN 4.22V 5% 400MW
A43CR2	1902-3070		DIO BKDN 4.22V 5% 400MW
A43CR3	1902-0533	1	DIO BKDN 4.99V 1W
A43CR4	1902-3059	2	DIO BKDN 3.83V 5% 400MW
A43CR5	1902-0048		DIO BKDN 6.81V 400MW
A43CR6	1902-3059		DIO BKDN 3.83V 5% 400MW
A43CR7	1901-0663	2	DIO SILICON JEDEC NS3000
A43CR8	1901-0663		DIO SILICON JEDEC NS3000
A43IC1	1820-0071	1	IC DUAL 4-I/P NAND BUFFER GATE
A43IC2	1820-0077	1	IC DUAL D-TYPE FLIP-FLOP
A43IC3	1820-0477		IC OPER AMPL
A43IC4	1820-0477		IC OPER AMPL
A43IC5	1820-0477		IC OPER AMPL
A43IC6	1820-0477		IC OPER AMPL
A43IC7	1820-0261	1	IC MONOSTABLE
A43L1	03760-70080	1	IND TOROID
A43L2	03760-70081		INDUCTOR ASSEMBLY
A43L2	03760-70081	2	INDUCTOR TOROID
A43Q1	1853-0038		XSTR SI PNP
A43Q2	1853-0038		XSTR SI PNP
A43Q3	1854-0039	2	XSTR SI NPN
A43Q4	1854-0039		XSTR SI NPN
A43Q5	1854-0589	2	XSTR SI NPN
A43Q6	1854-0589		XSTR SI NPN
	1200-0081	1	HEAT DISSIPATOR XSTR
A43R1	0766-0025	1	R FXD 101 OHM 5% 3W
A43R2	0698-7407	1	R FXD 150 OHM 5% 3W
A43R3	0757-0438		R FXD 5.11K OHM 1% 1/8W
A43R4	0757-0438		R FXD 5.11K OHM 1% 1/8W
A43R5	0757-0438		R FXD 5.11K OHM 1% 1/8W
A43R6	0698-3260	1	R FXD 464K OHM 1% 1/8W
A43R7	0757-0279		R FXD 3.16K OHM 1% 1/8W
A43R8	0698-0084	1	R FXD 2.15K OHM 1% 1/8W
A43R9	2100-2574		R VAR 500 OHM 10% 1/2W
A43R10	0698-3444		R FXD 316 OHM 1% 1/8W
A43R11	0698-3442		R FXD 237 OHM 1% 1/8W
A43R12	0698-3446		R FXD 383 OHM 1% 1/8W

Abbreviations are listed in the introduction to this section

Replaceable Parts (continued)

Ref Desig	HP Part No	TQ	Description
A43R13	0757-0427		R FXD 1.5K OHM 1% 1/8W
A43R14	0757-0439		R FXD 6.81K OHM 1% 1/8W
A43R15	0698-3152		R FXD 3.48K OHM 1% 1/8W
A43R16	0757-0407		R FXD 200 OHM 1% 1/8W
A43R17	0757-0280		R FXD 1K OHM 1% 1/8W
A43R18	0757-0458	1	R FXD 51.1K OHM 1% 1/8W
A43R19	0757-0442		R FXD 10K OHM 1% 1/8W
A43R20	0698-0082		R FXD 464 OHM 1% 1/8W
A43R21	0698-0082		R FXD 464 OHM 1% 1/8W
A43R22	0757-0407		R FXD 200 OHM 1% 1/8W
A43R23	0757-0416		R FXD 511 OHM 1% 1/8W
A43R24	0757-0416		R FXD 511 OHM 1% 1/8W
A43R25	0757-0407		R FXD 200 OHM 1% 1/8W
A43R26	0757-0384		R FXD 20 OHM 1% 1/8W
A43R27	0757-0384		R FXD 20 OHM 1% 1/8W

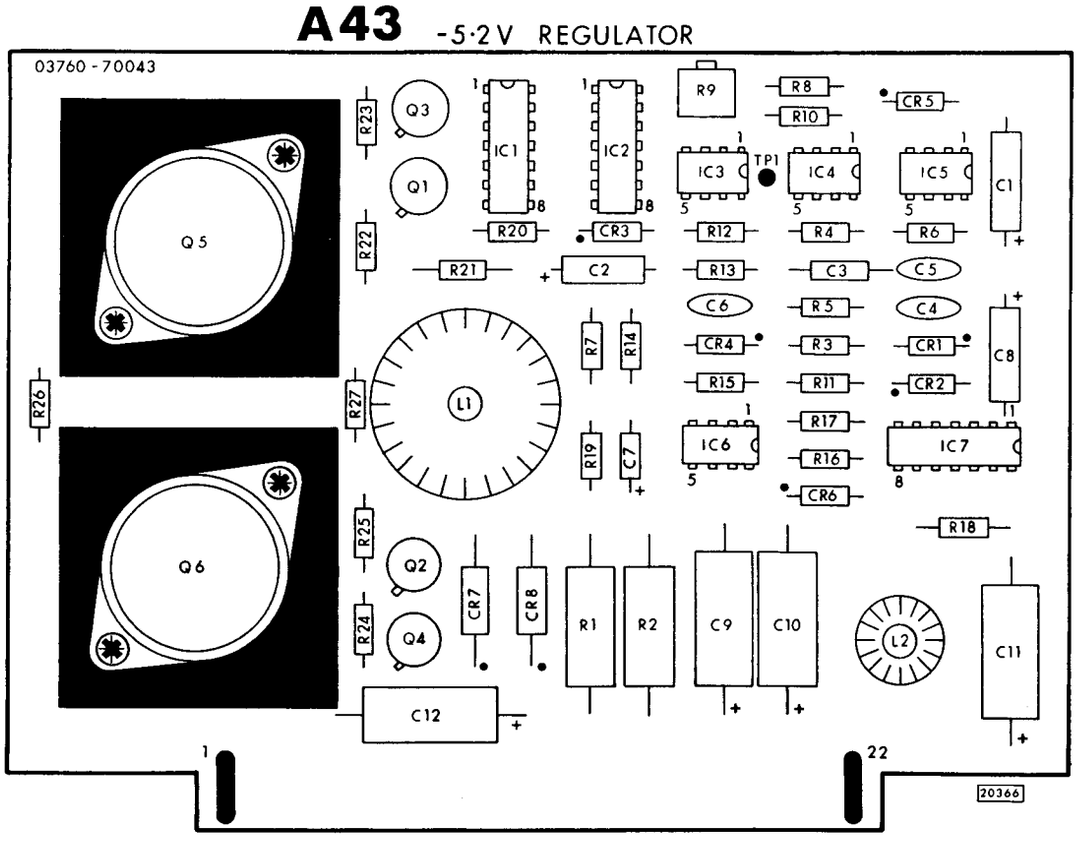

Figure A43-3 Component Location

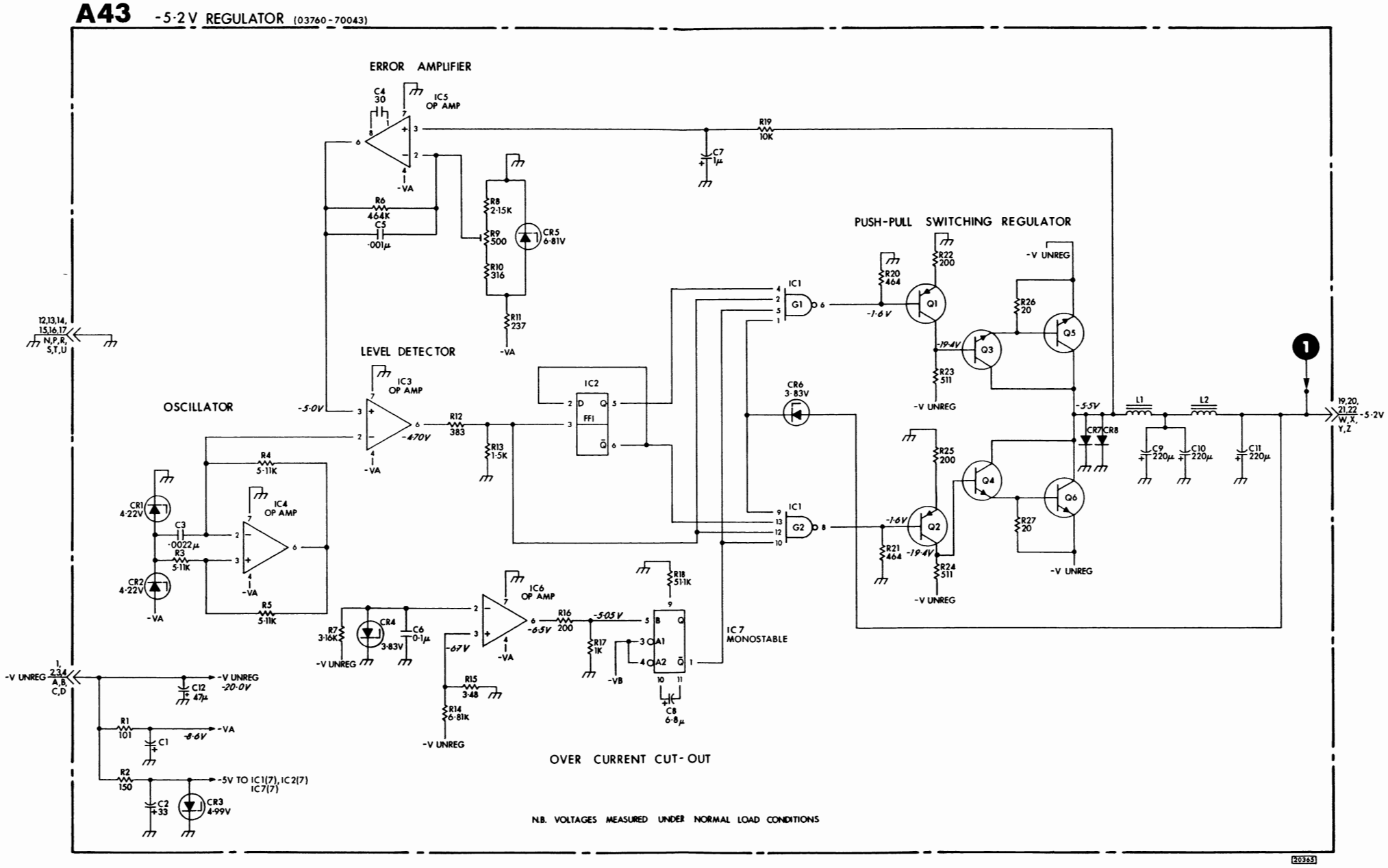

Figure A43-4 Schematic Diagram

ASSEMBLY SERVICE SHEET A44

FAN DRIVER ASSEMBLY A44

FAN MOTOR

The fan motor is a brushless dc device in which an electronic control circuit driven by Hall Generators in the motor replaces the mechanical commutation found in conventional dc motors. The motor consists of a two pole permanent magnet rotor, two pairs of stator windings and two Hall Generators as shown in Figure A44-1.

The outputs of the Hall Generators are proportional to the magnitude and directions of the dc bias currents and the flux in the air gap. As can be seen from A44-1, the Hall Generators are located at 90° to one another and therefore produce two sine waves 90° out of phase when the central magnet is rotated. These signals control two push-pull amplifiers in the A44 Assembly in such a way that only one stator winding in each pair is energised at a time. Figure A42-2 shows the two sine waves and the times at which the windings are energised by the push-pull amplifiers. The stator windings therefore set up a rotating field (see Figure A42-2) which reacts with the rotor field to produce the machine torque.

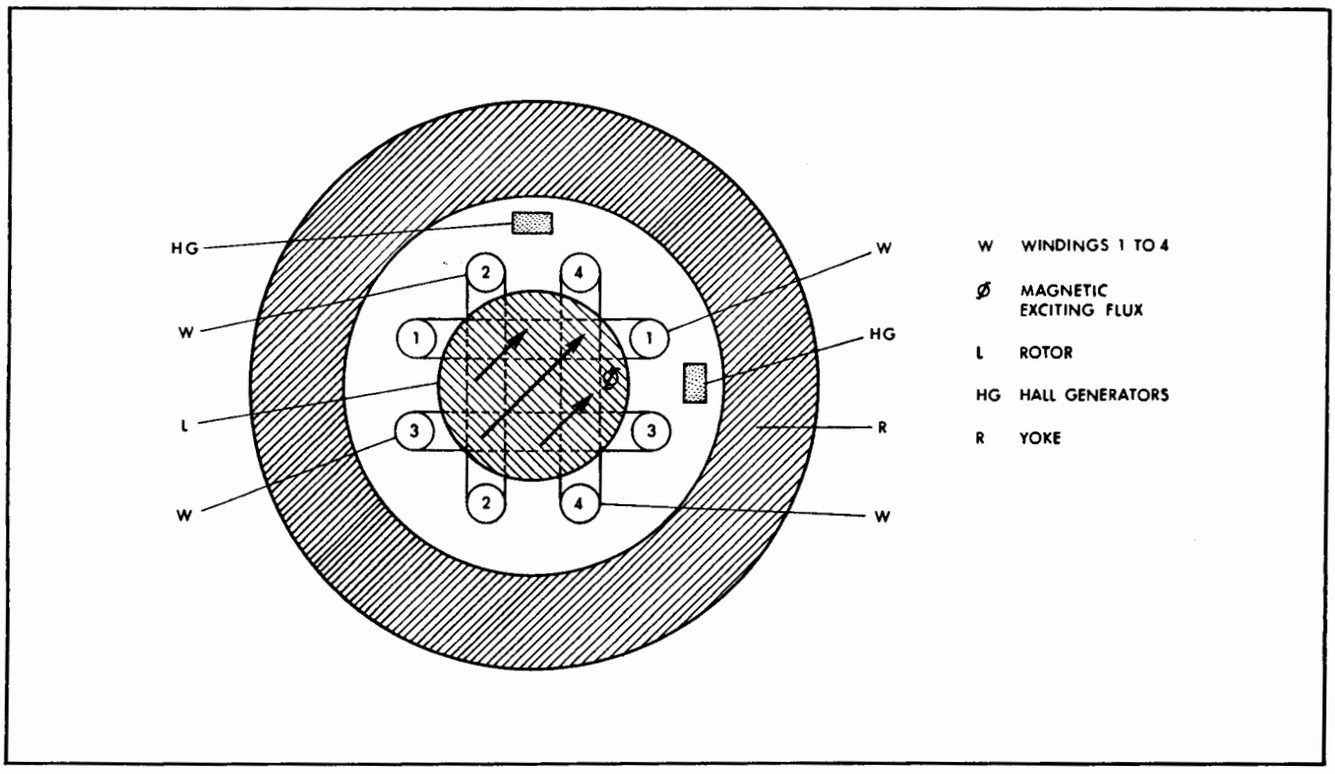

Figure A44-1 Fan Motor

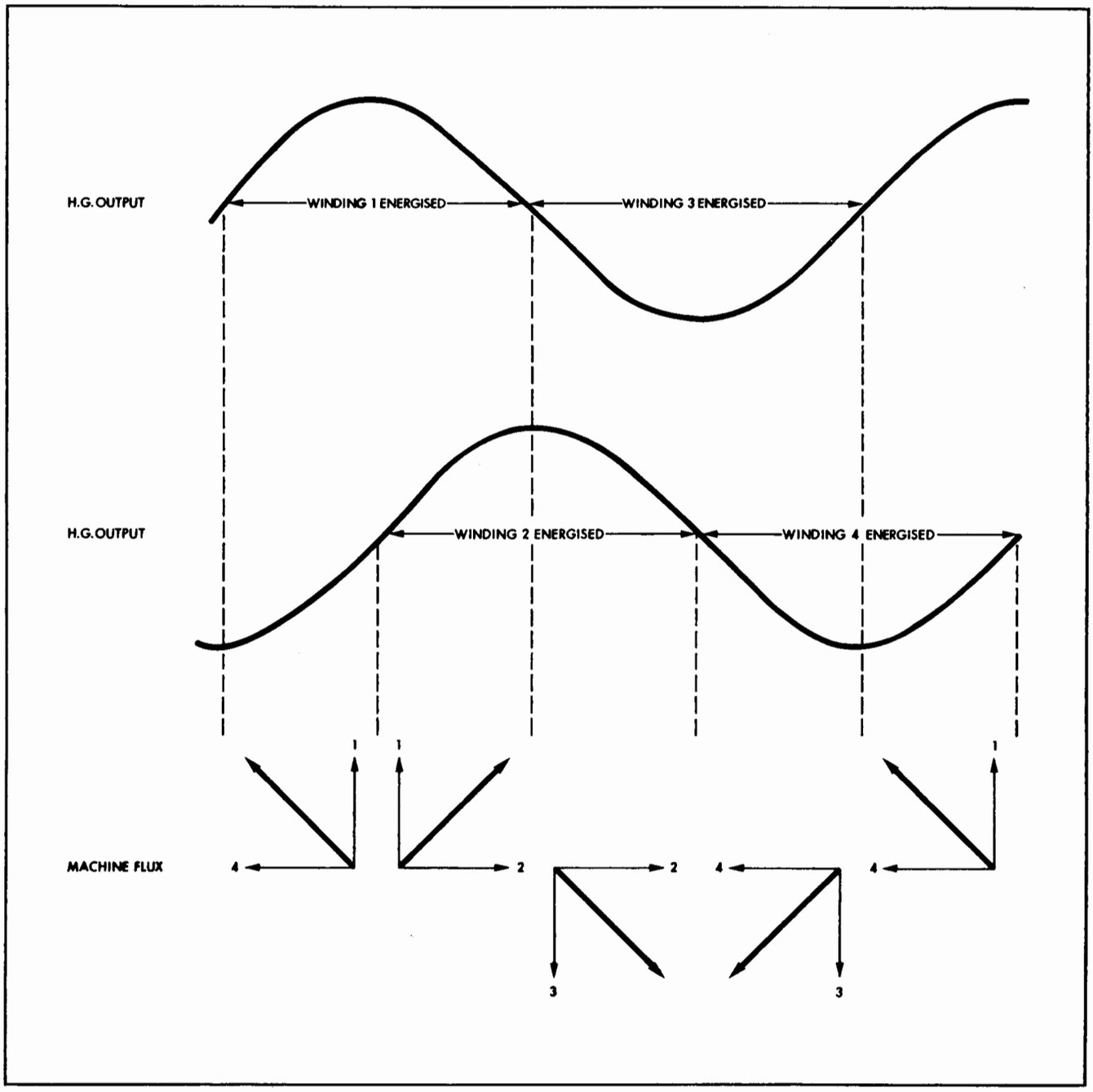

Figure A44-2 Electronic Commutation

SPEED CONTROL

The speed of the motor is controlled by the outputs of the Hall Generators which drive the push-pull amplifiers Q3 – Q10. These outputs are in turn controlled by the dc bias currents generated by Q2. When the motor rotates a back emf, proportional to its speed, is generated in the unenergised stator windings. This emf is rectified by CR3, CR6, CR7 and CR8 to provide a stabilising feedback signal which is applied to Q2 via Q1.

Replaceable Parts

Ref Desig	HP Part No	TQ	Description
A44	03760-70044		FAN DRIVER ASSY
A44C1	0180-0106	1	C FXD 60UF 20% 6WVDC
A44C2	0180-0229		C FXD 33UF 10% 10WVDC
A44C3	0150-0093		C FXD 0.01UF +80-10% 100WVDC
A44CR1	1910-0016	1	DIO GE
A44CR2	1902-3036	1	DIO BKDN 3.16V 5% 400MW
A44CR3	1901-0025	4	DIO SI
A44CR4	1901-0159	2	DIO SI 400PIV 750MA
A44CR5	1901-0159		DIO SI 400PIV 750MA
A44CR6	1901-0025		DIO SI
A44CR7	1901-0025		DIO SI
A44CR8	1901-0025		DIO SI
A44Q1	1854-0045	1	XSTR SI NPN
A44Q2	1854-0003	1	XSTR SI NPN
A44Q3	1853-0020		XSTR SI PNP
A44Q4	1853-0084	4	XSTR PNP SILICON
A44Q5	1853-0020		XSTR SI PNP
A44Q6	1853-0084		XSTR PNP SILICON
A44Q7	1853-0020		XSTR SI PNP
A44Q8	1853-0084		XSTR PNP SILICON
A44Q9	1853-0020		XSTR SI PNP
A44Q10	1853-0084		XSTR PNP SILICON
A44R1	0757-0280		R FXD 1K OHM 1% 1/8W
A44R2	0757-0444	1	R FXD 12.1K OHM 1% 1/8W
A44R3	0698-0085		R FXD 2.61K OHM 1% 1/8W
A44R4	0698-3458		R FXD 348 OHM 1% 1/8W
A44R5	0698-3153	1	R FXD 3.83K OHM 1% 1/8W
A44R6	0698-3438	2	R FXD 147 OHM 1% 1/8W
A44R7	0698-3430	1	R FXD 21.5 OHM 1% 1/8W
A44R8	0698-3438		R FXD 147 OHM 1% 1/8W
A44R9	0698-0001	1	R FXD 4.7 OHM 5% 1/2W

Abbreviations are listed in the introduction to this section

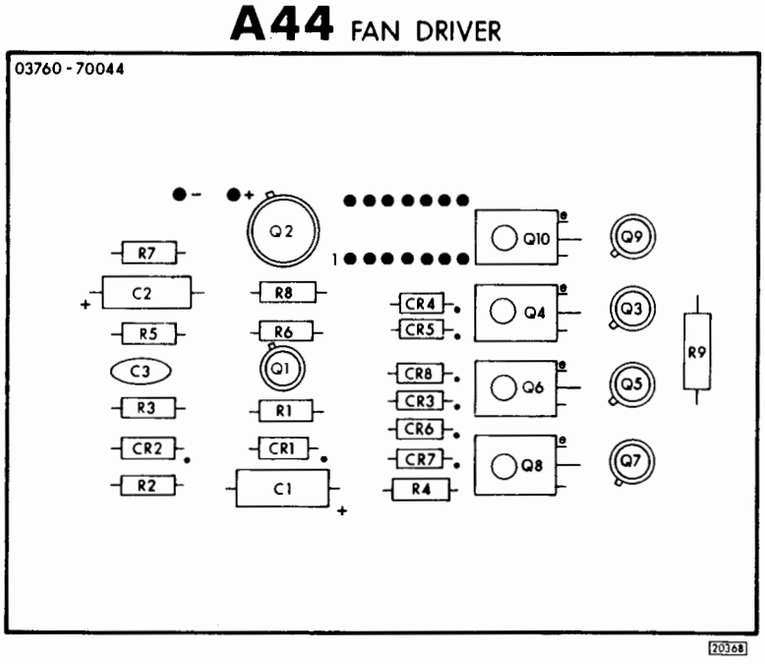

Figure A44-3 Component Location

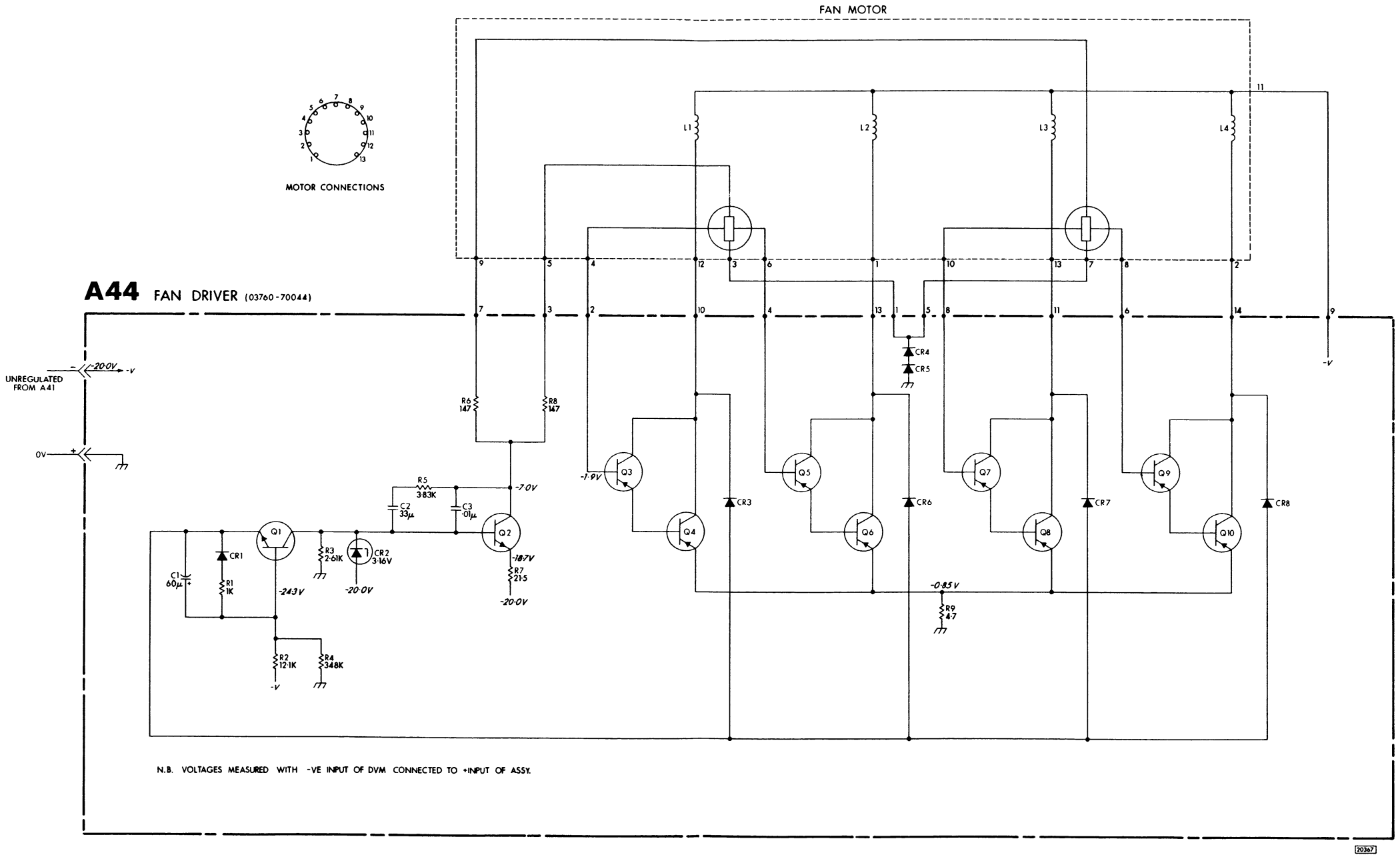

Figure A44-4 Schematic Diagram

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