IBM25CPC710 Bridge Chip: Enhancements and Changes in the DD3.x revisions

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November 8, 2001 Version 1.0

Abstract

This Application Note describes the differences between the CPC710-100+ (DD2) and the CPC710 (DD3.x) versions of the PowerPC Dual PCI/Memory Controller companion chip. The purpose of this note is to provide designers with an overview of the changes and point out performance enhancements and potential programming changes. For a detailed understanding of the operation of the CPC710-133, please refer to the User's Manual. For a detailed understanding of the physical pin out and electrical specifications, please refer to the Data Sheet.

Overview

The IBM25CPC710 DD3.x is a host bridge that interfaces a PowerPC 60x bus with system memory (SDRAM) and two independent PCI interfaces. It provides arbitration for one to four processors and supports up to two levels of pipelining per processor with 64-byte buffers (maximum of 6 buffers). Use of external slave devices on the 60x bus is also supported and requires additional external logic. The CPC710 DD3.x supports 60x bus speeds of up to 133MHz at 2.5V. Of course, given signal quality issues with higher bus speeds it is not recommended that the CPU bus run at 133Mhz in configurations that include more than 2 CPUs.

The bridge's two way interleaved memory controller supports SDRAM at 100 or 133 MHz; both single bank and dual bank, PC100, PC133 and registered DIMMs are supported. The memory controller design requires the use of an external multiplexer and two physical DIMMs.

The bridge contains two PCI host bus bridges: one provides an interface for a 32-bit, 33 MHz PCI bus for standard and native I/O. This bus supports either 3.3V or 5V logic level devices, and allows attachment of up to 2MB of boot ROM (and up to 256MB of extended boot ROM). The other PCI interface supports a 32- or 64-bit, 33 or 66 MHz PCI bus for high data throughput, but supports only 3.3V logic level devices. *This is a change from the previous revision*. Burst and non-burst data transfers to memory from the PCI (bridge acts as target on PCI bus) and from memory to the PCI (bridge acts as master on PCI bus) are supported; data transfers directly between PCI-32 and PCI-64 are not supported. *This is a change from the previous revision.*

A single channel DMA controller provides support for large data transfers between memory and the PCI busses. DMA to and from the CPU bus to memory, or between PCI-32 and PCI-64 is not supported. *This is a change from the previous revision.*

Processor Interface:

❖ Voltage Level and Bus Speed Differences

- The CPC710 DD3.x revision supports 60x bus operation at speeds of up to 133MHz, at an I/O voltage of 2.5V. This interface voltage level is supported on the PPC750L, 750CX, and 750CXe processors. *This is a change from the previous revision.*

❖ I/O Signal New Functionality

- Set bit 18 of 60x Bus Arbiter register (system register CPC0_ABCNTL) to 1 to allow the signal level of SYS_TA_ to be confirmed and held at a high logic level (after precharging) as soon as the CPC710 DD3.x exits the RESET state. This is to allow for proper operation in systems with high loads on the CPU bus.

❖ I/O Signal Additional Functionality for 4-way Processor Support

- Coming out of reset, the 60x bus arbitration logic of the CPC710 DD3.x defaults to the same dual processor mode used in the CPC710 DD2. To enable 4-way arbitration, the Master CPU should set chip control register CPC0_ABCNTL [17] to a "1". Then the SYS_HRESET2_, SYS_HRESET3_, SYS_SRESET2_ and SYS_SRESET3_ signals will go inactive, allowing CPUs 2 and 3 to exit the reset state.

- The two Reset registers CPC0_RSTR and CPC0_SRST have been modified to include bits to support program control operation of hard and soft reset signals for the additional processors.

  - Connectivity Reset Register bits CPC0_RSTR [4:5] controls signals SYS_HRESET2_ and SYS_HRESET3_ respectively. CPU Soft Reset Register bits CPC0_SRST [4:5] controls signals SYS_SRESET2_ and SYS_SRESET3_ respectively

  - The CPC0_PIDR Register has been modified to allow identification of each of the 4 processors; if CPC0_PIDR [24:31] is read as 'h00' it indicates the Processor corresponding to BR0_/BG0_ is active. Valid values for these bits are:
    - = 0x00==> Processor corresponding to BR0_/BG0_
    - = 0x01 ==> Processor corresponding to BR1_/BG1_
    - = 0x02 ==> Processor corresponding to BR2_/BG2_
    - = 0x03 ==> Processor corresponding to BR3_/BG3_

❖ I/O Signals for 4-way Processor Support

- The signals SYS_MCP0: 3 are used to indicate to the CPUs that the CPC710 has detected an error condition and a machine check is required. To help reduce pin count, output signals SYS_MCP2_ and SYS_MCP0_ are generated from one internal signal source. SYS_MCP3_ and SYS_MCP1_ also share a common internal signal source.
- The System Error Status Register has not been modified and only errors that occur with Processor 0 or 1 can be detected and reported.

Memory Interface:

❖ Extended SDRAM Addressing

- The signal MADDR13 has been added to support the following additional SDRAM organizations:
  - 13-12-2, 14-9-2, 14-10-2, 14-11-2, 14-12-2
  - Register SDRAM0_MCER [26:29] is used to select the SDRAM organization; refer to the CPC710-133 User's Manual for more information.

❖ Extended Memory Size

- The Memory controller has been modified to support up to six banks of dual DIMM interleaved 72-bit memory, for a total memory addressing range of 3.5GB. The memory controller now allows configuration of bank sizes up to 4GB per bank
  The choice of 4MB to 1GB (same as the CPC710-100+) or 4MB to 4GB is made with SDRAM0_MCCR [8].
  - If SDRAM0_MCCR [8] = 1 bank size range is from 4MB to 1GB
  - If SDRAM0_MCCR [8] = 0 bank size range is from 4MB to 4GB
  - Refer to the CPC710-133 User's Manual for more information.

❖ Supported Memory Types

- Supports JEDEC standard PC100 and PC133 SDRAMs, both single bank and dual bank.
- EDO memory is no longer supported on the CPC710 with the DD3.x revision.
- All types of registered DIMMs are now supported on the CPC710 with the DD3 version. New programming bits are defined in register SDRAM0_MCCR0 to support registered DIMMS.
  - Setting SDRAM0_MCCR [16] = 1 adds one additional clock cycle to the internal sequencer signals for read operations of registered DIMMs.
  - Setting SDRAM0_MCCR [19] =1 shifts the following signals by one clock cycle: MUX_SEL, MUX_CLKEN1B_, MUX_CLKEN2B_
  - Setting SDRAM0_MCCR [21] = 1 allows the data to be written to the memory to be held valid for an additional clock cycle.
  - Setting SDRAM0_MCCR [22] = 1 shifts the following signals by one clock cycle: MUX_CLKENA2_, MUX_OEB_, SDRAS0_, SDRAS1_, SDCAS0_, SDCAS1_, WE0_, WE1_, MADDR0_ODD, MADDR0_EVEN, MADDR1-13, BS0 and BS1

❖ Maximum Number of Memory Banks Decreased from 8 to 6

- CPC710 DD3.x revision does not support the use of registers MCER6 and MCER7.These registers were present in the CPC710-100+ DD2 version.
- Internal memory controller logic no longer generates SDCS12_ through SDCS15_. These signals were present in the CPC710-100+ DD2 version. The multiplexing capabilities defined in register SDRAM0_MCCR [11:15] have been modified from the usage in CPC710 DD2 revision. This multiplexing allows for support of SDRAM speeds up to 133 MHz. The higher speed is attained by limiting the loading (number of SDRAM packages) on each SDCS signal.

  - New encoding:
    - If SDRAM0_MCCR [11] = 1 signals SDCS_[0:3] use I/O pins SDCS_[4:7]
    - If SDRAM0_MCCR [12] = 1 signals SDCS_[0:3] use I/O pins SDCS_[8:11]
    - SDRAM0_MCCR [13] is no longer used
    - If SDRAM0_MCCR [14] = 1 signals SDQM use I/O pins SDRAS1_, SDCAS1_ and WE1_
    - If SDRAM0_MCCR [15] = 1 signals SDQM uses I/O pins PCG_ARB

❖ Extended Addressing of PCI Memory

- System memory addressing range increased from 2GB to 4GB. The standard addressing capability is 2GB; with the size defined by bits 24-31 of PCI local registers PCILx_PSSIZE. The address extension is implemented by setting bit 27 of chip control register CPC0_PGCHP. In this case, the FINE option for selection of less than1MB granularity (enabled in CPC710-100+ dd2 in the memory write protection register SDRAM0_MWPR) is not available.

PCI Interfaces:

❖ The PCI-64 Interface is no Longer 5 Volt Tolerant

- The I/O drivers used on the CPC710 DD3.x PCI-64 interface no longer support 5V logic levels – users must attach only 3.3V devices to the PCI-64 bus. *This is a change from the previous revision.*

❖ PCI-32 Interface Now Supports External Arbiter Usage

- The PCI-32 interface now allows use of an external PCI bus arbiter. A method similar to that used for disabling the PCI-64 internal arbiter is used to for disabling the PCI-32 internal arbiter.
  - At power on, after activation of the POWERGOOD signal, the signal P_REQ2_ is sampled. This initial sampling is done while PLL_RESET is active, and is independent of activation of the PCI clock on the bus. If the signal level is 0, the internal arbiter for the PCI-32 bus is disabled. Bit 16 of chip control register CPC0_PGCHP can be read to determine the detected arbitration mode; a “0” indicates the internal arbiter is in use, and a “1” indicates an external arbiter.
  - For the PCI-64 interface, the signal sampled after activation of the POWERGOOD signal is G_REQ2_. This initial sampling is done while PLL_RESET is active, and is independent of activation of the PCI clock on the bus. Bit 9 of chip control register CPC0_PGCHP can be read to determine the detected arbitration mode; a “0” indicates the internal arbiter is in use, and a “1” indicates an external arbiter.
- **NOTE:** Because the FLASH interface is present on the PCI-32 bus, configurations using an external PCI bus arbiter must prevent any external PCI-32 transactions from interfering or pre-empting FLASH transactions.

Power and PLL:

❖ New Supply Voltages

- 60x bus voltage level now 2.5V. To support the I/O interfaces on the PPC750CX/CXe (as well as the PPC750L) the 60x bus interface logic is now 2.5V. *This is a change from the previous revision.*
- VDD (core logic) is also 2.5V.
- OVDD (I/O logic) for SDRAM and PCI interfaces is 3.3V.
- The AVDD (PLL) is 2.5V.
  - AVDD is the voltage supply pin to the analog circuits in the PLL. Noise on AVDD will cause phase jitter at the output of the PLL. To provide isolation from the noisy internal digital VDD signal, AVDD is brought to a package pin. If little noise is expected at the board level, then AVDD can be connected directly to the digital VDD

plane. In most circumstances, however, it is prudent to place a filter circuit on AVDD; refer to the CPC710 DD3.x User's Manual for more information.

- The PLL is now set up and controlled by external signals PLL_RANGE [1:0] and 6 external signals PLL_TUNE [5:0] instead of PLL133 and PLL_TUNE [1:0]. *This is a change from the previous revision.*

Packaging Changes:

❖ FC-PBGA Package instead of CBGA

- The CPC710 DD3.x is offered in a 35mm 728 pin FC-PBGA (Flip Chip Plastic Ball Grid Array) package. *This is a change from the previous revision – the DD3.x is not pin/package compatible with the DD2.* Refer to the CPC710-133 PCI Bridge and Memory Controller Datasheet for more details on the physical packaging.

❖ I/O Pinout Deletions:

The following I/Os are no longer present on the DD3 revision:

INTERFACE	SIGNAL NAME	IMPACT
Memory Interface	SDCS_12, SDCS_13, SDCS_14, SDCS_15 SDRAS_2, SDRAS_3 SDCAS_2, SDCAS_3 WE_2, WE_3	Changes to the memory interface. Refer to Chapter 6 Of User's Manual for more details.
PCI 32-bit Interface	P_GNT_6, P_GNT_5, P_GNT_4, P_REQ_6, P_REQ_5, P_REQ_4	Decreases number of PCI devices supported by the internal bus arbiter, unless multiplexed (see below).
PCI 32-bit Interface	P_ISA_MASTER	
PCI 32-bit Interface	P_CFG [0:2]	CFGA [13:11] no longer driven offchip (used for save loads on PCI bus)
PCI 64-bit Interface	G_CFG [0:2]	CFGA [13:11] no longer driven offchip
Clock Inputs	PLL_133, PLN_RTC_CLOCK	DD3 has new strapping options. Timers now controlled only by PCI32 clock.
Test Signals	CE1_A, CE1_B, CE1_C1, CE1_C2, DI1, DI2, CE0_IO, RI, SCAN_GATE, TESTIN, CE_TRST, TESTOUT	Signals used only by manufacturing test.

❖ **I/O Pin Additions:**

The following I/Os are new on the DD3 revision:

INTERFACE	SIGNAL NAME	IMPACT
60x bus Interface	SYS_BG2_, SYS_BG3_, SYS_MCP2, SYS_MCP3, SYS_HRESET2, SYS_HRESET3, SYS_SRESET2, SYS_SRESET3	New for 4-way CPU support
60x bus Interface	SYS_TA_HIT	
Memory Interface	MADDR13	Used for newer memory sizes
Clock Inputs	PLL_RANGE0, PLL_RANGE1, PLL_TUNE2, PLL_TUNE3, PLL_TUNE4, PLL_TUNE5	New; used for setup and control of PLL

❖ **I/O Pins Multiplexed:**

The following I/Os are multiplexed on the DD3 revision:

INTERFACE	PIN FUNCTION OPTION	REGISTER BIT TO USE TO SELECT FUNCTION
Memory Interface	SDRAS_1 becomes SDQM	SDRAM0_MCCR [14] = 1
Memory Interface	SDCAS_1 becomes SDQM	SDRAM0_MCCR [14] = 1
Memory Interface	WE_1 becomes SDQM	SDRAM0_MCCR [14] = 1
Memory Interface	G_ARB becomes SDQM	SDRAM0_MCCR [15] = 1
60x bus Interface	DRAMREQ_ becomes NODLK_	CPC0_PGCHP [20] = 0
60x bus Interface	DRAMGNT_ becomes DLK_	CPC0_PGCHP [20] = 0
PCI 64-bit Interface	G_REQ_7 becomes P_REQ_6	CPC0_PGCHP [23] = 1
PCI 64-bit Interface	G_GNT_7 becomes P_GNT_6	CPC0_PGCHP [23] = 1
PCI 64-bit Interface	G_REQ_6 becomes P_REQ_5	CPC0_PGCHP [22] = 1
PCI 64-bit Interface	G_GNT_6 becomes P_GNT_5	CPC0_PGCHP [22] = 1
PCI 64-bit Interface	G_REQ_5 becomes P_REQ_4	CPC0_PGCHP [21] = 1
PCI 64-bit Interface	G_GNT_5 becomes P_GNT_4	CPC0_PGCHP [21] = 1

Hardware ID Changes for DD3.0 revision:

- **PCI-32 revision ID in PCIC0_REVID = x'03**
- **PCI-64 revision ID in PCIC1_REVID = x'03**
- **EC Level in CPC0_UCTL [24:31] = x'a0**

Performance Enhancements and Improvements:

- The CPC710 DD3.x revision has improvements to support PCI Long Burst Write operations and improvements in the deadlock prevention circuits. These enhancements can be selected by programming select bits in PCI local registers PCILx_PSWCR and PCILx_DLKCTRL.
  - Crossing a 4K boundary during burst operations results in a stop on the PCI bus. By default operation, snooping is done on the current PCI master's address. A new option is provided to allow for anticipation logic to snoop ahead to the next address. Set PCI local register PCILx_PSWCR [17] to "1" to enable the snoop ahead logic.
  - There have been several changes to the deadlock avoidance logic. The CPC710 DD2 errata #8 and #9, relating to defects in the deadlock circuitry, have been fixed in the CPC710 DD3.x revision. In addition, there are three improvements that can be selected by setting the appropriate bits.
    - PCILx_DLKCTRL [27] – when set to "0" enables the erratum #8 correction logic to prevent potential deadlock in multiprocessor configurations when one CPU is attempting a PCI read. For more details on the erratum, please read the CPC710 DD2 Errata List. Setting this bit to "1" disables the correction logic.
    - PCILx_DLKCTRL [28] – when set to "0" enables the erratum #9 correction logic to function correctly when the programmed value in the PCI local register PCILx_DLKCTRL [8:15] is greater than 0x0F. Setting this bit to a "1" disables the correction logic.
    - PCILx_DLKCTRL [29] - when set to "1" results in the following: When a read is already in progress to an address defined in the deadlock avoidance address range, an ARTRY will be generated for all accesses except the access to the main memory for that read. Setting this bit to a "0" disables this logic. The default state for this bit is recommended, as other methods of deadlock avoidance have proven to be flexible enough to resolve problems without use of this logic.
    - PCILx_DLKCTRL [30] - when set to "0" results in the following: The processor ID is taken into account in the deadlock avoidance logic. Setting this bit to a "1" causes the deadlock logic to ignore the processor ID.
    - PCILx_DLKCTRL [31] - when set to "0" results in the following: The deadlock avoidance logic using the signals MEMREQ/MEMACK and DLK/NODLK are masked. Setting this bit to a "1" causes the deadlock logic to generate these signals as usual.

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Printed in the United States of America November 2001